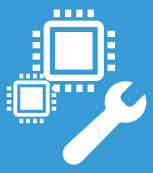
SILICON LABS

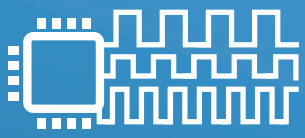
Timing Selector Guide

SPRING 2014

HIGH PERFORMANCE



CUSTOMIZABLE



FREQUENCY FLEXIBILITY

2-WEEK LEAD TIME

Timing Solutions

Comprehensive — complete portfolio of oscillators, clock generators, clock buffers and jitter attenuators

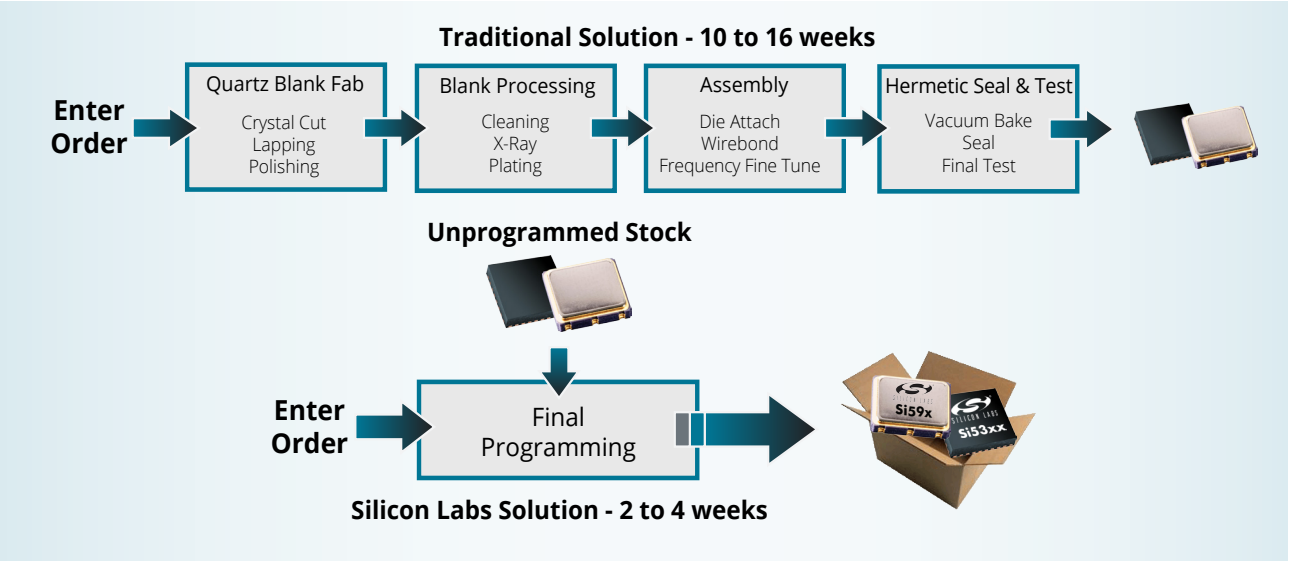
Flexible — Silicon Labs' devices support any-frequency synthesis, simplifying clock generation while minimizing BOM cost and complexity

Performance — highly-integrated, low jitter operation simplifies design and optimizes system performance

Customized — web-customizable clacks and oscillators, with quick turn, samples available in days, not weeks

Industry's Shortest Lead Times

Silicon Labs XO, VCXO and CMEMS Oscillators are built to order and available with 2 week lead times for samples. Need samples faster? Some devices are available with 24-hour lead times. Contact Silicon Labs website for details at www.silabs.com/short-lead-times



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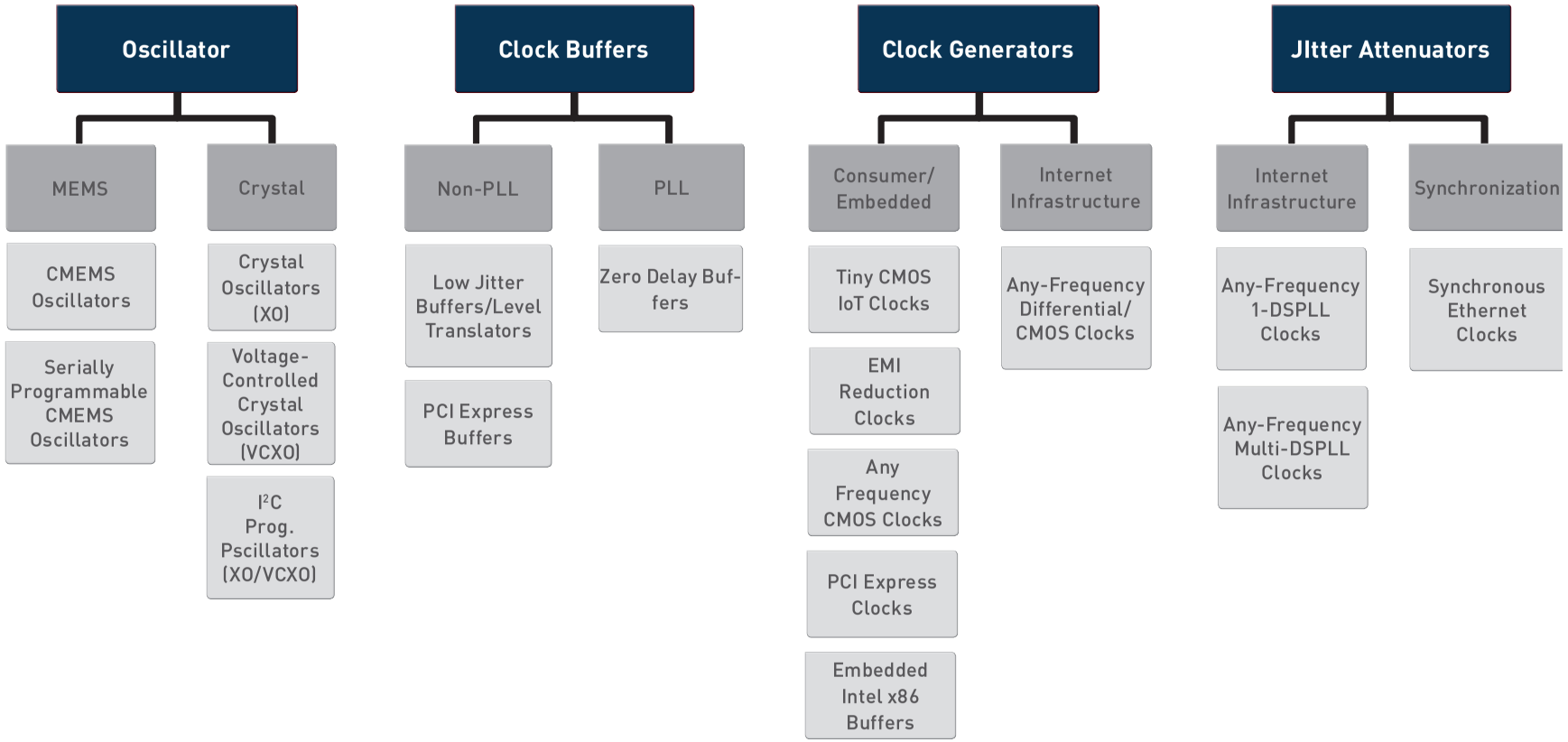


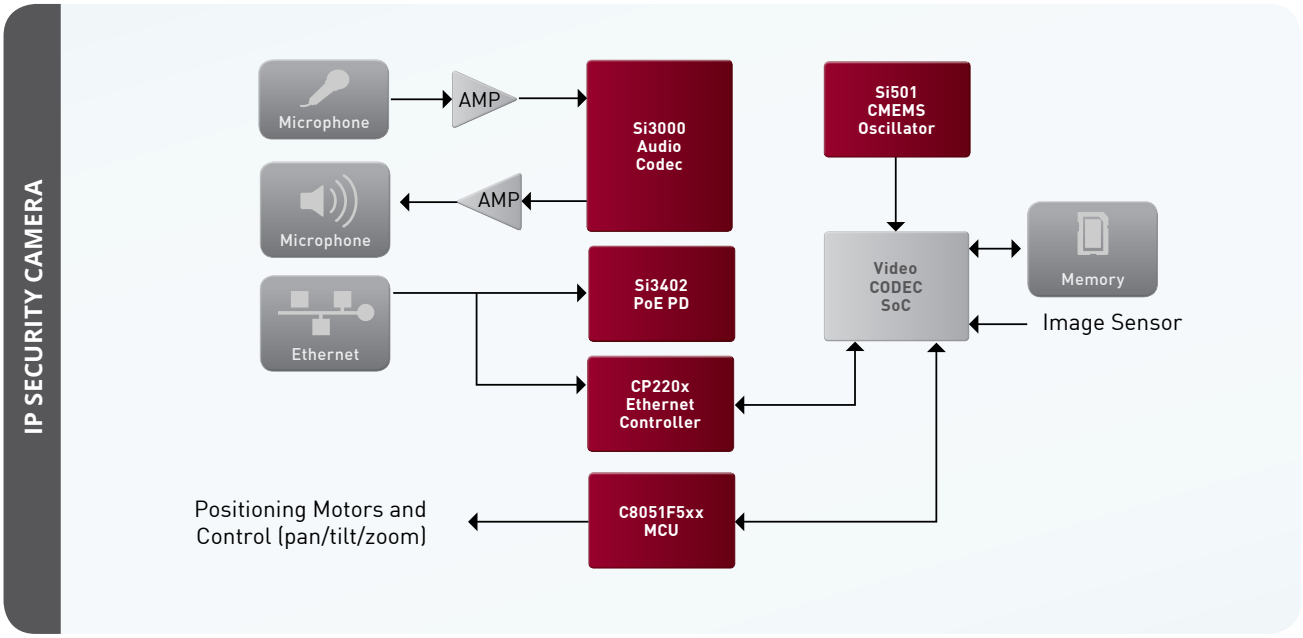
CMEMS Oscillators

WEB-CONFIGURABLE CUSTOM CLOCK BUFFERS AVAILABLE AT: www.silabs.com/cmems

Silicon Labs' CMEMS® general-purpose MEMS oscillators provide fast, easy customization for any frequency between 32 kHz and 100 MHz. They are a perfect fit for low cost, high shock applications, providing greater reliability, stability across temperature, and better aging than traditional crystal oscillators of the same class. Silicon Labs' Si501/2/3/4 CMEMS general-purpose oscillators provide lower cost, greater reliability, and better aging than traditional crystal oscillators of the same class. Their single-chip construction uses Silicon Labs' advanced CMEMS technology, and is highly robust against shock and vibration, and provides ±20 ppm frequency stability guaranteed for 10 years.

CMEMS FEATURES

- Wide frequency range: 32 kHz to 100 MHz
- Less than 2 week lead time for samples
- ±20/30/50 ppm frequency stability including 10-year aging
- LVCMOS output
- Low period jitter (11 ps PkPk)
- Low power
- Glitchless start and stop
- Industry standard footprints: 2 mm x 2.5 mm, 2.5 mm x 3.2 mm, 3.2 mm x 5 mm
- RoHS compliant, Pb-free
- Field programmable
- –20 to +70 °C: extended commercial temperature
- –40 to +85 °C: industrial temperature



PART NUMBER	CONTROL	FREQ.	FREQUENCY RANGE	STABILITY (PPM)	PERIOD JITTER (PkPk)	SUPPLY VOLTAGE	IDD (TYP)	OE	TEMP RANGE	OUTPUT FORMAT	PACKAGE
Si501	Pin	Single	0.032 - 100 MHz	±20, ±30, ±50	11	1.8 V 2.5 V 3.3 V	1-5 mA (freq. depedent)	Pin 1	-40 to 85 °C, -20 to 70 °C	LVCMOS	3.2 mm x 5.0 mm 2.5 mm x 3.2 mm 2.0 mm x 2.5 mm DFN4
Si502	Pin	Dual						Pin 1			
Si503	Pin	Quad						Pin 1			
Si504	1-Pin	Any						—			

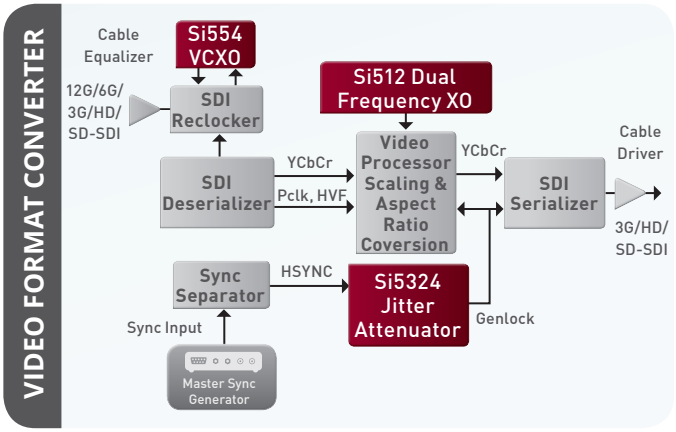
Crystal Oscillators (XO/VCXO)

REQUEST CUSTOM PART NUMBERS AND SAMPLES AT: www.silabs.com/oscillators

Silicon Labs' crystal oscillators and voltage controlled crystal oscillators (XO/VCXOs) leverage advanced DSPLL® circuitry to provide a low jitter clock at any frequency from 100 kHz to 1.4 GHz. Unlike a traditional XO, where a different crystal is required for each output frequency, Silicon Labs' XO/VCXOs use a fixed frequency crystal and DSPLL clock synthesis IC to generate any output frequency. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability, while providing best-in-class jitter performance and supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments. All devices are factory configurable for a wide variety of user specifications including frequency, supply voltage, output format and stability, thereby eliminating long lead times associated with custom oscillators.

XO/VCXO FEATURES

- Wide frequency range: 100 kHz to 1.4 GHz
- Samples of any XO/VCXO available in 2 weeks
- Superior jitter performance: <0.3 ps rms
- Excellent frequency stability, superior initial accuracy
- Single, dual, quad, I²C programmable options
- LVPECL, LVDS, CML, HCSL, CMOS options
- 1.8, 2.5, and 3.3 V options
- 5 x 7 mm, 3.2 x 5 mm options
- -40 to 85 °C operation



Crystal Oscillators (XO)

PART NUMBER	NUMBER OF REQUENCIES	FREQUENCY RANGE	JITTER (ps RMS)	STABILITY/APR (PPM)	FORMAT	VOLTAGE (V)	TEMP (°C)	PACKAGE SIZE (MM)
Si535	Single	select freq. 100 - 312 5 MHz	0.2	±20, ±31.5	LVDS, LVPECL	3.3, 2.5	-40 to 85	5 x 7
Si530/31	Single	10 - 1417 MHz	0.3	±20, ±31.5, ±61.5	CMOS, LVPECL, LVDS, CML	3.3 2.5 1.8	-40 to 85	5 x 7
Si532/33	Dual							
Si534	Quad							
Si570	Any (I²C Prog)							
Si590/91	Single	10 - 810 MHz	0.5	±20, ±30, ±50, ±100	CMOS, LVPECL, LVDS, CML	3.3 2.5 1.8	-40 to 85	5 x 7 mm 6-pad
Si598	Any (I²C Prog)							
Si510/11	Single	0.1 - 250 MHz	0.8	±30, ±50, ±100	CMOS, Dual CMOS, LVPECL, LVDS, HCSL	3.3 2.5 1.8	-40 to 85	5 x 7 3.2 x 5
Si512/13	Dual							
Si514	Any (I²C Prog)							

Voltage-Controlled Oscillators (VCXO)

PART NUMBER	NUMBER OF CENTER FREQUENCIES	FREQUENCY RANGE	JITTER (ps RMS)	STABILITY/APR (PPM)	FORMAT	VOLTAGE (V)	TEMP (°C)	PACKAGE SIZE (MM)
Si550	Single	10 - 1417 MHz	0.5	±12 to ±375	CMOS, LVPECL, LVDS, CML	3.3 2.5 1.8	-40 to 85	5 x 7
Si552	Dual							
Si554	Quad							
Si571	Any (I²C Prog)							
Si595	Single	10 - 810 MHz	0.7	±10 to ±370	CMOS, LVPECL, LVDS, CML	3.3 2.5 1.8	-40 to 85	5 x 7
Si597	Quad							
Si599	Any (I²C Prog)							
Si515	Single	0.1 - 250 MHz	1.0	±30to ±100	CMOS, Dual CMOS, LVPECL, LVDS, HCSL	3.3 2.5	-40 to 85	5 x 7 3.2 x 5
Si516	Dual							

Clock Buffers

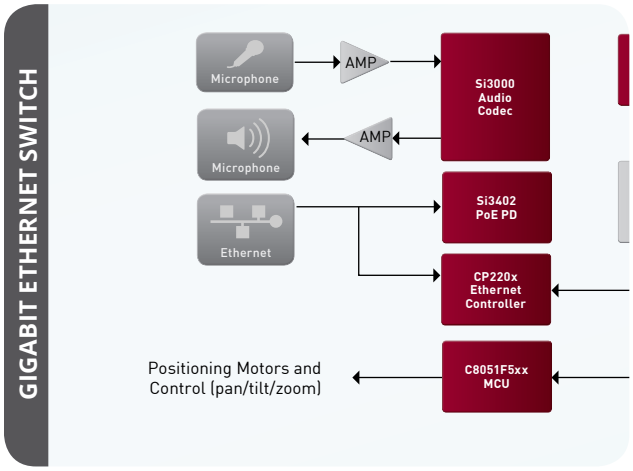
WEB-CONFIGURABLE CUSTOM CLOCK BUFFERS AVAILABLE AT: www.silabs.com/clock-buffer

Fanout Buffers/Level Translators

Silicon Labs' low jitter clock buffers produce multiple copies of an input clock at the same frequency with minimal additive jitter. LVDS, LVPECL, HCSL, CML, LVCMOS, SSTL and HSTL buffers are available, including devices that support multiple formats per device.

UNIVERSAL BUFFER FEATURES

- Wide operating frequency DC - 1.25 GHz
- 2-10 differential or 4-20 LVCMOS outputs
- Accepts any differential or single-ended input
- Pin-selectable signal format per bank (LVPECL, Low Power LVPECL, LVDS, CML, HCSL, LVCMOS)
- Ultra-low additive jitter: 45 fs rms (12 kHz - 20 MHz)
- 2:1 mux with glitchless clock switching
- Synchronous output enable/Individual output enable
- Integrated voltage level translation
- Selectable drive strength to tailor jitter/EMI performance
- Optional output clock division: div-1, div-2, div-4
- Low output-output skew: <50 ps
- Excellent PSRR
- Independent VDD and VDDO: 1.8, 2.5 or 3.3 V



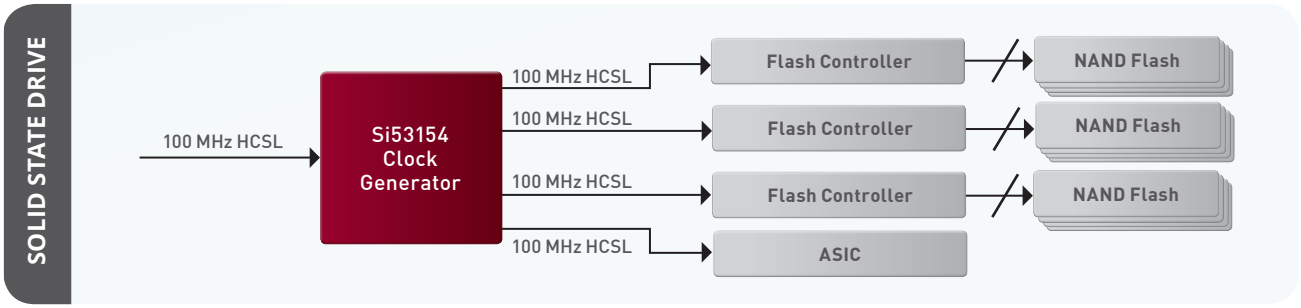
PART NUMBER	CLOCK INPUT/ OUTPUTS	ADDITIVE JITTER (RMS)	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	VDD	VDDO	OUTPUT	PACKAGE
Si53306	1/4	45 fs	1 - 725 MHz	1 - 725 MHz	1.8, 2.5, 3.3 V	1.8, 2.5, 3.3 V	LVPECL, LVDS, HCSL, LVCMOS, CML	QFN16
Si53301	2/6	100 fs	1 - 725 MHz	1 - 725 MHz	1.8, 2.5, 3.3 V	1.8, 2.5 V	LVPECL, LVDS, HCSL, LVCMOS, CML	QFN44
Si53302	2/10	100 fs	1 - 725 MHz	1 - 725 MHz	1.8, 2.5, 3.3 V	1.8, 2.5 V	LVPECL, LVDS, HCSL, LVCMOS, CML	QFN44
Si53320	2/10	100 fs	1 - 725 MHz	1 - 725 MHz	2.5, 3.3 V	2.5, 3.3 V	LVPECL	TSSOP20
Si53321	2/10	45 fs	DC - 1250 MHz	DC - 1250 MHz	2.5, 3.3 V	2.5, 3.3 V	LVPECL	QFN32, QFP32
Si53322	1/2	45 fs	DC - 1250 MHz	DC - 1250 MHz	2.5, 3.3 V	2.5, 3.3 V	LVPECL	QFN16
Si53323	2/4	45 fs	DC - 1250 MHz	DC - 1250 MHz	2.5, 3.3 V	2.5, 3.3 V	LVPECL	QFN16
Si53340	2/4	45 fs	DC - 1250 MHz	DC - 1250 MHz	1.8, 2.5, 3.3 V	1.8, 2.5, 3.3 V	LVDS	QFN16
Si53360	1/8	100 fs	1 - 200 MHz	1 - 200 MHz	1.8, 2.5, 3.3 V	1.8, 2.5 V	LVCMOS	TSSOP16
Si5330	1/4	150 fs	5 - 710 MHz	5 - 710 MHz	1.8, 2.5, 3.3 V	1.8, 2.5, 3.3 V	LVPECL, LVDS, HCSL, SSTL, HSTL	QFN24
Si5335	1/4	150 fs	1 - 350 MHz	1 - 350 MHz	1.8, 2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL,CML	QFN24
SL18860DC	1/3	—	10 - 52 MHz	10 - 52 MHz	1.8, 2.5, 3.3 V	—	LVCMOS	TDFN10
SL2304NZ	1/4	—	1 - 140 MHz	1 - 140 MHz	3.3 V	—	LVCMOS	8TSSOP/8SOIC
SL23EP04NZ	1/4	—	DC - 220 MHz	DC - 220 MHz	2.5 V, 3.3 V	—	LVCMOS	TSSOP8
SL2305NZ	1/5	—	1 - 140 MHz	1 - 140 MHz	3.3 V	—	LVCMOS	TSSOP8/SOIC8
SL2309NZ	1/9	—	DC - 140 MHz	DC - 140 MHz	3.3 V	3.3 V	LVCMOS	SOIC16
SL23EP09NZ	1/9	—	1 - 220 MHz	1 - 220 MHz	2.5 V, 3.3 V	—	LVCMOS	TSSOP16/SOIC16

PCI Express Clock Buffers (PCIe)

Silicon Labs offers the lowest power, highest performance PCI-Express clock generators on the market. All devices in feature low power push-pull output buffer technology, providing benefits of low power consumption, reduced external terminating resistors and smaller packaging. To optimize performance, the devices support programmable drive strength, rise/fall times and output impedance. Support for down spread spectrum clock generation is also provided. The devices support the standard HCSL PCIe signal format and can be externally terminated to support LVPCEL, LVDS or CML levels.

PCIe CLOCK BUFFER FEATURES

- Complete portfolio of PCI Express Gen 1/2/3 clocks/buffers
- Push-pull HCSL output buffer technology
- Fully integrated termination resistors on PCIe outputs
- Low power consumption
- Programmable spread spectrum
- Available pin-strapping for spread enable
- I²C/SMBus programmable
- Supports optional LVPECL, LVDS, or CML levels
- -40 to 85 °C operation
- Individual output enable control
- Small form factor QFN packaging



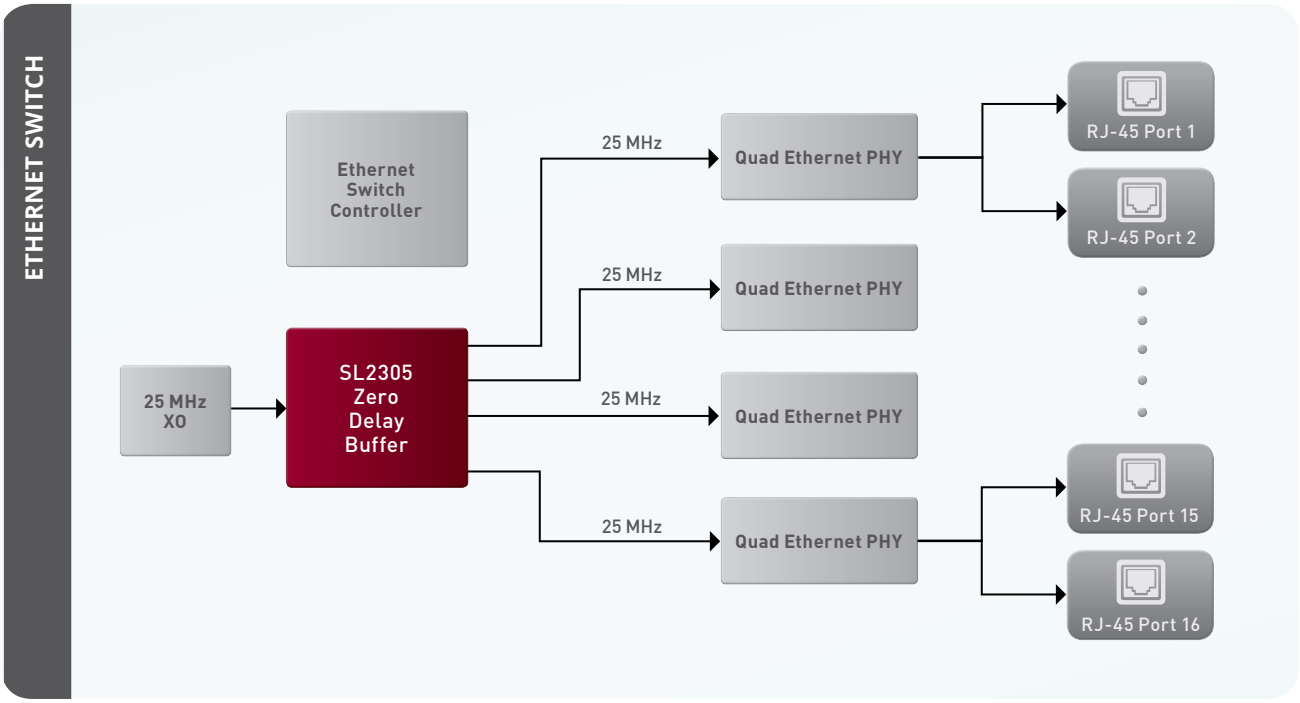
PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PHASE JITTER (RMS)	VDD	VDDO	OUTPUT	PACKAGE
Si53102	—	1/2	100 MHz	100 MHz	0.2 ps	2.5, 3.3 V	—	HSCL	TDFN8
Si53152	Pin/I²C	1/2	100 MHz	100 MHz	0.1 ps	3.3 V	3.3 V	HCSL	QFN24
Si53154	Pin/I²C	1/4	100 MHz	100 MHz	0.1 ps	3.3 V	3.3 V	HSCL	QFN24
Si53156	Pin/I²C	1/6	100 MHz	100 MHz	0.1 ps	3.3 V	3.3 V	HSCL	QFN32
Si53159	Pin/I²C	1/9	100 MHz	100 MHz	0.1 ps	3.3 V	3.3 V	HSCL	QFN48

Zero Delay Buffers

Silicon Labs' zero delay clock buffers are used in applications that require zero propagation delay between the input and output clocks. Silicon Labs' zero delay buffers provide low power consumption and simplify the distribution of spread spectrum clocks.

ZERO DELAY BUFFER FEATURES

- Low propagation delay
- Low output-to-output skew
- Low device-to-device skew
- Low output jitter
- Supports spread spectrum clock distribution
- Wide operation frequency from 10 to 220 MHz
- 3.3 V to 2.5 V power supply range
- Low power dissipation



PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PHASE JITTER (RMS)	VDD	VDDO	OUTPUT	PACKAGE
SL2305	Pin	1/5	1 - 140 MHz	1 - 140 MHz	—	3.3 V	—	LVCMOS	TSSOP8/SOIC8
SL2309	Pin	1/9	10 - 140 MHz	10 - 140 MHz	—	3.3 V	—	LVCMOS	TSSOP16/SOIC16
SL23EP04	Pin	1/4	10 - 220 MHz	10 - 220 MHz	—	2.5 V, 3.3 V	—	LVCMOS	SOIC8
SL23EP05	Pin	1/5	10 - 220 MHz	10 - 220 MHz	—	2.5 V, 3.3 V	—	LVCMOS	TSSOP8/SOIC8
SL23EP08	Pin	1/8	10 - 220 MHz	10 - 220 MHz	—	2.5 V, 3.3 V	—	LVCMOS	TSSOP16/SOIC16
SL23EP09	Pin	1/9	10 - 220 MHz	10 - 220 MHz	—	2.5 V, 3.3 V	—	LVCMOS	TSSOP16/SOIC16

Clock Generation

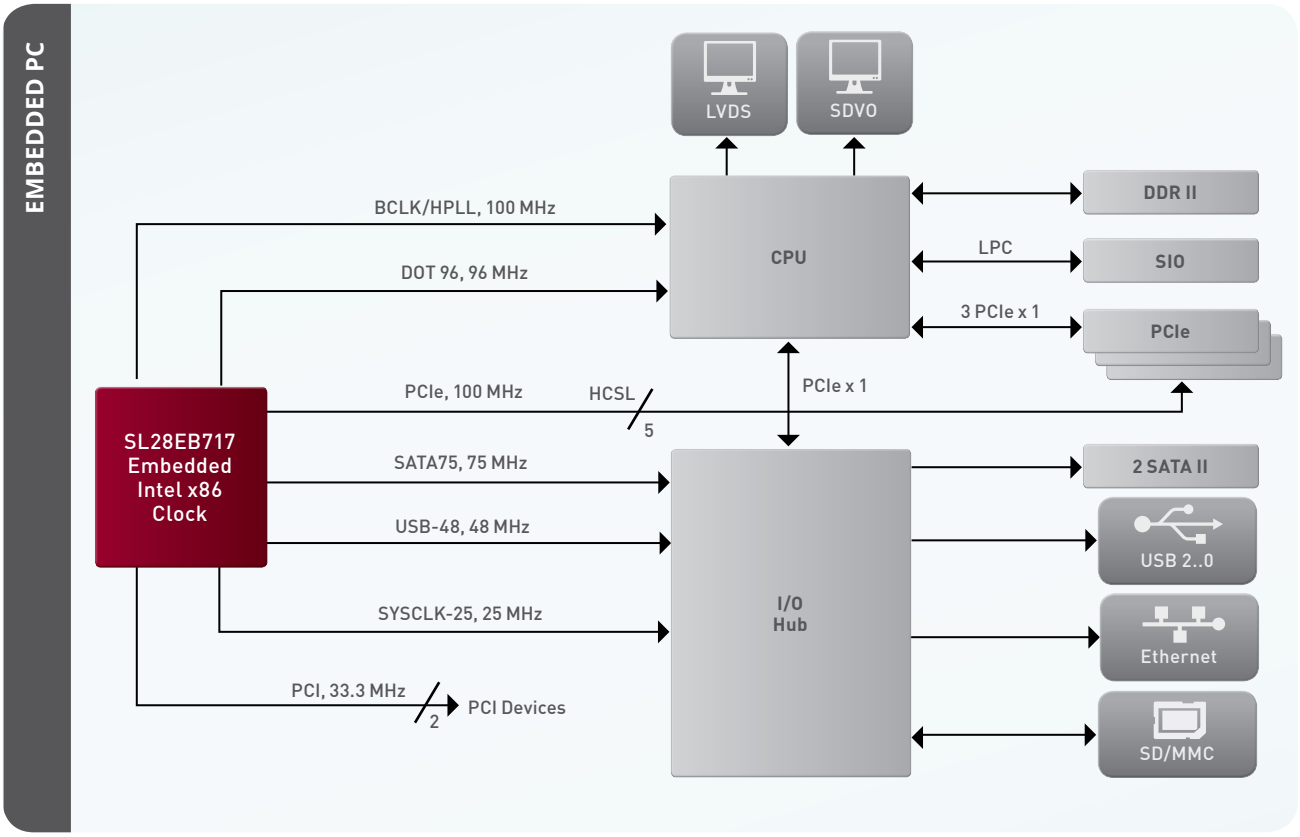
WEB-CONFIGURABLE FACTORY-CUSTOMIZED CLOCK GENERATORS AVAILABLE AT: www.silabs.com/custom-timing

Embedded Intel x86 Clocks

Silicon Labs offers an family of Intel-compliant x86 clocks for embedded computing, communications and industrial applications. These devices provide all necessary clock generation for the CPU, memory controller (chipset north bridge), I/O controller (chipset south bridge) as well as the latest timing requirements for industry standards such as SATA, USB, LAN, PCI Express and legacy PCI.

EMBEDDED INTEL x86 CLOCK FEATURES

- Clocking support for Intel processors
- Multi-PLL platform for independent, asynchronous signal generation
- Low power consumption push-pull differential buffers
- Available true differential current steering buffers
- Signal power management for notebook applications
- Dynamic enable/disable for PCIe hot plug applications
- Integrated voltage regulator and damping resistors on differential clocks
- Integrates external graphics clocking requirements
- Available center spread LCD clock for optimized display screen EMI reduction
- Integrated LAN clock for cost/component savings
- Integrated IEEE1394 clock for cost/space component savings
- 8-step programmable slew rate control for rise time and fall time control
- Dynamic independent PLL overclocking for enthusiast applications
- Underclocking capabilities for power management support and debugging
- Best in the industry spread spectrum technology for optimum system EMI reduction



Embedded Intel x86 Clocks (cont.)

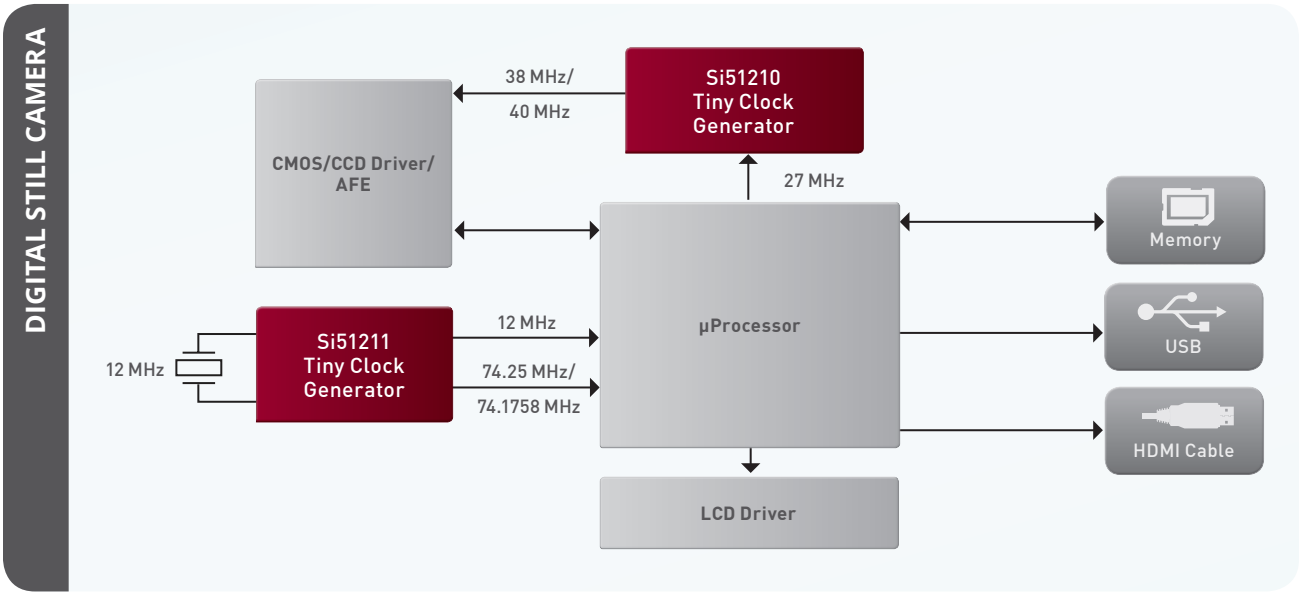
PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	VDD	VDDO	OUTPUT	PACKAGE
SL28EB717	Pin/I²C	1/13	25 MHz	12 MHz, 14.318 MHz, 25 MHz, 27 MHz, 33 MHz, 48 MHz, 75 MHz, 96 MHz, 83.33 MHz-166 MHz, 100 MHz	3.3 V	3.3 V	LVCMOS, HCSL	48QFN
SL28EB719	Pin/I²C	1/13	25 MHz	12 MHz, 14.318 MHz, 25 MHz, 27 MHz, 33 MHz, 48 MHz, 75 MHz, 96 MHz, 83.33 MHz-166 MHz, 100 MHz	3.3 V	3.3 V	LVCMOS, HCSL	TSSOP48
SL28EB740	Pin/I²C	1/16	25 MHz	12 MHz, 14.318 MHz, 25 MHz, 33 MHz, 48 MHz, 75 MHz, 96 MHz, 83.33 MHz-166 MHz, 100 MHz	3.3 V	3.3 V	LVCMOS, HCSL	TSSOP56
SL28EB742	Pin/I²C	1/16	14.318 MHz	14.3 MHz, 33 MHz, 48 MHz, 96 MHz, 100 MHz, 133 MHz, 166 MHz	3.3 V	3.3 V	LVCMOS, HCSL	QFN56

Tiny IoT Clocks

Silicon Labs' highly flexible, factory and I²C programmable tiny clock LVCMOS generators can be customized to generate multiple frequencies with significantly lower jitter, lower power and smaller size than competing solutions making them an ideal fit for Internet of Things (IoT) applications. Customization options are available for frequency selection, output enable control, or minimizing EMI, including customizable spread percentage, modulation rate, output impedance and rise time/fall time.

Si512xx TINY IoT CLOCK FEATURES

- Up to three customizable output frequencies: 3 to 200 MHz
- Accepts 8 to 48 MHz crystal or 3 to 166 MHz reference clock
- Low cycle-to-cycle jitter: <150 ps
- Low power: 2.3 mA (typ) at 48 MHz output, 25 MHz xtal, VDD = 3.3 V
- Center spread modulation from 0.25 to 1.0%, (0.125% resolution)
- Programmable spread modulation rate from 30 - 62 kHz
- 4 Custom drive strength options for each output
- Customizable control pins (PD#/OE/SSON#/FS)
- 1.8, 2.5; 3.3
- Ultra-compact packages
  - 6-pin TDFN (1.2 mm x 1.4 mm x 0.75 mm)
  - 8-pin TDFN (1.6 mm x 1.4 mm x 0.75 mm)
- Factory programmable OTP
- Two week sample lead time



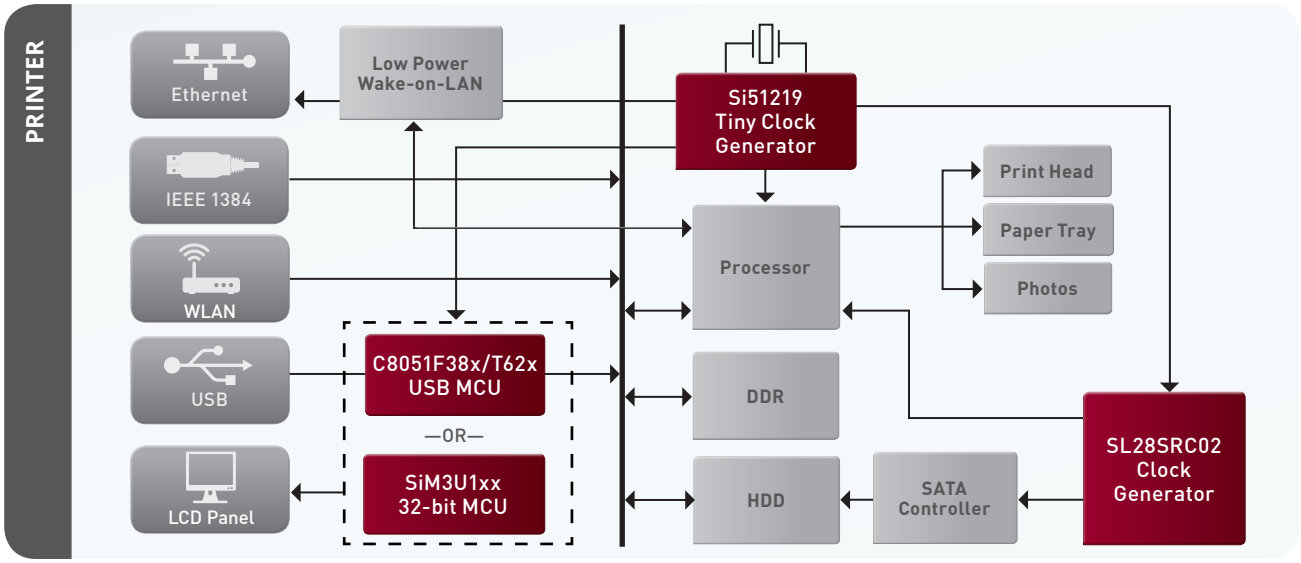
PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PERIOD JITTER (PP)	VDD	VDDO	OUTPUT	PACKAGE
Si51210	Pin	1/2	3 - 166 (Clock), 8 - 48 (Xtal)	3 to 200 MHz	—	2.5 to 3.3 V	—	LVCMOS	TDFN6
Si51211	Pin	1/3	3 - 166 (Clock), 8 - 48 (Xtal)	3 to 200 MHz	—	2.5 to 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	TDFN8
Si51214	Pin	1/2	3 - 166 (Clock), 8 - 48 (Xtal)	3 to 133 MHz	—	1.8 V	—	LVCMOS	TDFN6
Si51218	Pin	1/3	3 - 166 (Clock), 8 - 48 (xtal)	32 kHz to 200 MHz	—		2.5 to 3.3 V	LVCMOS	TDFN8
Si51219	Pin	1/3	3 - 166 (Clock), 8 - 48 (Xtal)	3 to 200 MHz	—	2.5 to 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	TSSOP8

EMI Reduction Clocks

Silicon Labs' programmable spread spectrum clock generators feature a wide range of programming options allowing system designers to minimize EMI at the application level. Configurable parameters include spread spectrum percentage/ modulation rate, programmable edge rates, programmable output impedance and programmable skew.

EMI REDUCTION CLOCK FEATURES

- Output frequencies from 1 to 200 MHz
- CLKOUT, REFCLK or SSCLK output options
- CLKIN or XO input options
- 8 to 48 MHz crystal input range
- 1 to 166 MHz clock input range
- Spread percent from 0 to 5.0%
- Down or center spread options
- Spread modulation frequency from 16 to 128 kHz
- On-chip load caps 8 to 20 pF
- User-definable control pins Powerdown, Output Enable, Spread Enable, Frequency Select, Spread Select control pins
- 7 programmable tr/tf options
- Industry's smallest SSCG: 1.2 mm x 1.4 mm



PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PHASE JITTER (RMS)	VDD	VDDO	OUTPUT	PACKAGE
SL15300	Pin	1/4	3 - 166 (Clock), 8 - 48 (Xtal)	3 - 200 MHz	—	1.8, 2.5, 3.3 V	—	LVCMOS	TSSOP8
SL16020DC	Pin/I²C	1/2	27 (Xtal)	27 MHz, 100 MHz	—	3.3 V	—	LVCMOS	TDFN10
Si5335	Pin	1/4	10 - 350 (Clock), 25/27 (Xtal)	1 - 350 MHz	1.0 ps	1.8, 2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML	QFN24
Si51210	Pin	1/2	3 - 166 (Clock), 8 - 48 (Xtal)	3 - 200 MHz	—	2.5 - 3.3 V	—	LVCMOS	TDFN6
Si51211	Pin	2/3	3 - 166 (Clock), 8 - 48 (Xtal)	3 - 200 MHz	—	2.5 - 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	TDFN8
Si51214	Pin	1/2	3 - 166 (Clock), 8 - 48 (Xtal)	3 - 200 MHz	—	1.8 V	—	LVCMOS	TDFN6
Si51219	Pin	2/3	3 - 166 (Clock), 8 - 48 (Xtal)	3 - 200 MHz	—	2.5 - 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	TSSOP8
Si52142	Pin/I²C	1/3	25 MHz	100 MHz, 25 MHz	1.0 ps	3.3 V	3.3 V	HSCL, LVCMOS	QFN24
Si52143	Pin/I²C	1/5	25 MHz	100 MHz, 25 MHz	1.0 ps	3.3 V	3.3 V	HSCL, LVCMOS	QFN24
Si52144	Pin/I²C	1/4	25 MHz	100 MHz	1.0 ps	3.3 V	3.3 V	HSCL	QFN24
Si52146	Pin/I²C	1/6	25 MHz	100 MHz	1.0 ps	3.3 V	3.3 V	HSCL	QFN32
Si52147	Pin/I²C	1/9	25 MHz	100 MHz	1.0 ps	3.3 V	3.3 V	HSCL	QFN48

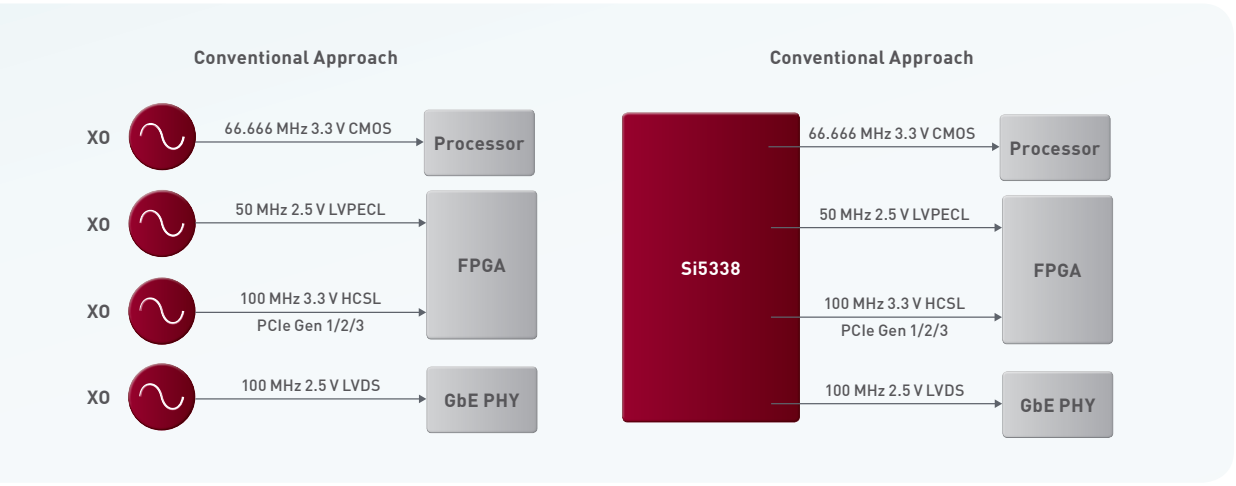
Any-Frequency, Any-Output Differential/CMOS Clocks (Si5338)

Silicon Labs' differential + LVCMOS clock generators provide any rate, any output frequency synthesis enabling a single device to replace multiple crystal oscillator and fixed-frequency clock generators. Any combination of output frequencies can be generated exactly with 0 ppm error. Independent signal format and VDDO options provide integrated level translation, supporting LVPECL/LVDS/HCSL/LVCMOS clock generation up to 710 MHz with sub 1 ps rms phase jitter.

Si5338 FEATURES

- Generates any frequency on any output, from 160 kHz to 350 MHz and select frequencies to 710 MHz
- Exact clock synthesis (0 ppm error)
- Crystal or clock input
- 4 differential outputs or 8 single-ended outputs
- Any format, any output: LVPECL, LVDS, HCSL, LVCMOS, HSTL, SSTL and CML
- Independent VDDO per output eliminates external level translators (1.5, 1.8, 2.5, 3.3 V)
- Low phase jitter: 1 ps rms
- I²C programmable or pin-controlled
- Excellent PSRR, no discrete components
- Spread spectrum clock generation
- User-definable control pins: Powerdown, Output Enable, Frequency Select, Spread Select
- Factory-customizable clocks w/2 week lead times
  www.silabs.com/custom-timing

CLOCK TREE SIMPLIFIED



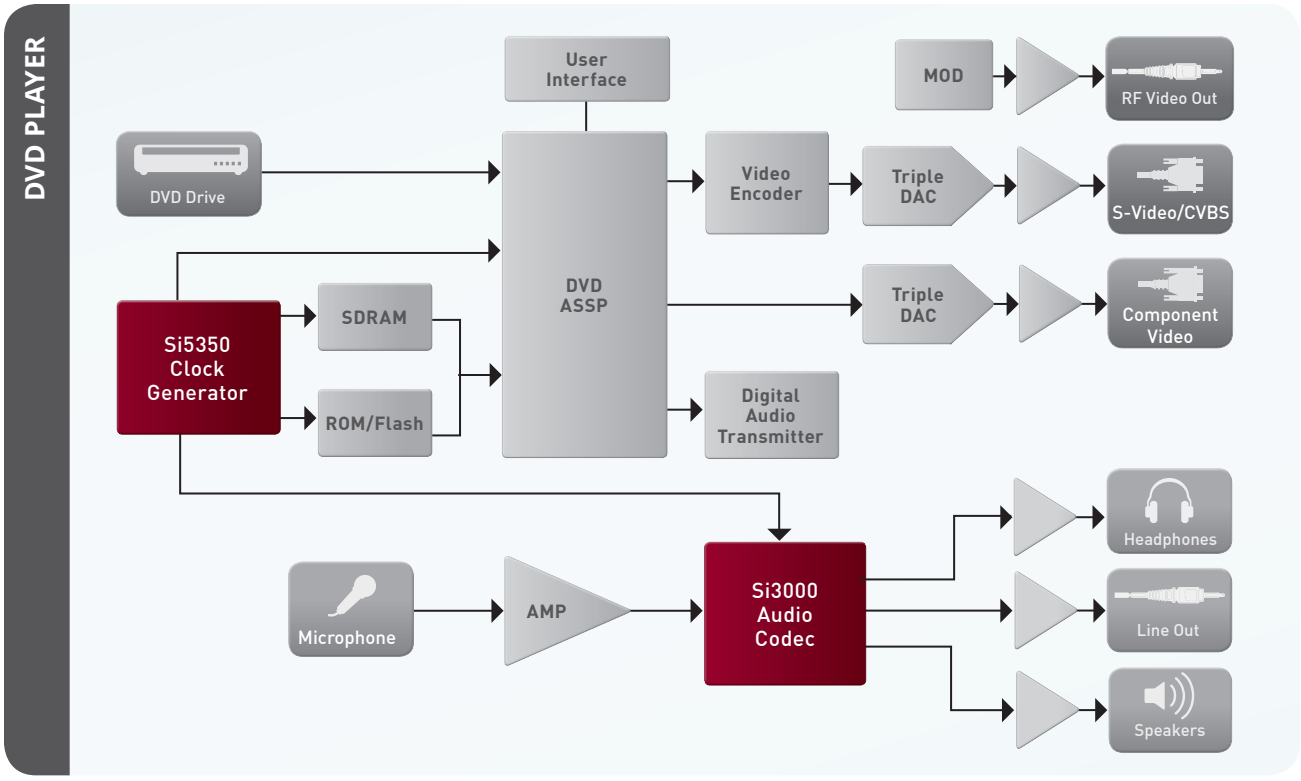
PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHZ)	OUTPUT FREQUENCY (MHZ)	PHASE JITTER (RMS)	VDD	VDDO	OUTPUT	PACKAGE
Si5335	Pin	1/4	10 - 350 (Clock), 25/27 (Xtal)	1 - 350 MHz	1.0 ps	1.8, 2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML	QFN24
Si5338	I²C	1/4	5 - 710 (Clock), 8 - 30 (Xtal)	0.16 - 710 MHz 0.16 - 350 MHz 0.16 - 200 MHz	1.0 ps	1.8, 2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML	QFN24

Any-Frequency, Any-Output CMOS Clocks (Si5350)

Silicon Labs' highly flexible factory and I²C programmable LVCMOS clock generators can be customized to generate multiple independent non-integer-related frequencies with equivalent frequency synthesis capability of 8 PLLs, with exact frequency synthesis (0 ppm error), significantly lower jitter, lower power and smaller size than competing solutions. Factory customization options are available to minimize EMI, including configurable edge rates, output impedance, output skew and spread spectrum.

Si5350 FEATURES

- Generates any frequency on any output, 8 kHz to 160 MHz
- Exact clock synthesis: 0 ppm error
- Similar frequency flexibility as 8 independent PLLs
- Crystal or clock input
- <100 ps pk-pk period jitter
- Glitchless switching between output frequencies
- I²C programmable or pin-controlled
- Excellent PSRR: no discrete components
- Two week sample lead time for any custom clock
- Spread spectrum clock generation -0.1 to -2.5% down, ±0.1 to ±1.5% center
- User-definable control pins Powerdown, Output Enable, Spread Enable, Frequency Select control pins
- Small form factor; MSOP10, QFN20



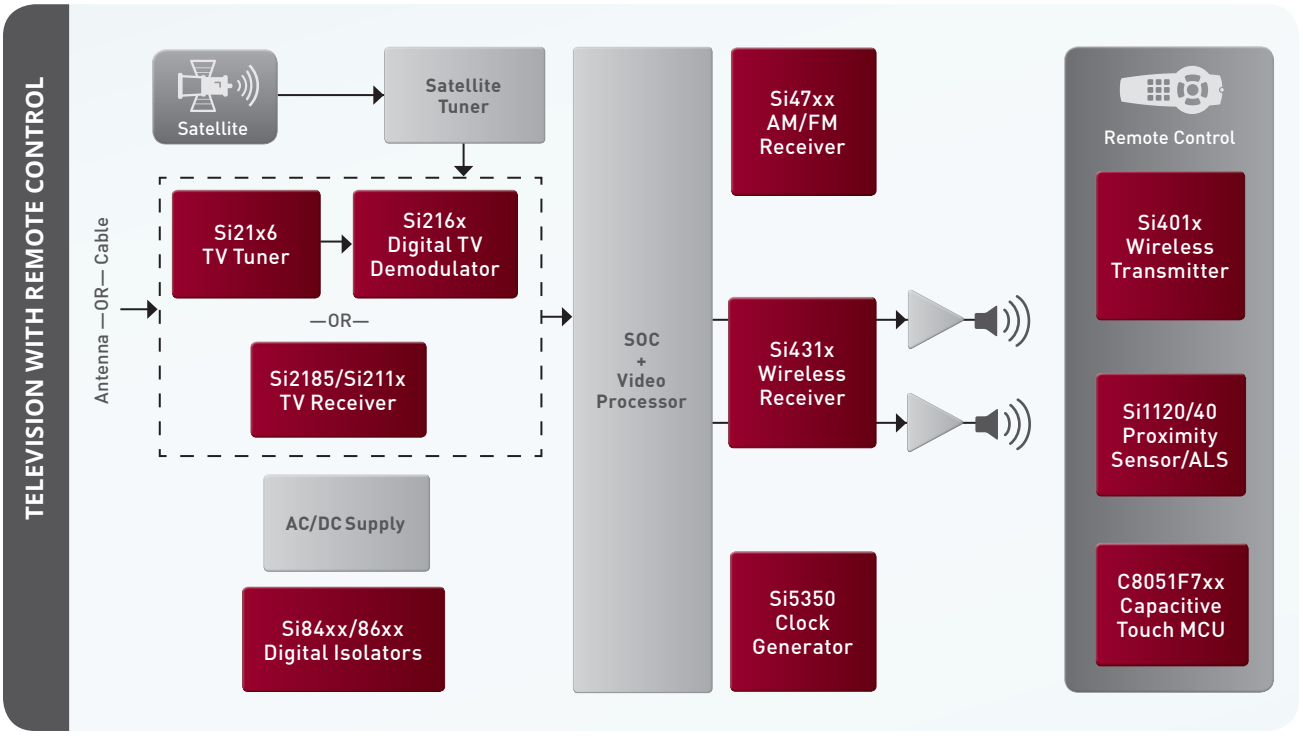
PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PERIOD JITTER (PP)	VDD	VDDO	OUTPUT	PACKAGE
Si5350A/51A	Pin/I²C	1/3 or 8	25/27 (Xtal)	8 kHz - 160 MHz	100 ps	2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	MSOP10, QFN20
Si5350C/51C	Pin/I²C	1/3 or 8	10 - 100 (Clock), 25/27 (Xtal)	8 kHz - 160 MHz	100 ps	2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	MSOP10, QFN20
Si5350A	Pin	1/3	25/27 (Xtal)	8 kHz to 160 MHz	100 ps	2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	MSOP10
Si5350C	Pin	1/3	10 - 100 (Clock), 25/27 (Xtal)	8 kHz to 160 MHz	100 ps	2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	MSOP10
Si5351A	I²C	1/3	25/27 (Xtal)	8 kHz to 160 MHz	100 ps	2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	MSOP10

Any-Frequency CMOS Clock Generator + VCXOs

These integrated clock + VCXO devices feature an integrated voltage controlled oscillator (VCXO), while eliminating the need for custom, pullable crystals. Free-running and VCXO clocks can be generated by one device, making them ideal for cost-sensitive consumer applications.

Si5350B/51B FEATURES

- Generates any frequency on any output, 8 kHz to 160 MHz
- Exact clock synthesis: 0 ppm error
- Similar frequency flexibility as 8 independent PLLs
- Accepts crystal and analog control voltage input (VCXO)
- <100 ps pk-pk period jitter for any configuration
- Glitchless switching between output frequencies
- Integrated VCXO uses standard non-pullable crystal
- I²C programmable or pin-controlled
- Excellent PSRR: no discrete components
- Two week sample lead time for any custom clock
- Spread spectrum clock generation -0.5 to -2.5% down, ±0.1 to ±1.5% center
- User-definable control pins Powerdown, Output Enable, Spread Enable or Frequency Select control pins
- Small form factor; MSOP10, QFN20



PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PERIOD JITTER (PP)	VDD	VDDO	OUTPUT	PACKAGE
Si5350B	Pin	1/3 or 8	25/27 (Xtal) VCXO	8 kHz - 160 MHz	100 ps	2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	MSOP10/QFN20
Si5351B	I²C	1/8	25/27 (Xtal) VCXO	8 kHz - 160 MHz	100 ps	2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS	QFN20

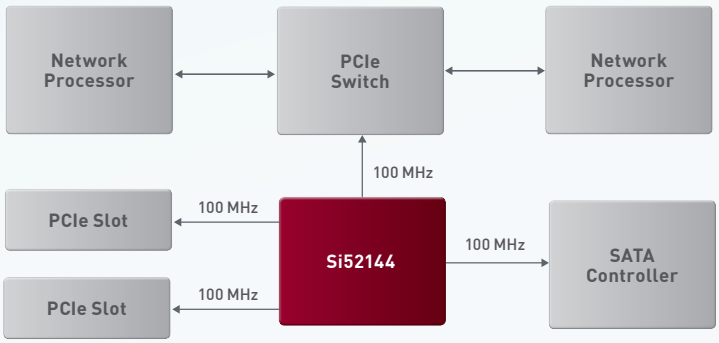
PCI Express Clock Generators (PCIe)

Silicon Labs offers the lowest power, highest performance PCI-Express clock generators on the market. All devices feature low power push-pull output buffer technology, providing benefits of low power consumption, reduced external terminating resistors and smaller packaging. To optimize performance, the devices support programmable drive strength, rise/fall times and output impedance. Support for down spread spectrum clock generation is also provided. The devices supprt the standard PCIe HCSL signaling format and can be externally terminated to support LVPECL, LVOS or CML levels.

PCIe CLOCK GENERATOR FEATURES

- Complete portfolio of PCI Express Gen 1/2/3 clocks/buffers
- Push-pull HCSL output buffer technology
- Fully integrated termination resistors on PCIe outputs
- Low power consumption
- Programmable spread spectrum
- Available pin strapping for spread enable
- I²C/SMBus programmable
- Supports optional LVPECL, LVDS, or CML levels
- -40 to 85 °C operation
- Individual output enable control
- Small form factor QFN packaging

IP GATEWAY



PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PHASE JITTER (RMS)	VDD	VDDO	OUTPUT	PACKAGE
Si52111		1/1	25 MHz	100 MHz	1.0 ps	3.3 V	3.3 V	HCSL	TDFN10
Si52112		1/2	25 MHz	100 MHz	1.0 ps	3.3 V	3.3 V	HCSL	TDFN10
Si52142	Pin/I²C	1/3	25 MHz	100 MHz, 25 MHz	1.0 ps	3.3 V	3.3 V	HSCL, LVCMOS	QFN24
Si52143	Pin/I²C	1/5	25 MHz	100 MHz, 25 MHz	1.0 ps	3.3 V	3.3 V	HSCL, LVCMOS	QFN24
Si52144	Pin/I²C	1/4	25 MHz	100 MHz	1.0 ps	3.3 V	3.3 V	HSCL	QFN24
Si52146	Pin/I²C	1/6	25 MHz	100 MHz	1.0 ps	3.3 V	3.3 V	HSCL	QFN32
Si52147	Pin/I²C	1/9	25 MHz	100 MHz	1.0 ps	3.3 V	3.3 V	HSCL	QFN48
Si5335	Pin	1/4	10 - 350 (Clock), 25/27 (Xtal)	1 - 350 MHz	1.0 ps	1.8, 2.5, 3.3 V	1.8, 2.5, 3.3 V	LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML	QFN24
Si5338	I²C	1/4	5 - 710 (Clock) 8 - 30 (Xtal)	0.16 - 710 MHz	1.0 ps	1.8, 2.5, 3.3 V	1.8, 2.5, 3.3 V	LVPECL, LVDS, LVCMOS, HCSL, SSTL, HSTL	QFN24

Jitter Attenuators

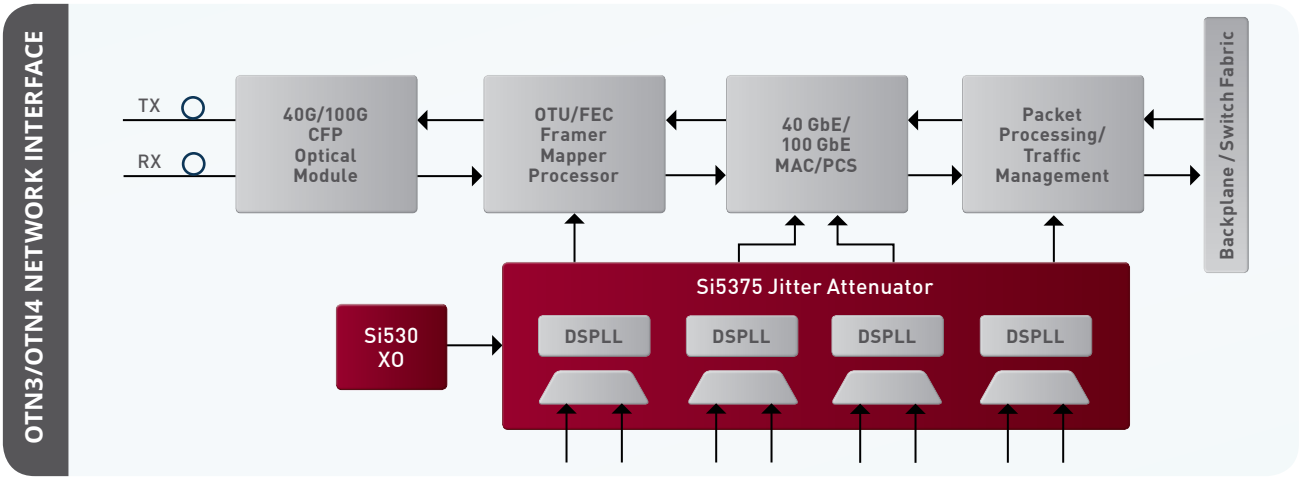
REQUEST SAMPLES AND DOWNLOAD DOCUMENTATION AT: www.silabs.com/clocks

Silicon Labs' jitter attenuators generate any output frequency from any input frequency while providing jitter cleaning and clock distribution in high-performance timing applications requiring sub 0.5 ps jitter performance. The devices accept multiple clock inputs ranging from 2 kHz to 710 MHz and generate multiple low jitter, independent, synchronous clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. These devices are based on Silicon Labs' proven third-generation DSPLL® technology, which generates any output frequency from any input frequency with 300 fs rms jitter performance in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components.

JITTER ATTENUATOR FEATURES

- Generates any output frequency from any input frequency
- Ultra-low jitter: 290 fs RMS
- 1-DSPLL and 4-DSPLL versions available
- Integrated loop filter with selectable loop bandwidth
- Hitless switching with phase buildout (auto/manual)
- Freerun or synchronous operating modes
- Best-in-class PSRR
- I²C/SPI or pin-controlled
- User-selectable output clock signal format (LVPECL, LVDS, CML, CMOS)
- Single supply: 1.8, 2.5 or 3.3 V ±10% operation
- Easy-to-use DSPLLsim* configuration software

*see page 16 for more about our DSPLLsim software



PART NUMBER	# OF PLLS	CONTROL	CLOCK INPUTS/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	JITTER (12 KHz TO 20 MHz)	PLL BANDWIDTH	HITLESS SWITCHING	DIGITAL HOLD	FREE RUN	SIGNAL FORMAT	PACKAGE
Si5315	1	Pin	2/2	0.008 - 644	0.008 - 644	450 fs rms typ	60 Hz - 8 kHz	•	•		CMOS, LVDS, LVPECL, CML	QFN36
Si5317	1	Pin	1/2	1 - 710	1 - 710	290 fs rms typ	60 Hz - 8 kHz		•			QFN36
Si5319	1	I²C/SPI	1/1	0.002 - 710	0.002 - 1417	300 fs rms typ	60 Hz - 8 kHz			•		QFN36
Si5324	1	I²C/SPI	2/2	0.002 - 710	0.002 - 1417	290 fs rms typ	4 Hz - 525 Hz	•	•	•		QFN36
Si5326	1	I²C/SPI	2/2	0.002 - 710	0.002 - 1417	300 fs rms typ	60 Hz - 8 kHz	•	•	•		QFN36
Si5327	1	I²C/SPI	2/2	0.002 - 710	0.002 - 808	500 fs rms typ	4 Hz - 525 Hz	•	•	•		QFN36
Si5368	1	I²C/SPI	4/5	0.002 - 710	0.002 - 1417	300 fs rms typ	60 Hz - 8 kHz	•	•	•		TQFP100
Si5369	1	I²C/SPI	4/5	0.002 - 710	0.002 - 1417	300 fs rms typ	4 Hz - 525 Hz	•	•	•		TQFP100
Si5374	4	I²C	8/8	0.002 - 710	0.002 - 808	410 fs rms typ	4 Hz - 525 Hz	•	•	•		BGA80
Si5375	4	I²C	4/4	0.002 - 710	0.002 - 808	410 fs rms typ	60 Hz - 8 kHz		•	•		BGA80
Si5376	4	I²C	8/8	0.002 - 710	0.002 - 808	410 fs rms typ	60 Hz - 8 kHz	•	•	•		BGA80

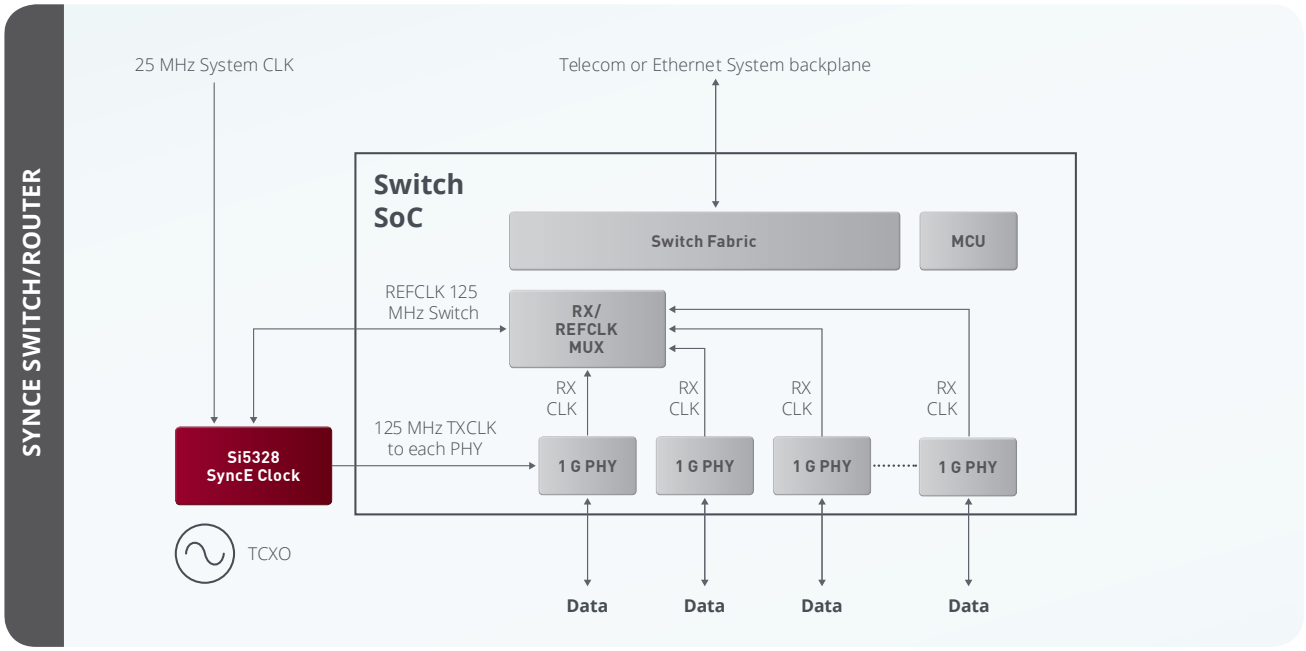
Synchronous Ethernet Clocks

REQUEST SAMPLES AND DOWNLOAD DOCUMENTATION AT: www.silabs.com/synce

Silicon Labs Synchronous Ethernet (SyncE) locks provide full compliance with ITU G.8262 requirements while providing any-frequency synthesi, jitter cleaning and wander filtering. The Si5328 offers the industry's lowest jitter SyncE clock, making it ideal for checking Ethernet PHYs from GbE to 100 GbE.

SYNCE CLOCK FEATURES

- Fully compliant with SyncE clock requirements (ITU G.8262)
- Generates any output frequency (8 kHz to 808 MHz) from any input frequency (8 kHz to 710 MHz)
- Dual clock outputs with 0.3 ps RMS jitter and any signal format (LVDS, LVPECL, CML, CMOS)
- Integrated loop filter with selectable loop bandwidths: 0.1 Hz; 1 to 10 Hz
- Compact factor 6 mm x 6 mm QFN
- Reprogrammable to any frequency without BOM changes



PART NUMBER	# OF INPUTS	INPUT CLOCK FREQUENCY RANGE	# OUTPUT CLOCKS	OUTPUT CLOCK FREQUENCY RANGE	PHASE JITTER (RMS TYP)	EEC OPTION 1 AND 2 WANDER FILTERING	PACKAGE
Si5328B	2	8 kHz - 710 MHz	2	8 kHz - 808 MHz	0.3 ps	Yes	QFN36
Si5328C	2	8 kHz - 346 MHz	2	8 kHz - 346 MHz	0.3 ps	Yes	QFN36

Software Tools

FULL DOCUMENTATION, SOFTWARE AND APPLICATION NOTES ARE AVAILABLE AT: www.silabs.com/timing

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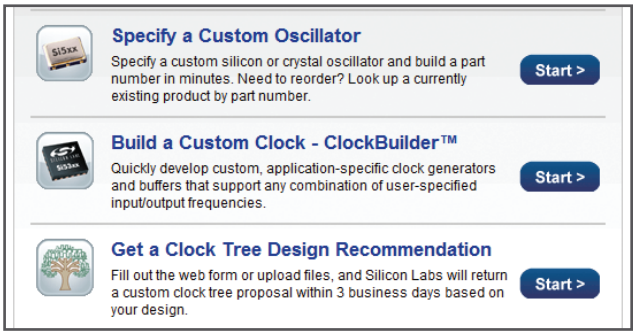

SUPPORTED DEVICES	CONTROL	SOFTWARE
Si5340/1, Si5342/4/5, Si5346/7	N/A	ClockBuilder Pro Software
Si5340/1, Si5342/4/5, Si5346/7	N/A	ClockBuilder Go App for iOS
Si5338, Si5334, Si5335, Si5356	I^2C	Si5338/35/34/56 ClockBuilder Desktop Software
Si5351	I^2C	Si5351 ClockBuilder Desktop Software
Si5350, Si5335, Si5355	N/A	ClockBuilder Web Utility
Si531x, Si532x, Si536x	N/A	DSPLLsim (Precision Clock EVB Software)
Si5374, Si5375, Si5376	N/A	Si537x DSPLLsim (Si537x Precision Clock EVB Software)
Si5040, Si5041	N/A	Si504x EVB Software
Si5320, Si5321, Si5364	N/A	Jitter Calculator

Timing Solutions for Communications Protocols

	PROTOCOL	DATA RATE (Gbps)	COMMON REF CLOCK (MHz)	SILICON LABS (XO)	SILICON LABS (VCXO)	SILICON LABS (CLOCK)
Video	SD/HD SDI	0.27, 1.485	27, 54, 108, 270	Si51x	Si51x	Si5324 (Genlock) Si5335/38
	3G SDI	2.97	148.5, 148.3516	Si53x	Si55x	Si5324 (Genlock) Si5335/38
	6G SDI	5.94	297, 296.7032	Si53x	Si55x	Si5324/45, Si5335/38
Computing	Fibre Channel	1.0625, 2.2125, 4.25, 8.5, 10.52, 14.025	106.25, 212.5, 75, 150	Si51x, Si53x	Si51x	Si5326/45, Si5335/38
	SAS	1.5, 3, 6	75	Si51x, Si50x	Si51x	Si5335/38, Si5350/51
	SAS12G	12	150	Si51x, Si50x	Si51x	Si5335/38, Si5355/56
	SATA	1.5, 3, 6	100	Si51x, Si50x	Si51x	Si5335/38, Si5350/51
Communications	ASI	0.27	54	Si51x	Si51x	Si5335/38
	CEI-6G/SR/LR	4.976 - 6.375	159.38	Si51x	Si51x	Si5335/38
	CEI-28G/VSR	19.9 - 28.05	156.25, 312.5	Si53x	Si55x	Si5326/45
	CPRI	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144, 9.8304	61.44, 122.88	Si53x	Si55x	Si5380
	Display Port	1.62, 2.7	162, 270	Si501	—	Si5350/51
	10 GbE XAUI	3.125	156.25	Si51x	Si51x	Si5335/38
	40G/100G Ethernet	10.3125	644.1328	Si53x	Si55x	Si5326/45
	GbE Ethernet	1.25	25, 100, 125	Si51x	Si51x	Si5326/45, Si5335/38
	GPON	1.244 (up), 2.488 (down)	155.52	Si51x	Si51x	Si5326/45, Si5335/38
	JESD204B	12.5, 6.375	125, 153.6, 156.25	—	—	Si5380
	OTN OTU-2	10.709	669.3125	Si53x	Si55x	Si5326/45
	OTN 10 GbE with FEC	11.1, 11.3	693.483	Si53x	Si55x	Si5326/45
	IEEE 802.3ba 10GBASE-KR	10.3125	322.2656, 644.5312	Si53x	Si55x	Si5326/45
	Interlaken	3.125 - 12.5	312.5, 322.2656	Si53x, Si51x	Si55x, Si51x	Si5326, Si5335/38
	OBSAI	0.768, 1.536, 3.072, 6.144	76.8, 115.2, 153.6	Si53x	Si55x	Si5380
	PCIe Gen1 Gen2	2.5, 5	100, 125	Si51x	Si51x	Si5335/38, Si5121x
	PCIe Gen3	8	100, 125	Si51x	Si51x	Si5335/38, Si5121x
	SGMII/QSGMII	1.25, 4 x 1.25	125	Si51x, Si59x	Si51x, Si59x	Si5335/38
	RXAUI	6.25	156.25, 312.5	Si51x, Si59x	Si51x, Si59x	Si5335/38
	QPI	6.4	100, 133.33, 200, 250, 266.67, 333.33, 400	Si51x, Si59x	Si51x, Si59x	Si5335/38
	Serial Rpid IO	1.25, 2.5, 3.125, 5, 6.25	125, 156.25, 312.5	Si51x	Si51x	Si5335/38, Si5350/51
	SFI-5.1	2.488 - 3.125	621, 321.5, 156.25	Si51x	Si51x	Si5335/38
	SFI-5.2	9.9 - 11.3	62.5, 100, 125, 156.25, 322.2656, 644.53125	Si53x	Si55x	Si5326/45
	SONET OC_3/12/48/192/768	0.155, 0.622, 2.488, 9.953	19.44, 77.76, 155.52, 622.08	Si51x, Si53x	Si51x, Si55x	Si5326/45, Si5335/38
	V-by-One	3, 3.75	Varied	Si51x	Si51x	Si5335/38
	10GbE XFI	10.3125	161.1328	Si51x, Si53x	Si51x, Si55x	Si5326/45, Si5335/38

Silicon Labs' products are designed and manufactured to ISO 9001, ISO 14001 and ISO/TS 16949 standards.

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WEB, June 2014, Rev I SEL-CLK

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