# SLG46531

## GreenPAK 5
## Programmable Mixed Signal Matrix

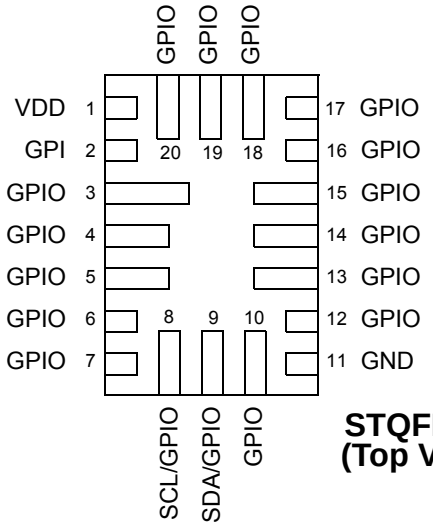
### Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macro Cells
- Read Back Protection (Read Lock)
- 1.8 V (±5%) to 5 V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch

### Applications

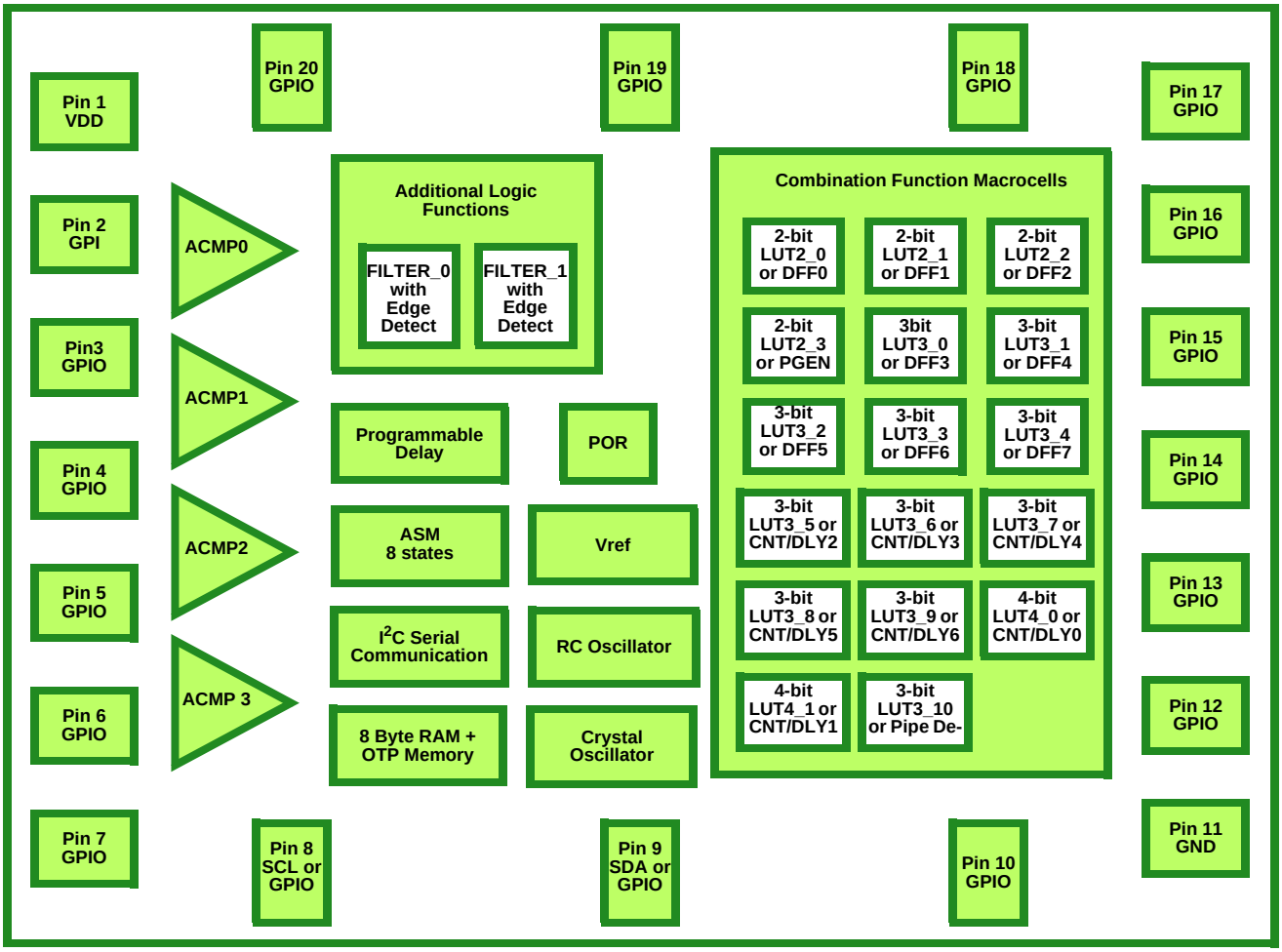
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

### Pin Configuration




**STQFN-20**
**(Top View)**

### Block Diagram



## 1.0 Overview

The SLG46531 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macro cells of the SLG46531. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macro cells in the device include the following:

- Four Analog Comparators (ACMP)
- Two Voltage References (Vref)
- Seventeen Combination Function Macrocells
  - Three Selectable DFF/Latch or 2-bit LUTs
  - One Selectable Continuous DFF/Latch or 3-bit LUT
  - Four Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Five 8-bit delays/counters or 3-bit LUTs
  - Two 16-bit delays/counters or 4-bit LUTs
- Asynchronous State Machine
  - Eight States
  - Flexible input logic from state transitions
- Serial Communications
  - $I^2C$ Protocol compliant
- Pipe Delay – 16 stage/3 output (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Functions – 2 Deglitch Filters with Edge Detectors
- Two Oscillators (OSC)
  - Configurable 25 kHz/2 MHz
  - 25 MHz RC Oscillator
- Crystal Oscillator
- Eight Byte RAM + OTP User Memory
  - RAM Memory space that is readable and writeable via $I^2C$
  - User defined initial values transferred from OTP

## 2.0 Pin Description

### 2.1 Functional Pin Description

| Pin # | Pin Name | Function |
|---|---|---|
| 1 | VDD | Power Supply |
| 2 | GPI | General Purpose Input |
| 3 | GPIO | General Purpose I/O with OE |
| 4 | GPIO | General Purpose I/O |
| 5 | GPIO | General Purpose I/O with OE |
| 6 | GPIO | General Purpose I/O or Analog Comparator 0 (+) |
| 7 | GPIO | General Purpose I/O with OE or External Vref (ACMP0 IN-) |
| 8 | SCL/GPIO | General Purpose I/O SCL or GPIOD (NMOS open drain only) |
| 9 | SDA/GPIO | General Purpose I/O SDA or GPIOD (NMOS open drain only) |
| 10 | GPIO | General Purpose I/O with OE or Analog Comparator 1 (+) |
| 11 | GND | Ground |
| 12 | GPIO | General Purpose I/O or External Vref (ACMP1 IN-) |
| 13 | GPIO | General Purpose I/O with OE or Analog Comparator 2 (+) |
| 14 | GPIO | General Purpose I/O with OE or External Vref (ACMP2 IN-) |
| 15 | GPIO | General Purpose I/O or Analog Comparator 3 (+) |
| 16 | GPIO | General Purpose I/O with OE |
| 17 | GPIO | General Purpose I/O |
| 18 | GPIO | General Purpose I/O with OE and Vref output (VREF1) |
| 19 | GPIO | General Purpose I/O with OE and Vref output (VREF0) |
| 20 | GPIO | General Purpose I/O or External Clock Input |

## 3.0 User Programmability

The SLG46531 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to construct combinatorial logic elements. Three of the I/O Pins provide a connection for the bit patterns into the OTP on board memory. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Silego to integrate into a production process.

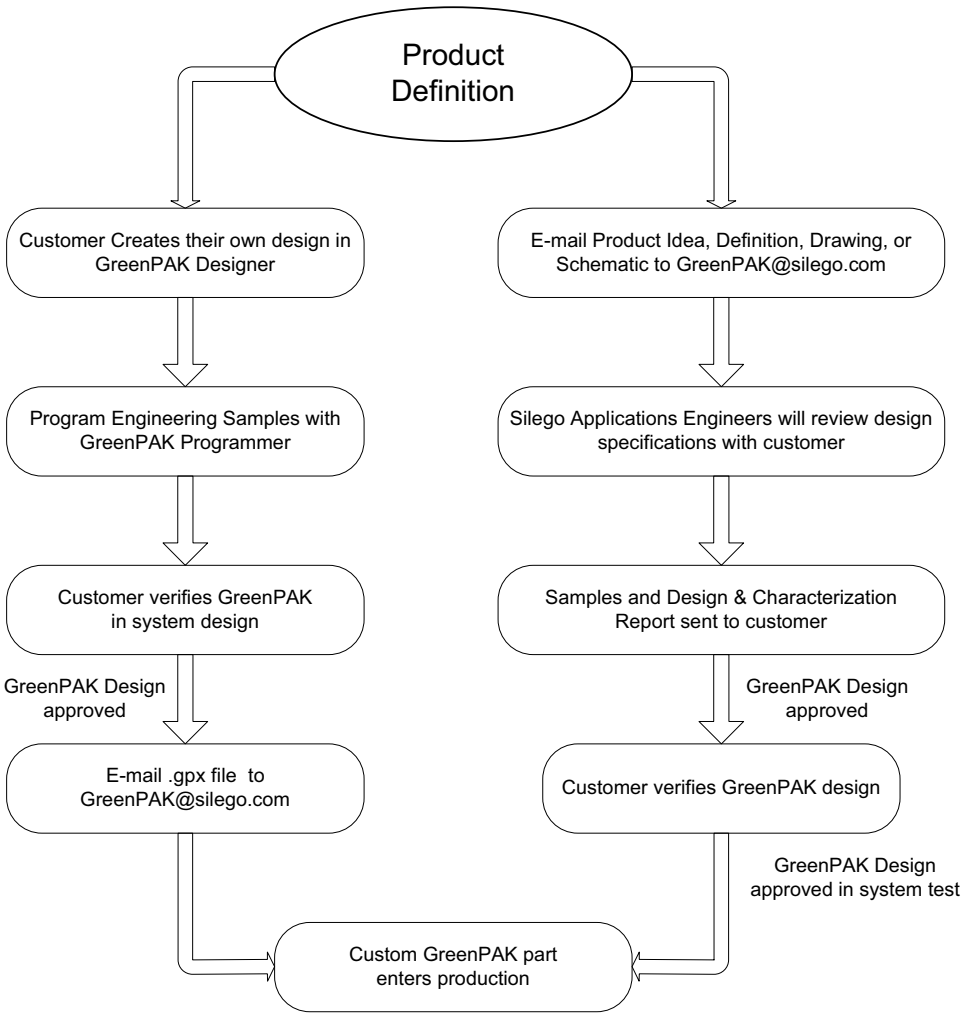



**Figure 1. Steps to create a custom Silego GreenPAK device**

## 4.0 Ordering Information

| Part Number | Type |
|---|---|
| SLG46531V | 20-pin STQFN |
| SLG46531VTR | 20-pin STQFN - Tape and Reel (3k units) |

## 5.0 Electrical Specifications

### 5.1 Absolute Maximum Conditions

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| Supply voltage on VDD relative to GND | -0.5 | 7 | V |
| DC Input voltage | GND - 0.5 | VDD + 0.5 | V |
| Current at Input Pin | -1.0 | 1.0 | mA |
| Storage Temperature Range | -65 | 150 | °C |
| Junction Temperature | -- | 150 | °C |
| ESD Protection (Human Body Model) | 2000 | -- | V |
| ESD Protection (Charged Device Model) | 1300 | -- | V |
| Moisture Sensitivity Level | 1 | | |

### 5.2 Electrical Characteristics (1.8 V ±5% $V_{DD}$)

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 1.71 | 1.80 | 1.89 | V |
| $T_A$ | Operating Temperature | | -40 | 25 | 85 | °C |
| $V_{PP}$ | Programming Voltage | | 7.25 | 7.50 | 7.75 | V |
| $V_{ACMP}$ | ACMP Input Voltage Range | Positive Input | 0 | -- | $V_{DD}$ | V |
| | | Negative Input | 0 | -- | 1.0 | V |
| $V_{IH}$ | HIGH-Level Input Voltage | Logic Input | 1.06 | -- | $V_{DD}$ | V |
| | | Logic Input with Schmitt Trigger | 1.28 | -- | $V_{DD}$ | V |
| | | Low-Level Logic Input | 0.94 | -- | $V_{DD}$ | V |
| $V_{IL}$ | LOW-Level Input Voltage | Logic Input | 0 | -- | 0.76 | V |
| | | Logic Input with Schmitt Trigger | 0 | -- | 0.49 | V |
| | | Low-Level Logic Input | 0 | -- | 0.52 | V |
| $V_{HYS}$ | Schmitt Trigger Hysteresis Voltage | Logic Input with Schmitt Trigger | 0.10 | 0.41 | 0.66 | V |
| $I_{LKG}$ | Input leakage (Absolute Value) | | -- | 1 | 1000 | nA |
| $V_{OH}$ | HIGH-Level Output Voltage | Push-Pull, $I_{OH}$ = 100 µA, 1X Driver | 1.69 | 1.79 | -- | V |
| | | PMOS OD, $I_{OH}$ = 100 µA, 1X Driver | 1.69 | 1.79 | -- | V |
| | | Push-Pull, $I_{OH}$ = 100 µA, 2X Driver | 1.70 | 1.79 | -- | V |
| | | PMOS OD, $I_{OH}$ = 100 µA, 2X Driver | 1.70 | 1.79 | -- | V |
| $V_{OL}$ | LOW-Level Output Voltage | Push-Pull, $I_{OL}$= 100 µA, 1X Driver | -- | 0.009 | 0.013 | V |
| | | Push-Pull, $I_{OL}$ = 100 µA, 2X Driver | -- | 0.004 | 0.006 | V |
| | | Open Drain, $I_{OL}$ = 100 µA, 1X Driver | -- | 0.006 | 0.009 | V |
| | | Open Drain, $I_{OL}$ = 100 µA, 2X Driver | -- | 0.003 | 0.004 | V |
| | | Open Drain NMOS 4X, $I_{OL}$ = 100 µA | -- | 0.001 | 0.002 | V |

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{OH}$ | HIGH-Level Output Current | Push-Pull, $V_{OH}$ = $V_{DD}$ - 0.2, 1X Driver | 1.07 | 1.70 | -- | mA |
| | | PMOS OD, $V_{OH}$ = $V_{DD}$ - 0.2, 1X Driver | 1.07 | 1.70 | -- | mA |
| | | Push-Pull, $V_{OH}$ = $V_{DD}$ - 0.2, 2X Driver | 2.22 | 3.41 | -- | mA |
| | | PMOS OD, $V_{OH}$ = $V_{DD}$ - 0.2, 2X Driver | 2.22 | 3.41 | -- | mA |
| $I_{OL}$ | LOW-Level Output Current | Push-Pull, $V_{OL}$ = 0.15 V, 1X Driver | 0.92 | 1.69 | -- | mA |
| | | Push-Pull, $V_{OL}$ = 0.15 V, 2X Driver | 1.83 | 3.38 | -- | mA |
| | | Open Drain, $V_{OL}$ = 0.15 V, 1X Driver | 1.38 | 2.53 | -- | mA |
| | | Open Drain, $V_{OL}$ = 0.15 V, 2X Driver | 2.75 | 5.07 | -- | mA |
| | | Open Drain NMOS 4X, $V_{OL}$ = 0.15 V | 7.21 | 9.00 | -- | mA |
| $V_O$ | Maximal Voltage Applied to any PIN in High-Impedance State | | -- | -- | $V_{DD}$ | V |
| $I_O$ | Maximal Average or DC Current | Total Current on Pin 2 – Pin 10 or on Pin 12 – Pin 20 | -- | -- | 90 | mA |
| $T_{SU}$ | Startup Time | From VDD rising past $PON_{THR}$ | 0.63 | 1.36 | 1.87 | ms |
| $PON_{THR}$ | Power On Threshold | $V_{DD}$ Level Required to Start Up the Chip | 1.41 | 1.54 | 1.66 | V |
| $POFF_{THR}$ | Power Off Threshold | $V_{DD}$ Level Required to Switch Off the Chip | 1.00 | 1.15 | 1.31 | V |
| $R_{PUP}$ | Pull Up Resistance | 1 M Pull Up | 859.8 | 1097.1 | 1358.9 | kΩ |
| | | 100 k Pull Up | 86.47 | 110.13 | 136.18 | kΩ |
| | | 10 k Pull Up | 10.82 | 12.86 | 15.36 | kΩ |
| $R_{PDWN}$ | Pull Down Resistance | 1 M Pull Down | 873.9 | 1097.0 | 1359.0 | kΩ |
| | | 100 k Pull Down | 88.89 | 110.53 | 136.55 | kΩ |
| | | 10 k Pull Down | 9.65 | 12.75 | 15.76 | kΩ |

### 5.3 Electrical Characteristics (3.3 V ±10% $V_{DD}$)

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| $T_A$ | Operating Temperature | | -40 | 25 | 85 | °C |
| $V_{PP}$ | Programming Voltage | | 7.25 | 7.50 | 7.75 | V |
| $V_{ACMP}$ | ACMP Input Voltage Range | Positive Input | 0 | -- | $V_{DD}$ | V |
| | | Negative Input | 0 | -- | 1.0 | V |
| $V_{IH}$ | HIGH-Level Input Voltage | Logic Input | 1.81 | -- | $V_{DD}$ | V |
| | | Logic Input with Schmitt Trigger | 2.14 | -- | $V_{DD}$ | V |
| | | Low-Level Logic Input | 1.06 | -- | $V_{DD}$ | V |
| $V_{IL}$ | LOW-Level Input Voltage | Logic Input | 0 | -- | 1.31 | V |
| | | Logic Input with Schmitt Trigger | 0 | -- | 0.97 | V |
| | | Low-Level Logic Input | 0 | -- | 0.67 | V |
| $V_{HYS}$ | Schmitt Trigger Hysteresis Voltage | Logic Input with Schmitt Trigger | 0.29 | 0.62 | 0.94 | V |
| $I_{LGK}$ | Input leakage (Absolute Value) | | -- | 1 | 1000 | nA |
| $V_{OH}$ | HIGH-Level Output Voltage | Push-Pull, $I_{OH}$ = 3 mA, 1X Driver | 2.70 | 3.12 | -- | V |
| | | PMOS OD, $I_{OH}$ = 3 mA, 1X Driver | 2.70 | 3.12 | -- | V |
| | | Push-Pull, $I_{OH}$ = 3 mA, 2X Driver | 2.85 | 3.21 | -- | V |
| | | PMOS OD, $I_{OH}$ = 3 mA, 2X Driver | 2.86 | 3.21 | -- | V |
| $V_{OL}$ | LOW-Level Output Voltage | Push-Pull, $I_{OL}$= 3 mA, 1X Driver | -- | 0.13 | 0.23 | V |
| | | Push-Pull, $I_{OL}$ = 3 mA, 2X Driver | -- | 0.06 | 0.11 | V |
| | | Open Drain, $I_{OL}$ = 3 mA, 1X Driver | -- | 0.08 | 0.15 | V |
| | | Open Drain, $I_{OL}$ = 3 mA, 2X Driver | -- | 0.04 | 0.08 | V |
| | | Open Drain NMOS 4X, $I_{OL}$ = 3 mA | -- | 0.02 | 0.04 | V |
| $I_{OH}$ | HIGH-Level Output Current | Push-Pull, $V_{OH}$ = 2.4 V, 1X Driver | 6.05 | 12.08 | -- | mA |
| | | PMOS OD, $V_{OH}$ = 2.4 V, 1X Driver | 6.05 | 12.08 | -- | mA |
| | | Push-Pull, $V_{OH}$ = 2.4 V, 2X Driver | 11.54 | 24.16 | -- | mA |
| | | PMOS OD, $V_{OH}$ = 2.4 V, 2X Driver | 11.52 | 24.16 | -- | mA |
| $I_{OL}$ | LOW-Level Output Current | Push-Pull, $V_{OL}$ = 0.4 V, 1X Driver | 4.88 | 8.24 | -- | mA |
| | | Push-Pull, $V_{OL}$ = 0.4 V, 2X Driver | 9.75 | 16.49 | -- | mA |
| | | Open Drain, $V_{OL}$ = 0.4 V, 1X Driver | 7.31 | 12.37 | -- | mA |
| | | Open Drain, $V_{OL}$ = 0.4 V, 2X Driver | 14.54 | 24.74 | -- | mA |
| | | Open Drain NMOS 4X, $V_{OL}$ = 0.4 V | 31.32 | 41.06 | -- | mA |
| $I_O$ | Maximum Average or DC Current | Per each chip side | -- | -- | 90 | mA |
| $V_O$ | Maximal Voltage Applied to any PIN in High-Impedance State | | -- | -- | $V_{DD}$ | V |
| $I_O$ | Maximal Average or DC Current | Total Current on Pin 2 – Pin 10 or on Pin 12 – Pin 20 | -- | -- | 90 | mA |

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{SU}$ | Startup Time | From VDD rising past $PON_{THR}$ | 0.61 | 1.24 | 1.65 | ms |
| $PON_{THR}$ | Power On Threshold | $V_{DD}$ Level Required to Start Up the Chip | 1.41 | 1.54 | 1.66 | V |
| $POFF_{THR}$ | Power Off Threshold | $V_{DD}$ Level Required to Switch Off the Chip | 1.00 | 1.15 | 1.31 | V |
| $R_{PUP}$ | Pull Up Resistance | 1 M Pull Up | 873.2 | 1094.7 | 1364.3 | kΩ |
| | | 100 k Pull Up | 85.17 | 109.30 | 135.52 | kΩ |
| | | 10 k Pull Up | 9.61 | 11.86 | 14.73 | kΩ |
| $R_{PDWN}$ | Pull Down Resistance | 1 M Pull Down | 862.5 | 1096.3 | 1357.4 | kΩ |
| | | 100 k Pull Down | 87.95 | 109.76 | 136.06 | kΩ |
| | | 10 k Pull Down | 8.66 | 11.81 | 15.05 | kΩ |

### 5.4 Electrical Characteristics (5 V ±10% $V_{DD}$)

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| $T_A$ | Operating Temperature | | -40 | 25 | 85 | °C |
| $V_{PP}$ | Programming Voltage | | 7.25 | 7.50 | 7.75 | V |
| $V_{ACMP}$ | ACMP Input Voltage Range | Positive Input | 0 | -- | $V_{DD}$ | V |
| | | Negative Input | 0 | -- | 1.0 | V |
| $V_{IH}$ | HIGH-Level Input Voltage | Logic Input | 2.68 | -- | $V_{DD}$ | V |
| | | Logic Input with Schmitt Trigger | 3.34 | -- | $V_{DD}$ | V |
| | | Low-Level Logic Input | 1.15 | -- | $V_{DD}$ | V |
| $V_{IL}$ | LOW-Level Input Voltage | Logic Input | 0 | -- | 1.96 | V |
| | | Logic Input with Schmitt Trigger | 0 | -- | 1.41 | V |
| | | Low-Level Logic Input | 0 | -- | 0.77 | V |
| $V_{HYS}$ | Schmitt Trigger Hysteresis Voltage | Logic Input with Schmitt Trigger | 0.44 | 0.90 | 1.38 | V |
| $I_{LGK}$ | Input leakage (Absolute Value) | | -- | 1 | 1000 | nA |
| $V_{OH}$ | HIGH-Level Output Voltage | Push-Pull, $I_{OH}$ = 5 mA, 1X Driver | 4.15 | 4.76 | -- | V |
| | | PMOS OD, $I_{OH}$ = 5 mA, 1X Driver | 4.16 | 4.76 | -- | V |
| | | Push-Pull, $I_{OH}$ = 5 mA, 2X Driver | 4.32 | 4.89 | -- | V |
| | | PMOS OD, $I_{OH}$ = 5 mA, 2X Driver | 4.33 | 4.89 | -- | V |
| $V_{OL}$ | LOW-Level Output Voltage | Push-Pull, $I_{OL}$= 5 mA, 1X Driver | -- | 0.19 | 0.24 | V |
| | | Push-Pull, $I_{OL}$ =5 mA, 2X Driver | -- | 0.09 | 0.12 | V |
| | | Open Drain, $I_{OL}$ = 5 mA, 1X Driver | -- | 0.12 | 0.16 | V |
| | | Open Drain, $I_{OL}$ = 5 mA, 2X Driver | -- | 0.07 | 0.08 | V |
| | | Open Drain NMOS 4X, $I_{OL}$ = 5 mA | -- | 0.03 | 0.05 | V |
| $I_{OH}$ | HIGH-Level Output Current | Push-Pull, $V_{OH}$ = 2.4 V, 1X Driver | 22.08 | 34.04 | -- | mA |
| | | PMOS OD, $V_{OH}$ = 2.4 V, 1X Driver | 22.08 | 34.04 | -- | mA |
| | | Push-Pull, $V_{OH}$ = 2.4 V, 2X Driver | 41.76 | 68.08 | -- | mA |
| | | PMOS OD, $V_{OH}$ = 2.4 V, 2X Driver | 41.69 | 68.08 | -- | mA |
| $I_{OL}$ | LOW-Level Output Current | Push-Pull, $V_{OL}$ = 0.4 V, 1X Driver | 7.22 | 11.58 | -- | mA |
| | | Push-Pull, $V_{OL}$ = 0.4 V, 2X Driver | 13.83 | 23.16 | -- | mA |
| | | Open Drain, $V_{OL}$ = 0.4 V, 1X Driver | 10.82 | 17.38 | -- | mA |
| | | Open Drain, $V_{OL}$ = 0.4 V, 2X Driver | 17.34 | 34.76 | -- | mA |
| | | Open Drain NMOS 4X, $V_{OL}$ = 0.4 V | 41.06 | 55.18 | -- | mA |
| $I_O$ | Maximum Average or DC Current | Per each chip side | -- | -- | 90 | mA |
| $V_O$ | Maximal Voltage Applied to any PIN in High-Impedance State | | -- | -- | $V_{DD}$ | V |
| $I_O$ | Maximal Average or DC Current | Total Current on Pin 2 – Pin 10 or on Pin 12 – Pin 20 | -- | -- | 90 | mA |

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{SU}$ | Startup Time | From VDD rising past $PON_{THR}$ | 0.60 | 1.23 | 1.61 | ms |
| $PON_{THR}$ | Power On Threshold | $V_{DD}$ Level Required to Start Up the Chip | 1.41 | 1.54 | 1.66 | V |
| $POFF_{THR}$ | Power Off Threshold | $V_{DD}$ Level Required to Switch Off the Chip | 1.00 | 1.15 | 1.31 | V |
| $R_{PUP}$ | Pull Up Resistance | 1 M Pull Up | 864.6 | 1093.4 | 1348.1 | kΩ |
| | | 100 k Pull Up | 84.32 | 108.97 | 135.24 | kΩ |
| | | 10 k Pull Up | 8.74 | 11.37 | 14.52 | kΩ |
| $R_{PDWN}$ | Pull Down Resistance | 1 M Pull Down | 873.3 | 1096.1 | 1370.5 | kΩ |
| | | 100 k Pull Down | 87.57 | 109.48 | 135.89 | kΩ |
| | | 10 k Pull Down | 7.95 | 11.33 | 14.78 | kΩ |

### 5.5 $I^2C$ Specifications

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{SCL}$ | Clock Frequency, SCL | $V_{DD}$ = (1.71...5.5) V | -- | -- | 400 | kHz |
| $t_{LOW}$ | Clock Pulse Width Low | $V_{DD}$ = (1.71...5.5) V | 1300 | | | ns |
| $t_{HIGH}$ | Clock Pulse Width High | $V_{DD}$ = (1.71...5.5) V | 600 | -- | -- | ns |
| $t_I$ | Input Filter Spike Suppression (SCL, SDA) | $V_{DD}$ = 1.8 V ± 5 % | -- | -- | 168 | ns |
| | | $V_{DD}$ = 3.3 V ± 10% | | | 157 | |
| | | $V_{DD}$ = 5.0 V ± 10 % | | | 156 | |
| $t_{AA}$ | Clock Low to Data Out Valid | $V_{DD}$ = (1.71...5.5) V | -- | -- | 900 | ns |
| $t_{BUF}$ | Bus Free Time between Stop and Start | $V_{DD}$ = (1.71...5.5) V | 1300 | -- | -- | ns |
| $t_{HD_STA}$ | Start Hold Time | $V_{DD}$ = (1.71...5.5) V | 600 | -- | -- | ns |
| $t_{SU_STA}$ | Start Set-up Time | $V_{DD}$ = (1.71...5.5) V | 600 | -- | -- | ns |
| $t_{HD_DAT}$ | Data Hold Time | $V_{DD}$ = (1.71...5.5) V | 0 | -- | -- | ns |
| $t_{SU_DAT}$ | Data Set-up Time | $V_{DD}$ = (1.71...5.5) V | 100 | -- | -- | ns |
| $t_R$ | Inputs Rise Time | $V_{DD}$ = (1.71...5.5) V | -- | -- | 300 | ns |
| $t_F$ | Inputs Fall Time | $V_{DD}$ = (1.71...5.5) V | -- | -- | 300 | ns |
| $t_{SU_STD}$ | Stop Set-up Time | $V_{DD}$ = (1.71...5.5) V | 600 | -- | -- | ns |
| $t_{DH}$ | Data Out Hold Time | $V_{DD}$ = (1.71...5.5) V | 50 | -- | -- | ns |

### 5.6 Asynchronous State Machine (ASM) Specifications

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{st_out_delay}$ | Asynchronous State Machine Output Delay Time | $V_{DD}$ = 1.8 V ± 5 % | 225 | -- | 275 | ns |
| | | $V_{DD}$ = 3.3 V ± 10% | 95 | | 118 | |
| | | $V_{DD}$ = 5.0 V ± 10 % | 67 | -- | 77 | |
| $t_{st_out}$ | Asynchronous State Machine Output Transition Time | $V_{DD}$ = 1.8 V ± 5 % | -- | -- | 165 | ns |
| | | $V_{DD}$ = 3.3 V ± 10% | | | 70 | |
| | | $V_{DD}$ = 5.0 V ± 10 % | | -- | 46 | |
| $t_{st_pulse}$ | Asynchronous State Machine Input Pulse Acceptance Time | $V_{DD}$ = 1.8 V ± 5 % | 29 | -- | -- | ns |
| | | $V_{DD}$ = 3.3 V ± 10% | 14 | | | |
| | | $V_{DD}$ = 5.0 V ± 10 % | 9.2 | -- | | |

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{st_comp}$ | Asynchronous State Machine Input Compete Time | $V_{DD}$ = 1.8 V ± 5 % | -- | -- | 29 | ns |
| | | $V_{DD}$ = 3.3 V ± 10% | | | 14 | |
| | | $V_{DD}$ = 5.0 V ± 10 % | | -- | 10 | |

### 5.7 IDD Estimator

**Table 1. Typical Current estimated for each block**

| Symbol | Parameter | Note | $V_{DD}$ = 1.8 V | $V_{DD}$ = 3.3V | $V_{DD}$ = 5.0V | Unit |
|---|---|---|---|---|---|---|
| I | Current | Chip Quiescent | 0.45 | 0.75 | 1.12 | µA |
| | | OSC 2 MHz, predivide = 1 | 41.48 | 64.00 | 94.89 | µA |
| | | OSC 2 MHz, predivide = 8 | 25.68 | 32.41 | 43.22 | µA |
| | | OSC 25 kHz, predivide = 1 | 7.16 | 7.94 | 9.25 | µA |
| | | OSC 25 kHz, predivide = 8 | 6.97 | 7.60 | 8.68 | µA |
| | | OSC 25 MHz, predivide = 1 | 87.25 | 238.27 | 428.66 | µA |
| | | OSC 25 MHz, predivide = 1, Force On | 87.25 | 238.27 | 428.67 | µA |
| | | OSC 25 MHz, predivide = 8 | 78.01 | 212.45 | 390.17 | µA |
| | | ACMP (each) | 54.96 | 52.64 | 60.81 | µA |
| | | ACMP with buffer (each) | 75.06 | 72.74 | 81.25 | µA |
| | | Vref (each) | 49.70 | 47.32 | 55.60 | µA |
| | | Vref with Buffer (each) | 71.93 | 71.27 | 79.62 | µA |

### 5.8 Timing Estimator

**Table 2. Typical Delay estimated for each block**

| Symbol | Parameter | Note | $V_{DD}$ = 1.8 V | | $V_{DD}$ = 3.3V | | $V_{DD}$ = 5.0V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | rising | falling | rising | falling | rising | falling | |
| tpd | Delay | Digital Input without Schmitt Trigger | 45 | 50 | 19 | 21 | 14 | 15 | ns |
| tpd | Delay | Digital Input with Schmitt Trigger | 44 | 49 | 19 | 21 | 14 | 15 | ns |
| tpd | Delay | Low Voltage Digital input | 46 | 447 | 19 | 195 | 14 | 134 | ns |
| tpd | Delay | Digital input-- PMOS | 44 | - | 19 | - | 14 | - | ns |
| tpd | Delay | Digital input-- NMOS | - | 81 | - | 30 | - | 20 | ns |
| tpd | Delay | Output enable from pin, OE Hi-Z to 1 | 48 | - | 20 | - | 15 | - | ns |
| tpd | Delay | Output enable from pin, OE Hi-Z to 0 | - | 46 | - | 20 | - | 24 | ns |
| tpd | Delay | LUT2bit(LATCH) | 34 | 33 | 14 | 13 | 10 | 9 | ns |
| tpd | Delay | LATCH(LUT2bit) | 30 | 34 | 14 | 13 | 10 | 9 | ns |
| tpd | Delay | LUT3bit(LATCH) | 38 | 37 | 18 | 15 | 13 | 10 | ns |
| tpd | Delay | LATCH+nRESET(LUT3bit) | 45 | 42 | 21 | 17 | 15 | 12 | ns |
| tpd | Delay | LATCH | 33 | 5 | 14 | 14 | | | ns |
| tpd | Delay | LUT4bit | 28 | 33 | 14 | 13 | 10 | 9 | ns |
| tpd | Delay | LUT2bit | 31 | 31 | 14 | 13 | 10 | 9 | ns |
| tpd | Delay | LUT3bit | 35 | 33 | 15 | 13 | 11 | 10 | ns |
| tpd | Delay | CNT/DLY | 62 | 68 | 27 | 29 | 19 | 20 | ns |
| tpd | Delay | DFF | 32 | 28 | 14 | 12 | 11 | 9 | ns |
| tpd | Delay | P_DLY1C | 62 | 68 | 27 | 29 | 19 | 20 | ns |
| tpd | Delay | P_DLY2C | 667 | 656 | 303 | 297 | 225 | 221 | ns |
| tpd | Delay | P_DLY3C | 968 | 956 | 440 | 434 | 327 | 322 | ns |
| tpd | Delay | P_DLY4C | 1265 | 1252 | 576 | 570 | 428 | 423 | ns |
| tpd | Delay | Filter | 213 | 210 | 84 | 83 | 55 | 55 | ns |
| tpd | Delay | ACMP (5mV across inputs) | 1.6 | 1.9 | 1.5 | 1.8 | 1.6 | 1.8 | ns |
| tw | width | I/O with 1X push pull (min transmitted) | 20 | 20 | 20 | 20 | 20 | 20 | ns |

**Table 2. Typical Delay estimated for each block**

| Symbol | Parameter | Note | $V_{DD}$ = 1.8 V | | $V_{DD}$ = 3.3V | | $V_{DD}$ = 5.0V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | rising | falling | rising | falling | rising | falling | |
| tw | width | filter (min transmitted) | 150 | 150 | 55 | 55 | 35 | 35 | ns |

### 5.9 Typical Counter/Delay Offset Measurements

**Table 3. Typical Counter/Delay Offset Measurements**

| Parameter | RC OSC Freq | RC OSC Power | $V_{DD}$ = 1.8 V | $V_{DD}$ = 3.3V | $V_{DD}$ = 5.0V | Unit |
|---|---|---|---|---|---|---|
| Offset (start time) | 25 kHz | auto | 1.6 | 1.6 | 1.6 | µs |
| Offset (start time), fast start | 25 kHz | auto | 2.1 | 2.1 | 2.1 | µs |
| Offset (start time) | 2 MHz | auto | 0.4 | 0.2 | 0.2 | µs |
| Offset (start time), fast start | 2 MHz | auto | 0.7 | 0.5 | 0.4 | µs |
| Offset (start time) | 25 MHz | auto | 0.01 | 0.05 | 0.04 | µs |
| Frequency settling time | 25 kHz | auto | 19 | 14 | 12 | µs |
| Frequency settling time | 2 MHz | auto | 14 | 14 | 14 | µs |
| Variable (CLK period) | 25 kHz | forced | 0-40 | 0-40 | 0-40 | µs |
| Variable (CLK period) | 2 MHz | forced | 0-0.5 | 0-0.5 | 0-0.5 | µs |
| Variable (CLK period) | 25 MHz | | 0-0.04 | 0-0.04 | 0-0.04 | µs |
| Tpd (non-delayed edge) | 25 kHz/ 2 MHz | either | 35 | 14 | 10 | ns |

### 5.10 Expected Delays and Widths

**Table 4. Expected Delays and Widths (typical)**

| Symbol | Parameter | Note | $V_{DD}$ = 1.8 V | $V_{DD}$ = 3.3V | $V_{DD}$ = 5.0V | Unit |
|---|---|---|---|---|---|---|
| Width | Width, 1 cell | mode:(any)edge detect, edge detect output | 296 | 135 | 101 | ns |
| Width | Width, 2 cell | mode:(any)edge detect, edge detect output | 597 | 272 | 203 | ns |
| Width | Width, 3 cell | mode:(any)edge detect, edge detect output | 898 | 410 | 305 | ns |
| Width | Width, 4 cell | mode:(any)edge detect, edge detect output | 1195 | 546 | 407 | ns |
| time1 | Delay, 1 cell | mode:(any)edge detect, edge detect output | 55 | 24 | 18 | ns |
| time1 | Delay, 2 cell | mode:(any)edge detect, edge detect output | 55 | 24 | 18 | ns |
| time1 | Delay, 3 cell | mode:(any)edge detect, edge detect output | 55 | 24 | 18 | ns |
| time1 | Delay, 4 cell | mode:(any)edge detect, edge detect output | 55 | 24 | 18 | ns |
| time2 | Delay, 1 cell | mode: both edge delay, edge detect output | 367 | 165 | 106 | ns |
| time2 | Delay, 2 cell | mode: both edge delay, edge detect output | 667 | 300 | 193 | ns |
| time2 | Delay, 3 cell | mode: both edge delay, edge detect output | 968 | 440 | 279 | ns |
| time2 | Delay, 4 cell | mode: both edge delay, edge detect output | 1265 | 575 | 365 | ns |

### 5.11 Typical Pulse Width Performance

**Table 5. Typical Pulse Width Performance at T=25°C**

| Parameter | $V_{DD}$ = 1.8 V | $V_{DD}$ = 3.3V | $V_{DD}$ = 5.0V | Unit |
|---|---|---|---|---|
| Filtered Pulse Width for Filter 0 | < 114 | < 47 | < 30 | ns |
| Filtered Pulse Width for Filter 1 | <75 | <30 | <19 | ns |

### 5.12 OSC Specifications

**Table 6. 25 kHz RC OSC0 frequency limits**

| Power Supply Range (VDD) V | Temperature Range | | | | | |
|---|---|---|---|---|---|---|
| | +25 °C | | 0 °C ... +85 °C | | -40 °C ... +85 °C | |
| | Minimum Value, kHz | Maximum Value, kHz | Minimum Value, kHz | Maximum Value, kHz | Minimum Value, kHz | Maximum Value, kHz |
| 1.8 V ±5% | 24.240 | 25.781 | 21.963 | 27.188 | 21.963 | 27.562 |
| 3.3 V ±10% | 24.447 | 25.556 | 21.905 | 27.221 | 21.905 | 27.263 |
| 5 V ±10% | 24.315 | 25.911 | 22.045 | 27.099 | 22.045 | 27.422 |
| 2.5 V ... 4.5 V | 24.398 | 25.576 | 21.897 | 27.221 | 21.897 | 27.277 |
| 1.71 V… 5.5 V | 24.089 | 26.128 | 21.897 | 27.373 | 21.897 | 27.613 |

**Table 7. 25 kHz RC OSC0 frequency error (error calculated relative to nominal value)**

| Power Supply Range (VDD) V | Temperature Range | | | | | |
|---|---|---|---|---|---|---|
| | +25 °C | | 0 °C ... +85 °C | | -40 °C ... +85 °C | |
| | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) |
| 1.8 V ±5% | -2.76% | 3.42% | -11.89% | 9.07% | -11.89% | 10.57% |
| 3.3 V ±10% | -2.01% | 2.43% | -12.20% | 9.11% | -12.20% | 9.28% |
| 5 V ±10% | -2.51% | 3.89% | -11.61% | 8.65% | -11.61% | 9.95% |
| 2.5 V ... 4.5 V | -2.21% | 2.52% | -12.23% | 9.11% | -12.23% | 9.33% |
| 1.71 V… 5.5 V | -3.44% | 4.73% | -12.23% | 9.72% | -12.23% | 10.68% |

### 5.12.1 2 MHz RC Oscillator

**Table 8. 2 MHz RC OSC0 frequency limits**

| Power Supply Range (VDD) V | Temperature Range | | | | | |
|---|---|---|---|---|---|---|
| | +25 °C | | 0 °C ... +85 °C | | -40 °C ... +85 °C | |
| | Minimum Value, MHz | Maximum Value, MHz | Minimum Value, MHz | Maximum Value, MHz | Minimum Value, MHz | Maximum Value, MHz |
| 1.8 V ±5% | 1.932 | 2.058 | 1.793 | 2.171 | 1.793 | 2.171 |
| 3.3 V ±10% | 1.932 | 2.099 | 1.808 | 2.204 | 1.808 | 2.204 |
| 5 V ±10% | 1.981 | 2.194 | 1.759 | 2.316 | 1.759 | 2.316 |
| 2.5 V ... 4.5 V | 1.920 | 2.120 | 1.800 | 2.214 | 1.800 | 2.214 |
| 1.71 V… 5.5 V | 1.811 | 2.288 | 1.710 | 2.337 | 1.710 | 2.361 |

**Table 9. 2 MHz RC OSC0 frequency error (error calculated relative to nominal value)**

| Power Supply Range (VDD) V | Temperature Range | | | | | |
|---|---|---|---|---|---|---|
| | +25 °C | | 0 °C ... +85 °C | | -40 °C ... +85 °C | |
| | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) |
| 1.8 V ±5% | -3.23% | 3.10% | -10.21% | 8.73% | -10.21% | 8.73% |
| 3.3 V ±10% | -3.40% | 4.94% | -9.60% | 10.19% | -9.60% | 10.19% |
| 5 V ±10% | -5.44% | 9.70% | -12.03% | 2.32% | -12.03% | 15.81% |
| 2.5 V ... 4.5 V | -4.00% | 5.98% | -9.99% | 10.68% | -9.99% | 10.68% |
| 1.71 V… 5.5 V | -9.46% | 14.42% | -14.48% | 16.85% | -14.48% | 18.05% |

### 5.12.2 25 MHz RC Oscillator

**Table 10. 25 MHz RC OSC1 frequency limits**

| Power Supply Range (VDD) V | Temperature Range | | | | | |
|---|---|---|---|---|---|---|
| | +25 °C | | 0 °C ... +85 °C | | -40 °C ... +85 °C | |
| | Minimum Value, MHz | Maximum Value, MHz | Minimum Value, MHz | Maximum Value, MHz | Minimum Value, MHz | Maximum Value, MHz |
| 2.5 V ±10% | 22.344 | 27.023 | 21.687 | 27.777 | 21.687 | 27.706 |
| 3.3 V ±10% | 22.412 | 26.290 | 21.399 | 26.595 | 21.399 | 27.069 |
| 5 V ±10% | 23.049 | 26.646 | 21.900 | 27.220 | 21.900 | 27.647 |
| 2.5 V ... 4.5 V | 21.511 | 26.290 | 20.738 | 26.685 | 20.738 | 27.123 |
| 1.71 V… 5.5 V | 13.290 | 26.290 | 12.770 | 26.685 | 11.908 | 27.123 |

**Table 11. 25 MHz RC OSC1 frequency error (error calculated relative to nominal value)**

| Power Supply Range (VDD) V | Temperature Range | | | | | |
|---|---|---|---|---|---|---|
| | +25 °C | | 0 °C ... +85 °C | | -40 °C ... +85 °C | |
| | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) | Error (% at Minimum) | Error (% at Maximum) |
| 2.5 V ±10% | -10.37% | 8.40% | -13.00% | 9.42% | -13.00% | 11.14% |
| 3.3 V ±10% | -11.10% | 4.28% | -15.12% | 5.49% | -15.12% | 7.37% |
| 5 V ±10% | -9.80% | 4.27% | -14.30% | 6.52% | -14.30% | 8.19% |
| 2.5 V ... 4.5 V | -14.68% | 4.28% | -17.74% | 5.85% | -17.74% | 7.58% |
| 1.71 V… 5.5 V | -47.29% | 4.28% | -49.35% | 5.85% | -52.77% | 7.58% |

Note: 25 MHz RC OSC1 performance is not guaranteed at VDD < 2.5 V.

### 5.12.3 OSC Power On delay

**Table 12. Oscillators Power On delay at room temperature, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On", RC osc clock to matrix input: "Enable"**

| Power Supply Range (VDD) V | RC OSC0 2 MHz | | RC OSC0 25 kHz | | RC OSC1 | |
|---|---|---|---|---|---|---|
| | Typical Value, µs | Maximum Value, µs | Typical Value, ms | Maximum Value, ms | Typical Value, µs | Maximum Value, µs |
| 1.71 | 368.7 | 402.3 | 16.26 | 17.87 | 114.4 | 134.8 |
| 1.80 | 347.0 | 375.4 | 15.93 | 17.79 | 104.9 | 122.0 |
| 1.89 | 329.4 | 354.2 | 15.58 | 17.67 | 96.5 | 111.5 |
| 2.50 | 278.4 | 295.2 | 14.08 | 16.75 | 72.0 | 80.3 |
| 2.70 | 263.2 | 277.8 | 13.20 | 16.21 | 65.0 | 71.4 |
| 3.00 | 251.6 | 264.9 | 8.38 | 9.11 | 60.0 | 65.1 |
| 3.30 | 238.3 | 250.6 | 1.64 | 2.02 | 55.2 | 58.7 |
| 3.60 | 228.3 | 240.0 | 1.57 | 1.92 | 51.7 | 55.0 |
| 4.20 | 220.3 | 231.7 | 1.55 | 1.93 | 49.1 | 51.9 |
| 4.50 | 208.0 | 219.2 | 1.55 | 2.01 | 45.5 | 47.8 |
| 5.00 | 203.0 | 213.9 | 1.56 | 2.01 | 44.3 | 46.5 |
| 5.50 | 195.7 | 206.5 | 1.58 | 2.07 | 43.0 | 44.8 |

**Table 13. Oscillators Power On delay at room temperature, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On", RC osc clock to matrix input: "Enable", Fast Start-up Time Mode**

| Power Supply Range (VDD) V | RC OSC0 2 MHz | | RC OSC1 25 kHz | |
|---|---|---|---|---|
| | Typical Value, µs | Maximum Value, µs | Typical Value, ms | Maximum Value, ms |
| 1.71 | 741.8 | 924.7 | 20.78 | 21.36 |
| 1.80 | 703.9 | 861.5 | 20.80 | 21.26 |
| 1.89 | 672.5 | 809.0 | 20.81 | 21.42 |
| 2.50 | 578.5 | 651.8 | 20.84 | 21.40 |
| 2.70 | 546.8 | 592.8 | 20.88 | 21.42 |
| 3.00 | 520.6 | 549.2 | 20.93 | 21.63 |
| 3.30 | 490.4 | 515.8 | 21.00 | 21.65 |
| 3.60 | 468.9 | 504.7 | 21.09 | 21.75 |
| 4.20 | 453.0 | 496.6 | 21.18 | 21.98 |
| 4.50 | 430.1 | 478.2 | 21.36 | 22.34 |
| 5.00 | 420.7 | 468.5 | 21.39 | 22.34 |
| 5.50 | 406.1 | 451.9 | 21.38 | 22.34 |

### 5.13 ACMP Specifications

**Table 14. ACMP Power On Delay, minimal required ACMP wake time for the Wake and Sleep function. BG=550 µs. Regulator and Charge Pump automatic ON/OFF**

| Power Supply Range (VDD) V | Temperature Range | | | |
|---|---|---|---|---|
| | -40 ... +85 °C | | +25°C | |
| | Typical Value, µs | Maximum Value, µs | Typical Value, µs | Maximum Value, µs |
| 1.71 | 651.8 | 975.1 | 602.2 | 835.7 |
| 1.80 | 657.9 | 985.4 | 603.2 | 840.3 |
| 1.89 | 670.4 | 1020.3 | 608.6 | 857.8 |
| 2.50 | 672.0 | 1023.4 | 608.9 | 860.0 |
| 2.70 | 673.8 | 1025.7 | 609.2 | 861.9 |
| 3.00 | 674.9 | 1028.8 | 609.7 | 862.0 |
| 3.30 | 675.0 | 1028.2 | 609.3 | 862.2 |
| 3.60 | 673.4 | 1026.8 | 607.7 | 860.0 |
| 4.20 | 671.4 | 1022.5 | 605.2 | 855.5 |
| 4.50 | 662.2 | 1004.3 | 597.0 | 841.7 |
| 5.00 | 645.2 | 972.9 | 581.5 | 816.5 |
| 5.50 | 651.8 | 975.1 | 602.2 | 835.7 |

**Table 15. ACMP Power On Delay, minimal required ACMP wake time for the Wake and Sleep function. BG=100 µs (can be used for VDD>2.7V). Regulator and Charge Pump automatic ON/OFF**

| Power Supply Range (VDD) V | Temperature Range | | | |
|---|---|---|---|---|
| | -40 ... +85 °C | | +25°C | |
| | Typical Value, µs | Maximum Value, µs | Typical Value, µs | Maximum Value, µs |
| 2.70 | 149.4 | 212.7 | 132.4 | 176.2 |
| 3.00 | 149.3 | 212.7 | 131.8 | 176.1 |
| 3.30 | 149.2 | 213.5 | 131.3 | 176.1 |
| 3.60 | 149.0 | 212.5 | 130.9 | 175.8 |
| 4.20 | 148.6 | 211.9 | 130.2 | 174.9 |
| 4.50 | 148.0 | 211.1 | 129.4 | 173.9 |
| 5.00 | 146.1 | 208.8 | 127.7 | 171.5 |
| 5.50 | 142.7 | 203.2 | 124.7 | 167.1 |

**Table 16. ACMP Power On Delay, minimal required ACMP wake time for the Wake and Sleep function. BG=550 µs. Regulator auto ON/OFF and Charge Pump always OFF (can be used for VDD>3.0 V)**

| Power Supply Range (VDD) V | Temperature Range | | | |
|---|---|---|---|---|
| | -40 ... +85 °C | | +25°C | |
| | Typical Value, µs | Maximum Value, µs | Typical Value, µs | Maximum Value, µs |
| 3.00 | 673.6 | 1024.8 | 609.1 | 861.5 |
| 3.30 | 674.4 | 1027.5 | 609.5 | 862.0 |
| 3.60 | 674.6 | 1027.2 | 609.1 | 862.0 |
| 4.20 | 673.0 | 1025.3 | 607.6 | 859.4 |
| 4.50 | 671.1 | 1021.3 | 605.1 | 855.3 |
| 5.00 | 662.4 | 1004.7 | 597.0 | 841.1 |
| 5.50 | 645.0 | 970.4 | 581.4 | 815.8 |

**Table 17. ACMP Power On Delay, minimal required ACMP wake time for the Wake and Sleep function. BG=100 µs. Regulator auto ON/OFF and Charge Pump always OFF (can be used for VDD>3.0 V)**

| Power Supply Range (VDD) V | Temperature Range | | | |
|---|---|---|---|---|
| | -40 ... +85 °C | | +25°C | |
| | Typical Value, µs | Maximum Value, µs | Typical Value, µs | Maximum Value, µs |
| 3.00 | 149.2 | 212.7 | 131.6 | 176.0 |
| 3.30 | 149.1 | 213.3 | 131.2 | 175.9 |
| 3.60 | 148.9 | 212.5 | 130.8 | 175.7 |
| 4.20 | 148.6 | 211.7 | 130.2 | 174.7 |
| 4.50 | 148.0 | 211.1 | 129.4 | 173.8 |
| 5.00 | 146.1 | 208.9 | 127.7 | 171.4 |
| 5.50 | 142.8 | 204.0 | 124.8 | 167.1 |

## 6.0 Summary of Macro Cell Function

### 6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs
- Push Pull Outputs
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- 40 mA Open Drain 4X Drive output

### 6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

### 6.3 Analog Comparators (4 total)

- Selectable hysteresis 0 mV / 25 mV / 50 mV / 200 mV
- Wake and Sleep Control (Part of Combination Function Macrocell)

### 6.4 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external pins

### 6.5 Combination Function Macrocells (17 total)

- Three Selectable DFF/Latch or 2-bit LUTs
- Five Selectable DFF/Latch or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- One Selectable Programmable Pattern Generator or 4-bit LUT
- Five Selectable 8-bit CNT/DLY or 3-bit LUT
- Two Selectable 16-bit CNT/DLY or 4-bit LUT
- Wake and Sleep Controller

### 6.6 Asynchronous State Machine

- Eight States
- Flexible input logic from state transitions

### 6.7 Serial Communications

- $I^2C$ Protocol compliant

### 6.8 Pipe Delay (Part of Combination Function Macrocell)

- 16 stage / 3 output
- One 1 stage fixed output
- Two 1-16 stage selectable outputs.

### 6.9 Programmable Delay

- 125 ns/250 ns/375 ns/500 ns @ 3.3 V
- Includes Edge Detection function

### 6.10 Additional Logic Functions (2 total)

- Two Deglitch filter macro cells
- Includes Edge Detection function

### 6.11 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- 25 MHz RC Oscillator
- First stage divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider for 25 kHz and 2 MHz (5): Output to Matrix: OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, OSC/64

### 6.12 Crystal Oscillator

### 6.13 Eight byte RAM + OTP User Memory

- RAM Memory space that is readable and writeable via $I^2C$

## 7.0 I/O Pins

The SLG46531 has a total of 18 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Refer to Section 2.0 Pin Description for normal and programming modepin definitions.

Normal Mode pin definitions are as follows:

- Pin 1: $V_{DD}$ power supply
- Pin 2: general purpose input
- Pin 3: general purpose input or output with OE
- Pin 4: general purpose input or output
- Pin 5: general purpose input or output with OE
- Pin 6: general purpose input or output or analog comparator 0(+)
- Pin 7: general purpose input or output with OE or analog comparator 0(-)
- Pin 8: general purpose input or OD output SCL
- Pin 9: general purpose input or OD output SDA
- Pin 10: general purpose input or output with OE or analog comparator 1(+)
- Pin 11: ground
- Pin 12: general purpose input or output or analog comparator 1(-)
- Pin 13: general purpose input or output with OE or analog comparator 2(+)
- Pin 14: general purpose input or output with OE or analog comparator 2(-)
- Pin 15: general purpose input or output or analog comparator 3(+)
- Pin 16: general purpose input or output with OE
- Pin 17: general purpose input or output
- Pin 18: general purpose input or output with OE and Vref output (VREF2)
- Pin 19: general purpose input or output with OE and Vref output (VREF1)
- Pin 20: general purpose input or output or external clock input

Programming Mode pin definitions are as follows:

- Pin 1: $V_{DD}$ power supply
- Pin 2: $V_{PP}$ programming voltage
- Pin 8: Programming SCL
- Pin 9: Programming SDA
- Pin 11: ground
- Pin 16: programming mode control

Of the 18 user defined I/O pins on the SLG46531, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

### 7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input. Pins 6, 7, 10, 12, 13, 14, and 15 can also be configured to serve as analog inputs to the on-chip comparators. Pins 18 and 19 can also be configured as analog reference voltage inputs.

### 7.2 Output Modes

Pins 3, 4, 5, 6, 7, 8, 9, 10, 12, 13, 14, 15, 16, 17, 18, 19, and 20 can all be configured as digital output pins.

### 7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

### 7.4 I/O Register Settings

#### 7.4.1 PIN 2 Register Settings

**Table 18. PIN 2 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 2 Pull Down Resistor Value Selection | <1028:1029> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 2 Mode Control | <1030:1031> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Reserved |

#### 7.4.2 PIN 3 Register Settings

**Table 19. PIN 3 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 3 Pull Up/Down Resistor Selection | <1033> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 3 Pull Up/Down Resistor Value Selection | <1035:1034> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 3 Mode Control (sig_pin3_oe =0) | <1037:1036> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Reserved |
| PIN 3 Mode Control (sig_pin3_oe =1) | <1039:1038> | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X |

### 7.4.3 PIN 4 Register Settings

**Table 20. PIN 4 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 4 Driver Strength Selection | <1041> | 0: 1X<br>1: 2X |
| PIN 4 Pull Up/Down Resistor Selection | <1042> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 4 Pull Up/Down Resistor Value Selection | <1044:1043> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 4 Mode Control | <1047:1045> | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Reserved |

### 7.4.4 PIN 5 Register Settings

**Table 21. PIN 5 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 5 Pull Up/Down Resistor Selection | <1049> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 5 Pull Up/Down Resistor Value Selection | <1051:1050> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 5 Mode Control (sig_pin5_oe =0) | <1053:1052> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Reserved |
| PIN 5 Mode Control (sig_pin5_oe =1) | <1055:1054> | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X |

### 7.4.5 PIN 6 Register Settings

**Table 22. PIN 6 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 6 Driver Strength Selection | <1057> | 0: 1X<br>1: 2X |
| PIN 6 Pull Up/Down Resistor Selection | <1058> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 6 Pull Up/Down Resistor Value Selection | <1060:1059> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 6 Mode Control | <1063:1061> | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Analog Input/Output<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Analog Input & Open Drain |

### 7.4.6 PIN 7 Register Settings

**Table 23. PIN 7 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 7 Pull Up/Down Resistor Selection | <1065> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 7 Pull Up/Down Resistor Value Selection | <1067:1066> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 7 Mode Control (sig_pin7_oe =0) | <1069:1068> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output |
| PIN 7 Mode Control (sig_pin7_oe =1) | <1071:1070> | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X |

### 7.4.7 PIN 8 Register Settings

**Table 24. PIN 8 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 8 Driver Strength Selection | <1073> | 0: 1X<br>1: 2X |
| Select SCL & Virtual Input 0 or PIN8 | <1074> | 0: SCL & Virtual Input 0<br>1: PIN8 |
| PIN 8 Pull Down Resistor Value Selection | <1076:1075> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 8 Mode Control | <1079:1077> | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Reserved<br>101: Open Drain NMOS<br>110: Reserved<br>111: Reserved |

### 7.4.8 PIN 9 Register Settings

**Table 25. PIN 9 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN9 (or SDA) Driver Strength Selection | <1081> | 0: 1X<br>1: 2X |
| Select SDA & Virtual Input 1 or PIN9 | <1082> | 0: SDA & Virtual Input 1<br>1: PIN9 |
| PIN9 Pull Down Resistor Value Selection | <1084:1083> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 9 (or SDA) Mode Control | <1087:1085> | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Reserved<br>101: Open Drain NMOS<br>110: Reserved<br>111: Reserved |

### 7.4.9 PIN 10 Register Settings

**Table 26. PIN 10 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 10 4X Drive (4X, NMOS Open Drain) Selection | <1088> | 0: 4X Drive Off<br>1: 4X Drive On (if <884:882> = '101') |
| PIN 10 Pull Up/Down Resistor Selection | <1089> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 10 Pull Up/Down Resistor Value Selection | <1091:1090> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 10 Mode Control (sig_pin7_oe =0) | <1093:1092> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output |
| PIN 10 Mode Control (sig_pin7_oe =1) | <1095:1094> | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X |

### 7.4.10 PIN 12 Register Settings

**Table 27. PIN 12 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 12 4X Drive (4X, NMOS Open Drain) Selection | <1096> | 0: 4X Drive Off<br>1: 4X Drive On (if <892:890> = '101') |
| PIN 12 Driver Strength Selection | <1097> | 0: 1X<br>1: 2X |
| PIN 12 Pull Up/Down Resistor Selection | <1098> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 12 Pull Up/Down Resistor Value Selection | <1100:1099> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 12 Mode Control | <1103:1101> | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Analog Input/Output<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Analog Input & Open Drain |

### 7.4.11 PIN 13 Register Settings

**Table 28. PIN 13 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 13 Pull Up/Down Resistor Selection | <1105> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 13 Pull Up/Down Resistor Value Selection | <1107:1106> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 13 Mode Control (sig_pin13_oe =0) | <1109:1108> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output |
| PIN 13 Mode Control (sig_pin13_oe =1) | <1111:1110> | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X |

### 7.4.12 PIN 14 Register Settings

**Table 29. PIN 14 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 14 Pull Up/Down Resistor Selection | <1113> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 14 Pull Up/Down Resistor Value Selection | <1115:1114> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 14 Mode Control (sig_pin14_oe =0) | <1117:1116> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output |
| PIN 14 Mode Control (sig_pin14_oe =1) | <1119:1118> | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X |

### 7.4.13 PIN 15 Register Settings

**Table 30. PIN 15 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 15 Driver Strength Selection | <1121> | 0: 1X<br>1: 2X |
| PIN 15 Pull Up/Down Resistor Selection | <1122> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 15 Pull Up/Down Resistor Value Selection | <1124:1123> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 15 Mode Control | <1127:1125> | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Analog Input/Output<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Analog Input & Open Drain |

### 7.4.14 PIN 16 Register Settings

**Table 31. PIN 16 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 16 Pull Up/Down Resistor Selection | <1129> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 16 Pull Up/Down Resistor Value Selection | <1131:1130> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 16 Mode Control (sig_pin16_oe =1) | <1135:1134> | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X |
| PIN 16 Mode Control (sig_pin16_oe =0) | <1133:1132> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Reserved |

### 7.4.15 PIN 17 Register Settings

**Table 32. PIN 17 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 17 Driver Strength Selection | <1137> | 0: 1X<br>1: 2X |
| PIN 17 Pull Up/Down Resistor Selection | <1138> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 17 Pull Up/Down Resistor Value Selection | <1140:1139> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 17 Mode Control | <1143:1141> | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Reserved |

### 7.4.16 PIN 18 Register Settings

**Table 33. PIN 18 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 18 Pull Up/Down Resistor Selection | <1145> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 18 Pull Up/Down Resistor Value Selection | <1147:1146> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 18 Mode Control (sig_pin18_oe =0) | <1149:1148> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output |
| PIN 18 Mode Control (sig_pin18_oe =1) | <1151:1150> | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X |

### 7.4.17 PIN 19 Register Settings

**Table 34. PIN 19 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 19 Pull Up/Down Resistor Selection | <1153> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 19 Pull Up/Down Resistor Value Selection | <1155:1154> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 19 Mode Control (sig_pin19_oe =0) | <1157:1156> | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output |
| PIN 19 Mode Control (sig_pin18_oe =1) | <1159:1158> | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X |

### 7.4.18 PIN 20 Register Settings

**Table 35. PIN 20 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| PIN 20 Driver Strength Selection | <1161> | 0: 1X<br>1: 2X |
| PIN 20 Pull Up/Down Resistor Selection | <1162> | 0: Pull Down Resistor<br>1: Pull Up Resistor |
| PIN 20 Pull Up/Down Resistor Value Selection | <1164:1163> | 00: Floating<br>01: 10 kΩ Resistor<br>10: 100 kΩ Resistor<br>11: 1 MΩ Resistor |
| PIN 20 Mode Control | <1167:1165> | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Reserved |

### 7.5 GPI Structure

#### 7.5.1 GPI Structure (for Pin 2)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en=1, OE=0
01: Digital In with Schmitt Trigger, smt_en=1, OE=0
10: Low Voltage Digital In mode, lv_en = 1, OE=0
11: Reserved

Note 1: OE cannot be selected by user
Note 2: OE is Matrix output, Digital In is Matrix input

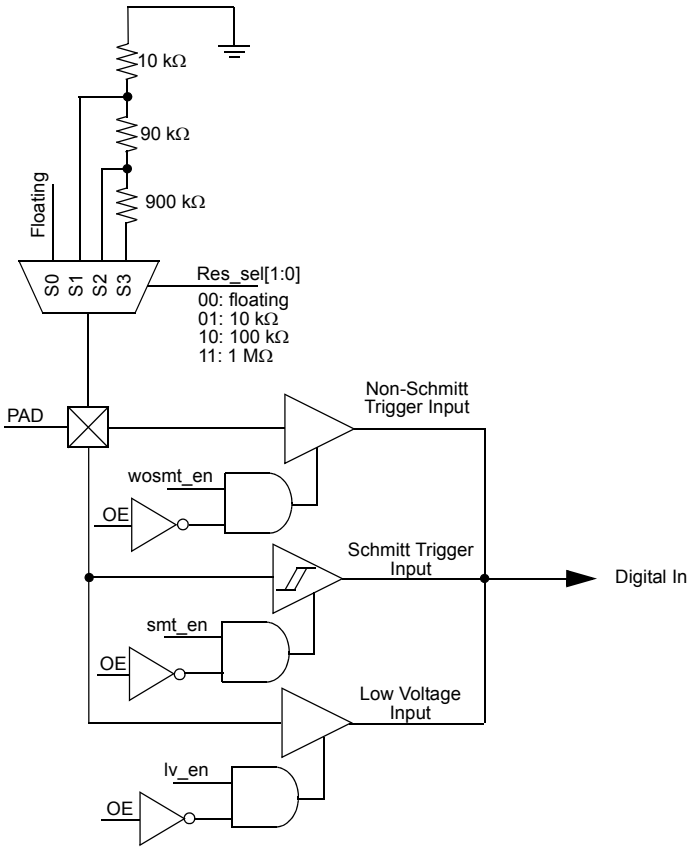



**Figure 2. PIN 2 GPI Structure Diagram**

### 7.6 Matrix OE IO Structure

#### 7.6.1 Matrix OE IO Structure (for Pins 3, 5, 7, 13, 14, 16, 18, 19)

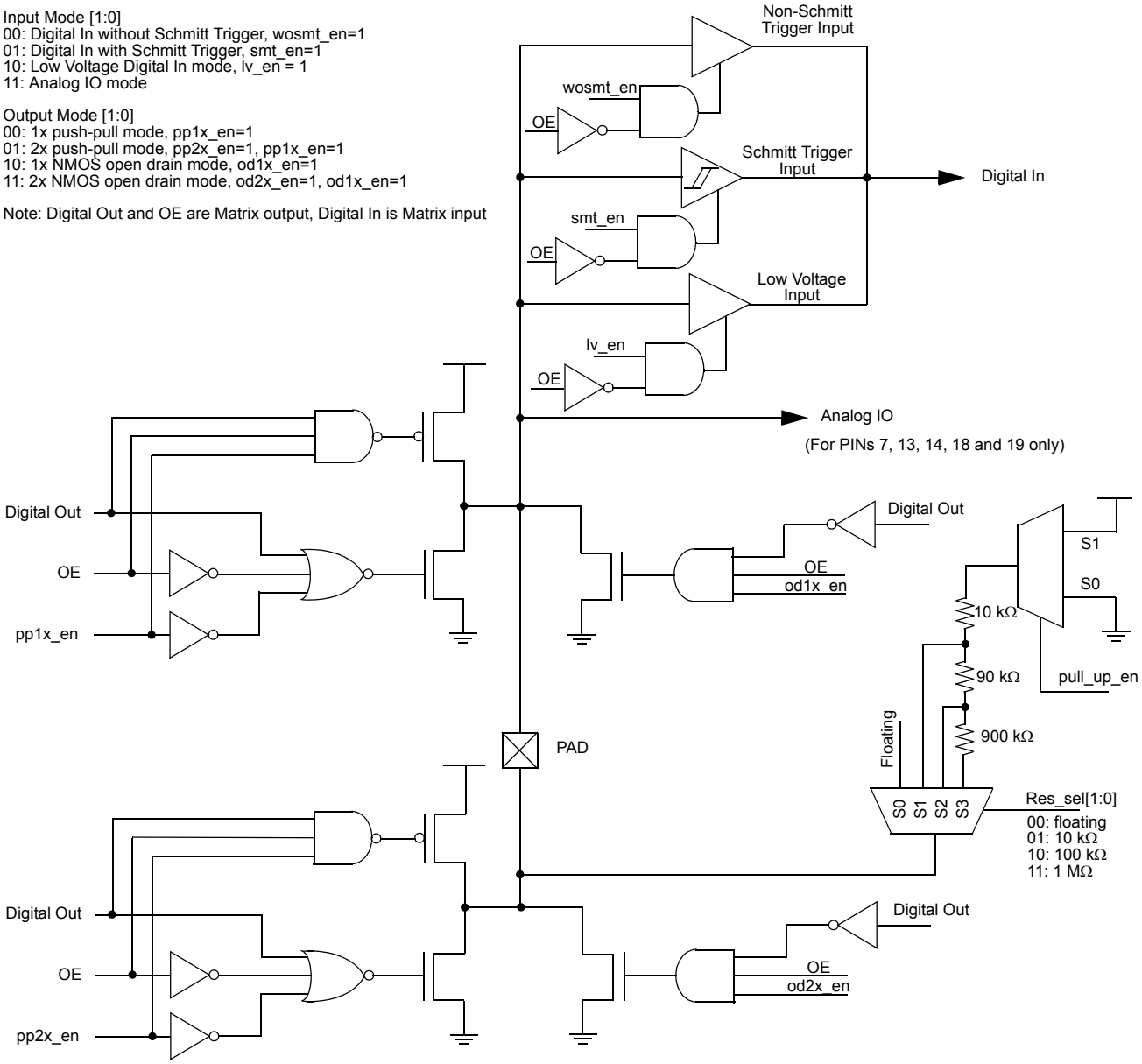



**Figure 3. Matrix OE IO Structure Diagram**

### 7.6.2 Matrix OE IO Structure (for Pins 8 and 9)

Pin 8, Pin 9 Mode [2:0]
000: Digital Input without Schmitt Trigger
001: Digital Input with Schmitt Trigger
010: Low Voltage Digital Input
011: Reserved
100: Reserved
101: Open Drain NMOS
110: Reserved
111: Reserved

Note: Digital Out and OE are Matrix output, Digital In is Matrix input

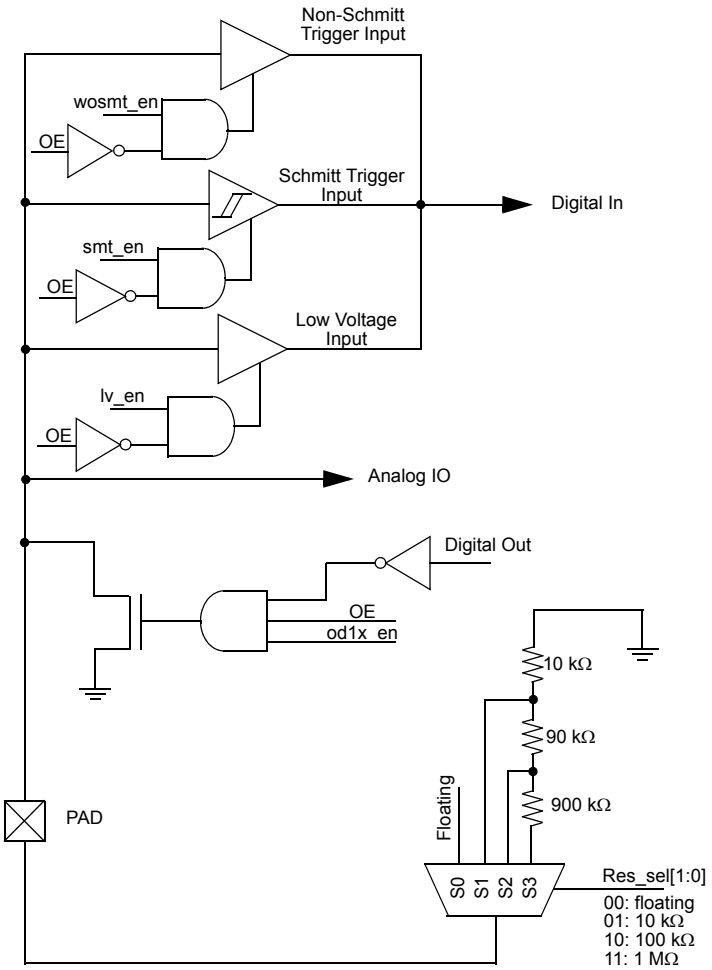



**Figure 4. Matrix OE IO Structure Diagram**

### 7.6.3 Matrix OE 4X Drive Structure (for Pin 10)

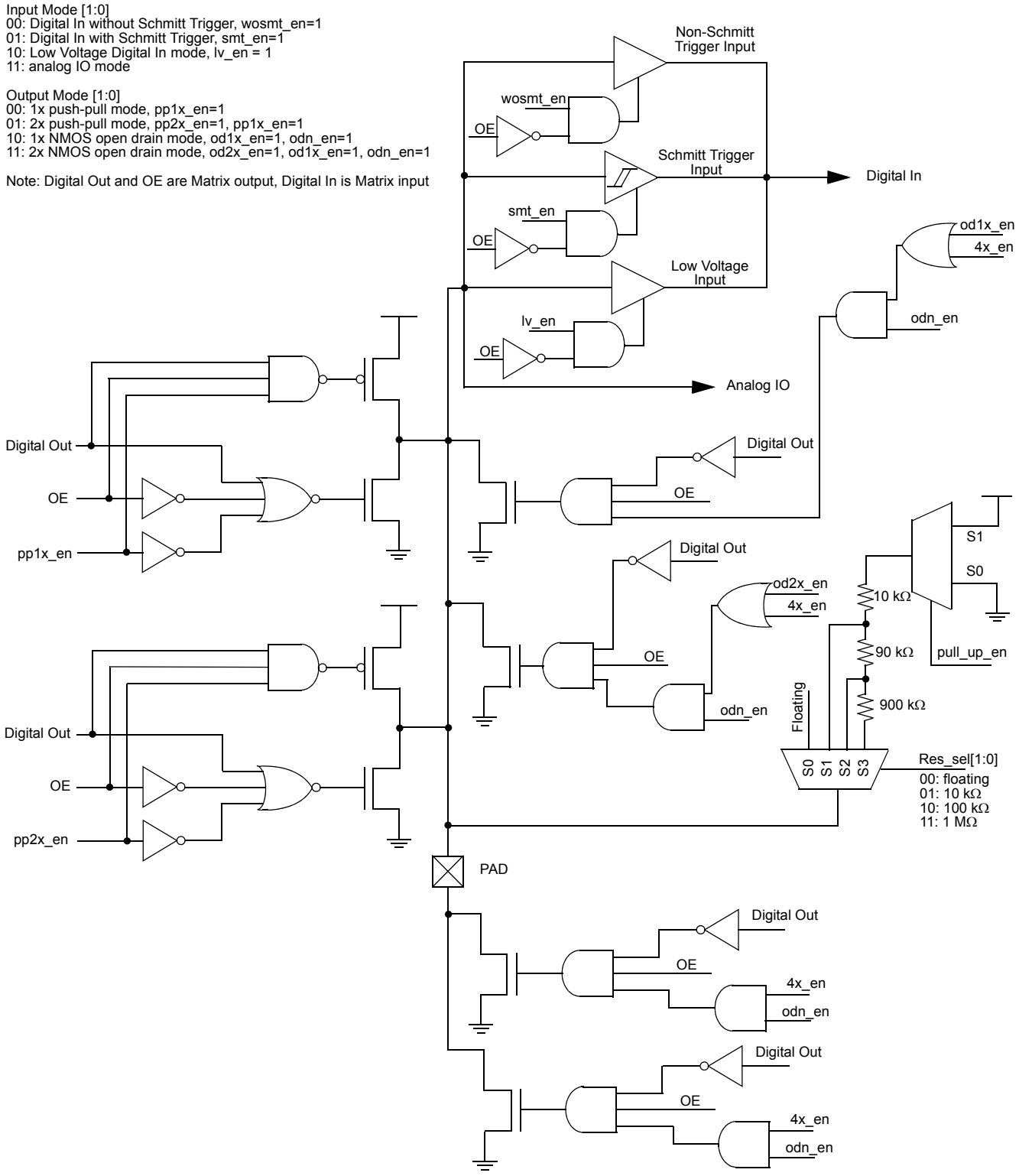



**Figure 5. Matrix OE IO 4X Drive Structure Diagram**

### 7.7 IO Structure

#### 7.7.1 IO Structure (for Pins 4, 6, 15, 17, 20)

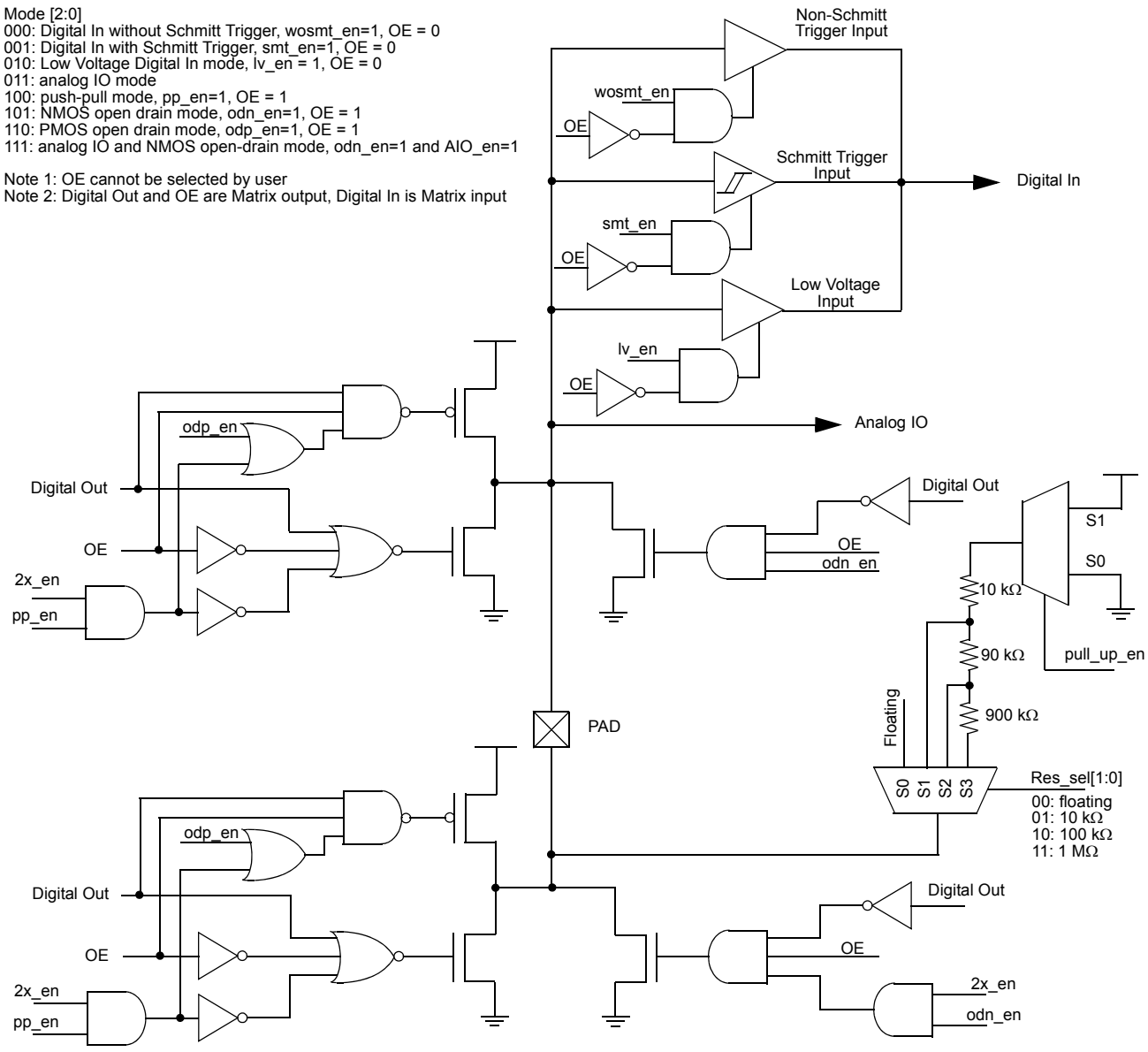



**Figure 6. IO Structure Diagram**

### 7.7.2 4X Drive Structure (for Pin 12)

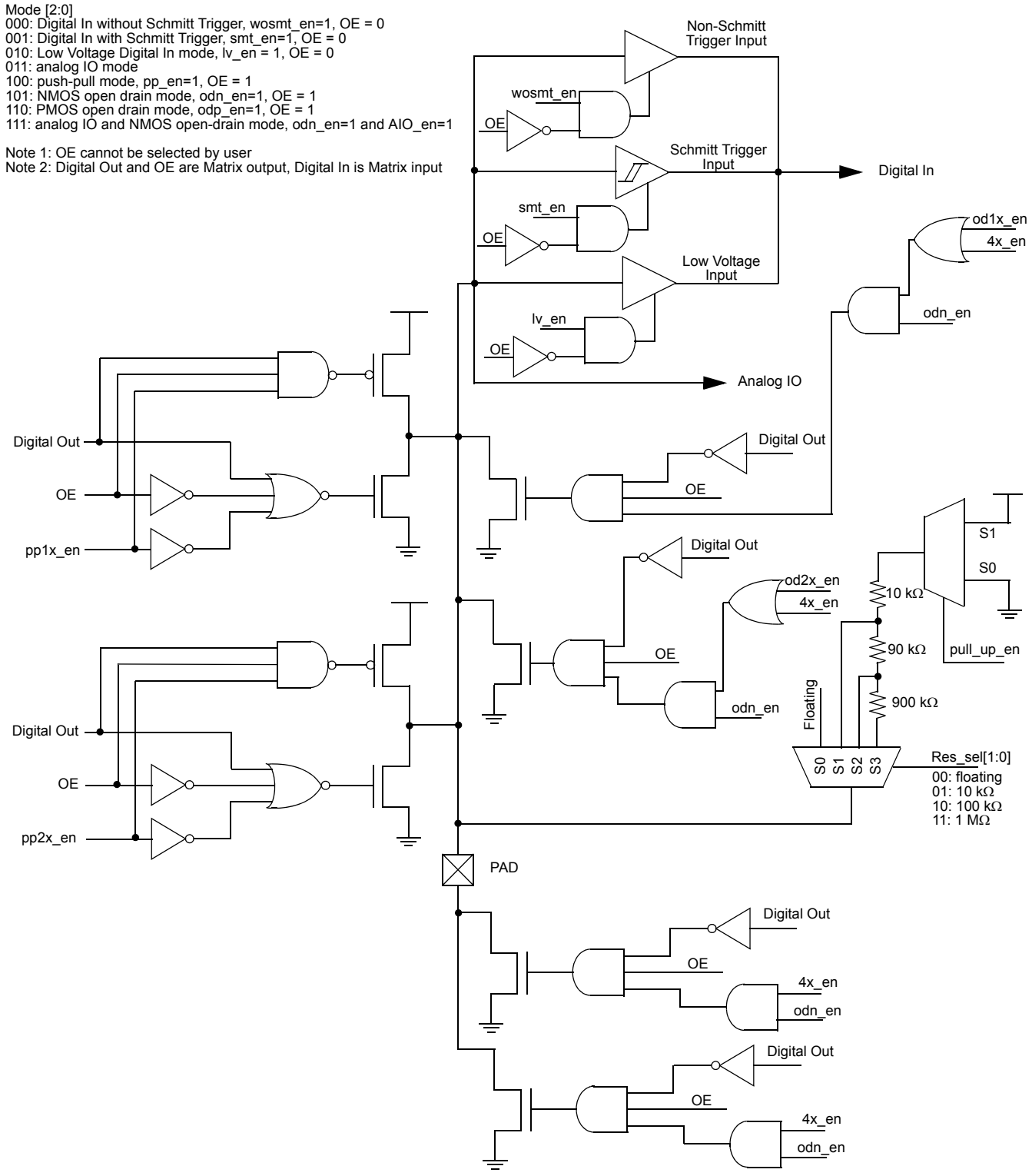



**Figure 7. IO 4X Drive Structure Diagram**

## 8.0 Connection Matrix

The Connection Matrix in the SLG46531 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46531 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 2048 register bits within the SLG46531 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 110 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including I/O pins, LUTs, analog comparators, other digital resources and VDD and Ground. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46531’s register table, see Section 21.0 Appendix A - SLG46531 Register Definition.

| Matrix Input Signal Functions | N |
|---|---|
| Ground | 0 |
| Pin 2 Digital In | 1 |
| Pin 3 Digital In | 2 |
| Pin 4 Digital In | 3 |
| ⋮ | ⋮ |
| Resetb_core | 62 |
| VDD | 63 |

| Matrix Inputs / Matrix Outputs | N | 0 | 1 | 2 | ⋯ | 109 |
|---|---|---|---|---|---|---|
| | Registers | reg<5:0> | reg<13:8> | reg<21:16> | ⋯ | reg<877:872> |
| | Function | Matrix OUT: ASM-state0-EN0 | Matrix OUT: ASM-state0-EN1 | Matrix OUT: ASM-state0-EN2 | ⋯ | Matrix OUT: PD of either Temp out or XTAL Osc |

**Figure 8. Connection Matrix**

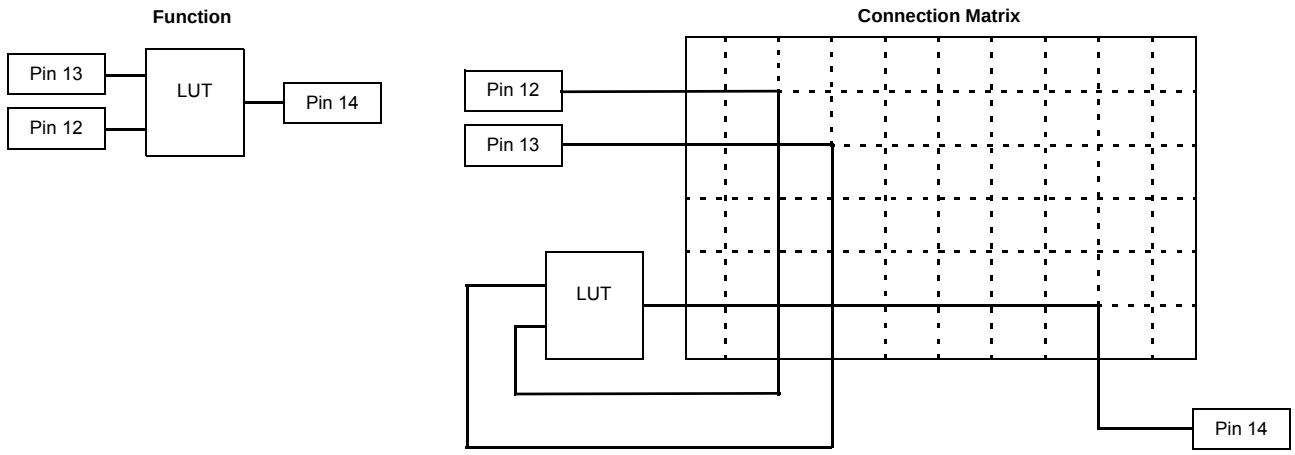



**Figure 9. Connection Matrix Example**

### 8.1 Matrix Input Table

**Table 36. Matrix Input Table**

| Matrix Input Number | Matrix Input Signal Function | Matrix Decode | | | | | |
|---|---|---|---|---|---|---|---|
| | | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | Ground | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | Pin2 Digital Input | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | Pin3 Digital Input | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | Pin4 Digital Input | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | Pin5 Digital Input | 0 | 0 | 0 | 1 | 0 | 0 |
| 5 | Pin6 Digital Input | 0 | 0 | 0 | 1 | 0 | 1 |
| 6 | Pin7 Digital Input | 0 | 0 | 0 | 1 | 1 | 0 |
| 7 | Pin10 Digital Input | 0 | 0 | 0 | 1 | 1 | 1 |
| 8 | LUT2_0 / DFF0 Output | 0 | 0 | 1 | 0 | 0 | 0 |
| 9 | LUT2_1 / DFF1 Output | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | LUT2_2 / DFF2 Output | 0 | 0 | 1 | 0 | 1 | 0 |
| 11 | LUT2_3 / PGEN Output | 0 | 0 | 1 | 0 | 1 | 1 |
| 12 | LUT3_0 / DFF3 Output | 0 | 0 | 1 | 1 | 0 | 0 |
| 13 | LUT3_1 / DFF4 Output | 0 | 0 | 1 | 1 | 0 | 1 |
| 14 | LUT3_2 / DFF5 Output | 0 | 0 | 1 | 1 | 1 | 0 |
| 15 | LUT3_3 / DFF6 Output | 0 | 0 | 1 | 1 | 1 | 1 |
| 16 | LUT3_4 / DFF7 Output | 0 | 1 | 0 | 0 | 0 | 0 |
| 17 | LUT3_5 / CNT_DLY2(8bit) Output | 0 | 1 | 0 | 0 | 0 | 1 |
| 18 | LUT3_6 / CNT_DLY3(8bit) Output | 0 | 1 | 0 | 0 | 1 | 0 |
| 19 | LUT3_7 / CNT_DLY4(8bit) Output | 0 | 1 | 0 | 0 | 1 | 1 |
| 20 | LUT3_8 / CNT_DLY5(8bit) Output | 0 | 1 | 0 | 1 | 0 | 0 |
| 21 | LUT3_9 / CNT_DLY6(8bit) Output | 0 | 1 | 0 | 1 | 0 | 1 |
| 22 | LUT4_0 / CNT_DLY0(16bit) Output | 0 | 1 | 0 | 1 | 1 | 0 |
| 23 | LUT4_1 / CNT_DLY1(16bit) Output | 0 | 1 | 0 | 1 | 1 | 1 |
| 24 | LUT3_10 / Pipe Delay (1st stage) Output | 0 | 1 | 1 | 0 | 0 | 0 |
| 25 | Pipe Delay Output0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 26 | Pipe Delay Output1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 27 | Internal OSC Pre-Divided by 1/2/4/8 Output and Post-Divided by 1/2/3/4/8/12/24/64 Output (25KHz/2MHz) | 0 | 1 | 1 | 0 | 1 | 1 |
| 28 | Internal OSC Pre-Divided by 1/2/4/8 Output and Post-Divided by 1/2/3/4/8/12/24/64 Output (25KHz/2MHz) | 0 | 1 | 1 | 1 | 0 | 0 |
| 29 | Internal OSC Pre-Divided by 1/2/4/8 Output (25MHz) | 0 | 1 | 1 | 1 | 0 | 1 |
| 30 | Filter0 / Edge Detect0 Output | 0 | 1 | 1 | 1 | 1 | 0 |
| 31 | Filter1 / Edge Detect1 Output | 0 | 1 | 1 | 1 | 1 | 1 |
| 32 | Pin8 Digital or I2C_virtual_0 Input | 1 | 0 | 0 | 0 | 0 | 0 |
| 33 | Pin9 Digital or I2C_virtual_1 Input | 1 | 0 | 0 | 0 | 0 | 1 |
| 34 | I2C_virtual_2 Input | 1 | 0 | 0 | 0 | 1 | 0 |
| 35 | I2C_virtual_3 Input | 1 | 0 | 0 | 0 | 1 | 1 |

**Table 36. Matrix Input Table**

| Matrix Input Number | Matrix Input Signal Function | Matrix Decode | | | | | |
|---|---|---|---|---|---|---|---|
| | | 5 | 4 | 3 | 2 | 1 | 0 |
| 36 | I2C_virtual_4 Input | 1 | 0 | 0 | 1 | 0 | 0 |
| 37 | I2C_virtual_5 Input | 1 | 0 | 0 | 1 | 0 | 1 |
| 38 | I2C_virtual_6 Input | 1 | 0 | 0 | 1 | 1 | 0 |
| 39 | I2C_virtual_7 Input | 1 | 0 | 0 | 1 | 1 | 1 |
| 40 | ASM-stateX-dout0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 41 | ASM-stateX-dout1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 42 | ASM-stateX-dout2 | 1 | 0 | 1 | 0 | 1 | 0 |
| 43 | ASM-stateX-dout3 | 1 | 0 | 1 | 0 | 1 | 1 |
| 44 | ASM-stateX-dout4 | 1 | 0 | 1 | 1 | 0 | 0 |
| 45 | ASM-stateX-dout5 | 1 | 0 | 1 | 1 | 0 | 1 |
| 46 | ASM-stateX-dout6 | 1 | 0 | 1 | 1 | 1 | 0 |
| 47 | ASM-stateX-dout7 | 1 | 0 | 1 | 1 | 1 | 1 |
| 48 | Pin12 Digital Input | 1 | 1 | 0 | 0 | 0 | 0 |
| 49 | Pin13 Digital Input | 1 | 1 | 0 | 0 | 0 | 1 |
| 50 | Pin14 Digital Input | 1 | 1 | 0 | 0 | 1 | 0 |
| 51 | Pin15 Digital Input | 1 | 1 | 0 | 0 | 1 | 1 |
| 52 | Pin16 Digital Input | 1 | 1 | 0 | 1 | 0 | 0 |
| 53 | Pin17 Digital Input | 1 | 1 | 0 | 1 | 0 | 1 |
| 54 | Pin18 Digital Input | 1 | 1 | 0 | 1 | 1 | 0 |
| 55 | Pin19 Digital Input | 1 | 1 | 0 | 1 | 1 | 1 |
| 56 | Pin20 Digital Input | 1 | 1 | 1 | 0 | 0 | 0 |
| 57 | ACMP_0 Output | 1 | 1 | 1 | 0 | 0 | 1 |
| 58 | ACMP_1 Output | 1 | 1 | 1 | 0 | 1 | 0 |
| 59 | ACMP_2 Output | 1 | 1 | 1 | 0 | 1 | 1 |
| 60 | ACMP_3 Output | 1 | 1 | 1 | 1 | 0 | 0 |
| 61 | Programmable Delay with Edge Detector Output | 1 | 1 | 1 | 1 | 0 | 1 |
| 62 | Resetb_core (POR) as matrix input | 1 | 1 | 1 | 1 | 1 | 0 |
| 63 | VDD | 1 | 1 | 1 | 1 | 1 | 1 |

## 8.2 Matrix Output Table

**Table 37. Matrix Output Table**

| Register Bit Address | Matrix Output Signal Function<br>Note: For each Address, the two most significant bits are unused) | Matrix Output Number |
|---|---|---|
| reg <7:0> | Matrix OUT: ASM-state0-EN0 | 0 |
| reg <15:8> | Matrix OUT: ASM-state0-EN1 | 1 |
| reg <23:16> | Matrix OUT: ASM-state0-EN2 | 2 |
| reg <31:24> | Matrix OUT: ASM-state1-EN0 | 3 |
| reg <39:32> | Matrix OUT: ASM-state1-EN1 | 4 |
| reg <47:40> | Matrix OUT: ASM-state1-EN2 | 5 |
| reg <55:48> | Matrix OUT: ASM-state2-EN0 | 6 |
| reg <63:56> | Matrix OUT: ASM-state2-EN1 | 7 |
| reg <71:64> | Matrix OUT: ASM-state2-EN2 | 8 |
| reg <79:72> | Matrix OUT: ASM-state3-EN0 | 9 |
| reg <87:80> | Matrix OUT: ASM-state3-EN1 | 10 |
| reg <95:88> | Matrix OUT: ASM-state3-EN2 | 11 |
| reg <103:96> | Matrix OUT: ASM-state4-EN0 | 12 |
| reg <111:104> | Matrix OUT: ASM-state4-EN1 | 13 |
| reg <119:112> | Matrix OUT: ASM-state4-EN2 | 14 |
| reg <127:120> | Matrix OUT: ASM-state5-EN0 | 15 |
| reg <135:128> | Matrix OUT: ASM-state5-EN1 | 16 |
| reg <143:136> | Matrix OUT: ASM-state5-EN2 | 17 |
| reg <151:144> | Matrix OUT: ASM-state6-EN0 | 18 |
| reg <159:152> | Matrix OUT: ASM-state6-EN1 | 19 |
| reg <167:160> | Matrix OUT: ASM-state6-EN2 | 20 |
| reg <175:168> | Matrix OUT: ASM-state7-EN0 | 21 |
| reg <183:176> | Matrix OUT: ASM-state7-EN1 | 22 |
| reg <191:184> | Matrix OUT: ASM-state7-EN2 | 23 |
| reg <199:192> | Matrix OUT: ASM-state-RSTB | 24 |
| reg <207:200> | Matrix OUT: PIN3 Digital Output Source | 25 |
| reg <215:208> | Matrix OUT: PIN3 Output Enable | 26 |
| reg <223:216> | Matrix OUT: PIN4 Digital Output Source | 27 |
| reg <231:224> | Matrix OUT: PIN5 Digital Output Source | 28 |
| reg <239:232> | Matrix OUT: PIN5 Output Enable | 29 |
| reg <247:240> | Matrix OUT: PIN6 Digital Output Source | 30 |
| reg <255:248> | Matrix OUT: PIN7 Digital Output Source | 31 |
| reg <263:256> | Matrix OUT: PIN7 Output Enable | 32 |
| reg <271:264> | Matrix OUT: PIN8 Digital Output Source (SCL with VI/Input & NMOS open-drain) | 33 |
| reg <279:272> | Matrix OUT: PIN9 Digital Output Source (SDA with VI/Input & NMOS open-drain) | 34 |
| reg <287:280> | Matrix OUT: PIN10 Digital Output Source | 35 |
| reg <295:288> | Matrix OUT: PIN10 Output Enable | 36 |
| reg <303:296> | Matrix OUT: PIN12 Digital Output Source | 37 |

**Table 37. Matrix Output Table**

| Register Bit Address | Matrix Output Signal Function<br>Note: For each Address, the two most significant bits are unused) | Matrix Output Number |
|---|---|---|
| reg <311:304> | Matrix OUT: PIN13 Digital Output Source | 38 |
| reg <319:312> | Matrix OUT: PIN13 Output Enable | 39 |
| reg <327:320> | Matrix OUT: PIN14 Digital Output Source | 40 |
| reg <335:328> | Matrix OUT: PIN14 Output Enable | 41 |
| reg <343:336> | Matrix OUT: PIN15 Digital Output Source | 42 |
| reg <351:344> | Matrix OUT: PIN16 Digital Output Source | 43 |
| reg <359:352> | Matrix OUT: PIN16 Output Enable | 44 |
| reg <367:360> | Matrix OUT: PIN17 Digital Output Source | 45 |
| reg <375:368> | Matrix OUT: PIN18 Digital Output Source | 46 |
| reg <383:376> | Matrix OUT: PIN18 Output Enable | 47 |
| reg <391:384> | Matrix OUT: PIN19 Digital Output Source | 48 |
| reg <399:392> | Matrix OUT: PIN19 Output Enable | 49 |
| reg <407:400> | Matrix OUT: PIN20 Digital Output Source | 50 |
| reg <415:408> | Matrix OUT: ACMP0 PDB (Power Down) | 51 |
| reg <423:416> | Matrix OUT: ACMP1 PDB (Power Down) | 52 |
| reg <431:424> | Matrix OUT: ACMP2 PDB (Power Down) | 53 |
| reg <439:432> | Matrix OUT: ACMP3 PDB (Power Down) | 54 |
| reg <447:440> | Matrix OUT: Input of Filter_0 with fixed time edge detector | 55 |
| reg <455:448> | Matrix OUT: Input of Filter_1 with fixed time edge detector | 56 |
| reg <463:456> | Matrix OUT: Input of Programmable Delay & Edge Detector | 57 |
| reg <471:464> | Matrix OUT: OSC 25KHz/2MHz PDB (Power Down) | 58 |
| reg <479:472> | Matrix OUT: OSC 25MHz PDB (Power Down) | 59 |
| reg <487:480> | Matrix OUT: IN0 of LUT2_0 or Clock Input of DFF0 | 60 |
| reg <495:488> | Matrix OUT: IN1 of LUT2_0 or Data Input of DFF0 | 61 |
| reg <503:496> | Matrix OUT: IN0 of LUT2_1 or Clock Input of DFF1 | 62 |
| reg <511:504> | Matrix OUT: IN1 of LUT2_1 or Data Input of DFF1 | 63 |
| reg <519:512> | Matrix OUT: IN0 of LUT2_2 or Clock Input of DFF2 | 64 |
| reg <527:520> | Matrix OUT: IN1 of LUT2_2 or Data Input of DFF2 | 65 |
| reg <535:528> | Matrix OUT: IN0 of LUT2_3 or Clock Input of PGEN | 66 |
| reg <543:536> | Matrix OUT: IN1 of LUT2_3 or RSTB of PGEN | 67 |
| reg <551:544> | Matrix OUT: IN0 of LUT3_0 or Clock Input of DFF3 | 68 |
| reg <559:552> | Matrix OUT: IN1 of LUT3_0 or Data Input of DFF3 | 69 |
| reg <567:560> | Matrix OUT: IN2 of LUT3_0 or RSTB (SETB) of DFF3 | 70 |
| reg <575:568> | Matrix OUT: IN0 of LUT3_1 or Clock Input of DFF4 | 71 |
| reg <583:576> | Matrix OUT: IN1 of LUT3_1 or Data Input of DFF4 | 72 |
| reg <591:584> | Matrix OUT: IN2 of LUT3_1 or RSTB (SETB) of DFF4 | 73 |
| reg <599:592> | Matrix OUT: IN0 of LUT3_2 or Clock Input of DFF5 | 74 |
| reg <607:600> | Matrix OUT: IN1 of LUT3_2 or Data Input of DFF5 | 75 |
| reg <615:608> | Matrix OUT: IN2 of LUT3_2 or RSTB (SETB) of DFF5 | 76 |

**Table 37. Matrix Output Table**

| Register Bit Address | Matrix Output Signal Function<br>Note: For each Address, the two most significant bits are unused) | Matrix Output Number |
|---|---|---|
| reg <623:616> | Matrix OUT: IN0 of LUT3_3 or Clock Input of DFF6 | 77 |
| reg <631:624> | Matrix OUT: IN1 of LUT3_3 or Data Input of DFF6 | 78 |
| reg <639:632> | Matrix OUT: IN2 of LUT3_3 or RSTB (SETB) of DFF6 | 79 |
| reg <647:640> | Matrix OUT: IN0 of LUT3_4 or Clock Input of DFF7 | 80 |
| reg <655:648> | Matrix OUT: IN1 of LUT3_4 or Data Input of DFF7 | 81 |
| reg <663:656> | Matrix OUT: IN2 of LUT3_4 or RSTB (SETB) of DFF7 | 82 |
| reg <671:664> | Matrix OUT: IN0 of LUT3_5 or Delay2 Input (or Counter2 RST Input) | 83 |
| reg <679:672> | Matrix OUT: IN1 of LUT3_5 or External Clock Input of Delay2 (or Counter2) | 84 |
| reg <687:680> | Matrix OUT: IN2 of LUT3_5 | 85 |
| reg <695:688> | Matrix OUT: IN0 of LUT3_6 or Delay3 Input (or Counter3 RST Input) | 86 |
| reg <703:696> | Matrix OUT: IN1 of LUT3_6 or External Clock Input of Delay3 (or Counter3) | 87 |
| reg <711:704> | Matrix OUT: IN2 of LUT3_6 | 88 |
| reg <719:712> | Matrix OUT: IN0 of LUT3_7 or Delay4 Input (or Counter4 RST Input) | 89 |
| reg <727:720> | Matrix OUT: IN1 of LUT3_7 or External Clock Input of Delay4 (or Counter4) | 90 |
| reg <735:728> | Matrix OUT: IN2 of LUT3_7 | 91 |
| reg <743:736> | Matrix OUT: IN0 of LUT3_8 or Delay5 Input (or Counter5 RST Input) | 92 |
| reg <751:744> | Matrix OUT: IN1 of LUT3_8 or External Clock Input of Delay5 (or Counter5) | 93 |
| reg <759:752> | Matrix OUT: IN2 of LUT3_8 | 94 |
| reg <767:760> | Matrix OUT: IN0 of LUT3_9 or Delay6 Input (or Counter6 RST Input) | 95 |
| reg <775:768> | Matrix OUT: IN1 of LUT3_9 or External Clock Input of Delay6 (or Counter6) | 96 |
| reg <783:776> | Matrix OUT: IN2 of LUT3_9 | 97 |
| reg <791:784> | Matrix OUT: IN0 of LUT3_10 or Input of Pipe Delay | 98 |
| reg <799:792> | Matrix OUT: IN1 of LUT3_10 or RSTB of Pipe Delay | 99 |
| reg <807:800> | Matrix OUT: IN2 of LUT3_10 or Clock of Pipe Delay | 100 |
| reg <815:808> | Matrix OUT: IN0 of LUT4_0 or Delay0 Input (or Counter0 RST/SET Input) | 101 |
| reg <823:816> | Matrix OUT: IN1 of LUT4_0 or External Clock Input of Delay0 (or Counter0) | 102 |
| reg <831:824> | Matrix OUT: IN2 of LUT4_0 or UP Input of FSM0 | 103 |
| reg <839:832> | Matrix OUT: IN3 of LUT4_0 or KEEP Input of FSM0 | 104 |
| reg <847:840> | Matrix OUT: IN0 of LUT4_1 or Delay1 Input (or Counter1 RST/SET Input) | 105 |
| reg <855:848> | Matrix OUT: IN1 of LUT4_1 or External Clock Input of Delay1 (or Counter1) | 106 |
| reg <863:856> | Matrix OUT: IN2 of LUT4_1 or UP Input of FSM1 | 107 |
| reg <871:864> | Matrix OUT: IN3 of LUT4_1 or KEEP Input of FSM1 | 108 |
| reg <879:872> | Matrix OUT: PD of either Temp-output with BG AND/OR crystal oscillator by reg<1268> | 109 |

### 8.3 Connection Matrix Virtual Inputs

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via $I^2C$. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The $I^2C$ address for reading and writing these register values is at byte 0244.

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An $I^2C$ write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs,(Pin8 Digital or I2C_virtual_0 Input) and (Pin9 Digital or I2C_virtual_1 Input). If the virtual input mode is selected, an $I^2C$ write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). Two register bits select whether the Connection Matrix input comes from the pin input or from the virtual register:

- reg <1074> Select SCL & Virtual Input 0 or PIN8
- reg <1082> Select SDA & Virtual Input 1 or PIN9

See table below for Connection Matrix Virtual Inputs.

| Matrix Input Number | Matrix Input Signal Function | Register Bit Addresses (d) |
|---|---|---|
| 32 | I2C_virtual_0 Input | reg<1952> |
| 33 | I2C_virtual_1 Input | reg<1953> |
| 34 | I2C_virtual_2 Input | reg<1954> |
| 35 | I2C_virtual_3 Input | reg<1955> |
| 36 | I2C_virtual_4 Input | reg<1956> |
| 37 | I2C_virtual_5 Input | reg<1957> |
| 38 | I2C_virtual_6 Input | reg<1958> |
| 39 | I2C_virtual_7 Input | reg<1959> |

### 8.4 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via $I^2C$. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The $I^2C$ addresses for reading these register values are at bytes 0240 to 0247. Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0244).

## 9.0 Combination Function Macro Cells

The SLG46531 has seventeen combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells;

- Three macrocells that can serve as either 2-bit LUTs or as D Flip Flops.
- Five macrocells that can serve as either 3-bit LUTs or as D Flip Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGEN)
- Five macrocells that can serve as either 3-bit LUTs or as 8-Bit Counter / Delays
- Two macrocells that can serve as either 4-bit LUTs or as 16-Bit Counter / Delays

Inputs/Outputs for the 17 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

### 9.1 2-Bit LUT or D Flip Flop Macrocells

There are three macrocells that can serve as either 2-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (d) and clock (clk) inputs for the Flip Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: if CLK = 0, then Q = D

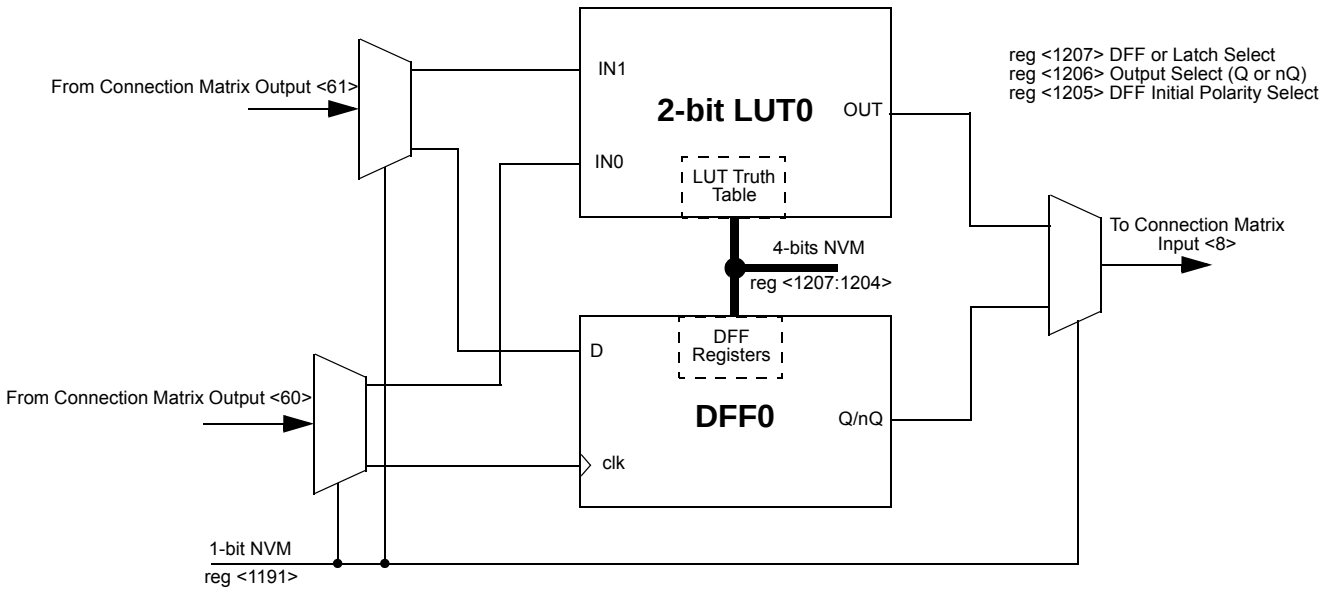



**Figure 10. 2-bit LUT0 or DFF0**

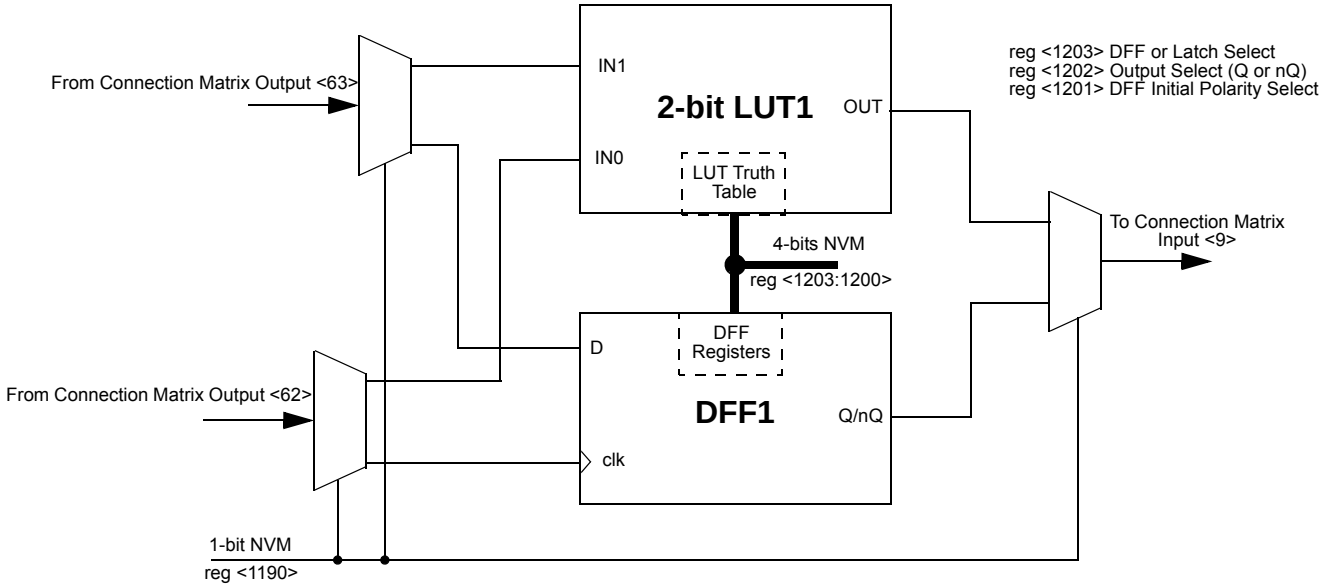



**Figure 11. 2-bit LUT1 or DFF1**

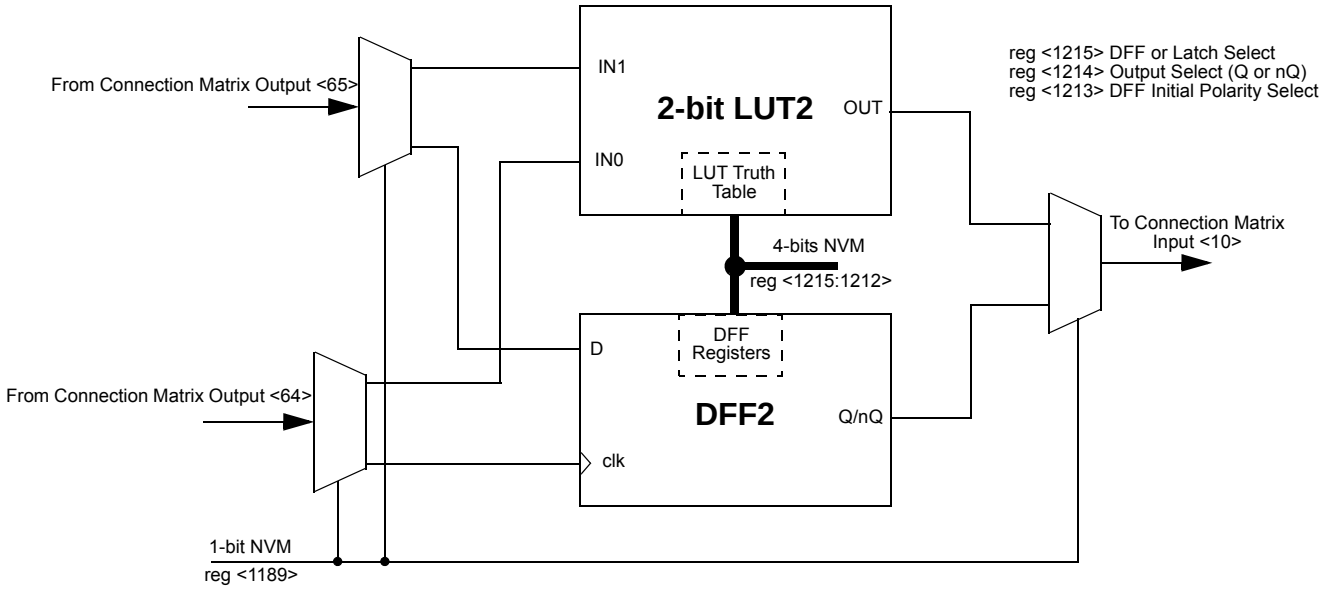



**Figure 12. 2-bit LUT2 or DFF2**

### 9.1.1 2-Bit LUT or D Flip Flop Macrocells Used as 2-Bit LUTs

**Table 38. 2-bit LUT0 Truth Table**

| IN1 | IN0 | OUT |
|---|---|---|
| 0 | 0 | reg <1204> |
| 0 | 1 | reg <1205> |
| 1 | 0 | reg <1206> |
| 1 | 1 | reg <1207> |

**Table 39. 2-bit LUT1 Truth Table**

| IN1 | IN0 | OUT |
|---|---|---|
| 0 | 0 | reg <1200> |
| 0 | 1 | reg <1201> |
| 1 | 0 | reg <1202> |
| 1 | 1 | reg <1203> |

**Table 40. 2-bit LUT2 Truth Table**

| IN1 | IN0 | OUT |
|---|---|---|
| 0 | 0 | reg <1212> |
| 0 | 1 | reg <1213> |
| 1 | 0 | reg <1214> |
| 1 | 1 | reg <1215> |

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

*2-Bit LUT0 is defined by reg<1207:1204>*

*2-Bit LUT1 is defined by reg<1203:1200>*

*2-Bit LUT2 is defined by reg<1215:1212>*

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 2-bit LUT logic cells.

**Table 41. 2-bit LUT Standard Digital Functions**

| Function | MSB | | | LSB |
|---|---|---|---|---|
| AND-2 | 1 | 0 | 0 | 0 |
| NAND-2 | 0 | 1 | 1 | 1 |
| OR-2 | 1 | 1 | 1 | 0 |
| NOR-2 | 0 | 0 | 0 | 1 |
| XOR-2 | 0 | 1 | 1 | 0 |
| XNOR-2 | 1 | 0 | 0 | 1 |

### 9.1.2 2-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

**Table 42. DFF0 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT2_0 or DFF0 Select | <1191> | 0: LUT2_0<br>1: DFF0 |
| DFF0 Initial Polarity Select | <1205> | 0: Low<br>1: High |
| DFF0 Output Select | <1206> | 0: Q output<br>1: nQ output |
| DFF0 or Latch Select | <1207> | 0: DFF function<br>1: Latch function |

**Table 43. DFF1 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT2_1 or DFF1 Select | <1190> | 0: LUT2_1<br>1: DFF1 |
| DFF1 Initial Polarity Select | <1201> | 0: Low<br>1: High |
| DFF1 Output Select | <1202> | 0: Q output<br>1: nQ output |
| Select or Latch select | <1203> | 0: DFF function<br>1: Latch function |

**Table 44. DFF2 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT2_2 or DFF2 Select | <1189> | 0: LUT2_2<br>1: DFF2 |
| DFF2 Initial Polarity Select | <1213> | 0: Low<br>1: High |
| DFF2 Output Select | <1214> | 0: Q output<br>1: nQ output |
| DFF2 or Latch Select | <1215> | 0: DFF function<br>1: Latch function |

### 9.2 Initial Polarity Operations

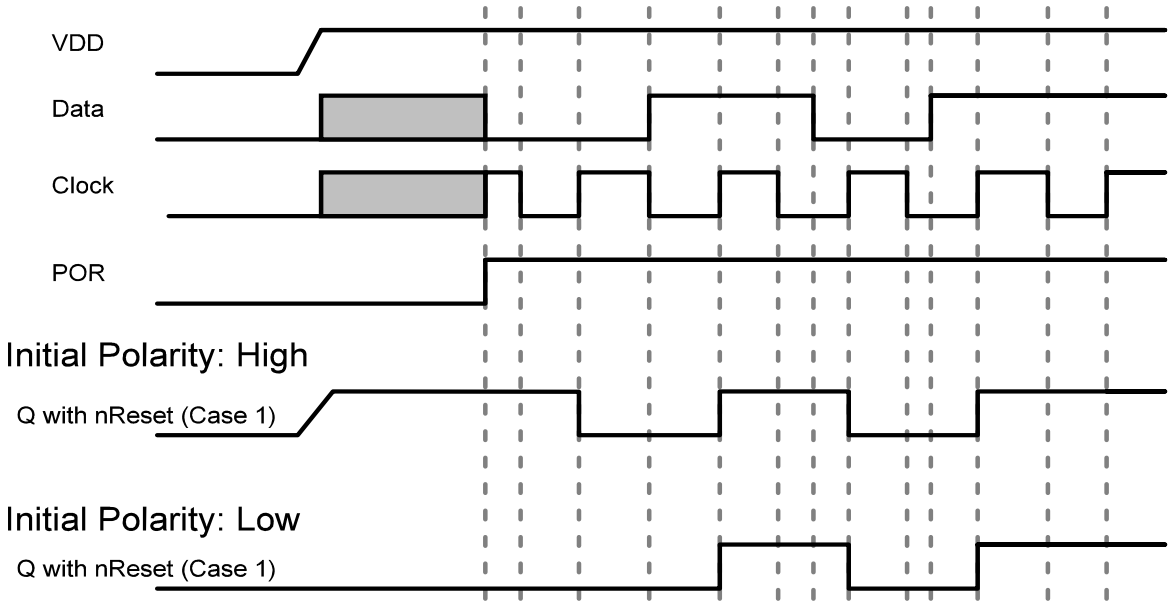



**Figure 13. DFF Polarity Operations**

### 9.3 2-bit LUT or Programmable Pattern Generator

The SLG46531 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGEN).

When used to implement LUT functions, the 2-bit LUT takes in four input signals from the connection matrix 0 and produce a single output, which goes back into the connection matrix 0. When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Pattern Generator, the output of the block with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

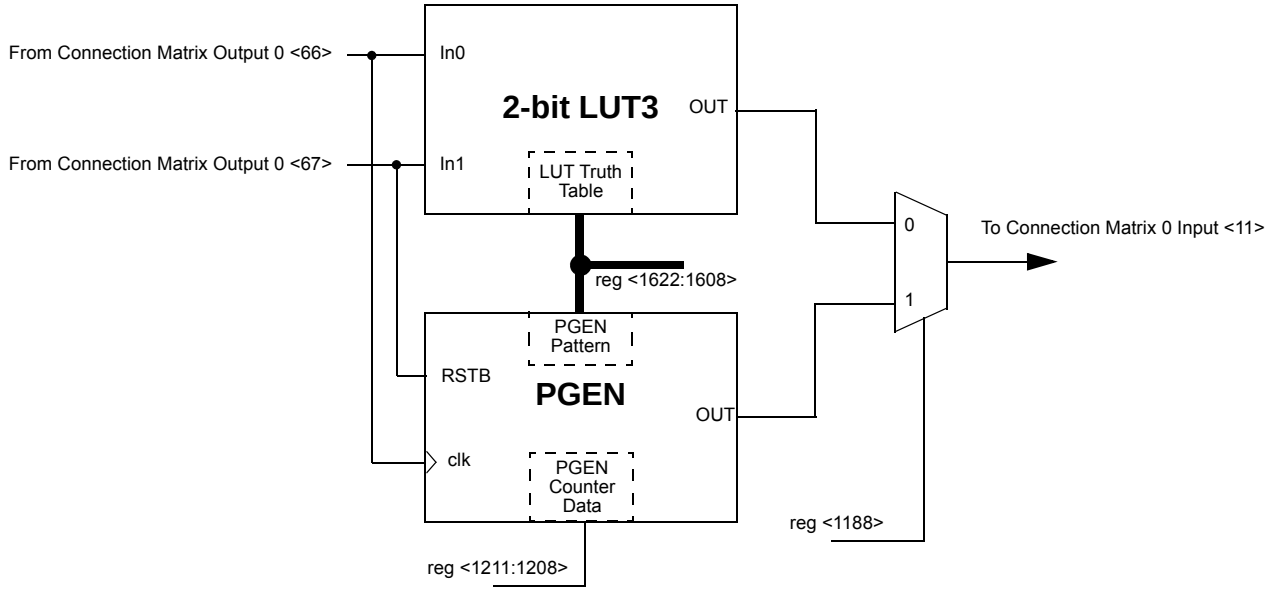



**Figure 14. 2-bit LUT3 or PGEN**

### 9.4 3-Bit LUT or D Flip Flop with Set/Reset Macrocells

There are five macrocells that can serve as either 3-bit LUTs or as D Flip Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (d) and clock (clk) and Set/Reset (rRST/nSET) inputs for the Flip Flop, with the output going back to the connection matrix.

DFF3 has a user selectable option to allow the macrocell output to either come from the Q/nQ output of one D Flip Flop, or two D Flip Flops in series, with the first D Flip Flop triggering on the rising clock edge, and the second D Flip Flop triggering on the falling clock edge.

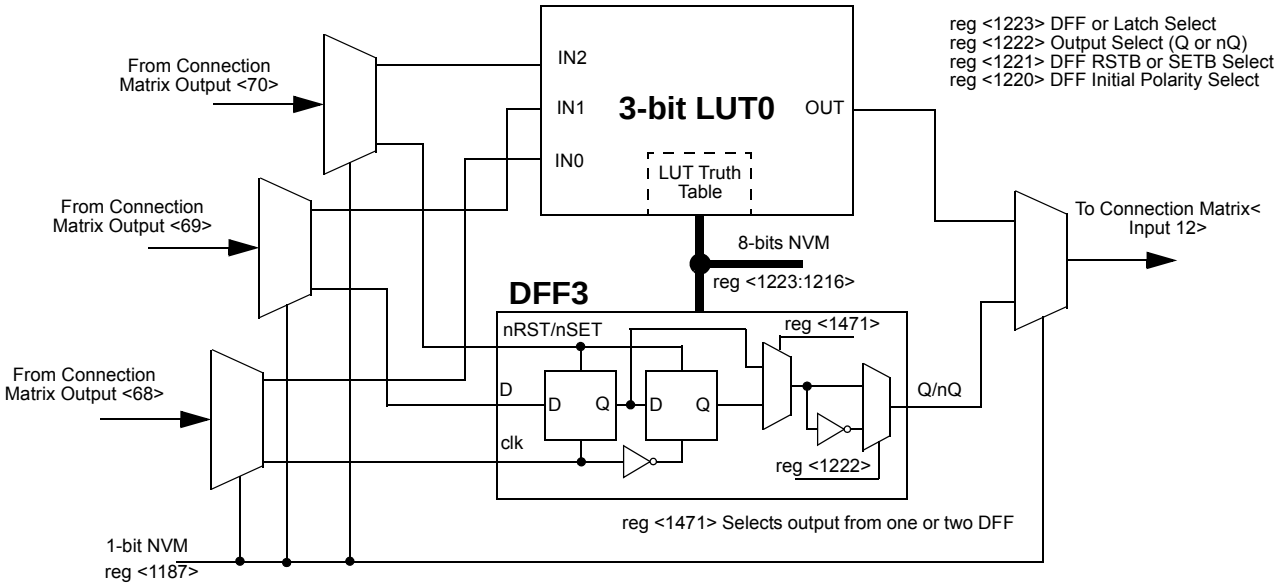



**Figure 15. 3-bit LUT0 or DFF3**

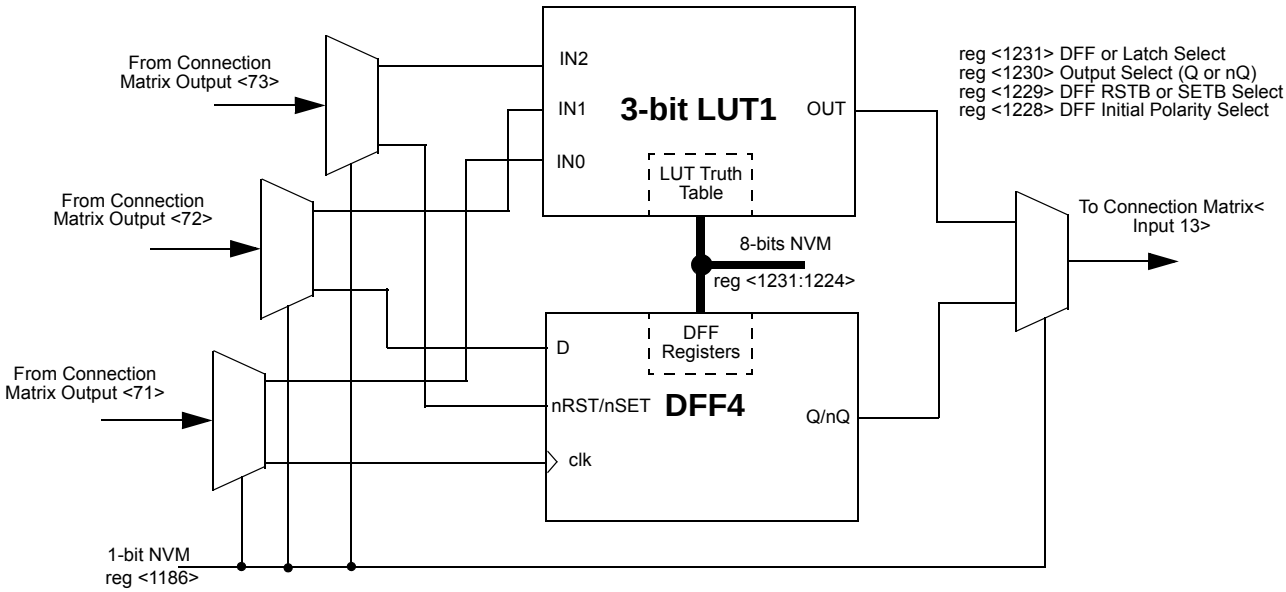



**Figure 16. 3-bit LUT1 or DFF4**

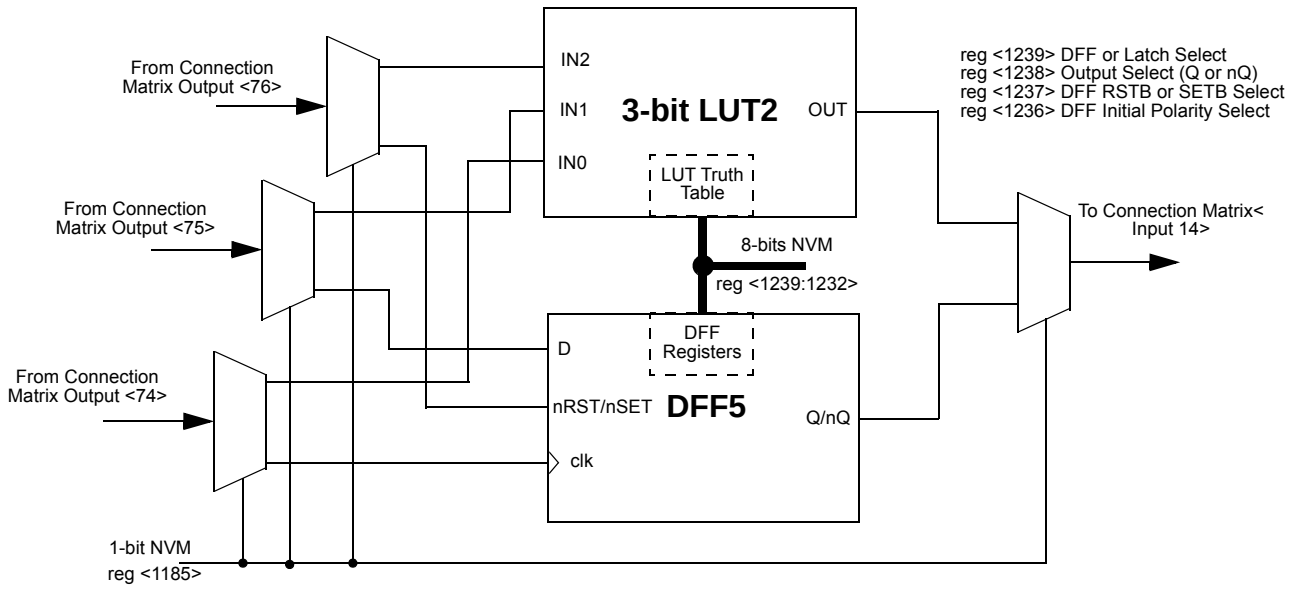



**Figure 17. 3-bit LUT2 or DFF5**

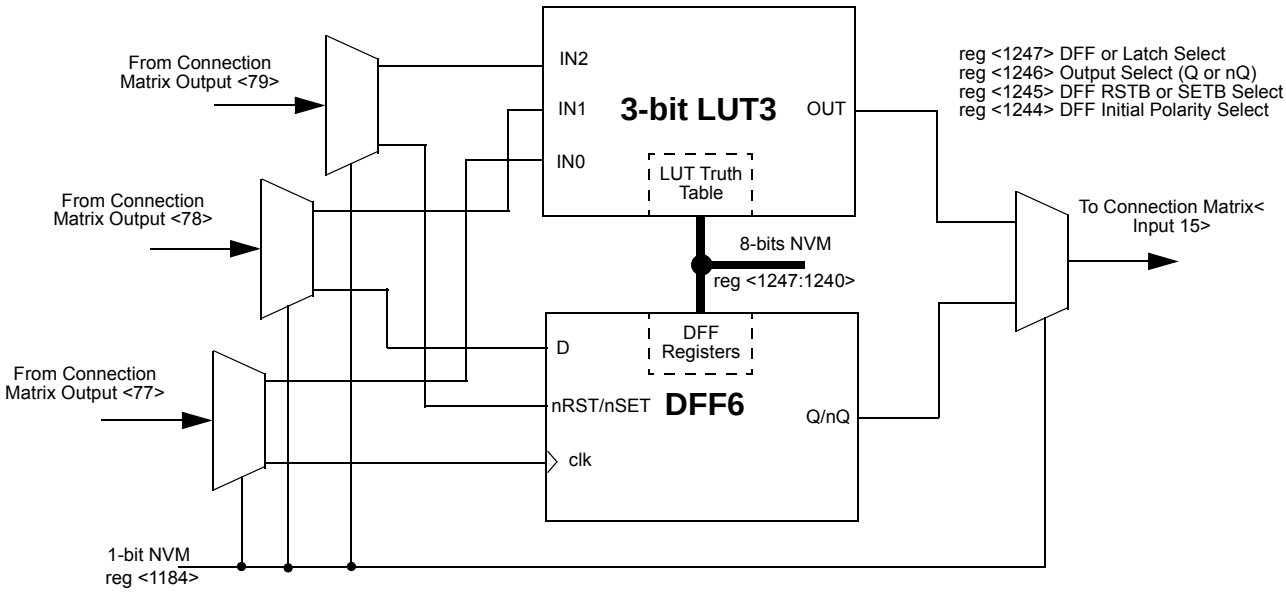



**Figure 18. 3-bit LUT3 or DFF6**

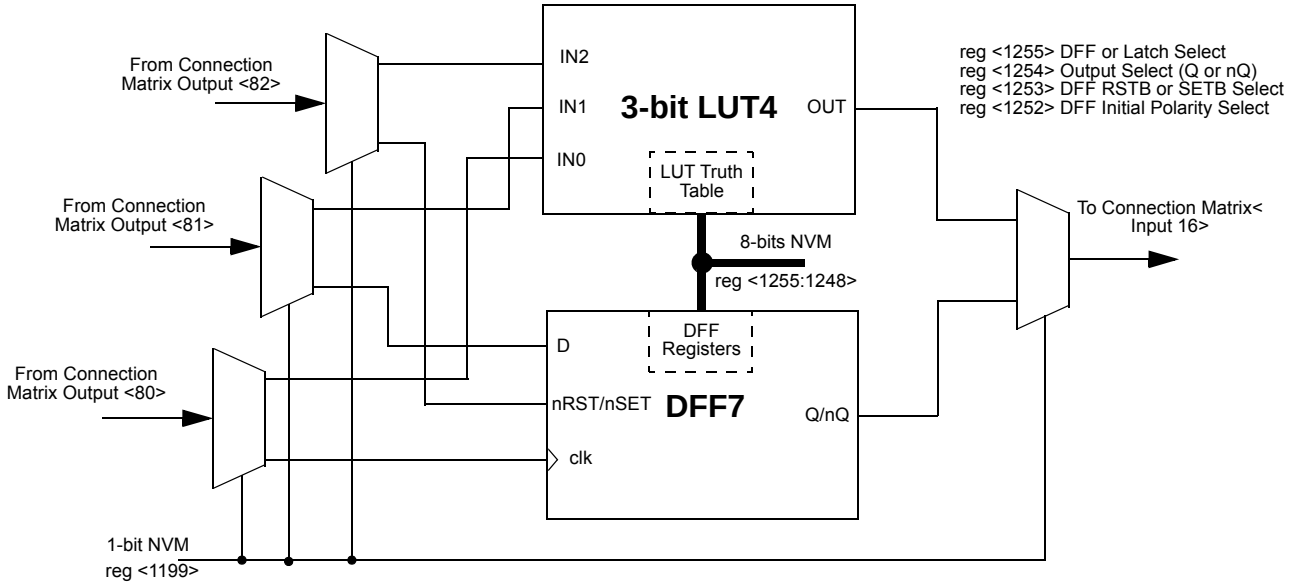



**Figure 19. 3-bit LUT4 or DFF7**

### 9.4.1 3-Bit LUT or D Flip Flop Macrocells Used as 3-Bit LUTs

**Table 45. 3-bit LUT0 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1216> |
| 0 | 0 | 1 | reg <1217> |
| 0 | 1 | 0 | reg <1218> |
| 0 | 1 | 1 | reg <1219> |
| 1 | 0 | 0 | reg <1220> |
| 1 | 0 | 1 | reg <1221> |
| 1 | 1 | 0 | reg <1222> |
| 1 | 1 | 1 | reg <1223> |

**Table 46. 3-bit LUT1 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1224> |
| 0 | 0 | 1 | reg <1225> |
| 0 | 1 | 0 | reg <1226> |
| 0 | 1 | 1 | reg <1227> |
| 1 | 0 | 0 | reg <1228> |
| 1 | 0 | 1 | reg <1229> |
| 1 | 1 | 0 | reg <1230> |
| 1 | 1 | 1 | reg <1231> |

**Table 47. 3-bit LUT2 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1232> |
| 0 | 0 | 1 | reg <1233> |
| 0 | 1 | 0 | reg <1234> |
| 0 | 1 | 1 | reg <1235> |
| 1 | 0 | 0 | reg <1236> |
| 1 | 0 | 1 | reg <1237> |
| 1 | 1 | 0 | reg <1238> |
| 1 | 1 | 1 | reg <1239> |

**Table 48. 3-bit LUT3 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1240> |
| 0 | 0 | 1 | reg <1241> |
| 0 | 1 | 0 | reg <1242> |
| 0 | 1 | 1 | reg <1243> |
| 1 | 0 | 0 | reg <1244> |
| 1 | 0 | 1 | reg <1245> |
| 1 | 1 | 0 | reg <1246> |
| 1 | 1 | 1 | reg <1247> |

**Table 49. 3-bit LUT4 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1248> |
| 0 | 0 | 1 | reg <1249> |
| 0 | 1 | 0 | reg <1250> |
| 0 | 1 | 1 | reg <1251> |
| 1 | 0 | 0 | reg <1252> |
| 1 | 0 | 1 | reg <1253> |
| 1 | 1 | 0 | reg <1254> |
| 1 | 1 | 1 | reg <1255> |

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

*3-Bit LUT0 is defined by reg<1223:1216>*

*3-Bit LUT1 is defined by reg<1231:1324>*

*3-Bit LUT2 is defined by reg<1239:1232>*

*3-Bit LUT3 is defined by reg<1247:1240>*

*3-Bit LUT5 is defined by reg<1235:1248>*

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six 3-bit LUT logic cells.

**Table 50. 3-bit LUT Standard Digital Functions**

| Function | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| AND-3 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NAND-3 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| OR-3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| NOR-3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| XOR-3 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| XNOR-3 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

### 9.4.2 3-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

**Table 51. DFF3 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_0 or DFF3 Select | reg<1187> | 0: LUT3_0<br>1: DFF3 |
| DFF3 Initial Polarity Select | reg<1220> | 0: Low<br>1: High |
| DFF3 rstb/setb Select | reg<1221> | 1: setb from matrix out<br>0: resetb from matrix out |
| DFF3 Output Select | reg<1222> | 0: Q output<br>1: nQ output |
| DFF3 or Latch Select | reg<1223> | 0: DFF function<br>1: Latch function |

**Table 52. DFF4 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_1 or DFF4 Select | reg<1186> | 0: LUT3_1<br>1: DFF4 |
| DFF4 Initial Polarity Select | reg<1128> | 0: Low<br>1: High |
| DFF4 rstb/setb Select | reg<1129> | 1: setb from matrix out<br>0: resetb from matrix out |
| DFF4 Output Select | reg<1130> | 0: Q output<br>1: nQ output |
| DFF4 or Latch Select | reg<1131> | 0: DFF function<br>1: Latch function |

**Table 53. DFF5 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_2 or DFF5 Select | reg<1185> | 0: LUT3_2<br>1: DFF5 |
| DFF5 Initial Polarity Select | reg<1236> | 0: Low<br>1: High |
| DFF5 rstb/setb Select | reg<1237> | 1: setb from matrix out<br>0: resetb from matrix out |
| DFF5 Output Select | reg<1238> | 0: Q output<br>1: nQ output |
| DFF5 or Latch Select | reg<1239> | 0: DFF function<br>1: Latch function |

**Table 54. DFF6 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_3 or DFF6 Select | reg<1184> | 0: LUT3_3<br>1: DFF6 |
| DFF6 Initial Polarity Select | reg<1244> | 0: Low<br>1: High |
| DFF6 rstb/setb Select | reg<1245> | 1: setb from matrix out<br>0: resetb from matrix out |
| DFF6 Output Select | reg<1246> | 0: Q output<br>1: nQ output |
| DFF6 or Latch Select | reg<1247> | 0: DFF function<br>1: Latch function |

**Table 55. DFF7 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_4 or DFF7 Select | reg<1199> | 0: LUT3_4<br>1: DFF7 |
| DFF7 Initial Polarity Select | reg<1252> | 0: Low<br>1: High |
| DFF7 rstb/setb Select | reg<1253> | 1: setb from matrix out<br>0: resetb from matrix out |
| DFF7 Output Select | reg<1254> | 0: Q output<br>1: nQ output |
| DFF7 or Latch Select | reg<1255> | 0: DFF function<br>1: Latch function |

### 9.5 Initial Polarity Operations

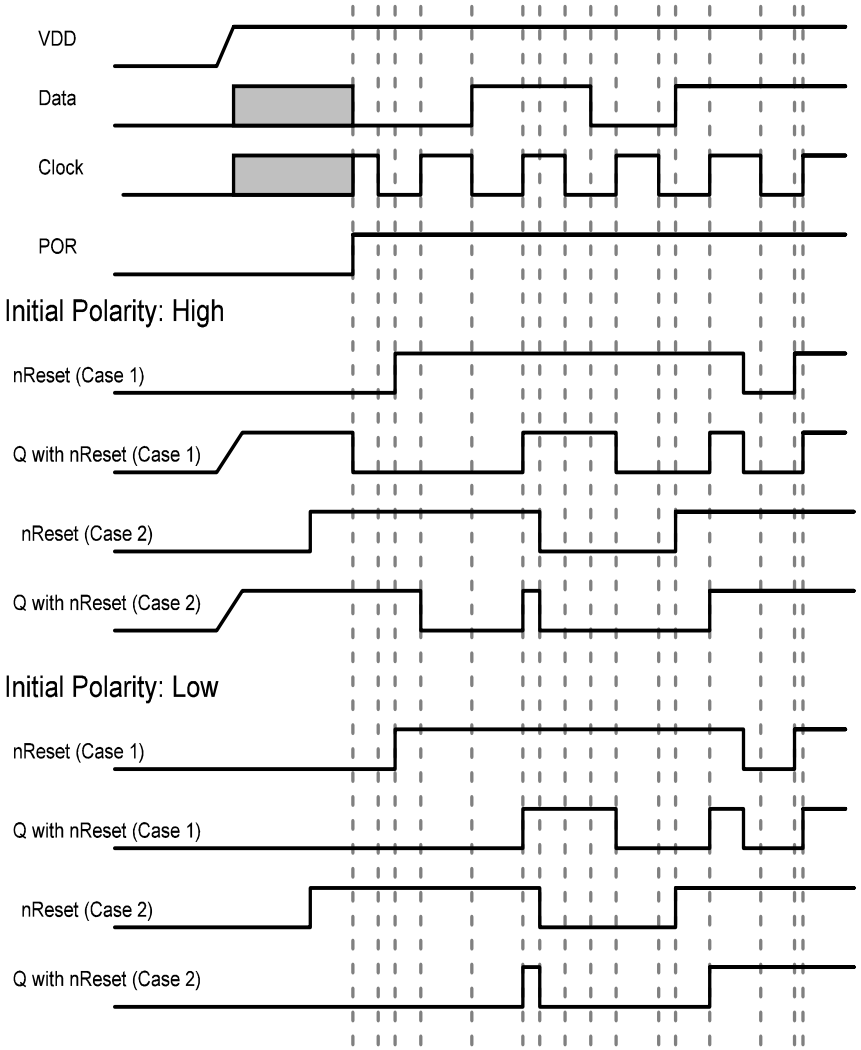



**Figure 20. DFF Polarity Operations with nReset**

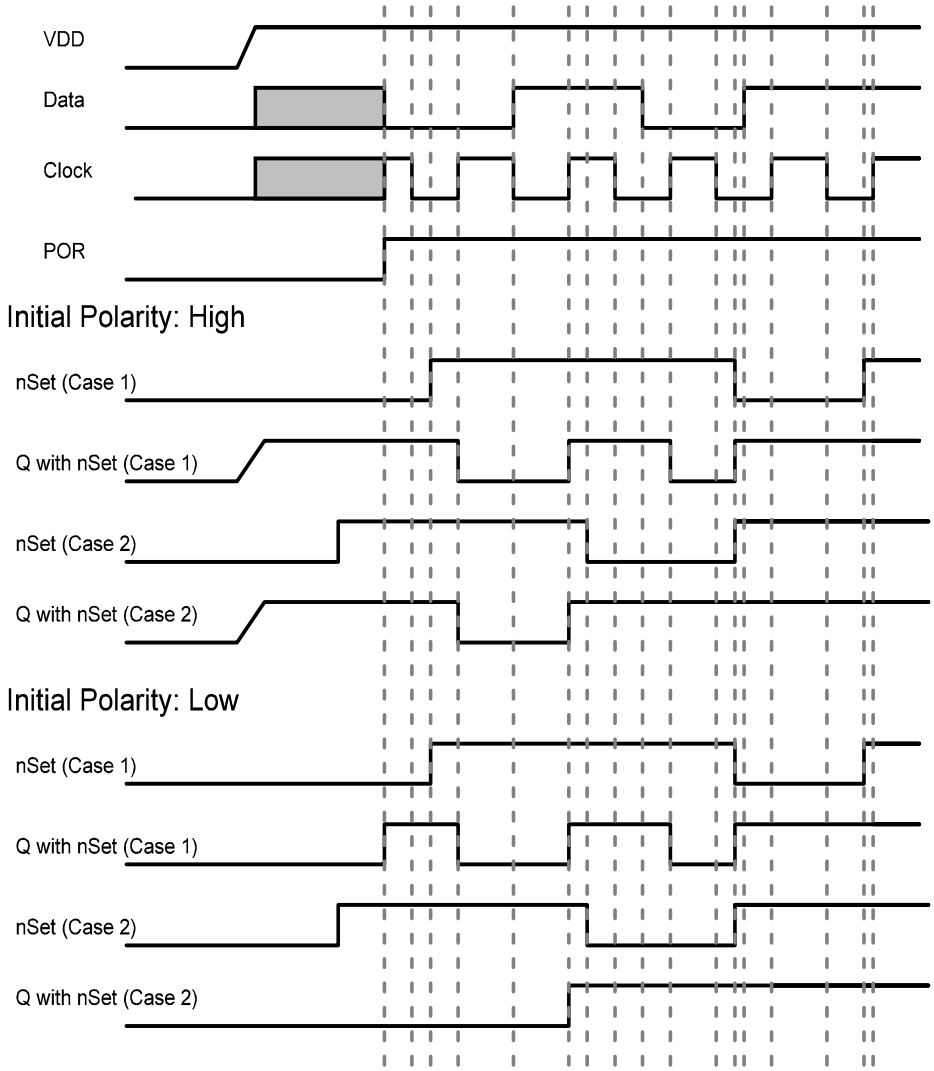



**Figure 21. DFF Polarity Operations with nSet**

### 9.6 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT take in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK) and Reset (RST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The first delay option (OUT2) is fixed at the output of the first flip-flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by reg <1259:1256> for OUT0 and reg <1263:1260> for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46531 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46531). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

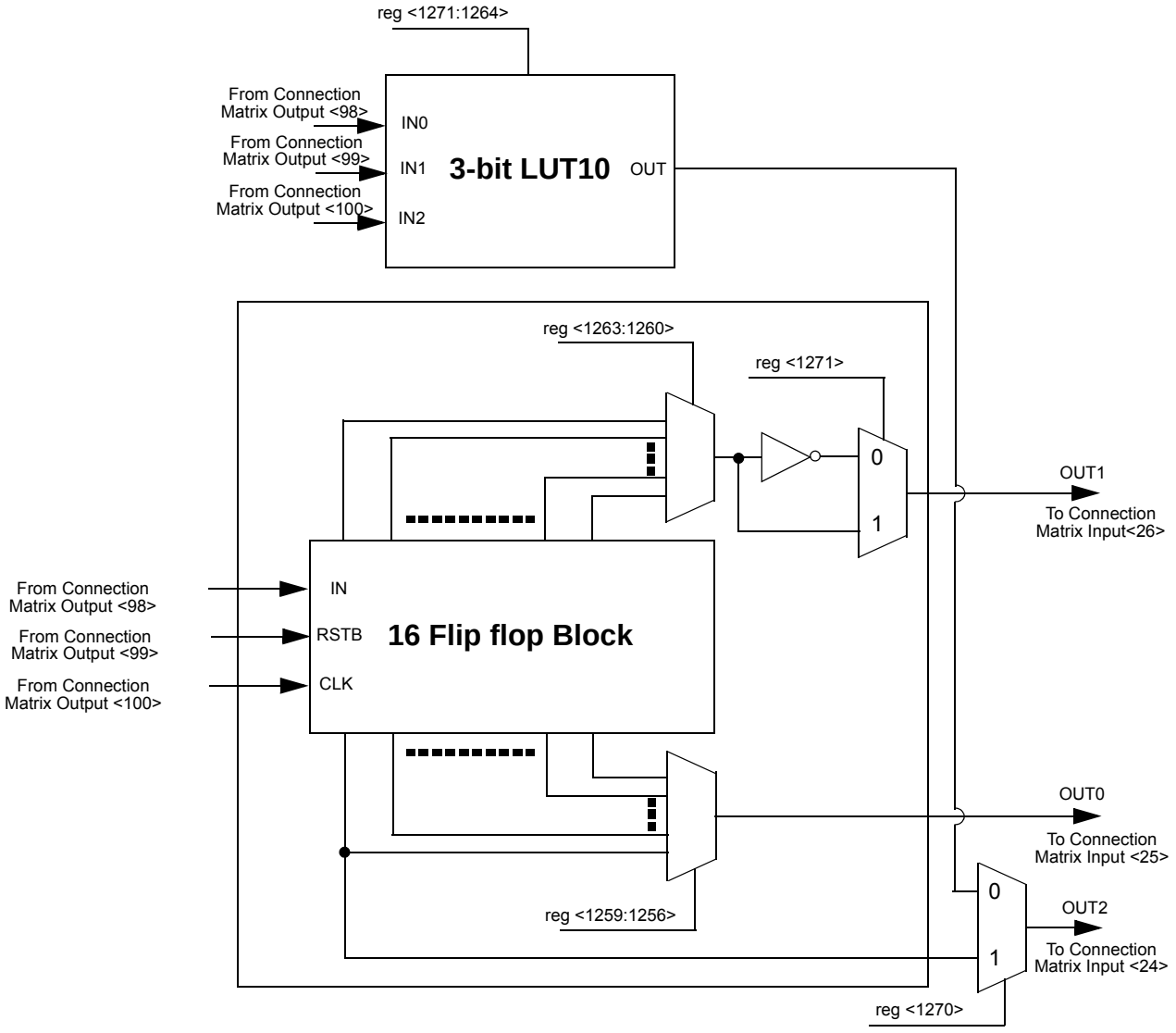



**Figure 22. 3-bit LUT10 or Pipe Delay**

### 9.6.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

**Table 56. 3-bit LUT10 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1264> |
| 0 | 0 | 1 | reg <1265> |
| 0 | 1 | 0 | reg <1266> |
| 0 | 1 | 1 | reg <1267> |
| 1 | 0 | 0 | reg <1268> |
| 1 | 0 | 1 | reg <1269> |
| 1 | 1 | 0 | reg <1270> |
| 1 | 1 | 1 | reg <1271> |

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

*3-Bit LUT10 is defined by reg<1271:1264>*

### 9.6.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

**Table 57. Pipe Delay Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_10 or Pipe Delay Output Select | reg<1270> | 0: LUT3_10<br>1: 1 Pipe Delay Output |
| OUT0 select | reg<1259:1256> | |
| OUT1 select | reg<1263:1260> | |
| Pipe delay OUT1 Polarity Select Bit | reg<1271> | 0: Non-inverted<br>1: Inverted |

### 9.7 3-Bit LUT or 8- Bit Counter / Delay Macrocells

There are five macrocells that can serve as either 3-bit LUTs or as Counter / Delays. When used to implement LUT function, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter / Delay function, two of the four input signals from the connection matrix go to the external clock (ext_clk) and reset (DLY_n/CNT_Reset) for the counter/delay, with the output going back to the connection matrix.

These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection or edge detection mode.

Two of the five macrocells can have their active count value read via $I^2C$ (CNT4 and CNT6). See Section 19.4.6.3 for further details

#### 9.7.1 3-Bit LUT or 8- Bit CNT/DLY Block Diagrams

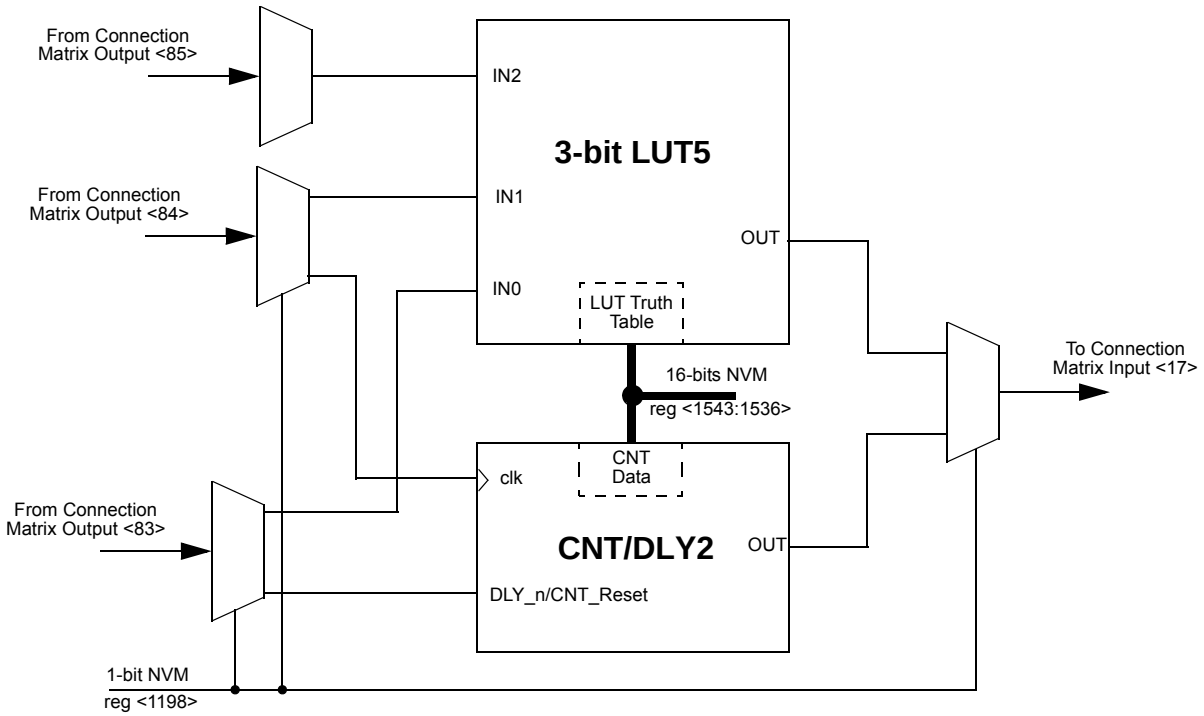



**Figure 23. 3-bit LUT5 or CNT/DLY2**

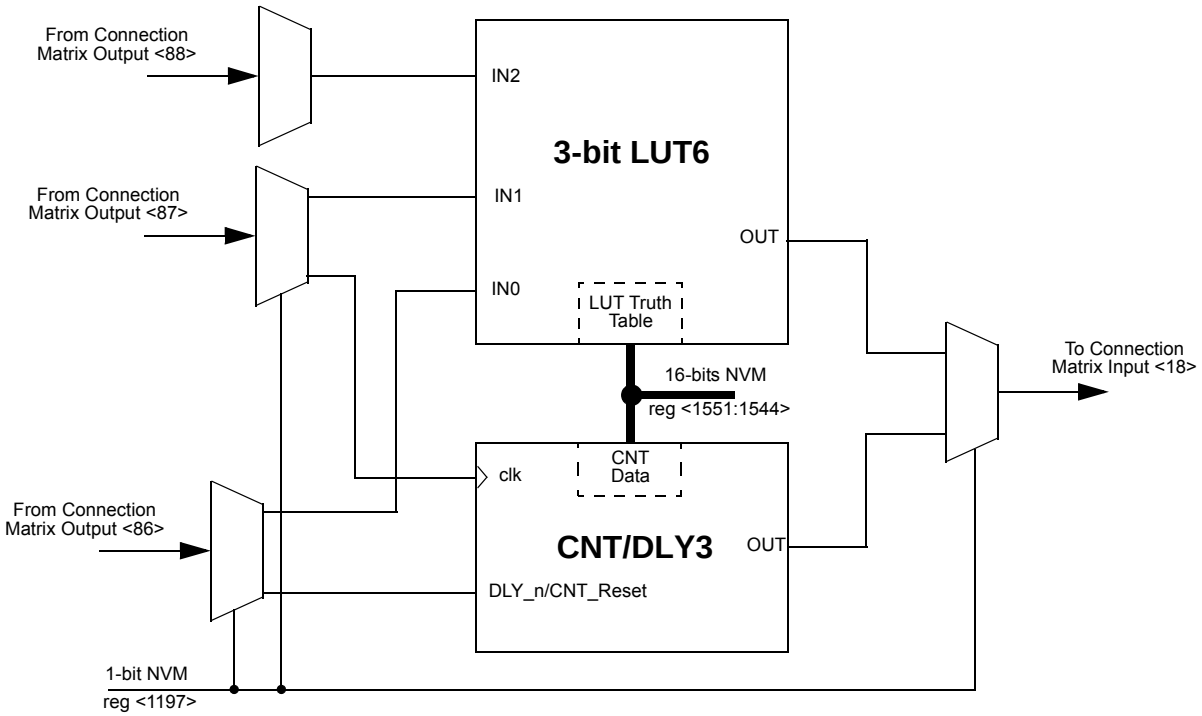



**Figure 24. 3-bit LUT6 or CNT/DLY3**

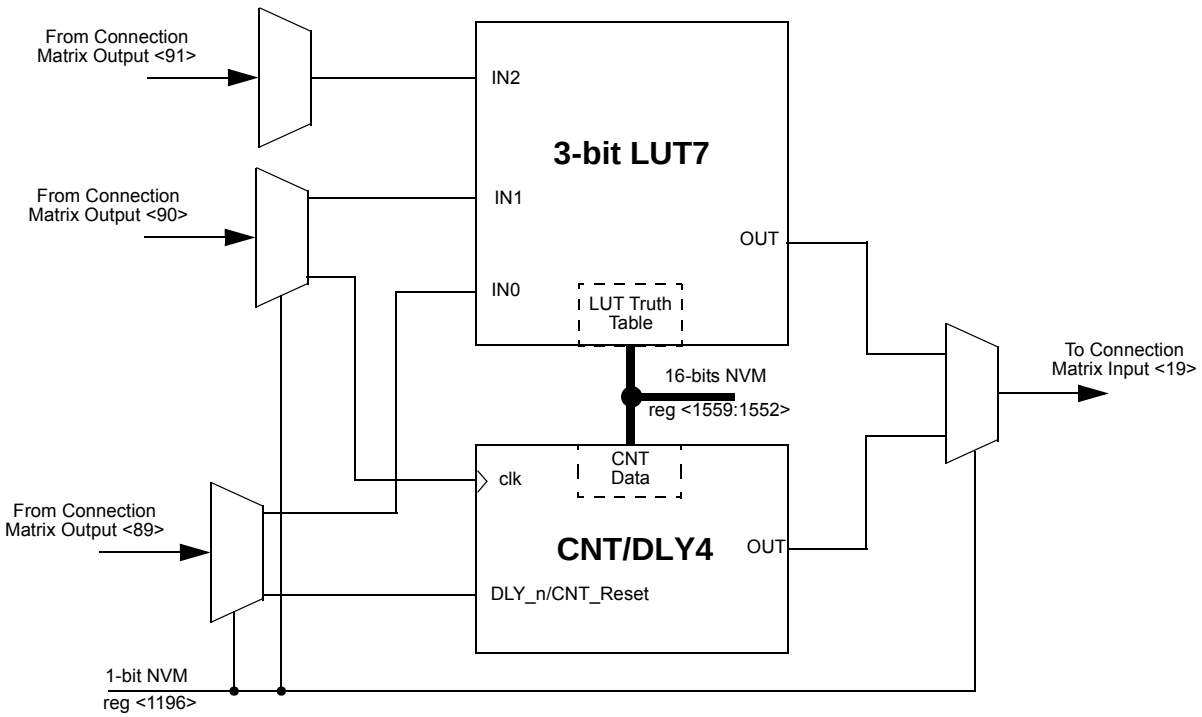



**Figure 25. 3-bit LUT7 or CNT/DLY4**

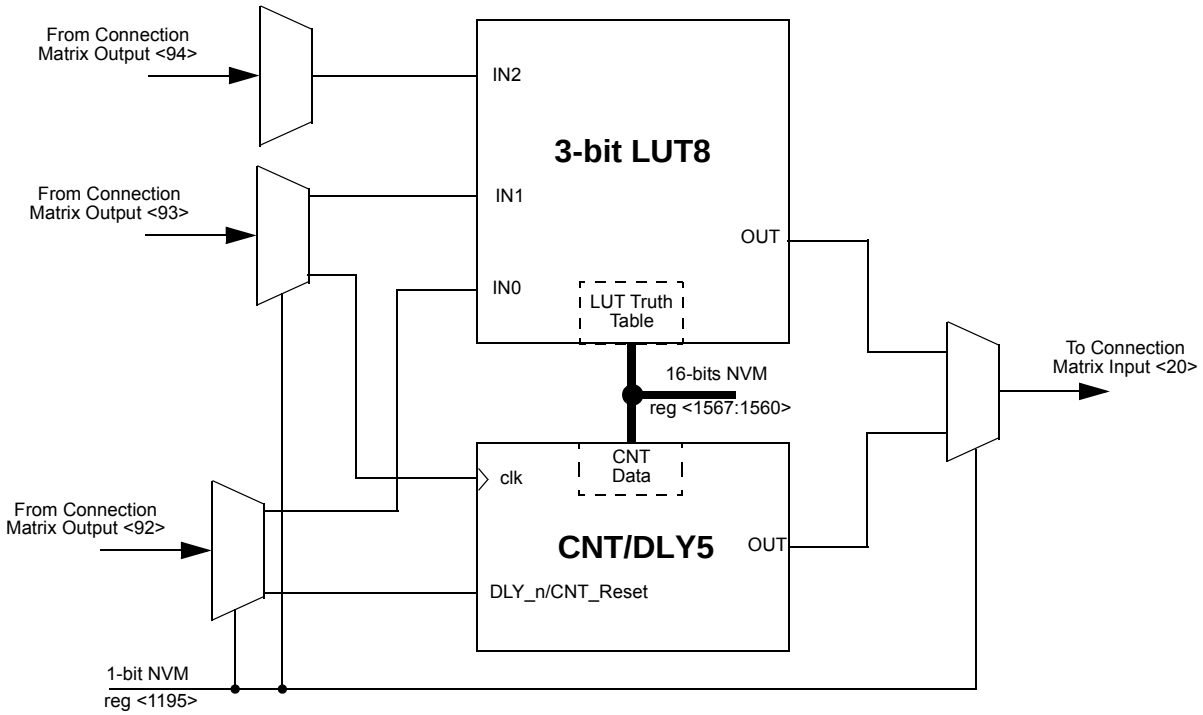



**Figure 26. 3-bit LUT8 or CNT/DLY5**

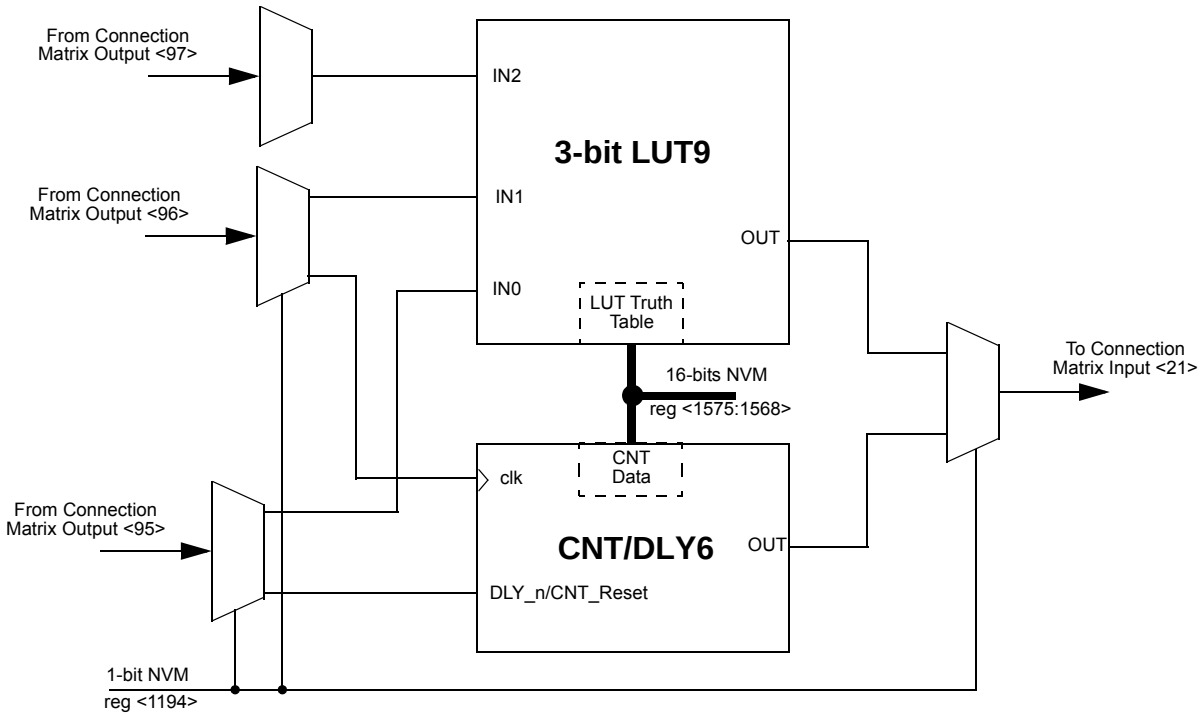



**Figure 27. 3-bit LUT9 or CNT/DLY6**

### 9.7.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

**Table 58. 3-bit LUT5 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1536> |
| 0 | 0 | 1 | reg <1537> |
| 0 | 1 | 0 | reg <1538> |
| 0 | 1 | 1 | reg <1539> |
| 1 | 0 | 0 | reg <1540> |
| 1 | 0 | 1 | reg <1541> |
| 1 | 1 | 0 | reg <1542> |
| 1 | 1 | 1 | reg <1543> |

**Table 59. 3-bit LUT6 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1544> |
| 0 | 0 | 1 | reg <1545> |
| 0 | 1 | 0 | reg <1546> |
| 0 | 1 | 1 | reg <1547> |
| 1 | 0 | 0 | reg <1548> |
| 1 | 0 | 1 | reg <1549> |
| 1 | 1 | 0 | reg <1550> |
| 1 | 1 | 1 | reg <1551> |

**Table 60. 3-bit LUT7 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1552> |
| 0 | 0 | 1 | reg <1553> |
| 0 | 1 | 0 | reg <1554> |
| 0 | 1 | 1 | reg <1555> |
| 1 | 0 | 0 | reg <1556> |
| 1 | 0 | 1 | reg <1557> |
| 1 | 1 | 0 | reg <1558> |
| 1 | 1 | 1 | reg <1559> |

**Table 61. 3-bit LUT8 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1560> |
| 0 | 0 | 1 | reg <1561> |
| 0 | 1 | 0 | reg <1562> |
| 0 | 1 | 1 | reg <1563> |
| 1 | 0 | 0 | reg <1564> |
| 1 | 0 | 1 | reg <1565> |
| 1 | 1 | 0 | reg <1566> |
| 1 | 1 | 1 | reg <1567> |

**Table 62. 3-bit LUT9 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | reg <1568> |
| 0 | 0 | 1 | reg <1569> |
| 0 | 1 | 0 | reg <1570> |
| 0 | 1 | 1 | reg <1571> |
| 1 | 0 | 0 | reg <1572> |
| 1 | 0 | 1 | reg <1573> |
| 1 | 1 | 0 | reg <1574> |
| 1 | 1 | 1 | reg <1575> |

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

*3-Bit LUT5 is defined by reg<1543:1536>*

*3-Bit LUT6 is defined by reg<1551:1544>*

*3-Bit LUT7 is defined by reg<1559:1552>*

*3-Bit LUT8 is defined by reg<1567:1560>*

*3-Bit LUT9 is defined by reg<1573:1568>*

### 9.7.3 3-Bit LUT or 8-Bit Counter / Delay Macrocells Used as 8-Bit Counter / Delay Register Settings

**Table 63. CNT/DLY2 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_5 or Counter2 Select | reg<1198> | 0: LUT3_5<br>1: Counter2 |
| Delay2 Mode Select or asynchronous counter reset | reg<1273:1272> | 00: on both falling and rising edges (for delay & counter reset)<br>01: on falling edge only (for delay & counter reset)<br>10: on rising edge only (for delay & counter reset)<br>11: no delay on either falling or rising edges / high level reset |
| Counter/delay2 Clock Source Select | reg<1276:1274> | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter1 Overflow |
| Counter/delay2 Output Selection for Counter mode | reg<1277> | 0: Default Output<br>1: Edge Detector Output |
| Counter/delay2 Mode Selection | reg<1279:1278> | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode |
| Counter/delay2 Control Data | reg<1543:1536> | 1 – 256 (delay time = (counter control data +1) /freq) |

**Table 64. CNT/DLY3 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_6 or Counter3 Select | reg<1197> | 0: LUT3_6<br>1: Counter3 |
| Delay3 Mode Select or asynchronous counter reset | reg<1281:1280> | 00: on both falling and rising edges (for delay & counter reset)<br>01: on falling edge only (for delay & counter reset)<br>10: on rising edge only (for delay & counter reset)<br>11: no delay on either falling or rising edges / high level reset |
| Counter/delay3 Clock Source Select | reg<1284:1282> | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter2 Overflow |
| Counter/delay3 Output Selection for Counter mode | reg<1285> | 0: Default Output<br>1: Edge Detector Output |
| Counter/delay2 Mode Selection | reg<1287:1286> | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode |
| Counter/delay3 Control Data | reg<1551:1544> | 1 – 256 (delay time = (counter control data +1) /freq) |

**Table 65. CNT/DLY4 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_7 or Counter4 Select | reg<1196> | 0: LUT3_7<br>1: Counter4 |
| Delay4 Mode Select or asynchronous counter reset | reg<1289:1288> | 00: on both falling and rising edges (for delay & counter reset)<br>01: on falling edge only (for delay & counter reset)<br>10: on rising edge only (for delay & counter reset)<br>11: no delay on either falling or rising edges / high level reset |
| Counter/delay4 Clock Source Select | reg<1292:1290> | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter3 Overflow |
| Counter/delay4 Output Selection for Counter mode | reg<1293> | 0: Default Output<br>1: Edge Detector Output |
| Counter/delay4 Mode Selection | reg<1295:1294> | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode |
| Counter/delay4 Control Data | reg<1559:1552> | 1 – 256 (delay time = (counter control data +1) /freq) |

**Table 66. CNT/DLY5 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_8 or Counter5 Select | reg<1195> | 0: LUT3_8<br>1: Counter5 |
| Delay5 Mode Select or asynchronous counter reset | reg<1297:1296> | 00: on both falling and rising edges (for delay & counter reset)<br>01: on falling edge only (for delay & counter reset)<br>10: on rising edge only (for delay & counter reset)<br>11: no delay on either falling or rising edges / high level reset |
| Counter/delay5 Clock Source Select | reg<1300:1298> | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter4 Overflow |
| Counter/delay5 Output Selection for Counter mode | reg<1301> | 0: Default Output<br>1: Edge Detector Output |
| Counter/delay5 Mode Selection | reg<1303:1302> | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode |
| Counter/delay5 Control Data | reg<1567:1560> | 1 – 256 (delay time = (counter control data +1) /freq) |

**Table 67. CNT/DLY6 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT3_9 or Counter5 Select | reg<1194> | 0: LUT3_9<br>1: Counter6 |
| Delay6 Mode Select or asynchronous counter reset | reg<1305:1304> | 00: on both falling and rising edges (for delay & counter reset)<br>01: on falling edge only (for delay & counter reset)<br>10: on rising edge only (for delay & counter reset)<br>11: no delay on either falling or rising edges / high level reset |
| Counter/delay6 Clock Source Select | reg<1308:1306> | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter5 Overflow |
| Counter/delay6 Output Selection for Counter mode | reg<1309> | 0: Default Output<br>1: Edge Detector Output |
| Counter/delay6 Mode Selection | reg<1311:1310> | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode |
| Counter/delay6 Control Data | reg<1575:1568> | 1 – 256 (delay time = (counter control data +1) /freq) |

### 9.7.4 CNT/DLY Timing Diagrams

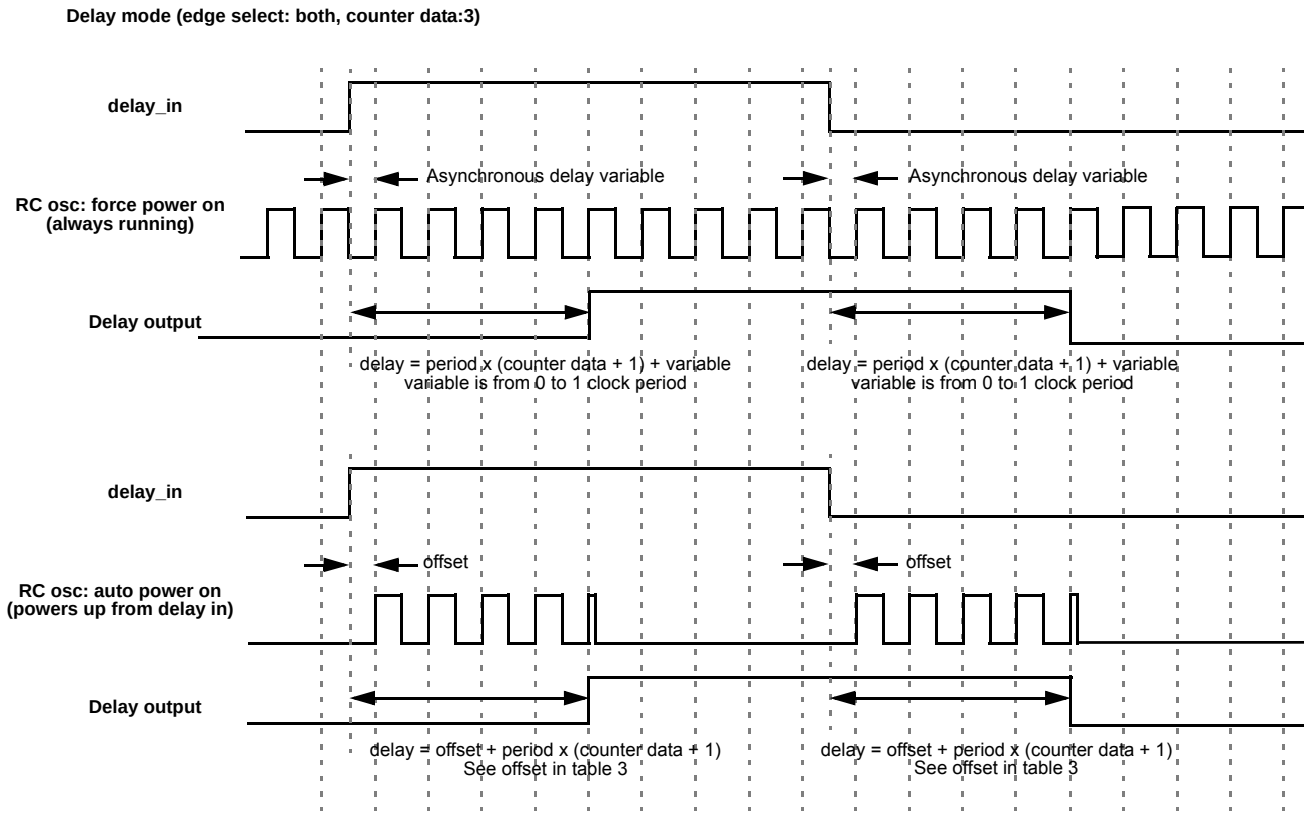



**Figure 28. Delay Mode Timing**

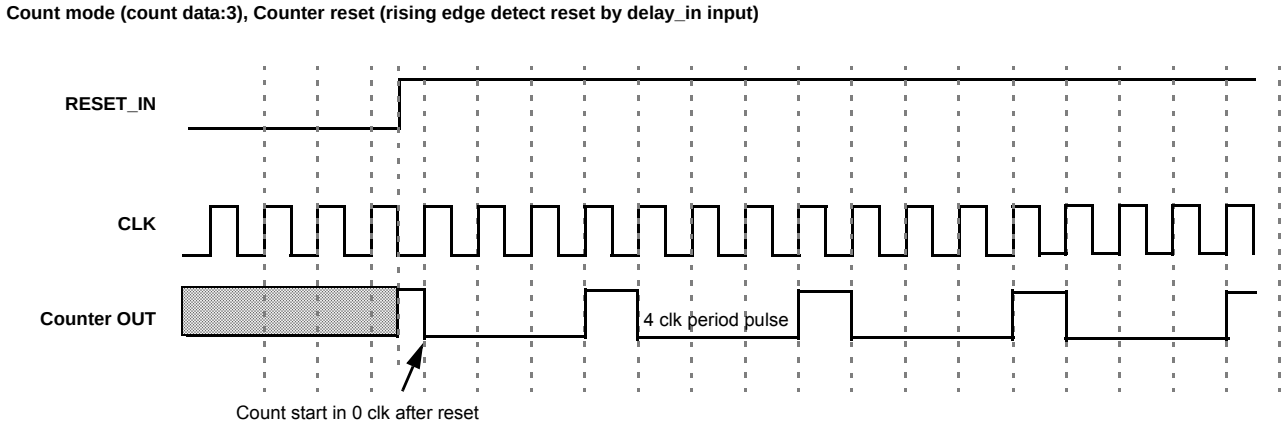



**Figure 29. Counter Mode Timing**

#### 9.7.4.1 One-shot mode

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. There is also an option to ignore or detect selected edge during pulse is outputting. The following diagram is showing one-shot function for non-inverted output. The following diagram is showing one-shot function for non-inverted output.

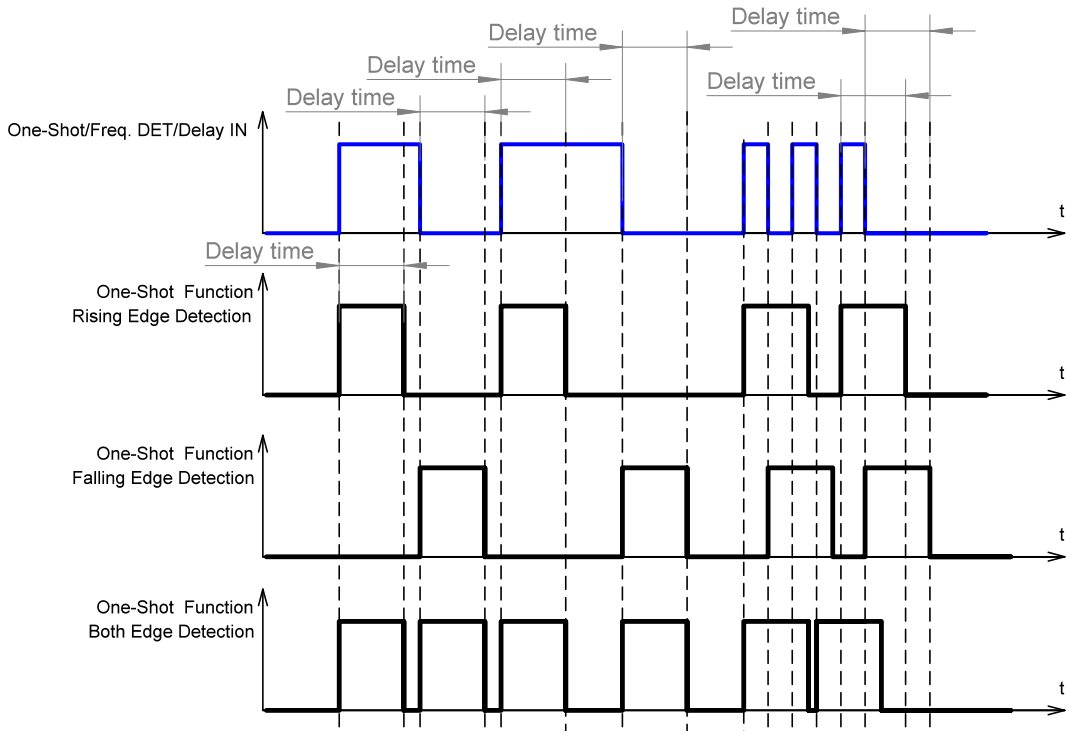



**Figure 30. One-shot function**

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

### 9.7.4.2 Frequency Detection Mode

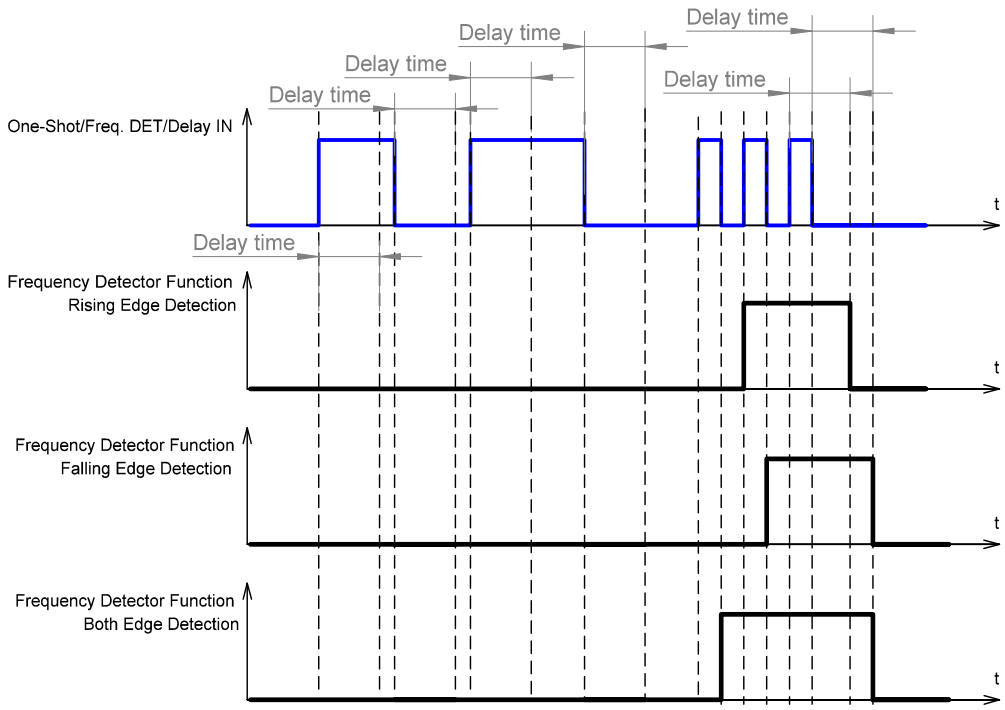



**Figure 31. Frequency Detection Mode**

Rising Edge: The output goes high if the time between two successive edges is less than the set time. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

The output goes low if the second edge has not come after the last rising/falling edge in specified time.

#### 9.7.4.3 Edge Detection Mode

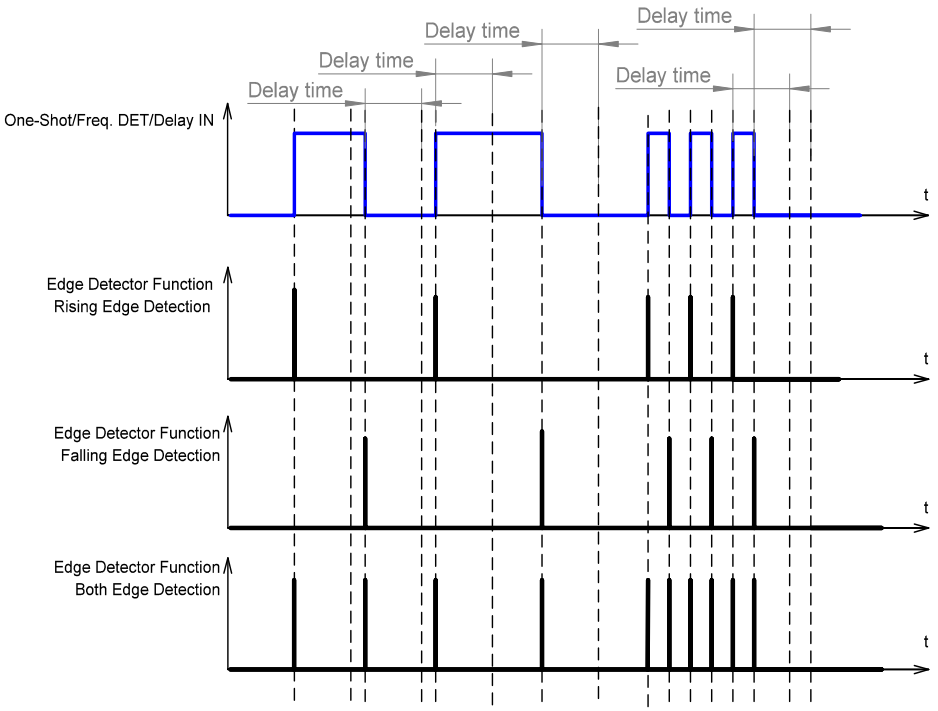



**Figure 32. Edge Detection Mode**

The macrocell generates high level short pulse when detecting the respective edge.

#### 9.7.4.4 Delay Mode

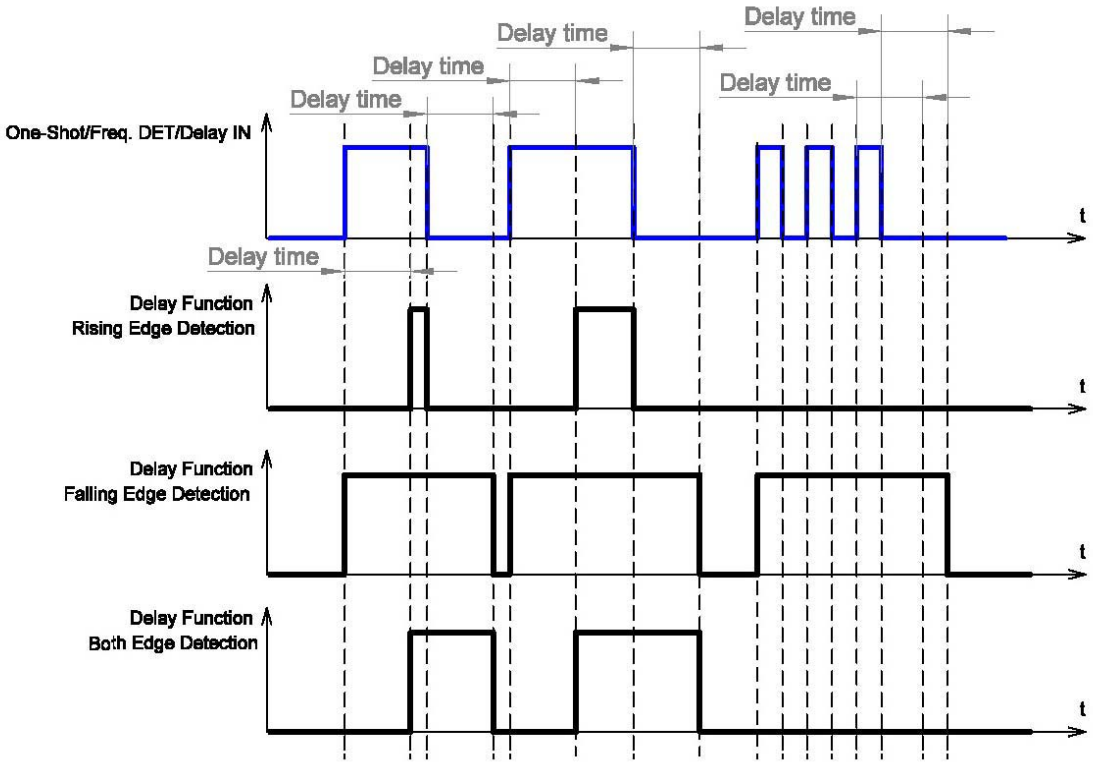



**Figure 33. Delay Mode**

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

### 9.8 4-Bit LUT or 16-Bit Counter / Delay Macrocells

There are two macrocells that can serve as either 4-bit LUTs or as 16-bit Counter / Delays. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 16-Bit Counter / Delay function, two of the four input signals from the connection matrix go to the external clock (ext_clk) and reset (DLY_n/CNT_Reset) for the counter/delay, with the output going back to the connection matrix.

These two macrocells have an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality

These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection or edge detection mode.

Both of these macrocells can have their active count value read via $I^2C$. See Section 19.4.6.3 for further details

#### 9.8.1 4-Bit LUT or 16-Bit CNT/DLY Block Diagram

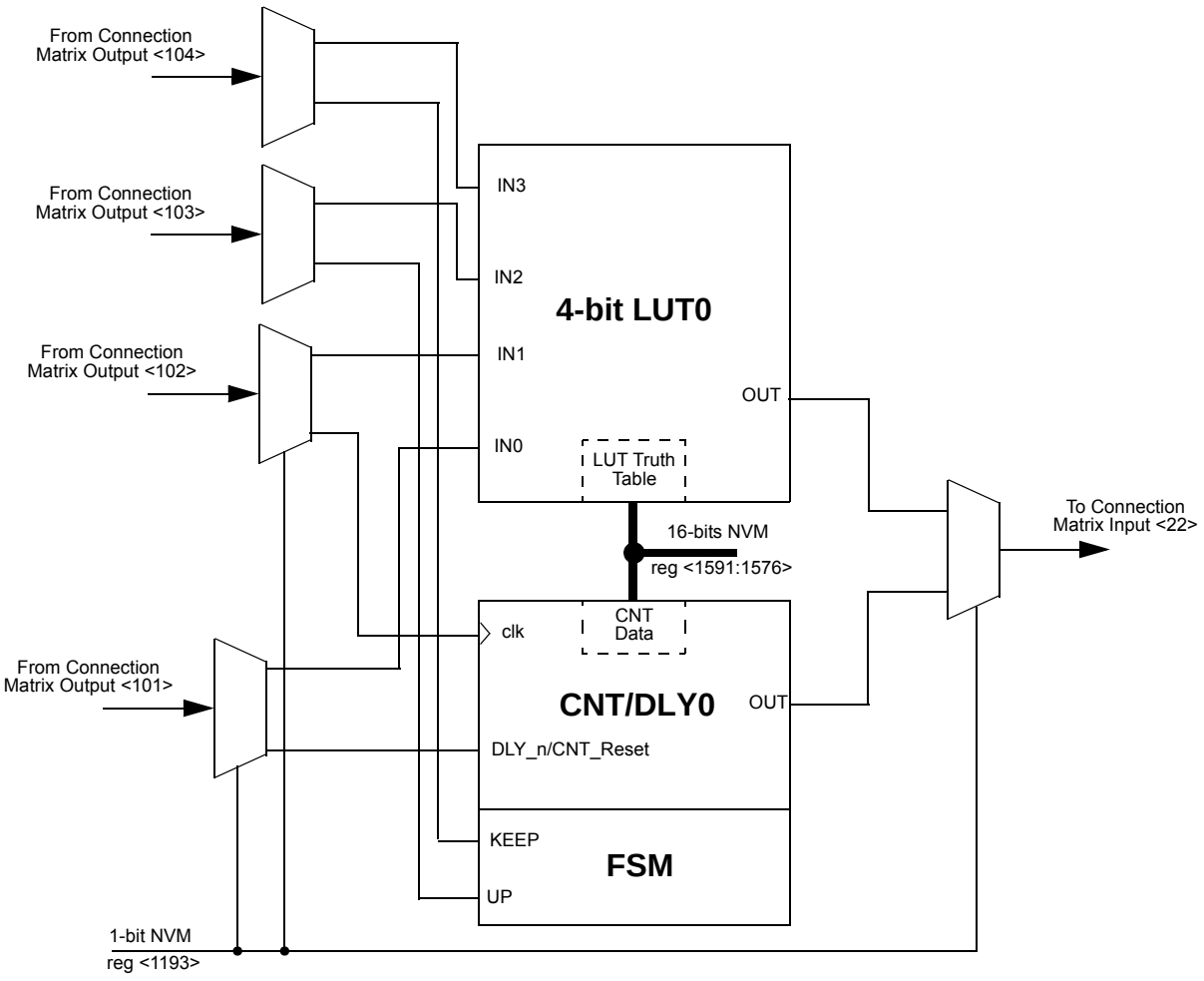



**Figure 34. 4-bit LUT0 or CNT/DLY0**

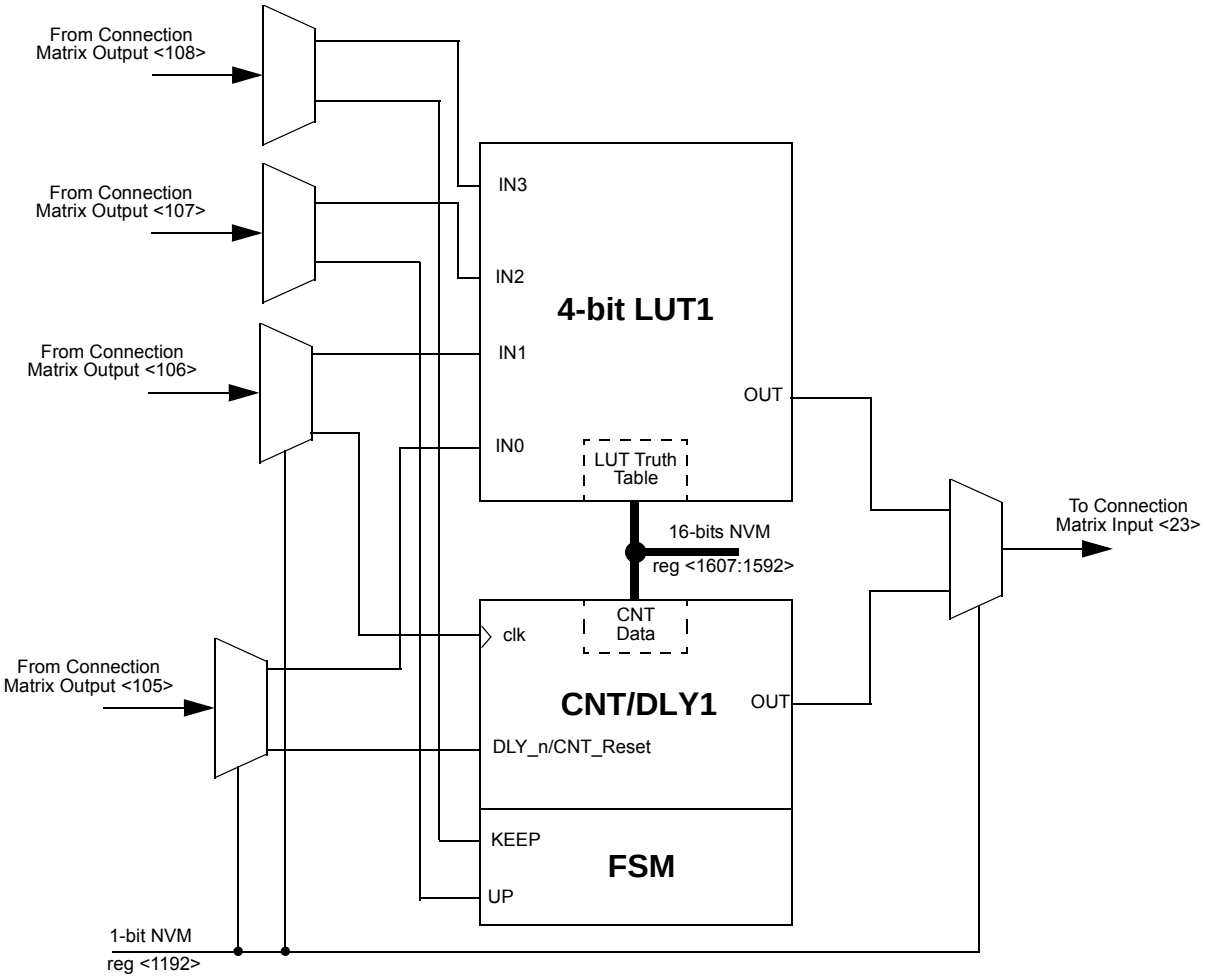



**Figure 35. 4-bit LUT1 or CNT/DLY1**

### 9.8.2 4-Bit LUT or 16-Bit Counter / Delay Macrocells Used as 4-Bit LUTs

**Table 68. 4-bit LUT0 Truth Table**

| IN3 | IN2 | IN1 | IN0 | OUT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | reg <1576> |
| 0 | 0 | 0 | 1 | reg <1577> |
| 0 | 0 | 1 | 0 | reg <1578> |
| 0 | 0 | 1 | 1 | reg <1579> |
| 0 | 1 | 0 | 0 | reg <1580> |
| 0 | 1 | 0 | 1 | reg <1581> |
| 0 | 1 | 1 | 0 | reg <1582> |
| 0 | 1 | 1 | 1 | reg <1583> |
| 1 | 0 | 0 | 0 | reg <1584> |
| 1 | 0 | 0 | 1 | reg <1585> |
| 1 | 0 | 1 | 0 | reg <1586> |
| 1 | 0 | 1 | 1 | reg <1587> |
| 1 | 1 | 0 | 0 | reg <1588> |
| 1 | 1 | 0 | 1 | reg <1589> |
| 1 | 1 | 1 | 0 | reg <1590> |
| 1 | 1 | 1 | 1 | reg <1591> |

**Table 69. 4-bit LUT1 Truth Table**

| IN3 | IN2 | IN1 | IN0 | OUT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | reg <1592> |
| 0 | 0 | 0 | 1 | reg <1593> |
| 0 | 0 | 1 | 0 | reg <1594> |
| 0 | 0 | 1 | 1 | reg <1595> |
| 0 | 1 | 0 | 0 | reg <1596> |
| 0 | 1 | 0 | 1 | reg <1597> |
| 0 | 1 | 1 | 0 | reg <1598> |
| 0 | 1 | 1 | 1 | reg <1599> |
| 1 | 0 | 0 | 0 | reg <1600> |
| 1 | 0 | 0 | 1 | reg <1601> |
| 1 | 0 | 1 | 0 | reg <1602> |
| 1 | 0 | 1 | 1 | reg <1603> |
| 1 | 1 | 0 | 0 | reg <1604> |
| 1 | 1 | 0 | 1 | reg <1605> |
| 1 | 1 | 1 | 0 | reg <1606> |
| 1 | 1 | 1 | 1 | reg <1607> |

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

*4-Bit LUT0 is defined by reg<1591:1576>*

*4-Bit LUT1 is defined by reg<1607:1592>*

**Table 70. 4-bit LUT Standard Digital Functions**

| Function | MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AND-4 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NAND-4 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| OR-4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| NOR-4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| XOR-4 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| XNOR-4 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

### 9.8.3 4-Bit LUT or 16-Bit Counter / Delay Macrocells Used as 16-Bit Counter / Delay Register Settings

**Table 71. CNT/DLY0 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT4_0 or Counter0 Select | reg<1193> | 0: LUT4_0<br>1: Counter0 |
| Delay0 Mode Select or asynchronous counter reset | reg<1313:1312> | 00: on both falling and rising edges (for delay & counter reset)<br>01: on falling edge only (for delay & counter reset)<br>10: on rising edge only (for delay & counter reset)<br>11: no delay on either falling or rising edges / high level reset |
| Counter/delay0 Clock Source Select | reg<1316:1314> | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25 MHz OSC clock<br>110: External Clock<br>111: Counter6 Overflow |
| CNT0/FSM0's Q are Set to data or Reset to 0s Selection | reg<1317> | 0: Reset to 0s<br>1: Set to data (Reg<1583:1576, 1591:1584>) |
| Counter/delay0 Mode Selection | reg<1319:1318> | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode |
| Counter/delay0 Control Data | reg<1591:1576> | 1 - 16384 (Delay Time = [Counter Control Data + 1] / Freq) |

**Table 72. CNT/DLY1 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| LUT4_1 or Counter1 Select | reg<1192> | 0: LUT4_1<br>1: Counter1 |
| Delay1 Mode Select or asynchronous counter reset | reg<1321:1320> | 00: on both falling and rising edges (for delay & counter reset)<br>01: on falling edge only (for delay & counter reset)<br>10: on rising edge only (for delay & counter reset)<br>11: no delay on either falling or rising edges / high level reset |
| Counter/delay1 Clock Source Select | reg<1324:1322> | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter0 Overflow |
| CNT0/FSM0's Q are Set to data or Reset to 0s Selection | reg<1325> | 0: Reset to 0s<br>1: Set to data (Reg<1599:1592, 1607:1600>) |
| Counter/delay1 Mode Selection | reg<1327:1326> | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode |
| Counter/delay1 Control Data | reg<1607:1592> | 1 - 16384 (Delay Time = [Counter Control Data + 1] / Freq) |

### 9.9 Wake and Sleep controller (WS)

The SLG46531 has a Wake and Sleep function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose reg<1319:1318>=11 and reg<1495>=1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

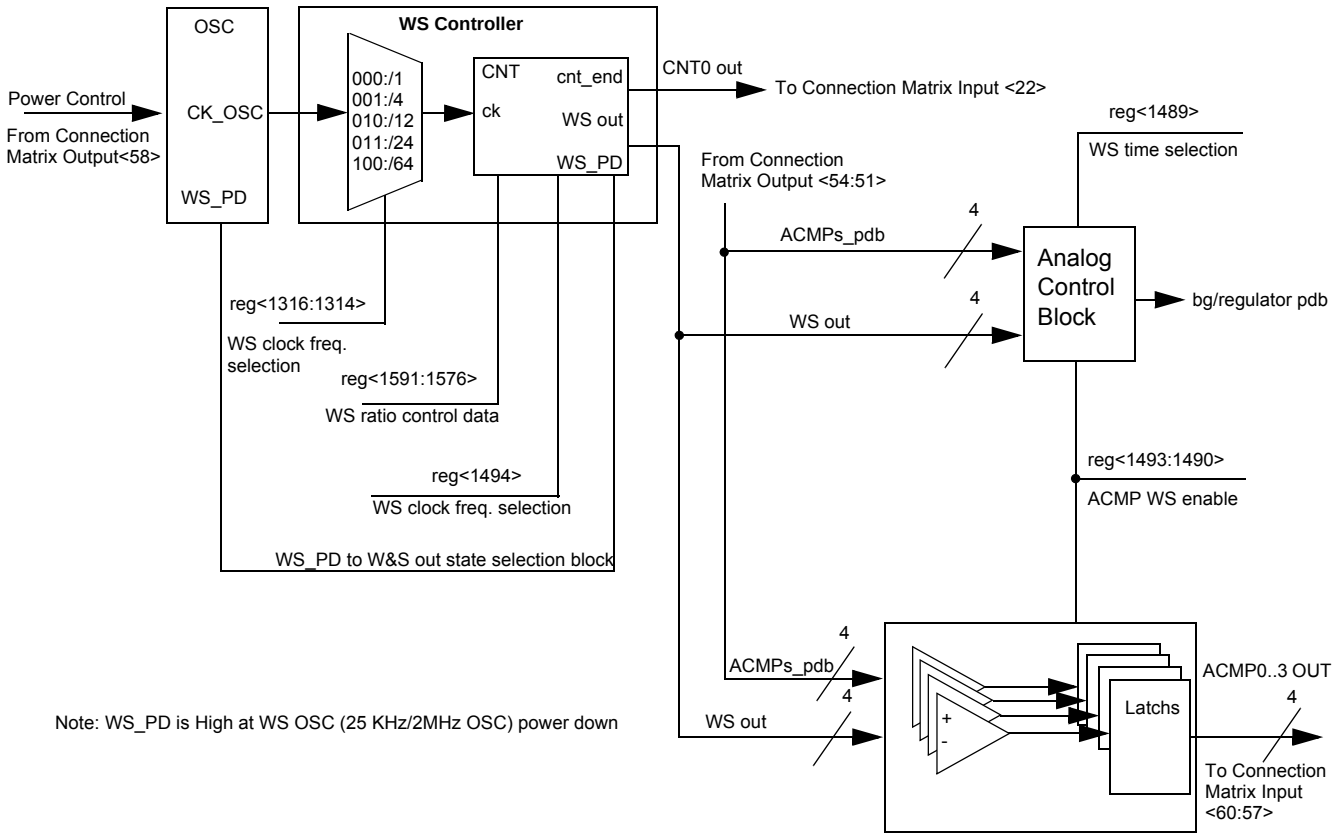



**Figure 36. WS controller**

To use any ACMP under WS controller the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately)
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs)
- Register WS => enable (for each ACMP separately)
- CNT/DLY0 set/reset input = 0 (for all ACMPs)

As the OSC any oscillator with any pre divider can be used. The user can select a period of time while the ACMPs are sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power Down option is selected; power down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on

If OSC is powered off (Power Down option is selected; power down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off
Both cases WS function is turned off

- Counter Data (Range: 1 - 65535)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time

- Q mode - defines the state of WS counter data when Set/Reset signal appears
  Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn the ACMPs on. When Reset signal goes out, the WS counter will go Low and turn the ACMPs off until the counter counts up to the end
  Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn the ACMPs off. When Set signal goes out, the WS counter will go on counting and High level signal will turn the ACMPs on while counter is counting up to the end

- Edge Select defines the edge for Q mode
  High level Set/Reset - switches mode Set/Reset when level is High
  Note: Q mode operates only in case of "High Level Set/Reset”

- Wake time selection - time required for wake signal to turn the ACMPs on
  Normal Wake Time - when WS signal is High, it takes a BG time (100/550 µs) to turn the ACMPs on They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP
  Short Wake Time - when WS signal is High, it takes a BG time (100/550 µs) to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535

  If Up = 0, CNT is counting down from user selected value to 0

### 9.9.1 WS Register Settings

**Table 73. WS Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| Counter/delay0 Clock Source Select | reg<1316:1314> | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter6 Overflow |
| WS time selection | reg<1489> | 0: Short Wake Time<br>1: Normal Wake Time |
| ACMP0 Wake & Sleep function Enable | reg<1490> | 0: Disable<br>1: Enable |
| ACMP1 Wake & Sleep function Enable | reg<1491> | 0: Disable<br>1: Enable |
| ACMP2 Wake & Sleep function Enable | reg<1492> | 0: Disable<br>1: Enable |
| ACMP3 Wake & Sleep function Enable | reg<1493> | 0: Disable<br>1: Enable |
| Wake Sleep Output State When WS Oscillator is Power Down if DLY/CNT0 Mode Selection is "11" | reg<1494> | 0: Low<br>1: High |
| Wake Sleep Ratio Control Mode Selection if DLY/CNT0 Mode Selection is "11" | reg<1495> | 0: Default Mode<br>1: Wake Sleep Ratio Control Mode |
| DLY/CNT0 (16bits, <15:0> = <1591:1576>) Control Data | reg<1591:1576> | 1 - 65535 |

## 10.0 Analog Comparators (ACMP)

There are four Analog Comparator (ACMP) macro cells in the SLG46531. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMPx_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be always on, always off, or power cycled based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

PWR UP = 1 => ACMP is powered up.
PWR UP = 0 => ACMP is powered down.

During ACMP power up, its output will remain low, and then becomes valid 2.08 ms (max) after ACMP power up signal goes high, see *Figure 37*. If VDD is greater or equal to 2.7 V, it is possible to decrease turn-on time by setting the BG ok delay to 100 µs, see *Figure 38*. The ACMP cells have an input "Low bandwidth" signal selection, which can be used to save power and reduce noise impact when lower bandwidth signals are being compared. To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the VDD signal.

Note: Regulator and Charge Pump set to automatic ON/OFF.

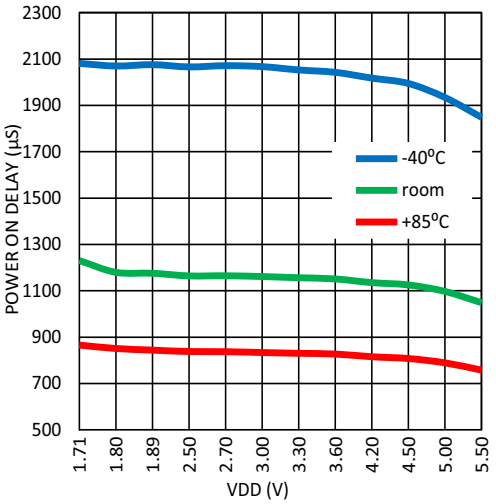



**Figure 37. Maximum Power On Delay vs. VDD, BG = 550 µs.**

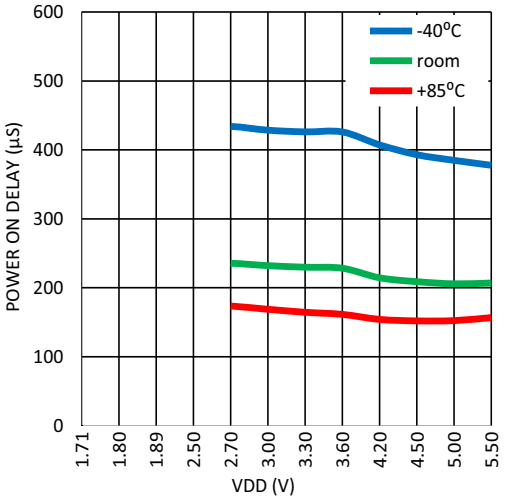



**Figure 38. Maximum Power On Delay vs. VDD, BG = 100 µs.**

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources. There is also a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 KΩ (typ.) resistors, see *Table 74*. For gain divider accuracy refer to *Table 75*. IN- voltage range: 0 - 1.2 V. Can use Vref selection VDD/4 and VDD/3 to maintain this input range.

Input bias current < 1 nA (typ).

**Table 74. Gain Divider Input Resistance**

| Gain | x1 | x0.5 | x0.33 | x0.25 |
|---|---|---|---|---|
| Input Resistance | 100 MΩ | 1 MΩ | 0.75 MΩ | 1 MΩ |

**Table 75. Gain Divider Accuracy**

| Gain | x0.5 | x0.33 | x0.25 |
|---|---|---|---|
| Accuracy | ±0.51% | ±0.34% | ±0.25% |

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV or 200 mV. The 50 mV and 200 mV hysteresis options can be used with internal voltage reference only, while 25 mV hysteresis option can be used with both internal and external voltage reference. The 50 mV and 200 mV hysteresis options are one way hysteresis. It means that the actual thresholds will be Vref (high threshold) and Vref - hysteresis (low threshold). The ACMP output will retain its previous value, if the input voltage is within threshold window (between Vref and Vref - hysteresis). Please note: for the 25 mV hysteresis option threshold levels will be Vref + hysteresis/2 (high threshold) and Vref – hysteresis/2 (low threshold).

Note: Any ACMP powered on enables the BandGap internal circuit as well. An analog voltage will appear on Vref even when the Force BandGap option is set as Disabled.

For high input impedance when using the gain divider (x0.25, x0.33, x0.5), it is possible to use the input buffer. However, this will add some offset, see *Figure 39* to *Figure 42*.

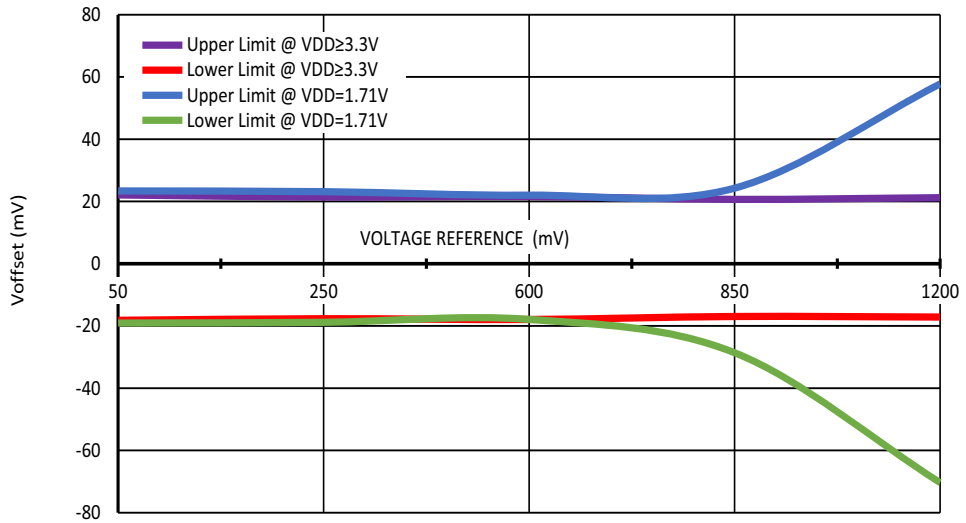



**Figure 39. Typical Buffer Input Voltage Offset vs. Voltage Reference at T = (-40.... +85)°C, Buffer Bandwidth = 1 kHz, Vhys = 0 mV, Gain = 1.**

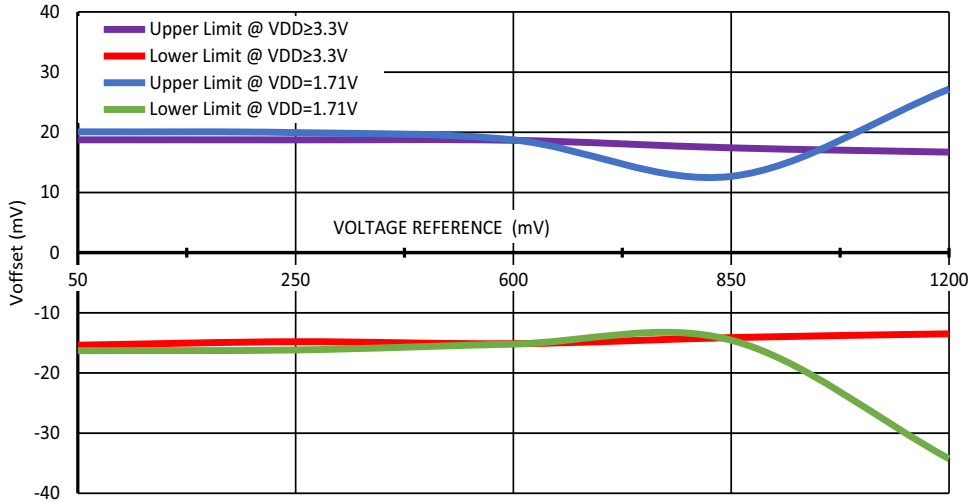



**Figure 40. Typical Buffer Input Voltage Offset vs. Voltage Reference at T = (-40.... +85)°C, Buffer Bandwidth = 5 kHz, Vhys = 0 mV, Gain = 1.**

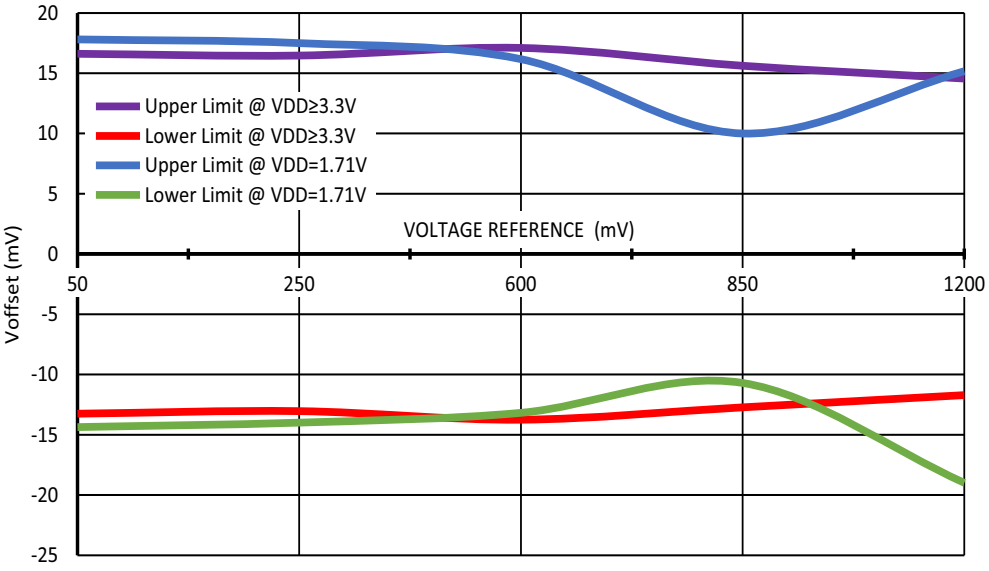



**Figure 41. Typical Buffer Input Voltage Offset vs. Voltage Reference at T = (-40.... +85)°C, Buffer Bandwidth = 20 kHz, Vhys = 0 mV, Gain = 1.**

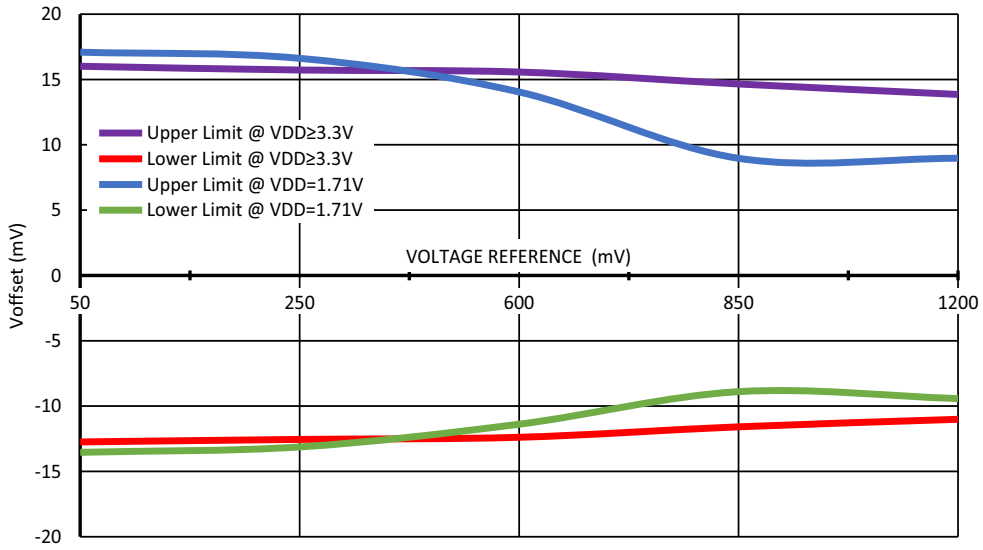



**Figure 42. Typical Buffer Input Voltage Offset vs. Voltage Reference at T = (-40.... +85)°C, Buffer Bandwidth = 50 kHz, Vhys = 0 mV, Gain = 1.**

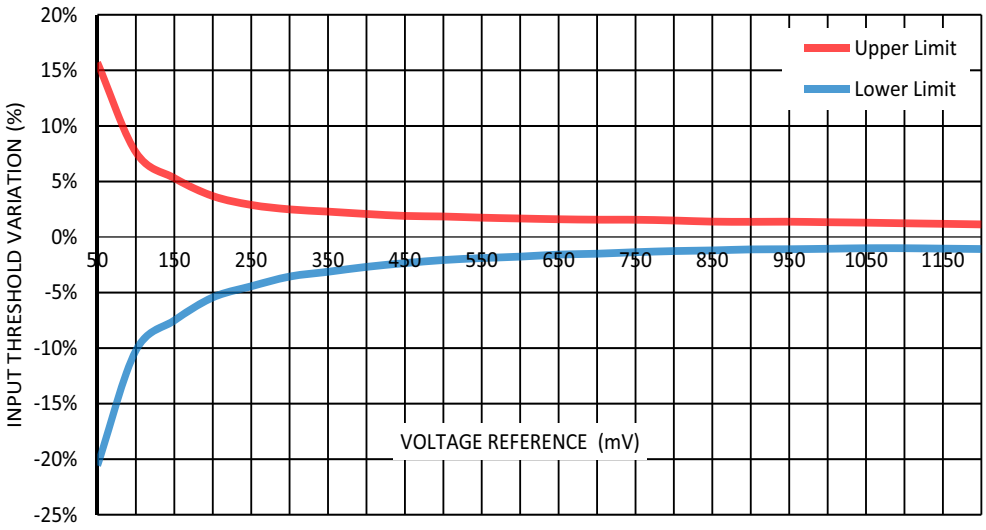



**Figure 43. Typical Input Threshold Variation (including Vref variation, ACMP offset) vs. Voltage Reference at T = (-40.... +85)°C, LMB Mode - Disable, Vhys = 0 mV.**

Note: when VDD < 1.8V voltage reference should not exceed 1100 mV.

**Table 76. Built-in Hysteresis Tolerance**

| Vhys (mV) | VDD=(1.7-1.8) V | | | | | | VDD=(1.89-5.5) V | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Vref = (50-500) mV | | Vref = (550-1000) mV | | Vref = (1050-1200) mV | | Vref = (50-500) mV | | Vref = (550-1000) mV | | Vref = (1050-1200) mV | |
| | min | max | min | max | min | max | min | max | min | max | min | max |
| 25 | 8.6 | 32.2 | 8.6 | 32.3 | 7.0 | 32.5 | 8.5 | 32.3 | 8.5 | 32.3 | 7.8 | 34.0 |
| 50 | 44.8 | 56.5 | 43.9 | 56.7 | 42.7 | 56.4 | 44.2 | 56.8 | 43.6 | 57.3 | 43.1 | 56.0 |
| 200 | 192.8 | 207.9 | 194.0 | 208.0 | 192.7 | 205.4 | 192.0 | 208.6 | 193.0 | 209.5 | 190.8 | 207.7 |

## 10.1 ACMP0 Block Diagram

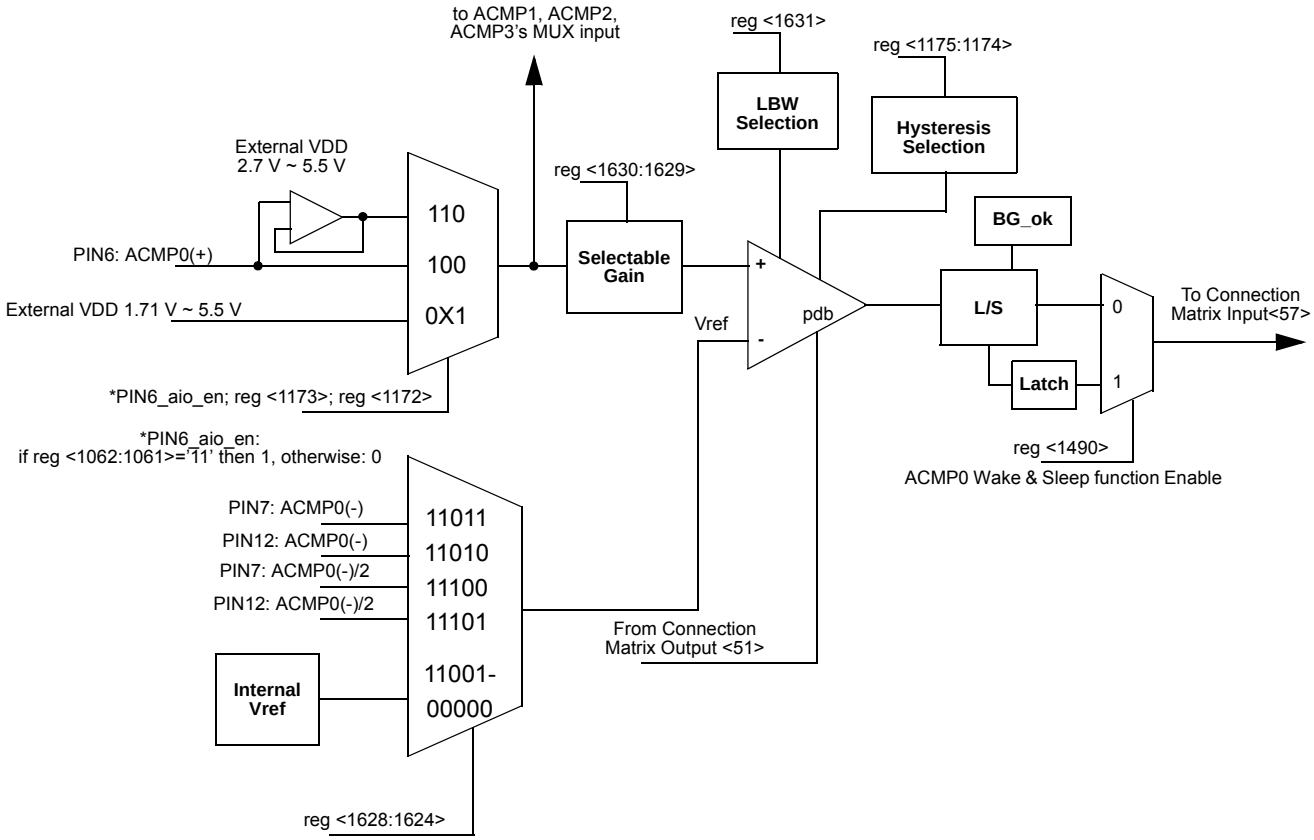


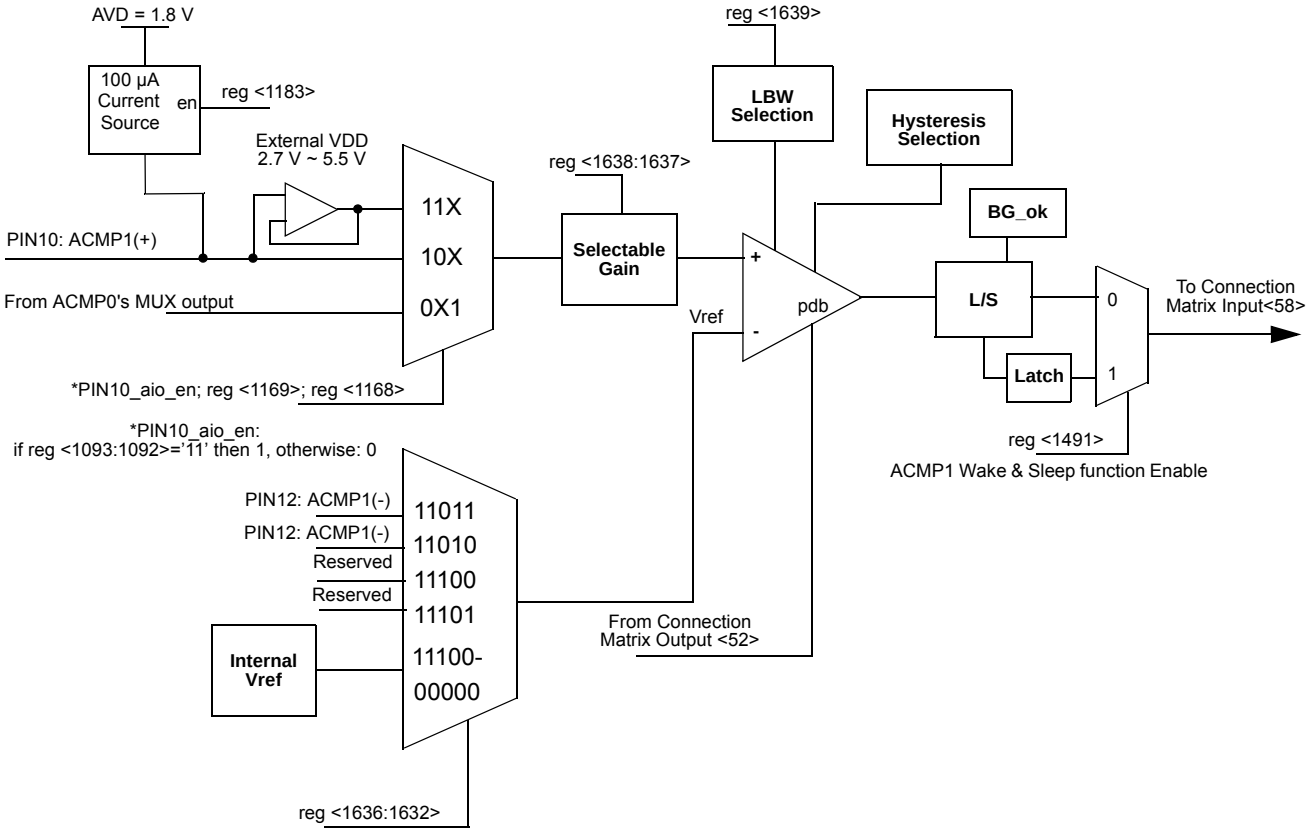

**Figure 44. ACMP0 Block Diagram**

### 10.2 ACMP0 Register Settings

**Table 77. ACMP0 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| ACMP0 Positive Input Source Select VDD | reg<1172> | 0: Disable<br>1: Enable |
| ACMP0 Analog Buffer Enable | reg<1173> | 0: Disable analog buffer<br>1: Enable analog buffer |
| ACMP0 Hysteresis Enable | reg<1175:1174> | 00: Disabled (0 mV)<br>01: Enabled (25 mV)<br>10: Enabled (50 mV)<br>11: Enabled (200 mV)<br><br>(01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50mV & 200mV hysteresis.) |
| ACMP0 Wake & Sleep function Enable | reg<1490> | 0: Disable<br>1: Enable |
| ACMP0 In Voltage Select | reg<1628:1624> | 00000: 50 mV 00001: 100 mV<br>00010: 150 mV 00011: 200 mV<br>00100: 250 mV 00101: 300 mV<br>00110: 350 mV 00111: 400 mV<br>01000: 450 mV 01001: 500 mV<br>01010: 550 mV 01011: 600 mV<br>01100: 650 mV 01101: 700 mV<br>01110: 750 mV 01111: 800 mV<br>10000: 850 mV 10001: 900 mV<br>10010: 950 mV 10011: 1 V<br>10100: 1.05 V 10101: 1.1 V<br>10110: 1.15 V 10111: 1.2 V<br>11000: VDD/3 11001: VDD/4<br>11010: EXT_VREF(PIN12)<br>11011: EXT_VREF(PIN7)<br>11100: EXT_VREF(PIN12)/2<br>11101: EXT_VREF(PIN7)/2 |
| ACMP0 Positive Input Divider | reg<1630:1629> | 00: 1.00X<br>01: 0.50X<br>10: 0.33X<br>11: 0.25X |
| ACMP0 Low Bandwidth (Max: 1 MHz) Enable | reg<1631> | 0: Off<br>1: On |

### 10.3 ACMP1 Block Diagram




Note: when 100 µA Current Source is enabled input voltage on Pin 10 should not exceed 1.8 V

**Figure 45. ACMP1 Block Diagram**

### 10.4 ACMP1 Register Settings

**Table 78. ACMP1 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| ACMP1 100uA Current Source Enable | reg<1183> | 0: Disable<br>1: Enable |
| ACMP1 Positive Input Source Select PIN10 | reg<1168> | 0: Disable<br>1: Enable |
| ACMP1 Analog Buffer Enable (max. band width 1 MHz) | reg<1169> | 0: Disable analog buffer<br>1: Enable analog buffer |
| ACMP1 Hysteresis Enable | reg<1171:1170> | 00: Disabled (0 mV)<br>01: Enabled (25 mV)<br>10: Enabled (50 mV)<br>11: Enabled (200 mV)<br><br>(01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50mV & 200mV hysteresis.) |
| ACMP1 Wake & Sleep function Enable | reg<1491> | 0: Disable<br>1: Enable |
| ACMP1 In Voltage Select | reg<1636:1632> | 00000: 50 mV 00001: 100 mV<br>00010: 150 mV 00011: 200 mV<br>00100: 250 mV 00101: 300 mV<br>00110: 350 mV 00111: 400 mV<br>01000: 450 mV 01001: 500 mV<br>01010: 550 mV 01011: 600 mV<br>01100: 650 mV 01101: 700 mV<br>01110: 750 mV 01111: 800 mV<br>10000: 850 mV 10001: 900 mV<br>10010: 950 mV 10011: 1 V<br>10100: 1.05 V 10101: 1.1 V<br>10110: 1.15 V 10111: 1.2 V<br>11000: VDD/3 11001: VDD/4<br>11010: EXT_VREF(PIN12)<br>11011: EXT_VREF(PIN12)<br>11100: EXT_VREF(PIN12)/2<br>11101: EXT_VREF(PIN12)/2 |
| ACMP1 Positive Input Divider | reg<1638:1637> | 00: 1.00X<br>01: 0.50X<br>10: 0.33X<br>11: 0.25X |
| ACMP1 Low Bandwidth (Max: 1 MHz) Enable | reg<1639> | 0: Off<br>1: On |

### 10.5 ACMP2 Block Diagram

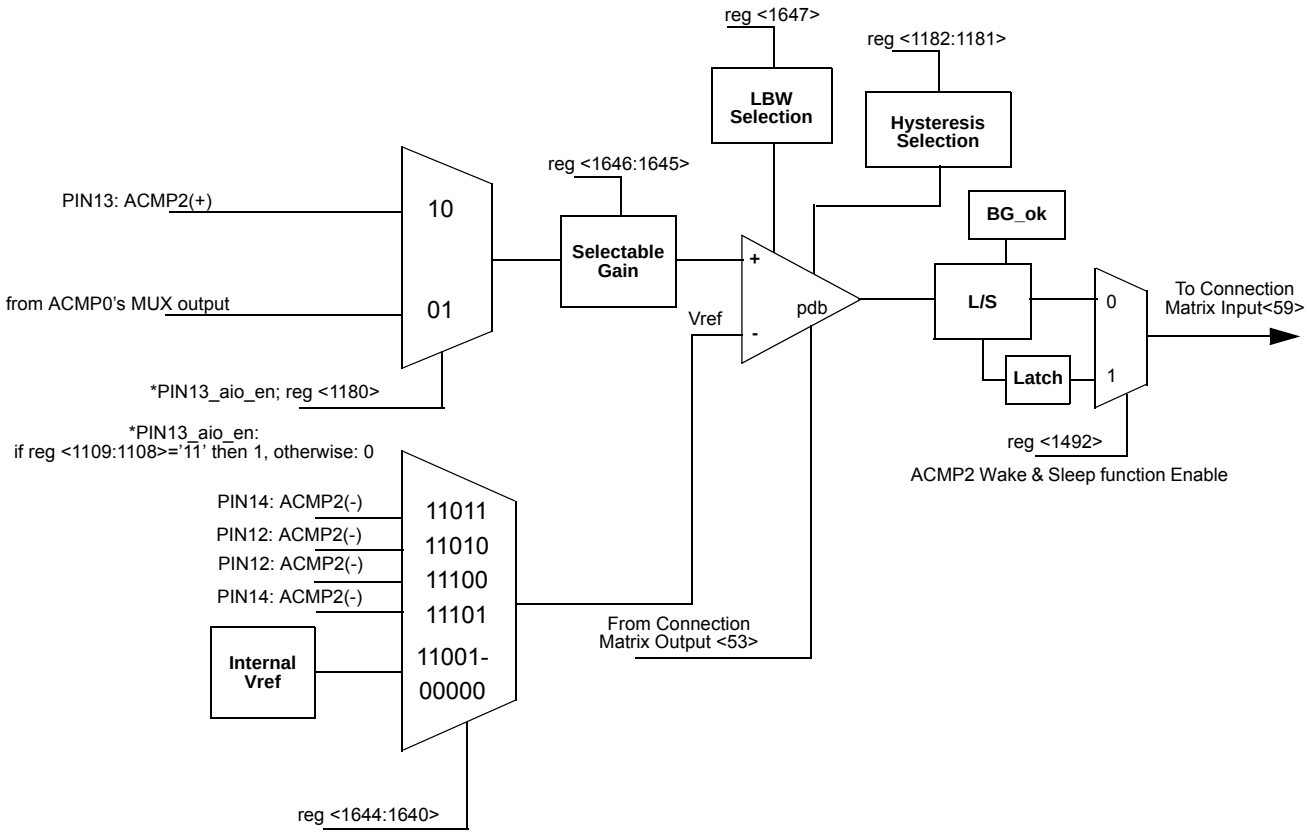



**Figure 46. ACMP2 Block Diagram**

### 10.6 ACMP2 Register Settings

**Table 79. ACMP2 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| ACMP2 Positive Input Source Select Pin 13 | reg<1180> | 0: Disable<br>1: Enable |
| ACMP2 Hysteresis Enable | reg<1182:1181> | 00: Disabled (0 mV)<br>01: Enabled (25 mV)<br>10: Enabled (50 mV)<br>11: Enabled (200 mV)<br><br>(01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50mV & 200mV hysteresis.) |
| ACMP2 Wake & Sleep function Enable | reg<1492> | 0: Disable<br>1: Enable |
| ACMP2 In Voltage Select | reg<1644:1640> | 00000: 50 mV 00001: 100 mV<br>00010: 150 mV 00011: 200 mV<br>00100: 250 mV 00101: 300 mV<br>00110: 350 mV 00111: 400 mV<br>01000: 450 mV 01001: 500 mV<br>01010: 550 mV 01011: 600 mV<br>01100: 650 mV 01101: 700 mV<br>01110: 750 mV 01111: 800 mV<br>10000: 850 mV 10001: 900 mV<br>10010: 950 mV 10011: 1 V<br>10100: 1.05 V 10101: 1.1 V<br>10110: 1.15 V 10111: 1.2 V<br>11000: VDD/3 11001: VDD/4<br>11010: EXT_VREF(PIN12)<br>11011: EXT_VREF(PIN14)<br>11100: EXT_VREF(PIN12)/2<br>11101: EXT_VREF(PIN14)/2 |
| ACMP2 Positive Input Divider | reg<1646:1645> | 00: 1.00X<br>01: 0.50X<br>10: 0.33X<br>11: 0.25X |
| ACMP2 Low Bandwidth (Max: 1 MHz) Enable | reg<1647> | 0: Off<br>1: On |

### 10.7 ACMP3 Block Diagram

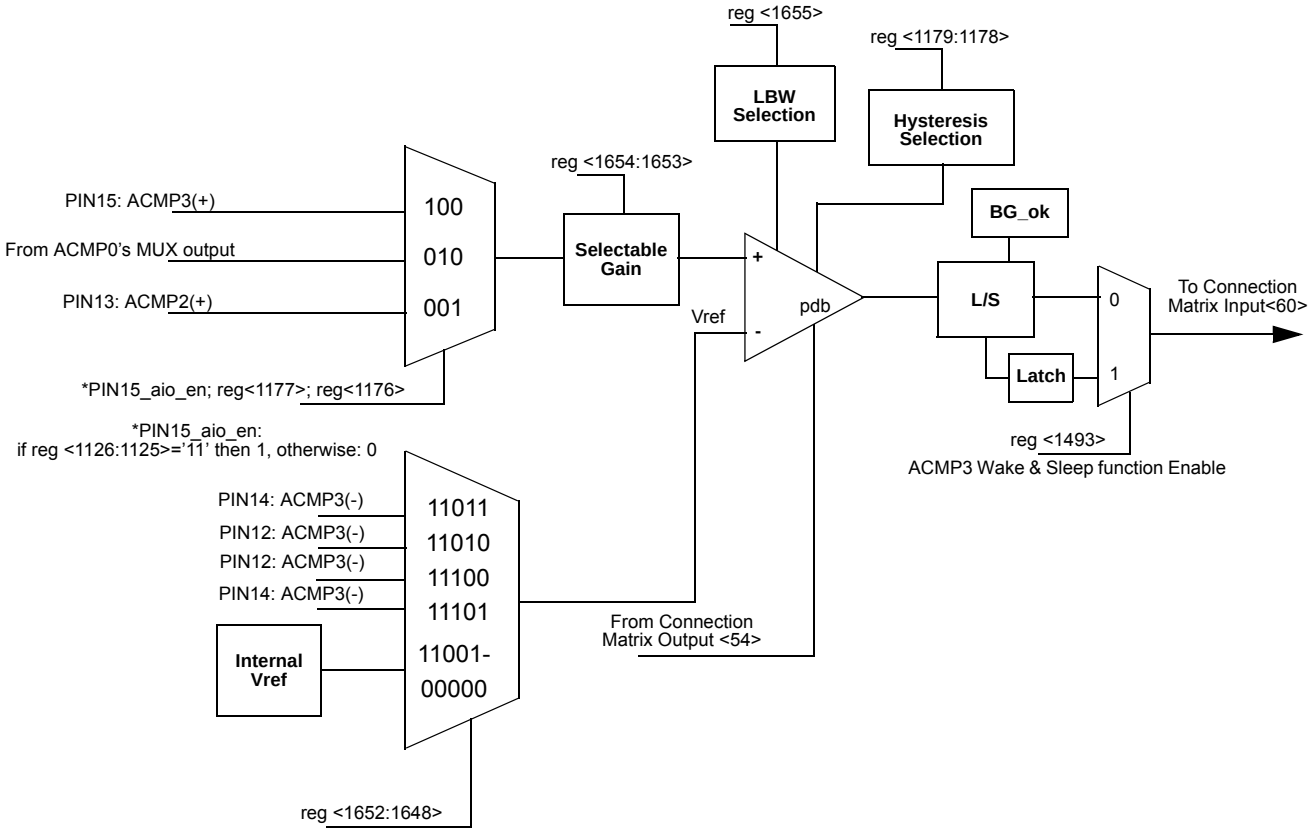



**Figure 47. ACMP3 Block Diagram**

### 10.8 ACMP3 Register Settings

**Table 80. ACMP3 Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| ACMP3 Positive Input Source Select Pin 15 | reg<1176> | 0: Disable<br>1: Enable |
| ACMP3 Positive Input Source Select Pin 13 | reg<1177> | 0: Disable<br>1: Enable |
| ACMP3 Hysteresis Enable | reg<1179:1178> | 00: Disabled (0 mV)<br>01: Enabled (25 mV)<br>10: Enabled (50 mV)<br>11: Enabled (200 mV)<br><br>(01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50 mV & 200 mV hysteresis.) |
| ACMP3 Wake & Sleep function Enable | reg<1493> | 0: Disable<br>1: Enable |
| ACMP3 In Voltage Select | reg<1652:1648> | 00000: 50 mV 00001: 100 mV<br>00010: 150 mV 00011: 200 mV<br>00100: 250 mV 00101: 300 mV<br>00110: 350 mV 00111: 400 mV<br>01000: 450 mV 01001: 500 mV<br>01010: 550 mV 01011: 600 mV<br>01100: 650 mV 01101: 700 mV<br>01110: 750 mV 01111: 800 mV<br>10000: 850 mV 10001: 900 mV<br>10010: 950 mV 10011: 1 V<br>10100: 1.05 V 10101: 1.1 V<br>10110: 1.15 V 10111: 1.2 V<br>11000: VDD/3 11001: VDD/4<br>11010: EXT_VREF(PIN12)<br>11011: EXT_VREF(PIN14)<br>11100: EXT_VREF(PIN12)/2<br>11101: EXT_VREF(PIN14)/2 |
| ACMP3 Positive Input Divider | reg<1654:1653> | 00: 1.00X<br>01: 0.50X<br>10: 0.33X<br>11: 0.25X |
| ACMP3 Low Bandwidth (Max: 1 MHz) Enable | reg<1655> | 0: Off<br>1: On |

## 11.0 Pipe Delay (PD)

The SLG46531 has a pipe delay logic cell that is shared with the LUT3_10 in one of the Combination Function macrocells. The user can select one of these functions to use in a design, but not both. Please see Section 9.6 3-Bit LUT or Pipe Delay Macrocell for the description of this Combination Function macrocell.

## 12.0 Programmable Delay / Edge Detector

The SLG46531 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See the timing diagrams below for further information.

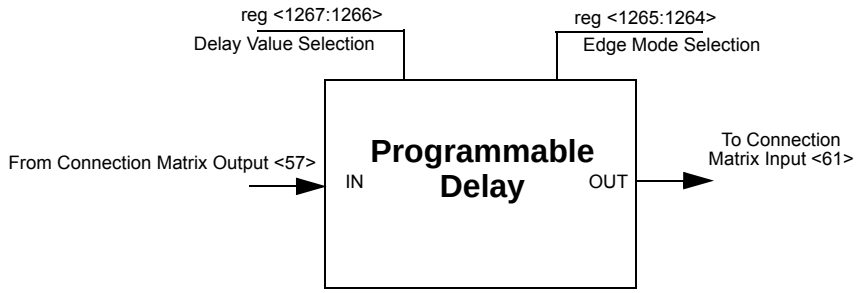



**Figure 48. Programmable Delay**

### 12.1 Programmable Delay Timing Diagram - Edge Detector Output

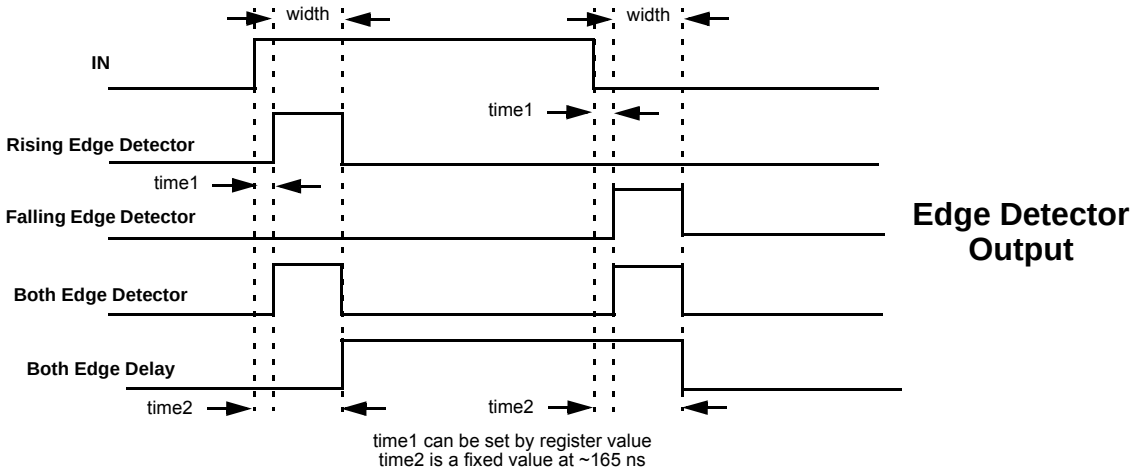



**Figure 49. Edge Detector Output**

Please refer to Table 4. Expected Delays and Widths (typical)

### 12.2 Programmable Delay Register Settings

**Table 81. Programmable Delay Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| Select the edge mode of programmable delay & edge detector | reg<1265:1264> | 00: Rising Edge Detector<br>01: Falling Edge Detector<br>10: Both Edge Detector<br>11: Both Edge Delay |
| Delay value select for programmable delay & edge detector (VDD = 3.3V, typical condition) | reg<1267:1266> | 00: 165 ns<br>01: 300 ns<br>10: 440 ns<br>11: 575 ns |

## 13.0 Additional Logic Functions

The SLG46531 has two additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two deglitch filters, each with edge detector functions. See section 5.11 Typical Pulse Width Performance.

### 13.1 Deglitch Filter / Edge Detector

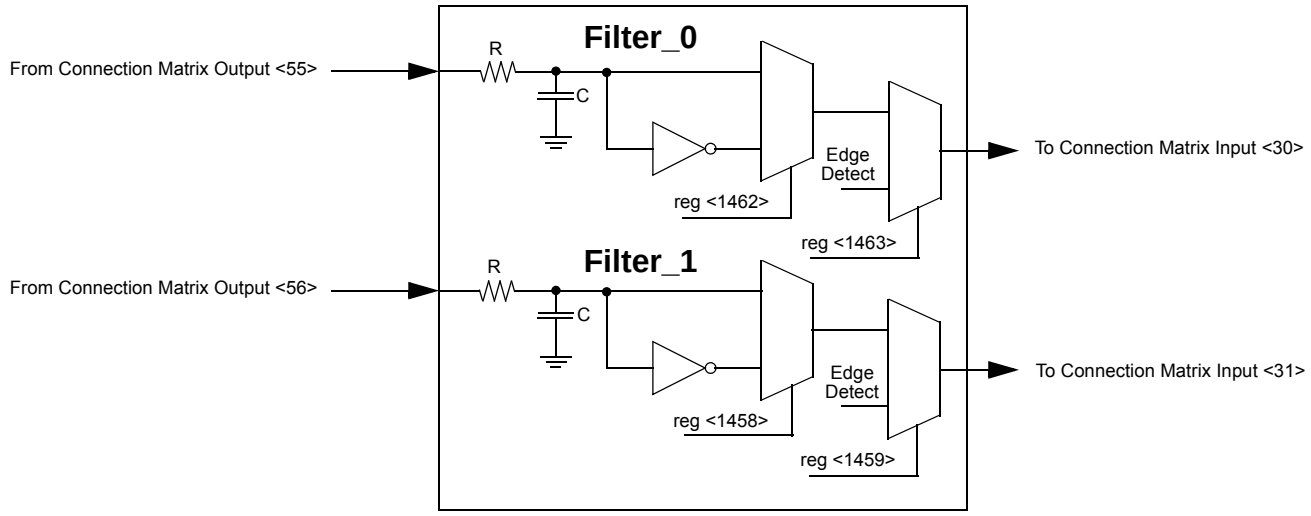



**Figure 50. Deglitch Filter / Edge Detector**

### 13.2 Deglitch Filter Register Settings

**Table 82. Programmable Delay Register Settings**

| Signal Function | Register Bit Address | Register Definition |
|---|---|---|
| Filter_1/Edge Detector_1 output Polarity Select | reg<1458> | 0: Filter_1 output<br>1: Filter_1 output inverted |
| Filter_1 or Edge Detector_1 Select (Typ. 30 nS @VDD=3.3 V) | reg<1459> | 0: Filter_1<br>1: Edge Detector_1 |
| Filter_0/Edge Detector_0 output Polarity Select | reg<1462> | 0: Filter_0 output<br>1: Filter_0 output inverted |
| Filter_0 or Edge Detector_0 Select (Typ. 47 nS @VDD=3.3 V) | reg<1463> | 0: Filter_0<br>1: Edge Detector_0 |

## 14.0 Voltage Reference (VREF)

### 14.1 Voltage Reference Overview

The SLG46531 has a Voltage Reference Macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the $V_{DD}$ power supply to the device, and externally supplied voltage references from pins 7,12 and 14. The macrocell also has the option to output reference voltages on pins 18 and 19. See table below for the available selections for each analog comparator. Also see *Figure 51* below, which shows the reference output structure.

### 14.2 VREF Selection Table

**Table 83. VREF Selection Table**

| SEL<4:0> | CMP0_VREF | CMP1_VREF | CMP2_VREF | CMP3_VREF |
|---|---|---|---|---|
| 11101 | vref_ext_acmp0/2 | vref_ext_acmp1/2 | vref_ext_acmp2/2 | vref_ext_acmp2/2 |
| 11100 | vref_ext_acmp1/2 | vref_ext_acmp1/2 | vref_ext_acmp1/2 | vref_ext_acmp1/2 |
| 11011 | vref_ext_acmp0 | vref_ext_acmp1 | vref_ext_acmp2 | vref_ext_acmp2 |
| 11010 | vref_ext_acmp1 | vref_ext_acmp1 | vref_ext_acmp1 | vref_ext_acmp1 |
| 11001 | VDD / 4 | VDD / 4 | VDD / 4 | VDD / 4 |
| 11000 | VDD / 3 | VDD / 3 | VDD / 3 | VDD / 3 |
| 10111 | 1.20 | 1.20 | 1.20 | 1.20 |
| 10110 | 1.15 | 1.15 | 1.15 | 1.15 |
| 10101 | 1.10 | 1.10 | 1.10 | 1.10 |
| 10100 | 1.05 | 1.05 | 1.05 | 1.05 |
| 10011 | 1.00 | 1.00 | 1.00 | 1.00 |
| 10010 | 0.95 | 0.95 | 0.95 | 0.95 |
| 10001 | 0.90 | 0.90 | 0.90 | 0.90 |
| 10000 | 0.85 | 0.85 | 0.85 | 0.85 |
| 01111 | 0.80 | 0.80 | 0.80 | 0.80 |
| 01110 | 0.75 | 0.75 | 0.75 | 0.75 |
| 01101 | 0.70 | 0.70 | 0.70 | 0.70 |
| 01100 | 0.65 | 0.65 | 0.65 | 0.65 |
| 01011 | 0.60 | 0.60 | 0.60 | 0.60 |
| 01010 | 0.55 | 0.55 | 0.55 | 0.55 |
| 01001 | 0.50 | 0.50 | 0.50 | 0.50 |
| 01000 | 0.45 | 0.45 | 0.45 | 0.45 |
| 00111 | 0.40 | 0.40 | 0.40 | 0.40 |
| 00110 | 0.35 | 0.35 | 0.35 | 0.35 |
| 00101 | 0.30 | 0.30 | 0.30 | 0.30 |
| 00100 | 0.25 | 0.25 | 0.25 | 0.25 |
| 00011 | 0.20 | 0.20 | 0.20 | 0.20 |
| 00010 | 0.15 | 0.15 | 0.15 | 0.15 |
| 00001 | 0.10 | 0.10 | 0.10 | 0.10 |
| 00000 | 0.05 | 0.05 | 0.05 | 0.05 |

| VDD | Practical VREF Range | Note |
|---|---|---|
| 2.0 V - 5.5 V | 50 mV ~ 1.2 V | |
| 1.7 V - 2.0V | 50 mV ~ 1.0 V | Do not operate above 1.0 V |

### 14.3 VREF Block Diagram

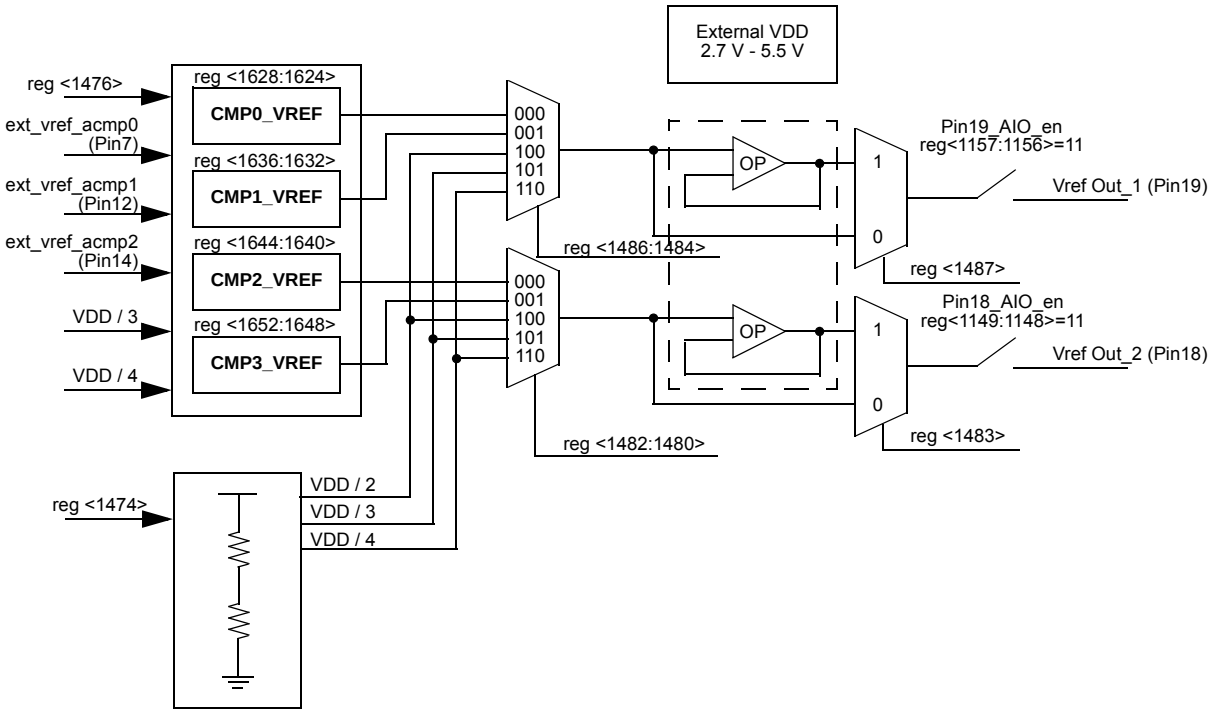



**Figure 51. Voltage Reference Block Diagram**

## 15.0 RC Oscillator (RC Osc)

The SLG46531 has three internal oscillators. RC Oscillator that runs at 25 kHz / 2 MHz (OSC0), Oscillator that runs at 25 MHz (OSC1) and Crystal Oscillator. It is possible to use all three oscillators simultaneously. The fundamental frequency can also come from clock input (Pin 18 or Pin 20 for 25 kHz / 2 MHz and Pin 17 for 25 MHz or Crystal OSC), see section 20.0 External Clocking.

### 15.1 25 kHz/2 MHz and 25 MHz RC Oscillators

There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The predivider allows the selection of /1, /2, /4 or /8 divide down frequency from the fundamental. The second stage divider (only for 25 kHz / 2 MHz Oscillator) has an input of frequency from the predivider, and outputs one of seven different frequencies on Connection Matrix Input lines <27> and <28>. See *Figure 52* and *Figure 53* below for details.

There are two modes of the POWER CONTROL pin, (reg<1658> for 25 kHz / 2 MHz OSC and reg<1657> for 25 MHz OSC):

- **POWER DOWN <0>**. If PWR CONTROL input of oscillator is LOW, the oscillator will be turned on. If PWR CONTROL input of oscillator is HIGH the oscillator will be turned off.
- **FORCE ON <1>**. If PWR CONTROL input of oscillator is HIGH, the oscillator will be turned on. If PWR CONTROL input of oscillator is LOW the oscillator will be turned off.

The PWR CONTROL signal has the highest priority.

The SLG46531 has a 25 kHz / 2 MHz OSC FAST START-UP function reg<1338> (1 – on, 0 – off). It allows the OSC to run immediately after power-up. Start-up time is less than one cycle. Note that when OSC FAST START-UP is on, the current consumption will rise.

The user can select two OSC POWER MODEs (reg<1343 for 25 kHz / 2 MHz OSC and reg<1341> for 25 MHz OSC):

- If **AUTO POWER ON <0>** is selected, the OSC will run when the SLG46531 is powered on.
- If **FORCE POWER ON <1>** is selected, the OSC will run only when any block that uses OSC is powered on.

OSC can be turned on by:

- Register control (force power on)
- Delay mode, when delay requires OSC
- PWM
- CNT/FSM

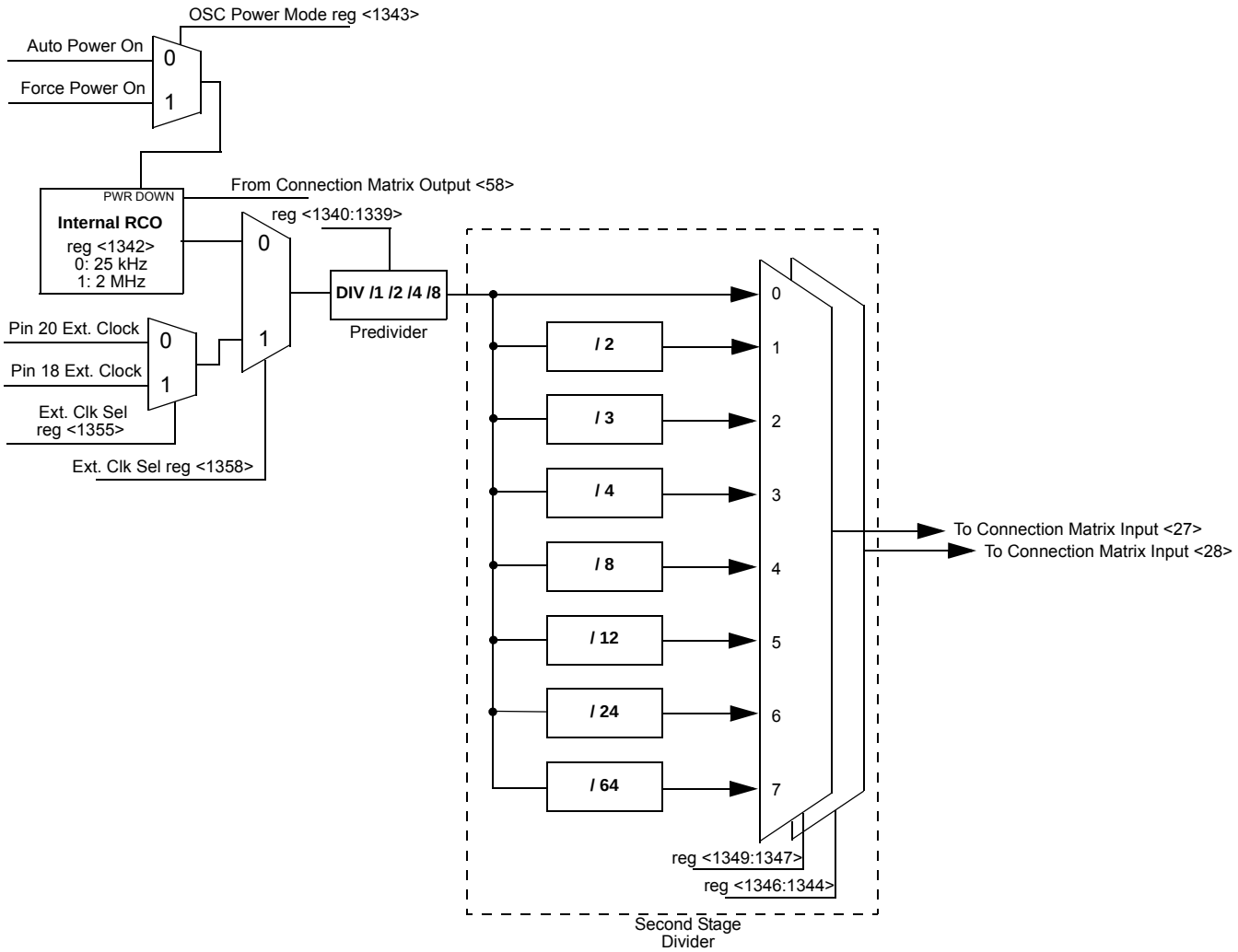



**Figure 52. 25 kHz / 2 MHz RC OSC Block Diagram**

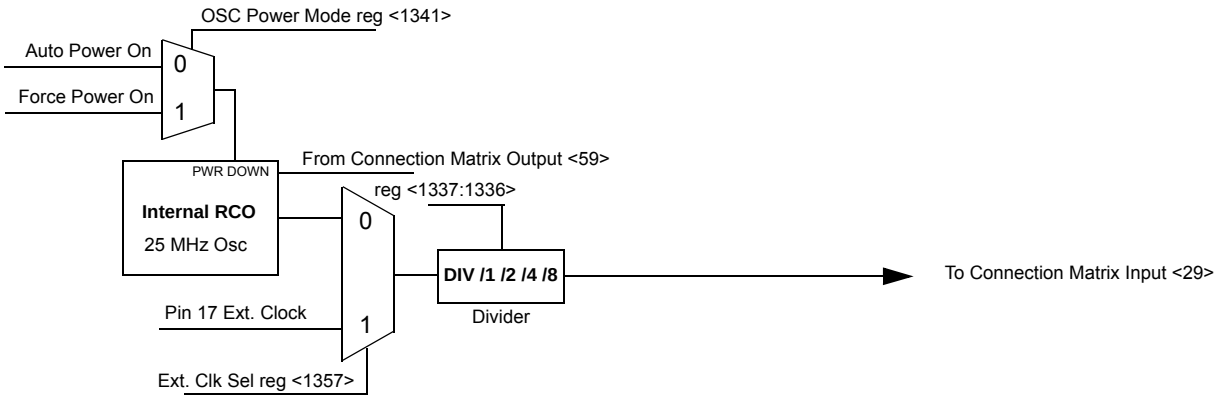



**Figure 53. 25 MHz RC OSC Block Diagram**

## 15.2 Oscillator Power On delay

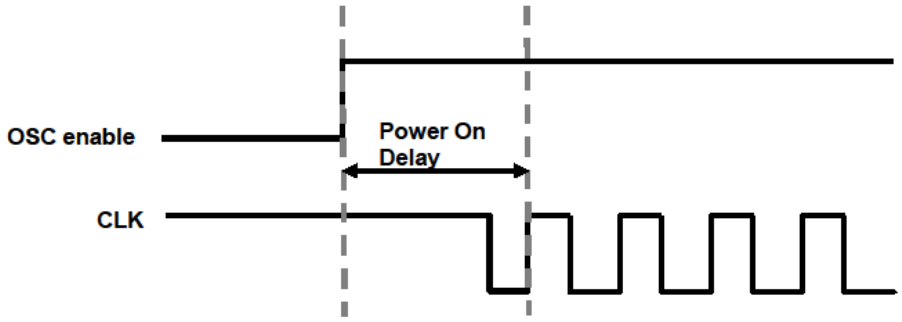



**Figure 54. Oscillator Startup Diagram**

Note 1: OSC power mode: “Auto Power On”.

Note 2: “OSC enable” signal appears when any block that uses OSC is powered on.

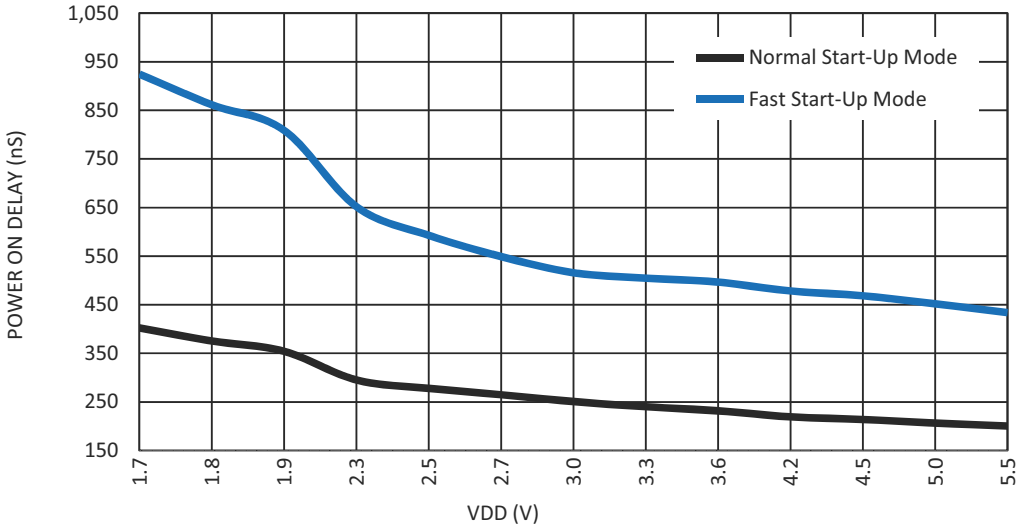



**Figure 55. RC Oscillator Maximum Power On Delay vs. VDD at room temperature, OSC0 = 2 MHz**

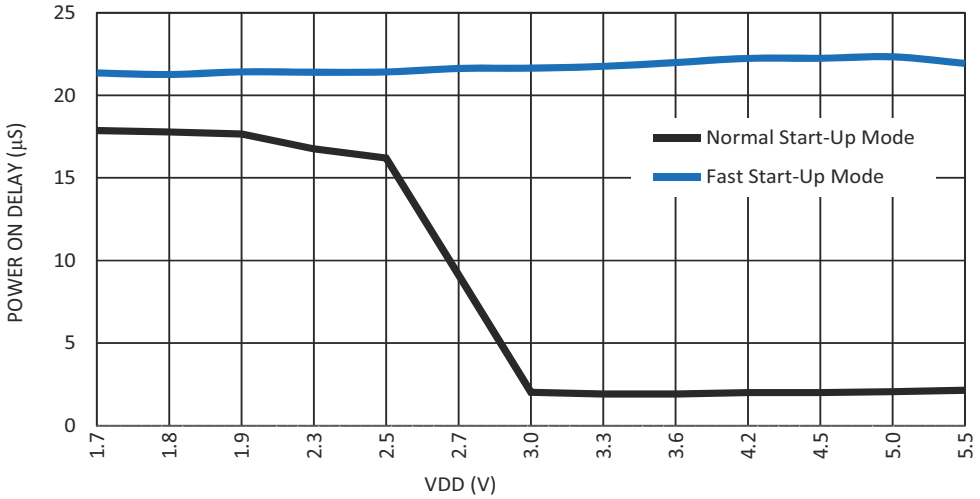



**Figure 56. RC Oscillator Maximum Power On Delay vs. VDD at room temperature, OSC0 = 25 kHz**

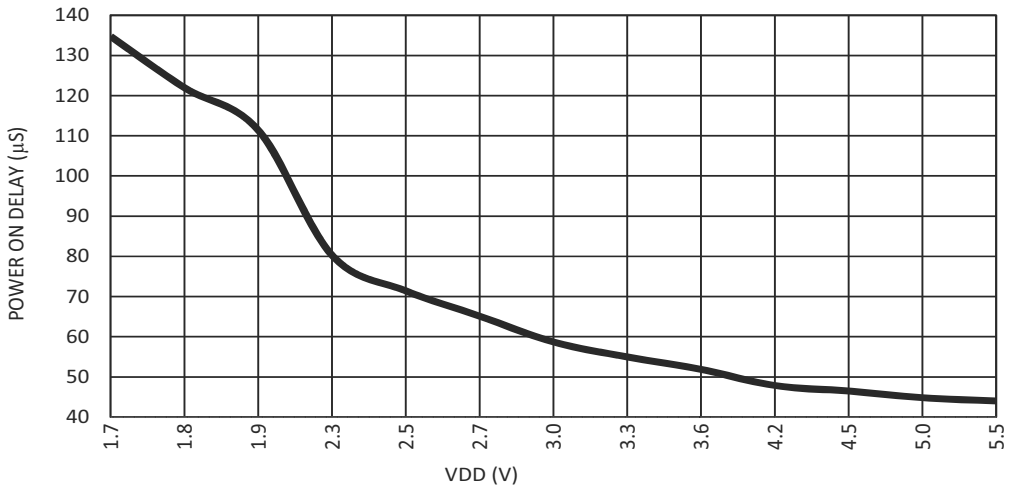



**Figure 57. OSC1 (25 MHz) Maximum Power On Delay vs. VDD at room temperature**

### 15.3 Oscillator Accuracy

Note: OSC power setting: Force Power On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

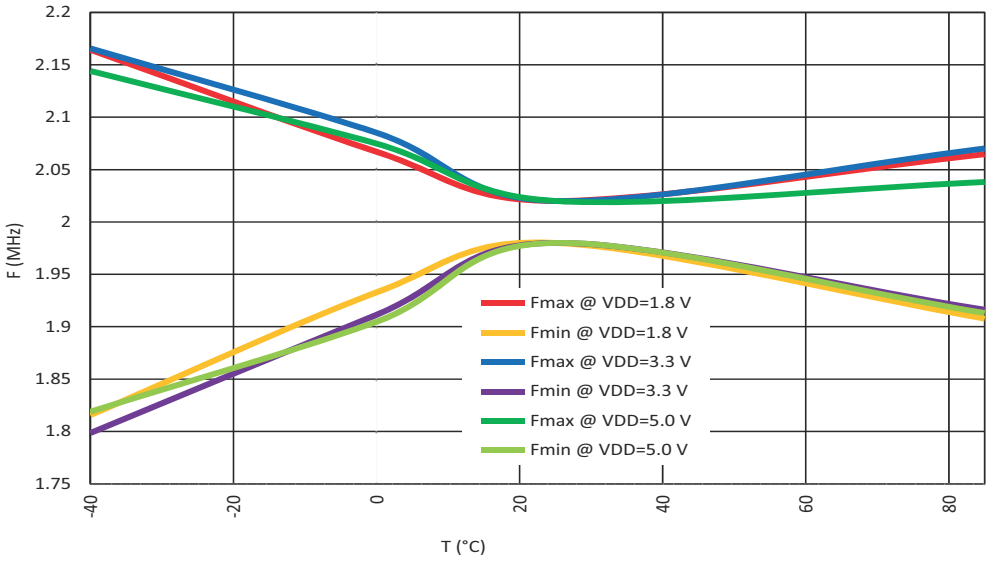



**Figure 58. RC Oscillator Frequency vs. Temperature, RC OSC0=2 MHz**

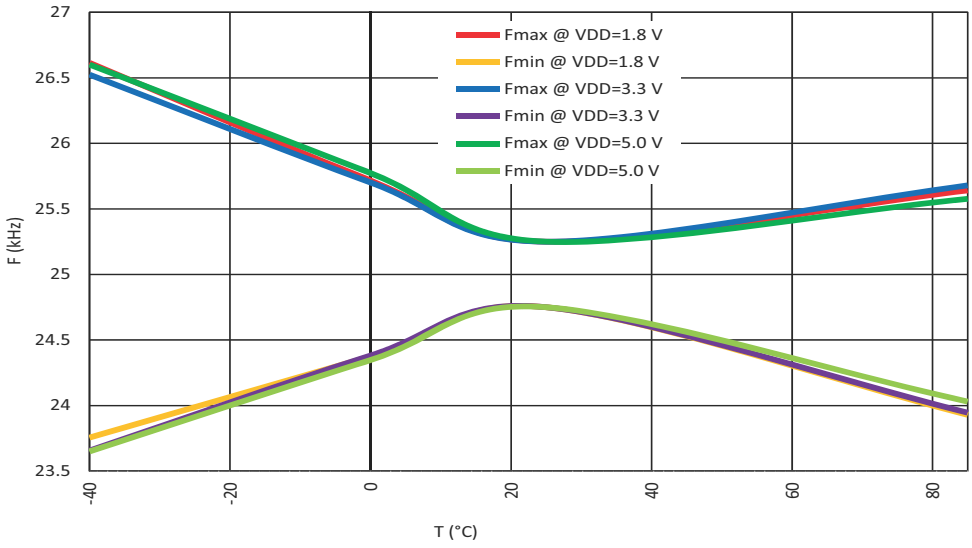



**Figure 59. RC Oscillator Frequency vs. Temperature, RC OSC0=25 kHz**

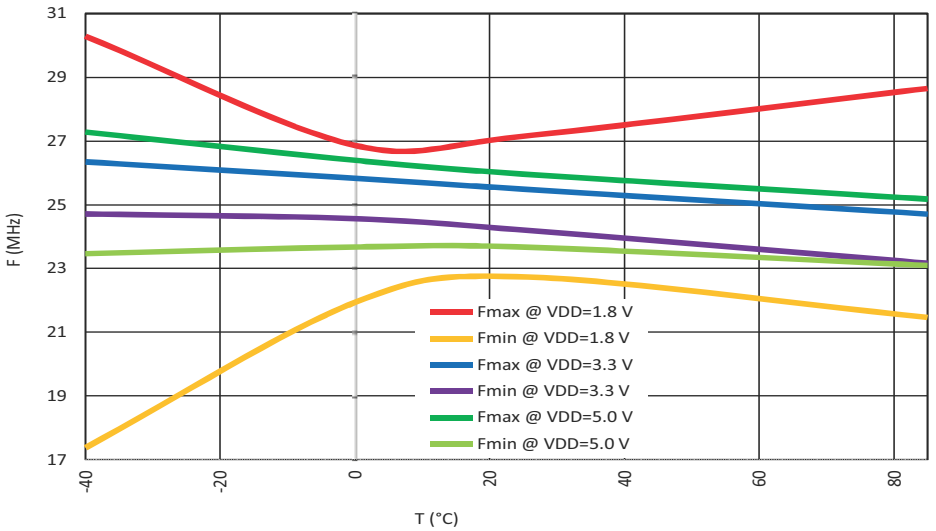



**Figure 60. OSC1 (25 MHz) Frequency vs. Temperature**

Note 1: For more information see section 5.12 OSC Specifications.

Note 2: 25 MHz RC OSC1 performance is not guaranteed at VDD < 2.5 V.

## 16.0 Crystal Oscillator

The Crystal OSC provides high precision and stability of the output frequency. Pin 17 and Pin 16 are input and output, respectively, of an inverting amplifier which is configured for use as an On-chip Oscillator, as shown in *Figure 62*. Either a quartz crystal or a ceramic resonator may be used. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. Refer to *Table 84*. For ceramic resonators, the capacitor values given by the manufacturer should be used. It is possible to use an external clock source, in which case no other external components are required, but the clock source must be connected to Pin 17.

The Power Down Mode is paired with temperature sensor. If it is enabled for Crystal OSC, it is not available for Temp Sensor and vice versa. However, it is possible to enable Power Down Mode for Crystal OSC and Temp Sensor simultaneously.

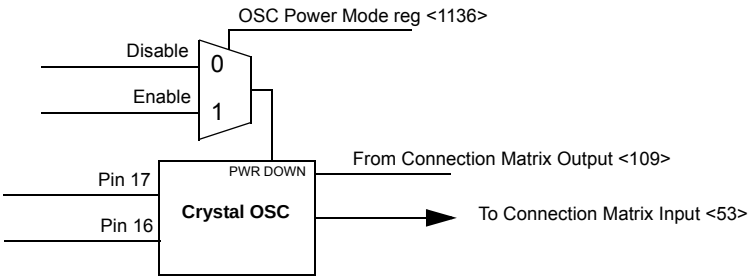



**Figure 61. Crystal OSC Block Diagram**

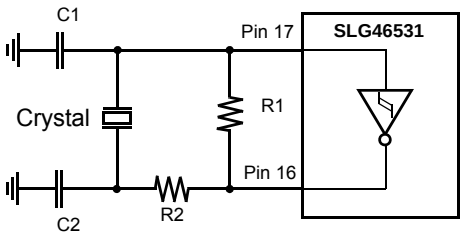



**Figure 62. External Crystal Connection**

**Table 84. External Components Selection Table**

| f | C1 | C2 | R1 | R2 |
|---|---|---|---|---|
| 32.768 kHz | 10 pF | 330 pF | 20 MΩ | 20 kΩ |
| 4 - 40 MHz | 12 pF | 12 pF | 1 MΩ | 0 Ω |

## 17.0 Power On Reset (POR)

The SLG46531 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the VDD power is first ramping to the device, and also while the VDD is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the I/O pins. This application note is created to explain the whole process of POR operation and GreenPAK chip behavior during the time while it is powering up and powering down.

### 17.1 General Operation

The SLG46531 is guaranteed to be powered down and non-operational when the VDD voltage (voltage on PIN1) is less than 0.6V, but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (see Note 1) than the VDD voltage is applied to any other PIN. For example, if VDD voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

*Note 1. There is a 0.6V margin due to forward drop voltage of the ESD protection diodes.*

To start the POR sequence in the SLG46531, the voltage applied on the VDD should be higher than the Power_ON threshold (see Note 2). The full operational VDD range for the SLG46531 is 1.71 V – 5.5 V (1.8 V ±5% - 5 V±10%). This means that the VDD voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the VDD voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46531 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

*Note 2. The Power_ON threshold can vary by PVT, but typically it is 1.6V.*

To power down the chip the VDD voltage should be lower than the operational and to guarantee that chip is powered down it should be less than 0.6 V.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the I/O structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can’t be bigger than the VDD, this rule also applies to the case when the chip is powered on.

### 17.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in *Figure 63*.

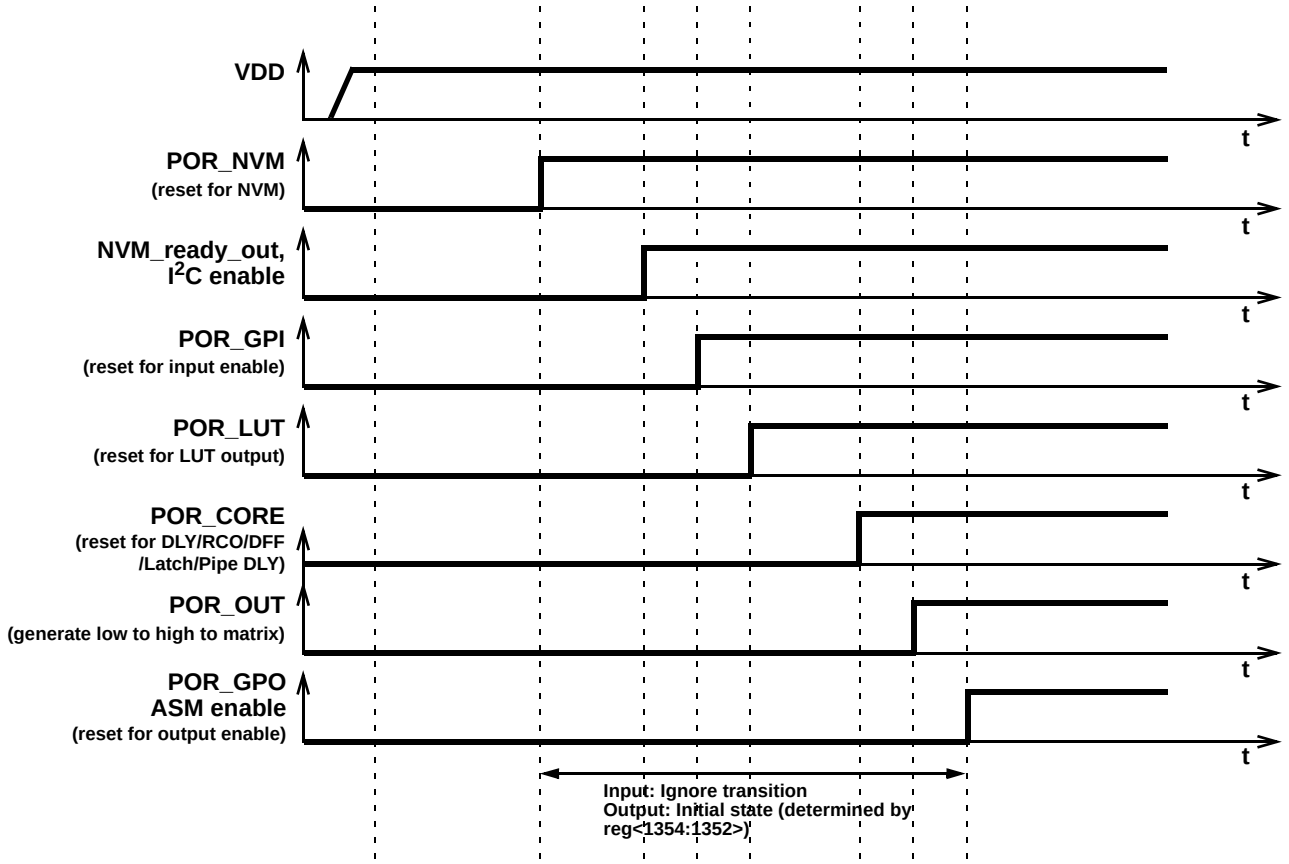



**Figure 63. POR sequence**

As can be seen from *Figure 63* after the VDD has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, VDD value, temperature and even will vary from chip to chip (process influence).

### 17.3 Blocks Output States During POR Sequence

To have a full picture of SLG46531 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (*Figure 64* describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

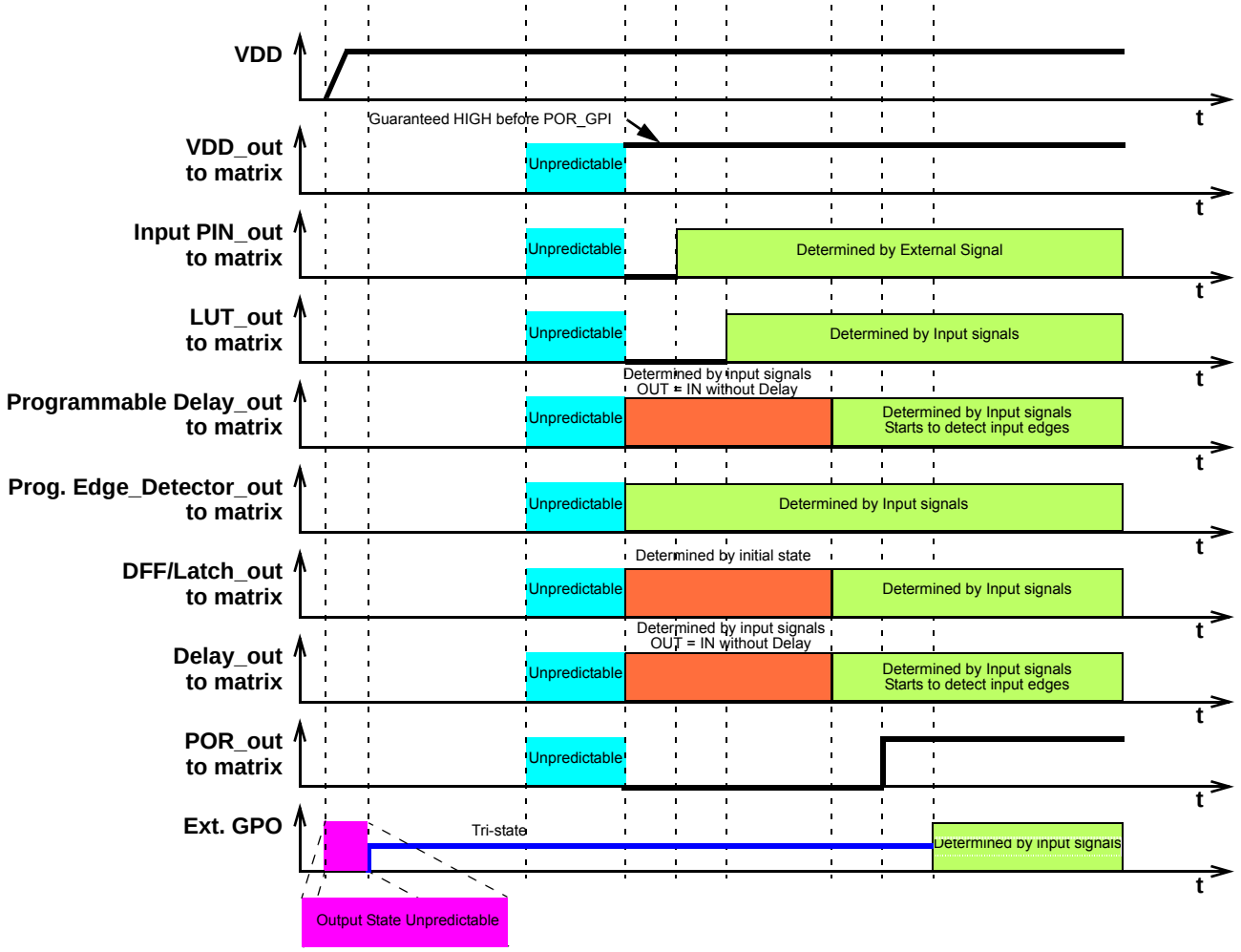



**Figure 64. Internal Block States during POR sequence**

### 17.3.1 Initialization

All internal blocks by default have initial low level. Starting from indicated power-up time of 1.15 V - 1.6 V, blocks in GPAK3 are powered on while forced to the reset state, All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal blocks and they start to initialize according to the following sequence:

1. Input PINs, ACMP, pull up/down;
2. LUTs;
3. DFFs, Delays/Counters, Pipe Delay;
4. POR output to matrix;
5. Output PIN corresponds to the internal logic

The VREF output pin driving signal can precede POR output signal going high by 3 μs - 5 μs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any PIN should not be higher than the VDD level. There are ESD Diodes between PIN –> VDD and PIN –> GND on each PIN. So if the input signal applied to PIN is higher than VDD, then current will sink through the diode to VDD. Exceeding VDD results in leakage current on the input PIN, and VDD will be pulled up, following the voltage on the input PIN.There is no effect from input pin when input voltage is applied at the same time as VDD.

### 17.3.2 Power Down

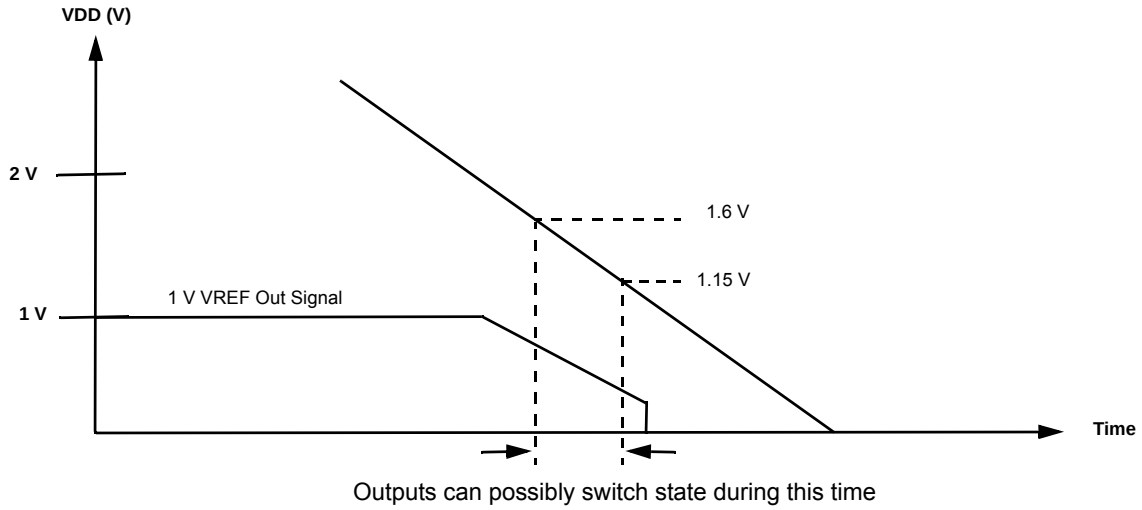



**Figure 65. Power Down**

During powerdown, blocks in SLG46531 are powered off and logic blocks may switch states after falling below 1.4 V. The I/O buffers are disabled when POR goes low at VDD ~1 V. Please note that during a slow rampdown, outputs can possibly switch state during this time.

## 18.0 Asynchronous State Machine (ASM) Macrocell

### 18.1 ASM Macrocell Overview

The Asynchronous State Machine (ASM) macrocell is designed to allow the user to create state machines with between 2 to 8 states. The user has flexibility to define the available states, the available state transitions, and the input signals (a, b, c …) that will cause transitions from one state to another state, as shown in *Figure 66*.

This macrocell has a total of 25 inputs, as shown in *Figure 67*, which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial / Reset state. Each of the 24 inputs is level sensitive and active high, meaning that a high level input will drive the user selected transition from one state to another. The fact that there are 24 inputs puts the upper bound of 24 possible state transitions total in the user defined state machine design. There is on nReset input which will drive an immediate state transition to the user-defined Initial / Reset state when active, shown in red, in the *Figure 66*.

There are a total of 8 outputs, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states. This information is held in the Connection Matrix Output RAM.

In using this macrocell, the user must take into consideration the critical timing required on all input and output signals. The timing waveforms and timing specifications for this macrocell are all measured relative to the input signals (which come into the macrocell on the Connection Matrix outputs) and on the outputs from the macrocell (which are direct connections to Connection Matrix inputs). The user must consider any delays from other logic and internal chip connections, including I/O delays, to insure that signals are properly processed, and state transitions are deterministic.

The GPAK Designer development tools support user designs for the ASM macrocell at both the physical level and logic level. *Figure 66* is a representation of the user design at the logical level, and *Figure 67* shows the physical resources inside the macrocell. To best utilize this macrocell, the user must develop a logical representation of their desired state machine, as well as a physical mapping of the input and outputs required for the desired functionality.

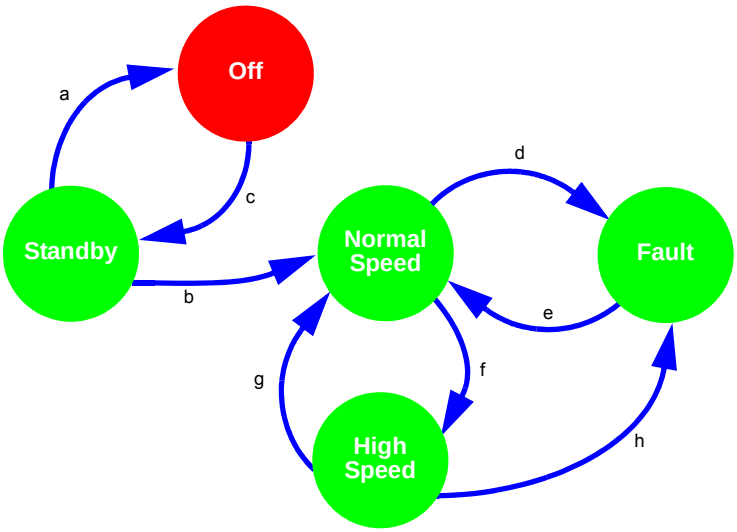



**Figure 66. Asynchronous State Machine State Transitions**

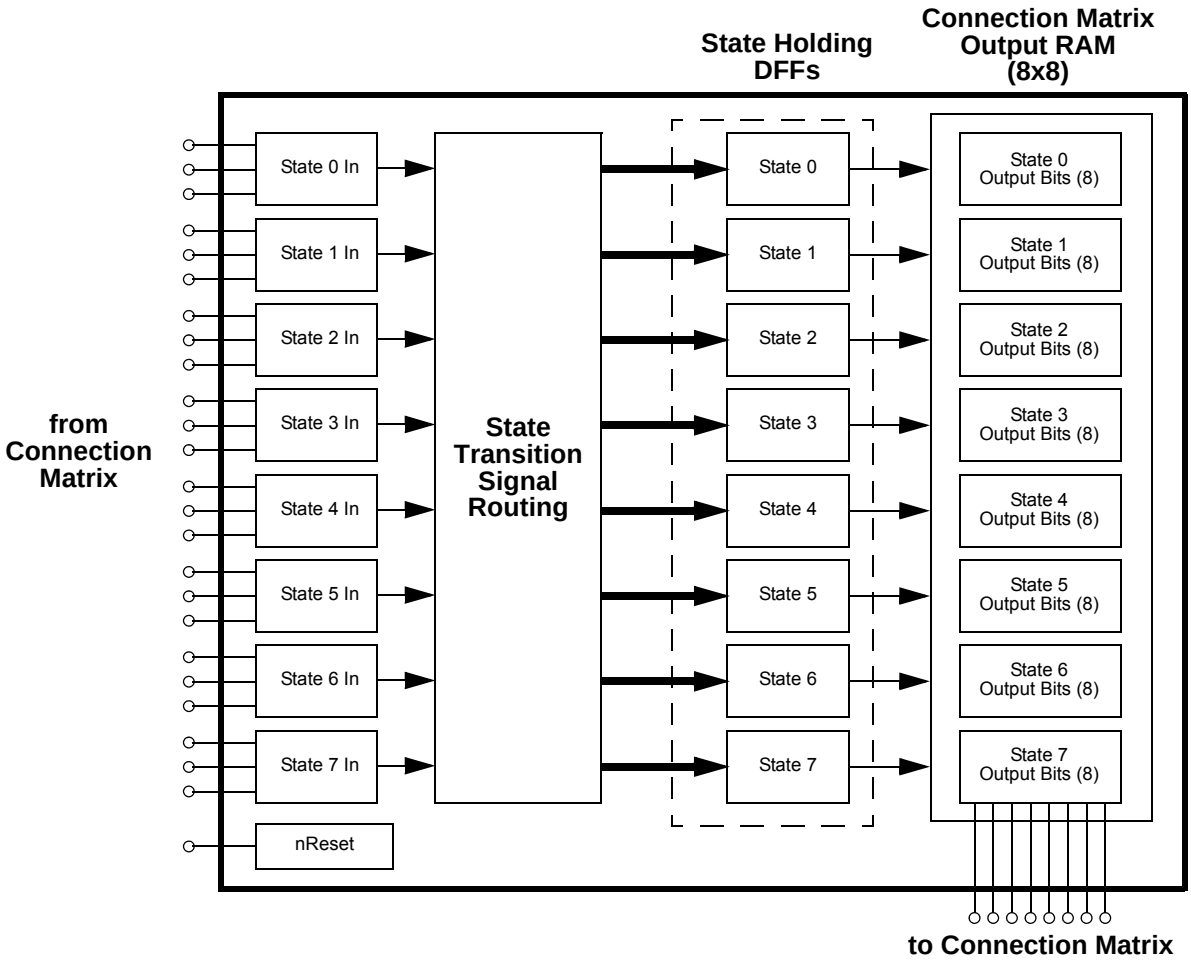



**Figure 67. Asynchronous State Machine**

### 18.2 ASM Inputs

The ASM macrocell has a total of 25 inputs which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial / Reset state.

There are a total of 24 inputs to the ASM macrocell for general state transitions, highlighted in red in *Figure 68*. Each of these inputs is level sensitive, and active high. A high level input will trigger a state transition.

These inputs are grouped so that each set of 3 inputs can drive a state transition **going into** a particular state. As an example, there are three inputs that can drive a state transition to State 1. This sets an upper bound on the number of transitions that the user can select going into a particular state to be 3, shown in *Figure 69*.

There is no limitation on the number of transitions that can be supported coming out of a particular state, the user can select to have transitions going from a state to all other states, shown in *Figure 70*.

The ASM macrocell also has a nReset input highlighted in blue in *Figure 68*. This input is level sensitive and active low. An active signal on this input will drive an immediate state transition to the user-defined Initial / Reset state. The user can choose which state within the ASM Editor inside GPAK Designer is the initial state.

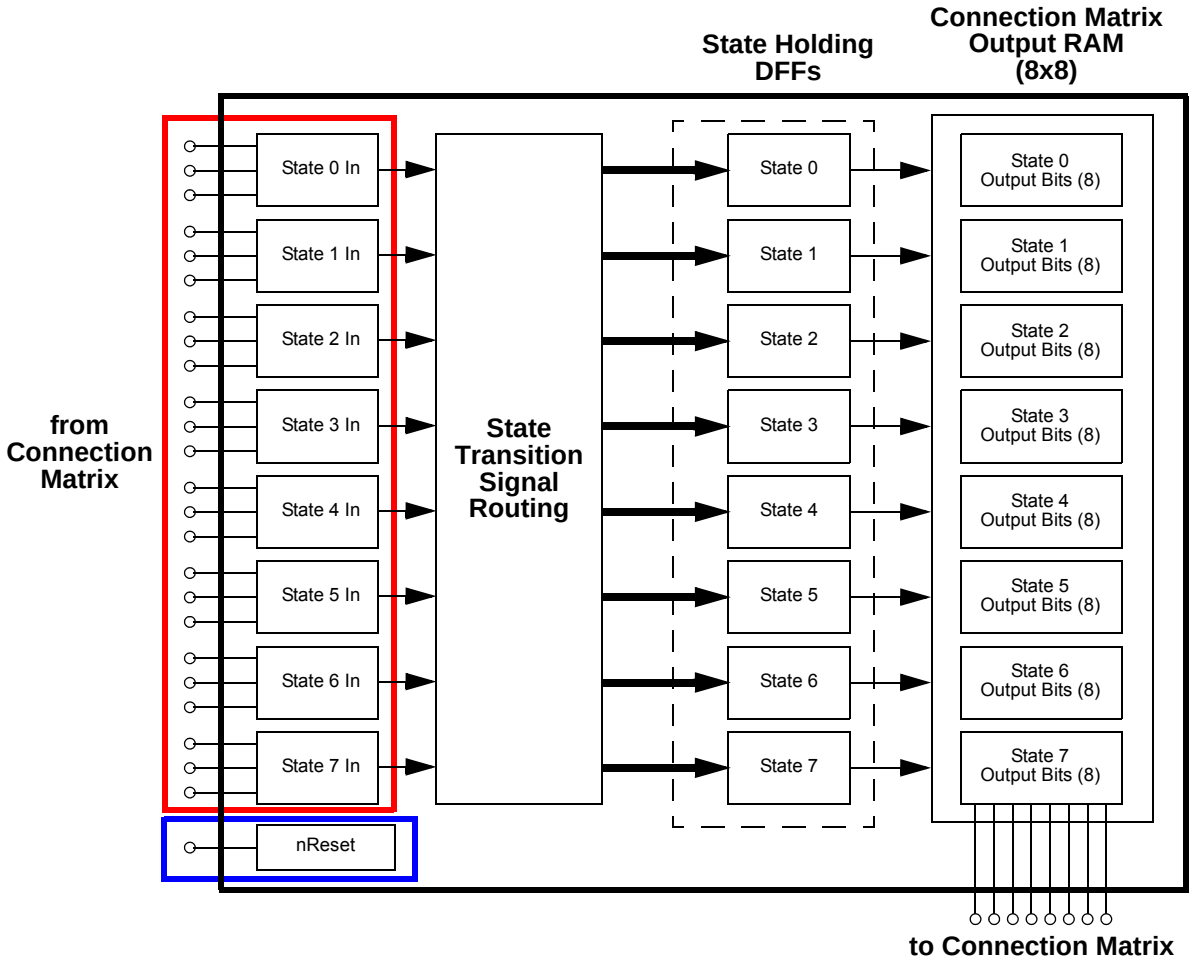



**Figure 68. Asynchronous State Machine Inputs**

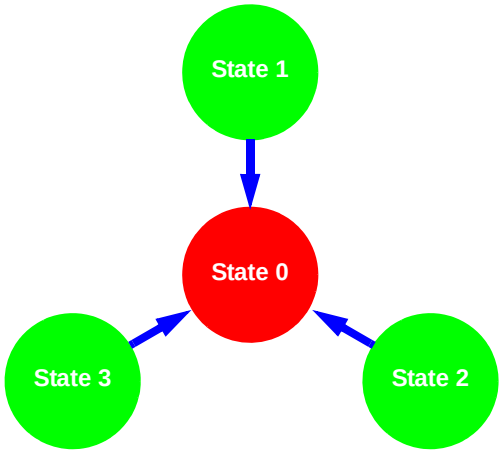



**Figure 69. Maximum 3 State Transitions into Given State**

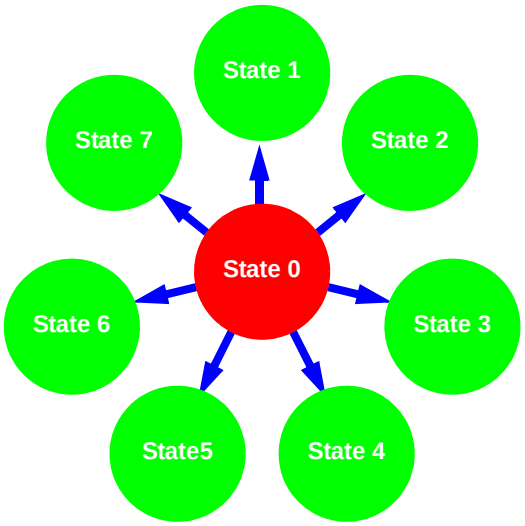



**Figure 70. Maximum 7 State Transitions out of a Given State**

### 18.3 ASM Outputs

There are a total of 8 outputs from the ASM macrocell, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states, this information is held in the Connection Matrix Output RAM, shown in *Figure 71*. The Connection Matrix Output RAM has a total of 64 bits, arranged as 8 bits per state. The values loaded in each of the 8 bits define the signal level on each of the 8 ASM macrocell outputs.

The ASM Editor inside the GPAK Designer software allows the user to make their selections for the value of each bit in the Connection Matrix Output RAM, which selects the level of the macrocell outputs based on the current state of the ASM block, as shown in *Figure 72*.

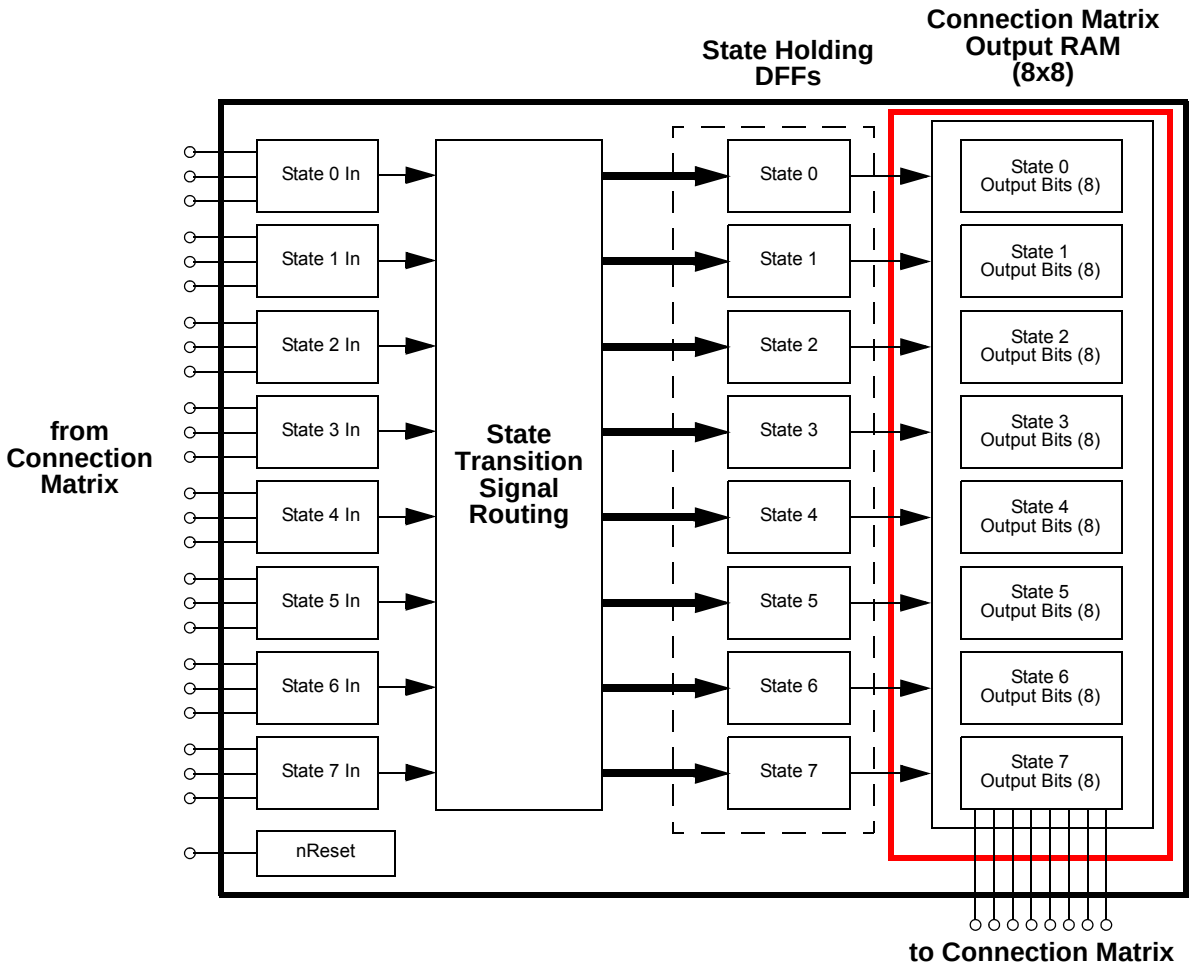



**Figure 71. Connection Matrix Output RAM**

Outputs

| | Input From | State# Name | State Output RAM Array Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | OUT7 | OUT6 | OUT5 | OUT4 | OUT3 | OUT2 | OUT1 | OUT0 |
| EN0 | Standby -> | State 0 Off | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| EN1 | *** -> | | | | | | | | | |
| EN2 | *** -> | | | | | | | | | |
| EN0 | Off -> | State 1 Standby | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| EN1 | *** -> | | | | | | | | | |
| EN2 | *** -> | | | | | | | | | |
| EN0 | Standby -> | State 2 Normal Spe.. | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| EN1 | High Speed -> | | | | | | | | | |
| EN2 | Fault -> | | | | | | | | | |
| EN0 | Normal Spe.. -> | State 3 High Speed | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| EN1 | *** -> | | | | | | | | | |
| EN2 | *** -> | | | | | | | | | |
| EN0 | Normal Spe.. -> | State 4 Fault | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| EN1 | High Speed -> | | | | | | | | | |
| EN2 | *** -> | | | | | | | | | |

**Figure 72. ASM Editor - Connection Matrix Output RAM**

### 18.4 Basic ASM Timing

The basic state transition timing from input on Matrix Connection output to output on Matrix Connection input is shown in *Figure 73* and *Figure 74*. The time from a valid input signal to the time that there is a valid change of state and valid signals being available on the state outputs is State Machine Output Delay Time (Tst_out_delay). The minimum and maximum values of Tst_out_delay define the differential timing between the shortest state transition (input on matrix output and output on matrix input) and the longest state transition (input on matrix output and output on matrix input).

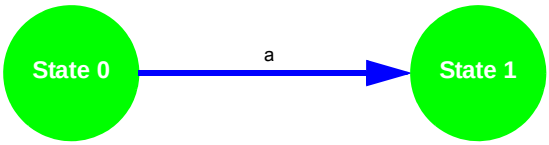



**Figure 73. State Transition**

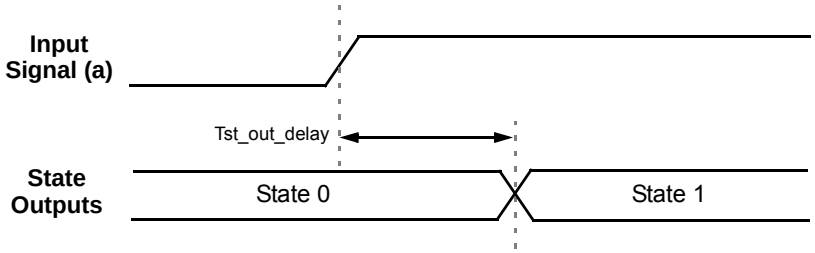



**Figure 74. State Transition Timing**

### 18.5 Asynchronous State Machines vs. Synchronous State Machines

It is important to note that this macrocell is designed for asynchronous operation, which means the following:

1. No clock source is needed, it reacts only to input signals
2. The input signals do not have to be synchronized to each other, the macrocell will react to the earliest valid signal for state transition.
3. This block does not have traditional set-up and hold time specifications which are related to incoming clock, as this macrocell has no clock source.
4. The macrocell only consumes power while in state transition.

### 18.6 ASM Power Considerations

A benefit of the asynchronous nature of this macrocell is that it will consume power only during state transitions. Shown in *Figure 73* and *Figure 75* below, the current consumption of the macrocell will be a fraction of a µA between state transitions, and will rise only during state transitions. See Section 5.7 IDD Estimator to find average current during state transitions.

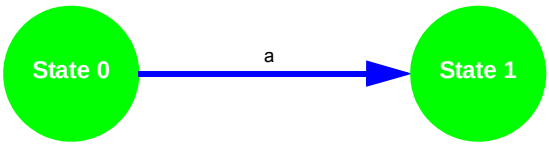



**Figure 75. State Transition**

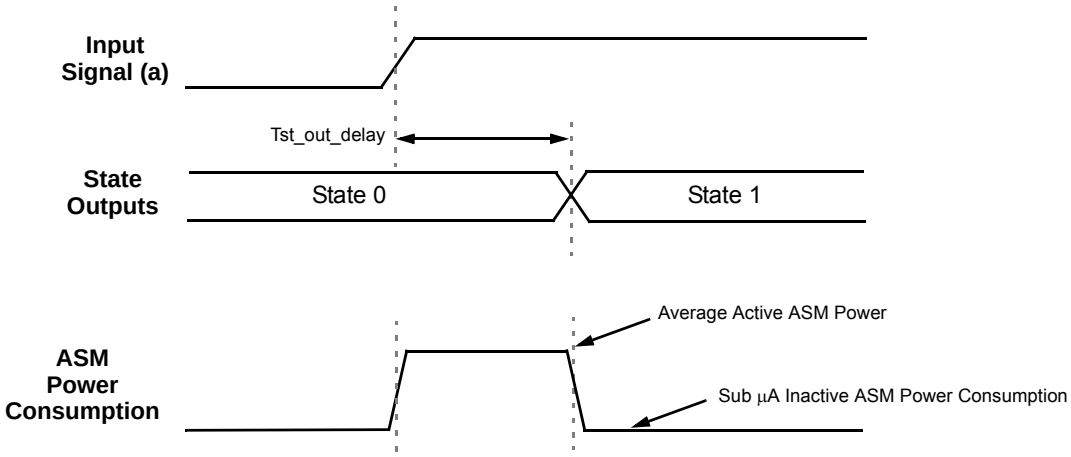



**Figure 76. State Transition Timing and Power Consumption**

### 18.7 ASM Logical vs. Physical Design

A successful design with the ASM macrocell must include both the logic level design as well as the physical level design. The GPAK Designer development software support user designs for the ASM macrocell at both the logic level and physical level. The logic level design of the user defined state machine takes place inside the ASM Editor. In the ASM Editor, the user can select and name states, define and name allowed state transitions, define the Initial / Reset state and define the output values for the 8 outputs in the Output RAM Matrix. The physical level design takes place in the general GPAK Designer window, and here the user makes connections for the sources for ASM input signals, as well as making connections for destinations for ASM output signals.

### 18.8 ASM Special Case Timing Considerations

#### 18.8.1 State Transition Pulse Input Timing

All inputs to the ASM macrocell are level sensitive. If the input to the state machine block for a state transition is a pulse, there is a minimum pulse width on the input to the state machine block (as measured at the matrix input to the block) which is guaranteed to result in a state transition shown in *Figure 77* and *Figure 78*. This pulse width is defined by the State Machine Input Pulse Acceptance Time (Tst_pulse). If a pulse width that is shorter than Tst_pulse is input to the state machine block, it is indeterminate whether the state transition will happen or not. If a pulse that is rejected (invalid due to the pulse width being narrower than the guaranteed minimum of Tst_pulse), this will not stop a valid pulse on another state transition input that does meet minimum pulse width.

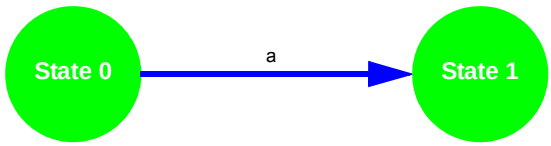



**Figure 77. State Transition**

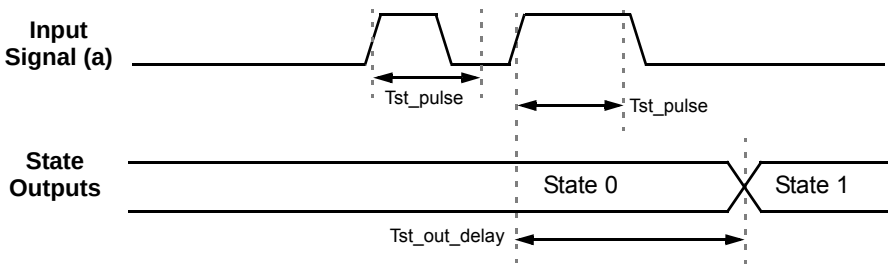



**Figure 78. State Transition Pulse Input Timing**

### 18.8.2 State Transition Competing Input Timing

There will be situations where two input signals can be valid inputs that will drive two different state transitions from a given state. In that sense, the two signals are “competing” (signals a and b in *Figure 79*), and the signal that arrives sooner should drive the state transition that will “win”, or drive the state transition. If one signal arrives Tst_comp before the other one, it is guaranteed to win, and the state transition that it codes for will be taken, as shown in *Figure 80*. If the two signals arrive within Tst_comp of each other, it will be indeterminate which state transition will win, but one of the transitions will take place as long as the winning signal satisfies the pulse width criteria described in the paragraph above, as shown in *Figure 81*.

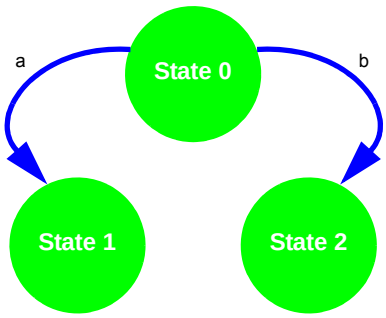



**Figure 79. State Transition - Competing Inputs**

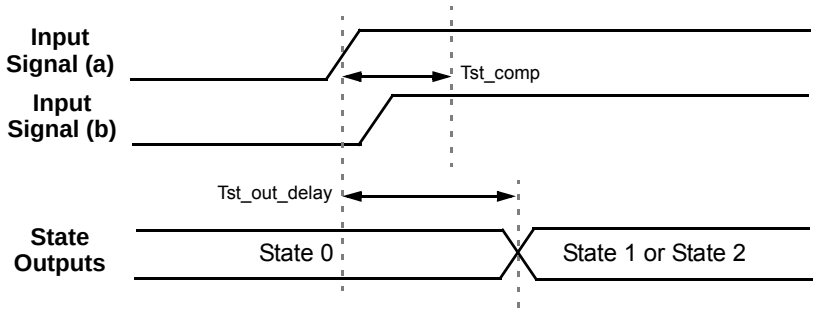



**Figure 80. State Transition Timing - Competing Inputs Indeterminate**

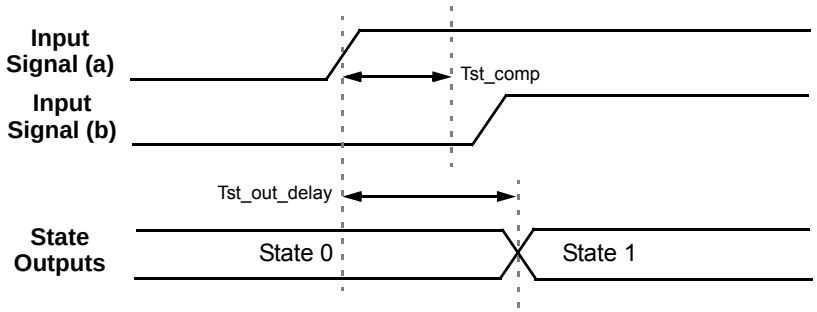



**Figure 81. State Transition Timing - Competing Inputs Determinable**

### 18.8.3 ASM State Transition Sequential Timing

It is possible to have a valid input signal for a transition out from a particular state be active before the state is active. If this is the case, the block will only stay in that particular state for Tst_out_delay time before making the transition to the next state. An example of this sequential behavior is shown in *Figure 82* and the associated timing is shown in *Figure 83*.

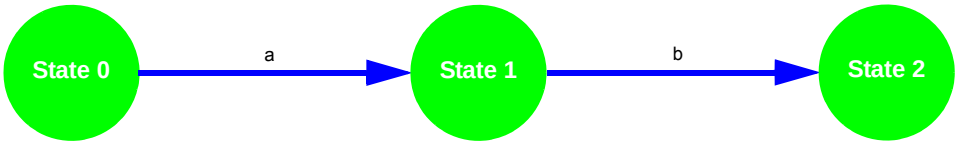



**Figure 82. State Transition - Sequential**

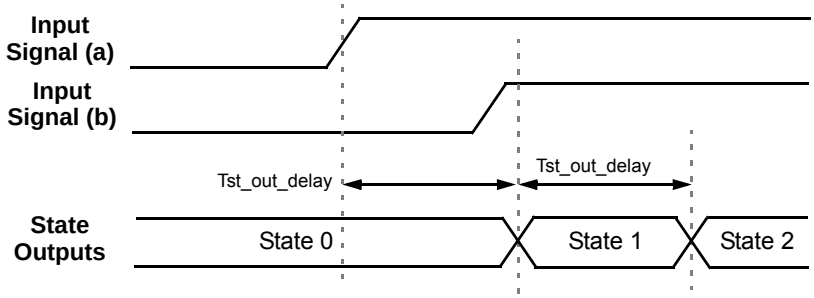



**Figure 83. State Transition - Sequential Timing**

### 18.8.4 State Transition Closed Cycling

It is possible to have a closed cycle of state transitions that will run continuously if there if there are valid inputs that are active at the same time. The rate at which the state transitions will take place is determined by Tst_out_delay. The example shown here in *Figure 84* involves cycling between two states, but any number of two – eight states can be included in state transition closed cycling of this nature. *Figure 85* shows the associated timing for closed cycling.

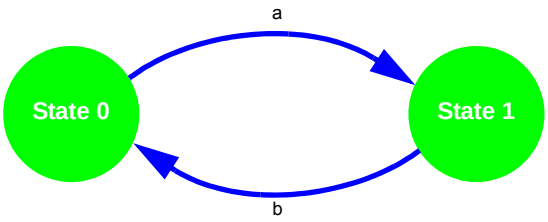



**Figure 84. State Transition - Closed Cycling**

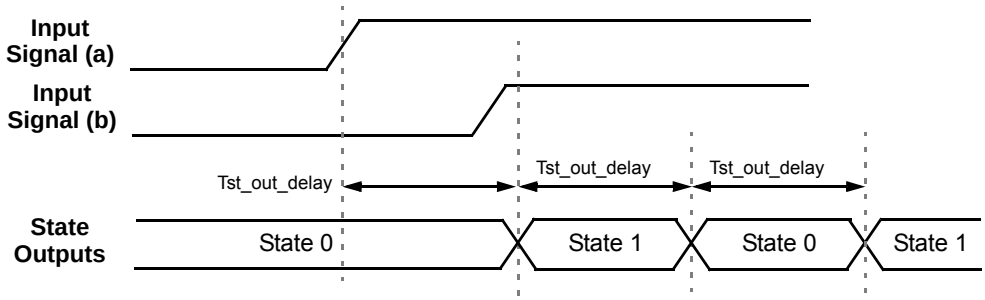



**Figure 85. State Transition - Closed Cycling Timing**

## 19.0 I²C Serial Communications Block

### 19.1 I²C Serial Communications Block Overview

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits reg<1832> and reg<1871>. See section 19.4.6.1 for more details on I²C read/write memory protection.

Note: GreenPAK I²C is fully compatible with standard I²C protocol.

### 19.2 I²C Serial Communications Device Addressing

Each command to the I²C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in *Figure 86*. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1867:1864>. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10,A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/$\overline{W}$ bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bits. Of this 2K bit address space, the valid addresses accessible to the I²C Macrocell on the SLG46531 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9 and A8) will be "0" for all commands to the SLG46531.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. *Figure 86* shows this basic command structure.

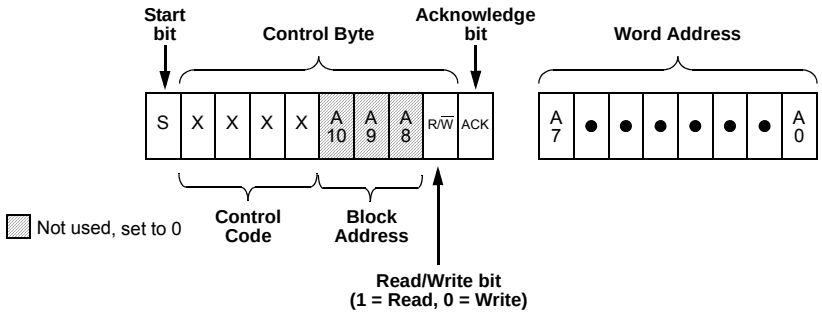



**Figure 86. Basic Command Structure**

### 19.3 I²C Serial General Timing

Shown in *Figure 87* is the general timing characteristics for the I²C Serial Communications block. Timing specifications can be found in the AC Characteristics section.

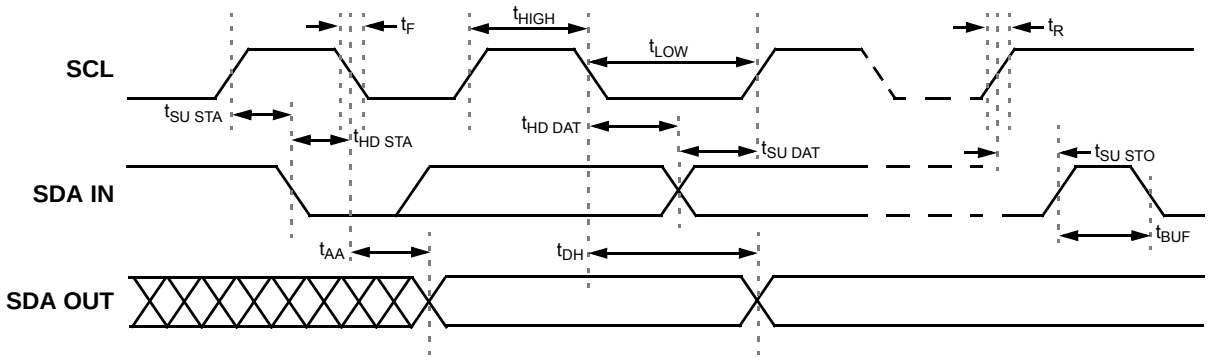



**Figure 87. I²C General Timing Characteristics**

### 19.4 I²C Serial Communications Commands

#### 19.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits] and the R/$\overline{W}$ bit (set to "0"), are placed onto the I²C bus by the Master. After the SLG46531 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46531 where the data byte is to be written. After the SLG46531 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46531 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46531 generates the Acknowledge bit.

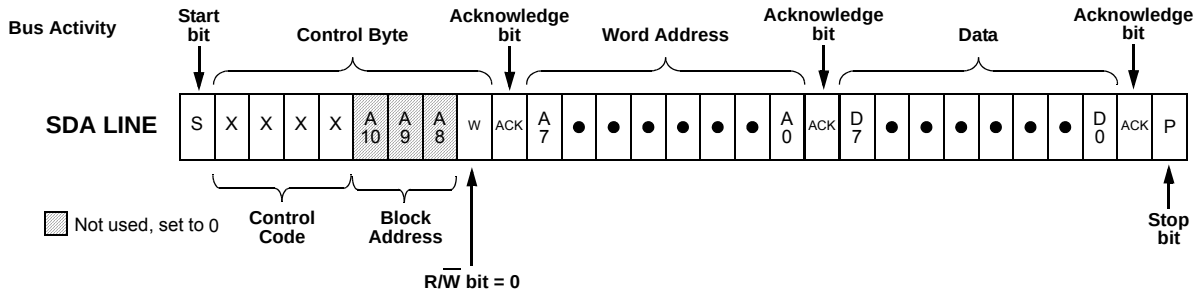



**Figure 88. Byte Write Command, R/$\overline{W}$ = 0**

### 19.4.2 Sequential Write Command

The write Control Byte, Word Address and the first data byte are transmitted to the SLG46531 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Master continues to transmit data bytes to the SLG46531. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46351 generates the Acknowledge bit.

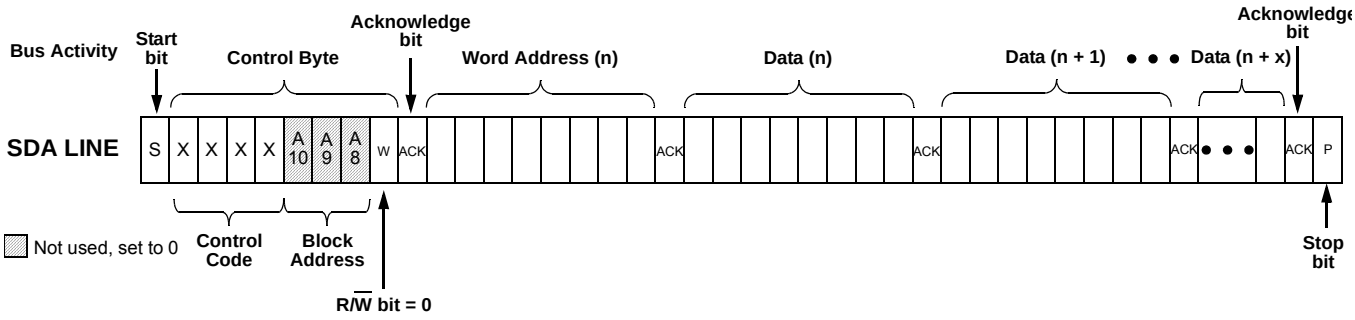



**Figure 89. Sequential Write Command, R/$\overline{W}$ = 0**

### 19.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Write or Random Read (which contains a write control byte) writes or reads data up to address n, the address pointer would get incremented to n+1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n+1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/$\overline{W}$ bit = “1”. The SLG46531 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

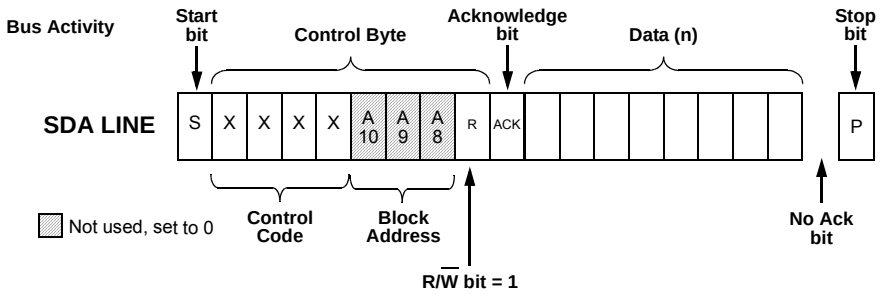



**Figure 90. Current Address Read Command, R/$\overline{W}$ = 1**

### 19.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG46531 issues an Acknowledge bit, followed by the requested eight data bits.

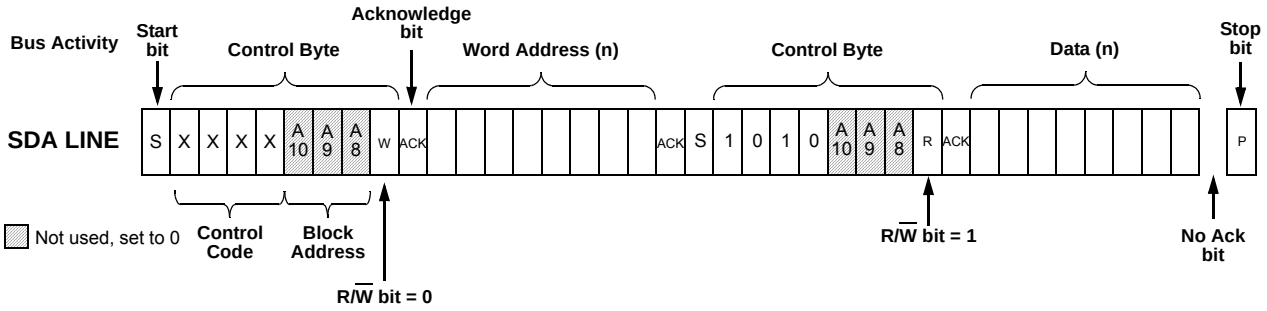



**Figure 91. Random Read Command**

### 19.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Current Address Read or Random Read command, except that once the SLG46531 transmits the first data byte, the Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

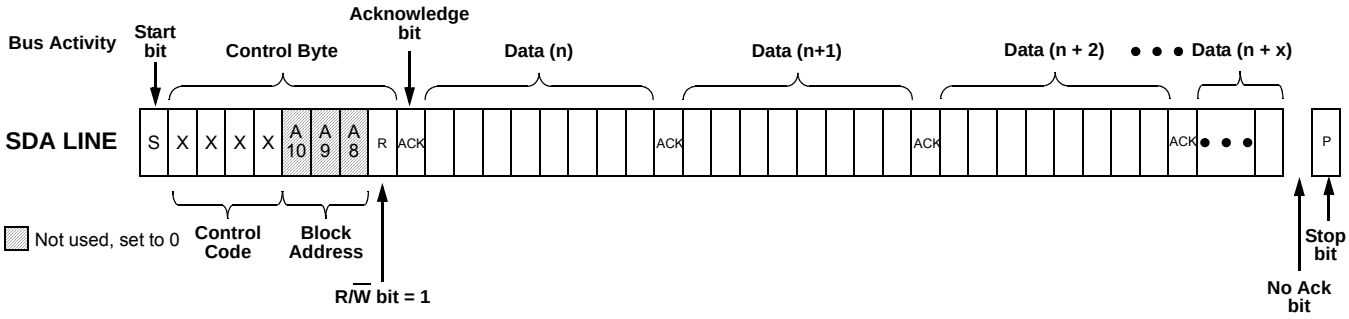



**Figure 92. Sequential Read Command**

### 19.4.6 I²C Serial Command Register Map

These register addresses are broken down into four Banks to give the user greater control on access to reading and writing information in each bank. Each of the four banks is 512 bits (64 bytes) in length. Writing information to register bits in these Banks will change the configuration of the device, resulting in either a change in the interconnection options provided by the Connection Matrix, or by changing the configuration of individual macrocells. During device use, all register bits can be read or written via I²C, unless protection bits are set to prevent this.

See Section 21.0 Appendix A - SLG46531 Register Definition for detailed information on all register bits

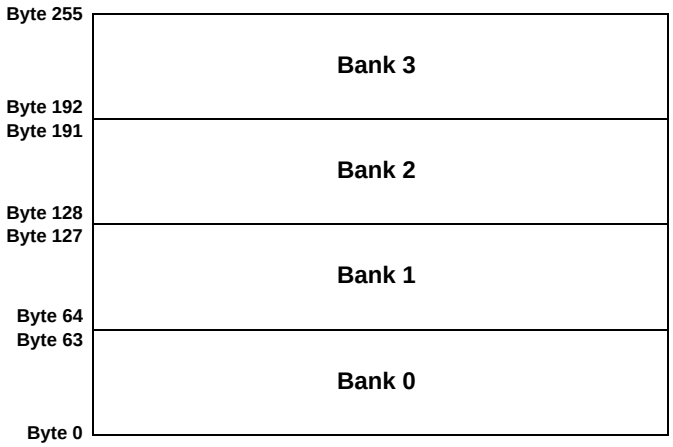



**Figure 93. Register Bank Map**

#### 19.4.6.1 I²C Serial Command Register Protection

All register bits in the first three Banks (0 – 2) can be read and written via I²C unless they are protected with two register bits stored in the NVM. The two register bits that select whether the bits within Banks 0 – 2 can be read or written are as follows:

- reg<1832> Bank 0/1/2 I²C read protection bit
- reg<1871> Bank 0/1/2 I²C write protection bit

Register bits in Bank 3 are always open to read and write commands via I²C with the following exceptions:

- reg<1663> IO Latching Enable During I²C Write Interface is protected from I²C write, see Note 1
- reg<1871> Bank 0/1/2 I²C-write protection bit is protected from I²C write
- reg<1867:1864> I²C Control Code Bit [3:0] is protected from I²C write

Note1. If reg<1663> = 1, all outputs are latched while inputs and internal blocks retain their status during I2C write

See Section 21.0 Appendix A - SLG46531 Register Definition for detailed information on all registers

#### 19.4.6.2 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting reg<1662> I²C reset bit to “1”, which causes the device to re-enable the Power On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of reg<1662> will be set to “0” automatically. The timing diagram shown below illustrates the sequence of events for this reset function.

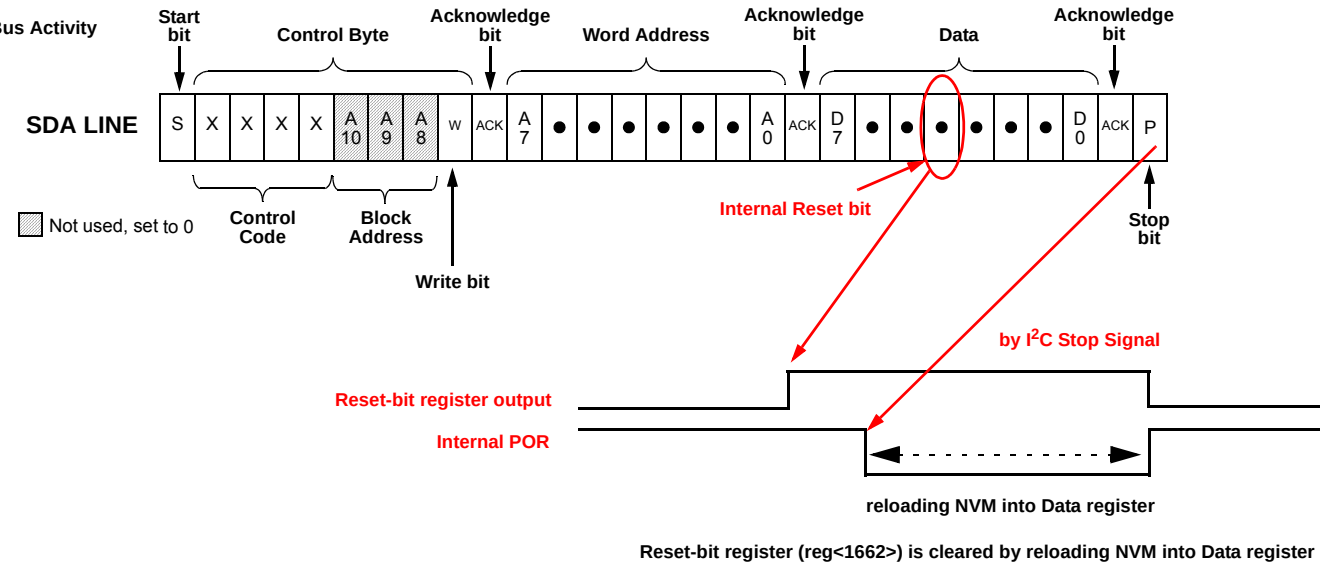



**Figure 94. Reset Command Timing**

#### 19.4.6.3 Reading Counter Data via I²C

The current count value in four counters in the device can be read via I²C. The counters that have this additional functionality are 16-bit CNT0 and CNT1, and 8-bit counters CNT4 and CNT6.

#### 19.4.6.4 User RAM and OTP Memory Array

There are eight bytes of RAM memory that can be read and written remotely by I²C commands. The initial contents of this memory space can be selected by the user, and this information will be transferred from OTP memory to the RAM memory space during the power-up sequence. The lowest order byte in this array (User Configurable RAM/OTP Byte 0) is located at I²C address 0xD8, and the highest order byte in this array is located at I²C address 0xDF.

**Table 85. RAM Array Table**

| I2C Address (hex) | Highest Bit Address | Lowest Bit Address | Memory Byte |
|---|---|---|---|
| D8 | 1735 | 1728 | User Configurable RAM/OTP Byte 0 |
| D9 | 1743 | 1736 | User Configurable RAM/OTP Byte 1 |
| DA | 1751 | 1744 | User Configurable RAM/OTP Byte 2 |
| DB | 1759 | 1752 | User Configurable RAM/OTP Byte 3 |
| DC | 1767 | 1760 | User Configurable RAM/OTP Byte 4 |
| DD | 1775 | 1768 | User Configurable RAM/OTP Byte 5 |
| DE | 1783 | 1776 | User Configurable RAM/OTP Byte 6 |
| DF | 1791 | 1784 | User Configurable RAM/OTP Byte 7 |

The error in the whole temperature range does not exceed ±10.3% (±5.7% in a range from -40°C to 100°C). TS output voltage variation over VDD at constant temperature is less than ±10.3% (±6.3% without buffer).

## 20.0 External Clocking

The SLG46531 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

### 20.1 Crystal Mode

When reg<1136> is set to 1, an external crystal can be connected to pins 16 and 17 for supplying an accurate clock source. See section 16.0 Crystal Oscillator. An external clocking signal on pin 17 can be used in place of the crystal. The high and low limits for crystal frequency that can be selected are 32.768 kHz and 40 MHz.

### 20.2 Pin 20 or Pin 18 Source for 25 KHz / 2 MHz Clock

When reg<1358> is set to 1, an external clocking signal on pins 18 or 20 will be routed in place of the internal RC oscillator derived 25 kHz/2 MHz clock source. When reg<1355> is set to 0, pin 20 is in use, when 1 – pin 18 is in use. See *Figure 52*. The high and low limits for external frequency that can be selected are 0 MHz and 77 MHz.

### 20.3 Pin 17 Source for 25 MHz Clock

When reg<1357> is set to 1, an external clocking signal on pin 17 will be routed in place of the internal RC oscillator derived 25 MHz clock source. See *Figure 53*. The high and low limits for external frequency that can be selected are 0 MHz and 84 MHz.

## 21.0 Appendix A - SLG46531 Register Definition

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **Note: For reg<0> to reg<1495>, I²C Read is valid (assuming reg <1832> = 0), I²C Write is valid (assuming reg <1871> = 0)** | | | | | |
| **Matrix 64-to-1 MUX's 6 selection bits** | | | | | |
| 00 | reg<5:0> | Matrix OUT | ASM-state0-EN0 | Valid | Valid |
| | reg<7:6> | Reserved | | Valid | Valid |
| 01 | reg<13:8> | Matrix OUT | ASM-state0-EN1 | Valid | Valid |
| | reg<15:14> | Reserved | | Valid | Valid |
| 02 | reg<21:16> | Matrix OUT | ASM-state0-EN2 | Valid | Valid |
| | reg<23:22> | Reserved | | Valid | Valid |
| 03 | reg<29:24> | Matrix OUT | ASM-state1-EN0 | Valid | Valid |
| | reg<31:30> | Reserved | | Valid | Valid |
| 04 | reg<37:32> | Matrix OUT | ASM-state1-EN1 | Valid | Valid |
| | reg<39:38> | Reserved | | Valid | Valid |
| 05 | reg<45:40> | Matrix OUT | ASM-state1-EN2 | Valid | Valid |
| | reg<47:46> | Reserved | | Valid | Valid |
| 06 | reg<53:48> | Matrix OUT | ASM-state2-EN0 | Valid | Valid |
| | reg<55:54> | Reserved | | Valid | Valid |
| 07 | reg<61:56> | Matrix OUT | ASM-state2-EN1 | Valid | Valid |
| | reg<63:62> | Reserved | | Valid | Valid |
| 08 | reg<69:64> | Matrix OUT | ASM-state2-EN2 | Valid | Valid |
| | reg<71:70> | Reserved | | Valid | Valid |
| 09 | reg<77:72> | Matrix OUT | ASM-state3-EN0 | Valid | Valid |
| | reg<79:78> | Reserved | | Valid | Valid |
| 0A | reg<85:80> | Matrix OUT | ASM-state3-EN1 | Valid | Valid |
| | reg<87:86> | Reserved | | Valid | Valid |
| 0B | reg<93:88> | Matrix OUT | ASM-state3-EN2 | Valid | Valid |
| | reg<95:94> | Reserved | | Valid | Valid |
| 0C | reg<101:96> | Matrix OUT | ASM-state4-EN0 | Valid | Valid |
| | reg<103:102> | Reserved | | Valid | Valid |
| 0D | reg<109:104> | Matrix OUT | ASM-state4-EN1 | Valid | Valid |
| | reg<111:110> | Reserved | | Valid | Valid |
| 0E | reg<117:112> | Matrix OUT | ASM-state4-EN2 | Valid | Valid |
| | reg<119:118> | Reserved | | Valid | Valid |
| 0F | reg<125:120> | Matrix OUT | ASM-state5-EN0 | Valid | Valid |
| | reg<127:126> | Reserved | | Valid | Valid |
| 10 | reg<133:128> | Matrix OUT | ASM-state5-EN1 | Valid | Valid |
| | reg<135:134> | Reserved | | Valid | Valid |
| 11 | reg<141:136> | Matrix OUT | ASM-state5-EN2 | Valid | Valid |
| | reg<143:142> | Reserved | | Valid | Valid |
| 12 | reg<149:144> | Matrix OUT | ASM-state6-EN0 | Valid | Valid |
| | reg<151:150> | Reserved | | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 13 | reg<157:152> | Matrix OUT | ASM-state6-EN1 | Valid | Valid |
| | reg<159:158> | Reserved | | Valid | Valid |
| 14 | reg<165:160> | Matrix OUT | ASM-state6-EN2 | Valid | Valid |
| | reg<167:166> | Reserved | | Valid | Valid |
| 15 | reg<173:168> | Matrix OUT | ASM-state7-EN0 | Valid | Valid |
| | reg<175:174> | Reserved | | Valid | Valid |
| 16 | reg<181:176> | Matrix OUT | ASM-state7-EN1 | Valid | Valid |
| | reg<183:182> | Reserved | | Valid | Valid |
| 17 | reg<189:184> | Matrix OUT | ASM-state7-EN2 | Valid | Valid |
| | reg<191:190> | Reserved | | Valid | Valid |
| 18 | reg<197:192> | Matrix OUT | ASM-state-RSTB | Valid | Valid |
| | reg<199:198> | Reserved | | Valid | Valid |
| 19 | reg<205:200> | Matrix OUT | PIN3 Digital Output Source | Valid | Valid |
| | reg<207:206> | Reserved | | Valid | Valid |
| 1A | reg<213:208> | Matrix OUT | PIN3 Output Enable | Valid | Valid |
| | reg<215:214> | Reserved | | Valid | Valid |
| 1B | reg<221:216> | Matrix OUT | PIN4 Digital Output Source | Valid | Valid |
| | reg<223:222> | Reserved | | Valid | Valid |
| 1C | reg<229:224> | Matrix OUT | PIN5 Digital Output Source | Valid | Valid |
| | reg<231:230> | Reserved | | Valid | Valid |
| 1D | reg<237:232> | Matrix OUT | PIN5 Output Enable | Valid | Valid |
| | reg<239:238> | Reserved | | Valid | Valid |
| 1E | reg<245:240> | Matrix OUT | PIN6 Digital Output Source | Valid | Valid |
| | reg<247:246> | Reserved | | Valid | Valid |
| 1F | reg<253:248> | Matrix OUT | PIN7 Digital Output Source | Valid | Valid |
| | reg<255:254> | Reserved | | Valid | Valid |
| 20 | reg<261:256> | Matrix OUT | PIN7 Output Enable | Valid | Valid |
| | reg<263:262> | Reserved | | Valid | Valid |
| 21 | reg<269:264> | Matrix OUT | PIN8 Digital Output Source (SCL with VI/Input & NMOS open-drain) | Valid | Valid |
| | reg<271:270> | Reserved | | Valid | Valid |
| 22 | reg<277:272> | Matrix OUT | PIN9 Digital Output Source (SDA with VI/Input & NMOS open-drain) | Valid | Valid |
| | reg<279:278> | Reserved | | Valid | Valid |
| 23 | reg<285:280> | Matrix OUT | PIN10 Digital Output Source | Valid | Valid |
| | reg<287:286> | Reserved | | Valid | Valid |
| 24 | reg<293:288> | Matrix OUT | PIN10 Output Enable | Valid | Valid |
| | reg<295:294> | Reserved | | Valid | Valid |
| 25 | reg<301:296> | Matrix OUT | PIN12 Digital Output Source | Valid | Valid |
| | reg<303:302> | Reserved | | Valid | Valid |
| 26 | reg<309:304> | Matrix OUT | PIN13 Digital Output Source | Valid | Valid |
| | reg<311:310> | Reserved | | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 27 | reg<317:312> | Matrix OUT | PIN13 Output Enable | Valid | Valid |
| | reg<319:318> | Reserved | | Valid | Valid |
| 28 | reg<325:320> | Matrix OUT | PIN14 Digital Output Source | Valid | Valid |
| | reg<327:326> | Reserved | | Valid | Valid |
| 29 | reg<333:328> | Matrix OUT | PIN14 Output Enable | Valid | Valid |
| | reg<335:334> | Reserved | | Valid | Valid |
| 2A | reg<341:336> | Matrix OUT | PIN15 Digital Output Source | Valid | Valid |
| | reg<343:342> | Reserved | | Valid | Valid |
| 2B | reg<349:344> | Matrix OUT | PIN16 Digital Output Source | Valid | Valid |
| | reg<351:350> | Reserved | | Valid | Valid |
| 2C | reg<357:352> | Matrix OUT | PIN16 Output Enable | Valid | Valid |
| | reg<359:358> | Reserved | | Valid | Valid |
| 2D | reg<365:360> | Matrix OUT | PIN17 Digital Output Source | Valid | Valid |
| | reg<367:366> | Reserved | | Valid | Valid |
| 2E | reg<373:368> | Matrix OUT | PIN18 Digital Output Source | Valid | Valid |
| | reg<375:374> | Reserved | | Valid | Valid |
| 2F | reg<381:376> | Matrix OUT | PIN18 Output Enable | Valid | Valid |
| | reg<383:382> | Reserved | | Valid | Valid |
| 30 | reg<389:384> | Matrix OUT | PIN19 Digital Output Source | Valid | Valid |
| | reg<391:390> | Reserved | | Valid | Valid |
| 31 | reg<397:392> | Matrix OUT | PIN19 Output Enable | Valid | Valid |
| | reg<399:398> | Reserved | | Valid | Valid |
| 32 | reg<405:400> | Matrix OUT | PIN20 Digital Output Source | Valid | Valid |
| | reg<407:406> | Reserved | | Valid | Valid |
| 33 | reg<413:408> | Matrix OUT | ACMP0 PDB (Power Down) | Valid | Valid |
| | reg<415:414> | Reserved | | Valid | Valid |
| 34 | reg<421:416> | Matrix OUT | ACMP1 PDB (Power Down) | Valid | Valid |
| | reg<423:422> | Reserved | | Valid | Valid |
| 35 | reg<429:424> | Matrix OUT | ACMP2 PDB (Power Down) | Valid | Valid |
| | reg<431:430> | Reserved | | Valid | Valid |
| 36 | reg<437:432> | Matrix OUT | ACMP3 PDB (Power Down) | Valid | Valid |
| | reg<439:438> | Reserved | | Valid | Valid |
| 37 | reg<445:440> | Matrix OUT | Input of Filter_0 with fixed time edge detector | Valid | Valid |
| | reg<447:446> | Reserved | | Valid | Valid |
| 38 | reg<453:448> | Matrix OUT | Input of Filter_1 with fixed time edge detector | Valid | Valid |
| | reg<455:454> | Reserved | | Valid | Valid |
| 39 | reg<461:456> | Matrix OUT | Input of Programmable Delay & Edge Detector | Valid | Valid |
| | reg<463:462> | Reserved | | Valid | Valid |
| 3A | reg<469:464> | Matrix OUT | OSC 25KHz/2MHz PDB (Power Down) | Valid | Valid |
| | reg<471:470> | Reserved | | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 3B | reg<477:472> | Matrix OUT | OSC 25MHz PDB (Power Down) | Valid | Valid |
| | reg<479:478> | Reserved | | Valid | Valid |
| 3C | reg<485:480> | Matrix OUT | IN0 of LUT2_0 or Clock Input of DFF0 | Valid | Valid |
| | reg<487:486> | Reserved | | Valid | Valid |
| 3D | reg<493:488> | Matrix OUT | IN1 of LUT2_0 or Data Input of DFF0 | Valid | Valid |
| | reg<495:494> | Reserved | | Valid | Valid |
| 3E | reg<501:496> | Matrix OUT | IN0 of LUT2_1 or Clock Input of DFF1 | Valid | Valid |
| | reg<503:502> | Reserved | | Valid | Valid |
| 3F | reg<509:504> | Matrix OUT | IN1 of LUT2_1 or Data Input of DFF1 | Valid | Valid |
| | reg<511:510> | Reserved | | Valid | Valid |
| 40 | reg<517:512> | Matrix OUT | IN0 of LUT2_2 or Clock Input of DFF2 | Valid | Valid |
| | reg<519:518> | Reserved | | Valid | Valid |
| 41 | reg<525:520> | Matrix OUT | IN1 of LUT2_2 or Data Input of DFF2 | Valid | Valid |
| | reg<527:526> | Reserved | | Valid | Valid |
| 42 | reg<533:528> | Matrix OUT | IN0 of LUT2_3 or Clock Input of PGEN | Valid | Valid |
| | reg<535:534> | Reserved | | Valid | Valid |
| 43 | reg<541:536> | Matrix OUT | IN1 of LUT2_3 or RSTB of PGEN | Valid | Valid |
| | reg<543:542> | Reserved | | Valid | Valid |
| 44 | reg<549:544> | Matrix OUT | IN0 of LUT3_0 or Clock Input of DFF3 | Valid | Valid |
| | reg<551:550> | Reserved | | Valid | Valid |
| 45 | reg<557:552> | Matrix OUT | IN1 of LUT3_0 or Data Input of DFF3 | Valid | Valid |
| | reg<559:558> | Reserved | | Valid | Valid |
| 46 | reg<565:560> | Matrix OUT | IN2 of LUT3_0 or RSTB (SETB) of DFF3 | Valid | Valid |
| | reg<567:566> | Reserved | | Valid | Valid |
| 47 | reg<573:568> | Matrix OUT | IN0 of LUT3_1 or Clock Input of DFF4 | Valid | Valid |
| | reg<575:574> | Reserved | | Valid | Valid |
| 48 | reg<581:576> | Matrix OUT | IN1 of LUT3_1 or Data Input of DFF4 | Valid | Valid |
| | reg<583:582> | Reserved | | Valid | Valid |
| 49 | reg<589:584> | Matrix OUT | IN2 of LUT3_1 or RSTB (SETB) of DFF4 | Valid | Valid |
| | reg<591:590> | Reserved | | Valid | Valid |
| 4A | reg<597:592> | Matrix OUT | IN0 of LUT3_2 or Clock Input of DFF5 | Valid | Valid |
| | reg<599:598> | Reserved | | Valid | Valid |
| 4B | reg<605:600> | Matrix OUT | IN1 of LUT3_2 or Data Input of DFF5 | Valid | Valid |
| | reg<607:606> | Reserved | | Valid | Valid |
| 4C | reg<613:608> | Matrix OUT | IN2 of LUT3_2 or RSTB (SETB) of DFF5 | Valid | Valid |
| | reg<615:614> | Reserved | | Valid | Valid |
| 4D | reg<621:616> | Matrix OUT | IN0 of LUT3_3 or Clock Input of DFF6 | Valid | Valid |
| | reg<623:622> | Reserved | | Valid | Valid |
| 4E | reg<629:624> | Matrix OUT | IN1 of LUT3_3 or Data Input of DFF6 | Valid | Valid |
| | reg<631:630> | Reserved | | Valid | Valid |
| 4F | reg<637:632> | Matrix OUT | IN2 of LUT3_3 or RSTB (SETB) of DFF6 | Valid | Valid |
| | reg<639:638> | Reserved | | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 50 | reg<645:640> | Matrix OUT | IN0 of LUT3_4 or Clock Input of DFF7 | Valid | Valid |
| | reg<647:646> | Reserved | | Valid | Valid |
| 51 | reg<653:648> | Matrix OUT | IN1 of LUT3_4 or Data Input of DFF7 | Valid | Valid |
| | reg<655:654> | Reserved | | Valid | Valid |
| 52 | reg<661:656> | Matrix OUT | IN2 of LUT3_4 or RSTB (SETB) of DFF7 | Valid | Valid |
| | reg<663:662> | Reserved | | Valid | Valid |
| 53 | reg<669:664> | Matrix OUT | IN0 of LUT3_5 or Delay2 Input (or Counter2 RST Input) | Valid | Valid |
| | reg<671:670> | Reserved | | Valid | Valid |
| 54 | reg<677:672> | Matrix OUT | IN1 of LUT3_5 or External Clock Input of Delay2 (or Counter2) | Valid | Valid |
| | reg<679:678> | Reserved | | Valid | Valid |
| 55 | reg<685:680> | Matrix OUT | IN2 of LUT3_5 | Valid | Valid |
| | reg<687:686> | Reserved | | Valid | Valid |
| 56 | reg<693:688> | Matrix OUT | IN0 of LUT3_6 or Delay3 Input (or Counter3 RST Input) | Valid | Valid |
| | reg<695:694> | Reserved | | Valid | Valid |
| 57 | reg<701:696> | Matrix OUT | IN1 of LUT3_6 or External Clock Input of Delay3 (or Counter3) | Valid | Valid |
| | reg<703:702> | Reserved | | Valid | Valid |
| 58 | reg 709:704> | Matrix OUT | IN2 of LUT3_6 | Valid | Valid |
| | reg<711:710> | Reserved | | Valid | Valid |
| 59 | reg<717:712> | Matrix OUT | IN0 of LUT3_7 or Delay4 Input (or Counter4 RST Input) | Valid | Valid |
| | reg<719:718> | Reserved | | Valid | Valid |
| 5A | reg<725:720> | Matrix OUT | IN1 of LUT3_7 or External Clock Input of Delay4 (or Counter4) | Valid | Valid |
| | reg<727:726> | Reserved | | Valid | Valid |
| 5B | reg<733:728> | Matrix OUT | IN2 of LUT3_7 | Valid | Valid |
| | reg<735:734> | Reserved | | Valid | Valid |
| 5C | reg<741:736> | Matrix OUT | IN0 of LUT3_8 or Delay5 Input (or Counter5 RST Input) | Valid | Valid |
| | reg<743:742> | Reserved | | Valid | Valid |
| 5D | reg<749:744> | Matrix OUT | IN1 of LUT3_8 or External Clock Input of Delay5 (or Counter5) | Valid | Valid |
| | reg<751:750> | Reserved | | Valid | Valid |
| 5E | reg<757:752> | Matrix OUT | IN2 of LUT3_8 | Valid | Valid |
| | reg<759:758> | Reserved | | Valid | Valid |
| 5F | reg<765:760> | Matrix OUT | IN0 of LUT3_9 or Delay6 Input (or Counter6 RST Input) | Valid | Valid |
| | reg<767:766> | Reserved | | Valid | Valid |
| 60 | reg<773:768> | Matrix OUT | IN1 of LUT3_9 or External Clock Input of Delay6 (or Counter6) | Valid | Valid |
| | reg<775:774> | Reserved | | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 61 | reg<781:776> | Matrix OUT | IN2 of LUT3_9 | Valid | Valid |
| | reg<783:782> | Reserved | | Valid | Valid |
| 62 | reg<789:784> | Matrix OUT | IN0 of LUT3_10 or Input of Pipe Delay | Valid | Valid |
| | reg<791:790> | Reserved | | Valid | Valid |
| 63 | reg<797:792> | Matrix OUT | IN1 of LUT3_10 or RSTB of Pipe Delay | Valid | Valid |
| | reg<799:798> | Reserved | | Valid | Valid |
| 64 | reg<805:800> | Matrix OUT | IN2 of LUT3_10 or Clock of Pipe Delay | Valid | Valid |
| | reg<807:806> | Reserved | | Valid | Valid |
| 65 | reg<813:808> | Matrix OUT | IN0 of LUT4_0 or Delay0 Input (or Counter0 RST/SET Input) | Valid | Valid |
| | reg<815:814> | Reserved | | Valid | Valid |
| 66 | reg<821:816> | Matrix OUT | IN1 of LUT4_0 or External Clock Input of Delay0 (or Counter0) | Valid | Valid |
| | reg<823:822> | Reserved | | Valid | Valid |
| 67 | reg<829:824> | Matrix OUT | IN2 of LUT4_0 or UP Input of FSM0 | Valid | Valid |
| | reg<831:830> | Reserved | | Valid | Valid |
| 68 | reg<837:832> | Matrix OUT | IN3 of LUT4_0 or KEEP Input of FSM0 | Valid | Valid |
| | reg<839:838> | Reserved | | Valid | Valid |
| 69 | reg<845:840> | Matrix OUT | IN0 of LUT4_1 or Delay1 Input (or Counter1 RST/SET Input) | Valid | Valid |
| | reg<847:846> | Reserved | | Valid | Valid |
| 6A | reg<853:848> | Matrix OUT | IN1 of LUT4_1 or External Clock Input of Delay1 (or Counter1) | Valid | Valid |
| | reg<855:854> | Reserved | | Valid | Valid |
| 6B | reg<861:856> | Matrix OUT | IN2 of LUT4_1 or UP Input of FSM1 | Valid | Valid |
| | reg<863:862> | Reserved | | Valid | Valid |
| 6C | reg<869:864> | Matrix OUT | IN3 of LUT4_1 or KEEP Input of FSM1 | Valid | Valid |
| | reg<871:870> | Reserved | | Valid | Valid |
| 6D | reg<877:872> | Matrix OUT | PD of either Temp-output with BG AND/OR crystal oscillator by reg<1268> | Valid | Valid |
| | reg<879:878> | Reserved | | Valid | Valid |
| 6E | reg<887:880> | Reserved | | Valid | Valid |
| 6F | reg<895:888> | Reserved | | Valid | Valid |
| 70 | reg<903:896> | Reserved | | Valid | Valid |
| 71 | reg<911:904> | Reserved | | Valid | Valid |
| 72 | reg<919:912> | Reserved | | Valid | Valid |
| 73 | reg<927:920> | Reserved | | Valid | Valid |
| 74 | reg<935:928> | Reserved | | Valid | Valid |
| 75 | reg<943:936> | Reserved | | Valid | Valid |
| 76 | reg<951:944> | Reserved | | Valid | Valid |
| 77 | reg<959:952> | Reserved | | Valid | Valid |
| 78 | reg<967:960> | Reserved | | Valid | Valid |
| 79 | reg<975:968> | Reserved | | Valid | Valid |
| 7A | reg<983:976> | Reserved | | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 7B | reg<991:984> | Reserved | | Valid | Valid |
| 7C | reg<999:992> | Reserved | | Valid | Valid |
| 7D | reg<1007:1000> | Reserved | | Valid | Valid |
| 7E | reg<1015:1008> | Reserved | | Valid | Valid |
| 7F | reg<1023:1016> | Reserved | | Valid | Valid |
| **PIN 2** | | | | | |
| 80 | reg<1024> | Reserved | | Valid | Valid |
| | reg<1025> | Reserved | | Valid | Valid |
| | reg<1027:1026> | Reserved | | Valid | Valid |
| | reg<1029:1028> | PIN2 Pull Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1031:1030> | PIN2 Mode Control | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Reserved | Valid | Valid |
| **PIN 3** | | | | | |
| 80 | reg<1032> | Reserved | | Valid | Valid |
| 81 | reg<1033> | PIN3 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1035:1034> | PIN3 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1037:1036> | PIN3 Mode Control (sig_pin3_oe=0) | 00: Digital Input without Schmitt Trigger,<br>01: Digital Input with Schmitt Trigger,<br>10: Low Voltage Digital Input<br>11: Reserved | Valid | Valid |
| | reg<1039:1038> | PIN3 Mode Control (sig_pin3_oe=1) | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X | Valid | Valid |
| **PIN 4** | | | | | |
| 82 | reg<1040> | Reserved | | Valid | Valid |
| | reg<1041> | PIN4 Driver Strength Selection | 0: 1X<br>1: 2X | Valid | Valid |
| | reg<1042> | PIN4 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1044:1043> | PIN4 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1047:1045> | PIN4 Mode Control | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved 100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Open Drain NMOS | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **PIN 5** | | | | | |
| 83 | reg<1048> | Reserved | | Valid | Valid |
| | reg<1049> | PIN5 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1051:1050> | PIN5 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1053:1052> | PIN5 Mode Control (sig_pin5_oe=0) | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Reserved | Valid | Valid |
| | reg<1055:1054> | PIN5 Mode Control (sig_pin5_oe=1) | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X | Valid | Valid |
| **PIN 6** | | | | | |
| 84 | reg<1056> | Reserved | | Valid | Valid |
| | reg<1057> | PIN6 Driver Strength Selection | 0: 1X<br>1: 2X | Valid | Valid |
| | reg<1058> | PIN6 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1060:1059> | PIN6 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1063:1061> | PIN6 Mode Control | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Analog Input/Output<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Analog Input & Open Drain | Valid | Valid |
| **PIN 7** | | | | | |
| 85 | reg<1064> | Reserved | | Valid | Valid |
| | reg<1065> | PIN7 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1067:1066> | PIN7 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1069:1068> | PIN7 Mode Control (sig_pin7_oe=0) | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output | Valid | Valid |
| | reg<1071:1070> | PIN7 Mode Control (sig_pin7_oe=1) | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **PIN 8** | | | | | |
| 86 | reg<1072> | Reserved | | Valid | Valid |
| | reg<1073> | PIN8 (or SCL) Driver Strength Selection | 0: 1X (I²C up to 400KHz)<br>1: 2X (I²C up to 1MHz) | Valid | Valid |
| | reg<1074> | Select SCL & Virtual Input 0 or PIN8 | 0: SCL & Virtual Input 0<br>1: PIN8 | Valid | Valid |
| | reg<1076:1075> | PIN8 (or SCL) Pull Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| 86 | reg<1079:1077> | PIN8 (or SCL) Mode Control | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger,<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Open Drain NMOS<br>101: Open Drain NMOS<br>110: Open Drain NMOS<br>111: Reserved | Valid | Valid |
| **PIN 9** | | | | | |
| 87 | reg<1080> | Reserved | | Valid | Valid |
| | reg<1081> | PIN9 (or SDA) Driver Strength Selection | 0: 1X (I²C up to 400KHz)<br>1: 2X (I²C up to 1MHz) | Valid | Valid |
| | reg<1082> | Select SDA & Virtual Input 1 or PIN9 | 0: SDA & Virtual Input 1<br>1: PIN9 | Valid | Valid |
| | reg<1084:1083> | PIN9 (or SDA) Pull Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1087:1085> | PIN9 (or SDA) Mode Control | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Open Drain NMOS<br>101: Open Drain NMOS<br>110: Open Drain NMOS<br>111: Reserved | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **PIN 10** | | | | | |
| 88 | reg<1088> | PIN10 Super Drive (4X, NMOS Open Drain) Selection | 0: Super Drive OFF<br>1: Super Drive ON (if sig_pin10_oe='1' & PIN10 Mode Control = '1X') | Valid | Valid |
| | reg<1089> | PIN10 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1091:1090> | PIN10 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1093:1092> | PIN10 Mode Control (sig_pin10_oe=0) | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output | Valid | Valid |
| | reg<1095:1094> | PIN10 Mode Control (sig_pin10_oe=1) | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X | Valid | Valid |
| **PIN 12** | | | | | |
| 89 | reg<1096> | PIN12 Super Drive (4X, NMOS Open Drain) Selection | 0: Super Drive OFF<br>1: Super Drive ON (if PIN12 Mode Control = '101') | Valid | Valid |
| | reg<1097> | PIN12 Driver Strength Selection | 0: 1X<br>1: 2X | Valid | Valid |
| 89 | reg<1098> | PIN12 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1100:1099> | PIN12 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1103:1101> | PIN12 Mode Control | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Analog Input/Output<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Analog Input & Open Drain | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **PIN 13** | | | | | |
| 8A | reg<1104> | Reserved | | Valid | Valid |
| | reg<1105> | PIN13 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1107:1106> | PIN13 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1109:1108> | PIN13 Mode Control (sig_pin13_oe=0) | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output | Valid | Valid |
| | reg<1111:1110> | PIN13 Mode Control (sig_pin13_oe=1) | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X | Valid | Valid |
| **PIN 14** | | | | | |
| 8B | reg<1112> | Reserved | | Valid | Valid |
| | reg<1113> | PIN14 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1115:1114> | PIN14 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1117:1116> | PIN14 Mode Control (sig_pin14_oe=0) | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output | Valid | Valid |
| | reg<1119:1118> | PIN14 Mode Control (sig_pin14_oe=1) | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X | Valid | Valid |
| **PIN 15** | | | | | |
| 8C | reg<:1120> | Reserved | | Valid | Valid |
| | reg<1121> | PIN15 Driver Strength Selection | 0: 1X<br>1: 2X | Valid | Valid |
| 8C | reg<1122> | PIN15 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1124:1123> | PIN15 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1127:1125> | PIN15 Mode Control | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Analog Input/Output<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Analog Input & Open Drain | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **PIN 16** | | | | | |
| 8D | reg<1128> | Reserved | | Valid | Valid |
| | reg<1129> | PIN16 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1131:1130> | PIN16 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1133:1132> | PIN16 Mode Control (sig_pin16_oe=0) | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Sel for XSOC (X2) | Valid | Valid |
| | reg<1135:1134> | PIN16 Mode Control (sig_pin16_oe=1) | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X | Valid | Valid |
| **PIN 17** | | | | | |
| 8E | reg<:1136> | X1 & X2 for crystal OSC enable | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1137> | PIN17 Driver Strength Selection | 0: 1X<br>1: 2X | Valid | Valid |
| | reg<1138> | PIN17 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1140:1139> | PIN17 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1143:1141> | PIN17 Mode Control | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Sel for XOSC (X1)<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Open Drain NMOS | Valid | Valid |
| **PIN 18** | | | | | |
| 8F | reg<1144> | Reserved | | Valid | Valid |
| 8F | reg<1145> | PIN18 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1147:1146> | PIN18 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1149:1148> | PIN18 Mode Control (sig_pin18_oe=0) | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output | Valid | Valid |
| | reg<1151:1150> | PIN18 Mode Control (sig_pin18_oe=1) | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **PIN 19** | | | | | |
| 90 | reg<1152> | Reserved | | Valid | Valid |
| | reg<1153> | PIN19 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1155:1154> | PIN19 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1157:1156> | PIN19 Mode Control (sig_pin19_oe=0) | 00: Digital Input without Schmitt Trigger<br>01: Digital Input with Schmitt Trigger<br>10: Low Voltage Digital Input<br>11: Analog Input/Output | Valid | Valid |
| | reg<1159:1158> | PIN19 Mode Control (sig_pin19_oe=1) | 00: Push Pull 1X<br>01: Push Pull 2X<br>10: Open Drain NMOS 1X<br>11: Open Drain NMOS 2X | Valid | Valid |
| **PIN 20** | | | | | |
| 91 | reg<1160> | Reserved | | Valid | Valid |
| | reg<1161> | PIN20 Driver Strength Selection | 0: 1X<br>1: 2X | Valid | Valid |
| | reg<1162> | PIN20 Pull Up/Down Resistor Selection | 0: Pull Down Resistor<br>1: Pull Up Resistor | Valid | Valid |
| | reg<1164:1163> | PIN20 Pull Up/Down Resistor Value Selection | 00: Floating<br>01: 10K<br>10: 100K<br>11: 1M | Valid | Valid |
| | reg<1167:1165> | PIN20 Mode Control | 000: Digital Input without Schmitt Trigger<br>001: Digital Input with Schmitt Trigger<br>010: Low Voltage Digital Input<br>011: Reserved<br>100: Push Pull<br>101: Open Drain NMOS<br>110: Open Drain PMOS<br>111: Open Drain NMOS | Valid | Valid |
| **ACMP1** | | | | | |
| 92 | reg<1168> | ACMP1 Positive Input Source Select PIN6 | 0: Disable<br>1: Enable | Valid | Valid |
| 92 | reg<1169> | ACMP1 Analog Buffer Enable (Max. BW 1MHz) | 0: Disable analog buffer<br>1: Enable analog buffer | Valid | Valid |
| | reg<1171:1170> | ACMP1 Hysteresis Enable | 00: 0mV<br>01: 25mV<br>10: 50mV,<br>11: 200mV<br>(01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50mV & 200mV hysteresis.) | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **ACMP0** | | | | | |
| 92 | reg<1172> | ACMP0 Positive Input Source Select VDD | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1173> | ACMP0 Analog Buffer Enable (Max. BW 1MHz) | 0: Disable analog buffer<br>1: Enable analog buffer | Valid | Valid |
| | reg<1175:1174> | ACMP0 Hysteresis Enable | 00: 0mV<br>01: 25mV<br>10: 50mV,<br>11: 200mV<br>(01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50mV & 200mV hysteresis.) | Valid | Valid |
| **ACMP3** | | | | | |
| 93 | reg<1176> | ACMP3 Positive Input Source Select PIN13 | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1177> | ACMP3 Positive Input Source Select PIN6 | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1179:1178> | ACMP3 Hysteresis Enable | 00: 0mV<br>01: 25mV<br>10: 50mV,<br>11: 200mV<br>(01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50mV & 200mV hysteresis.) | Valid | Valid |
| **ACMP2** | | | | | |
| 93 | reg<1180> | ACMP2 Positive Input Source Select PIN13 | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1182:1181> | ACMP2 Hysteresis Enable | 00: 0mV<br>01: 25mV<br>10: 50mV,<br>11: 200mV<br>(01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50mV & 200mV hysteresis.) | Valid | Valid |
| **ACMP1 100 uA Current Source Enable** | | | | | |
| 93 | reg<1183> | ACMP1 100uA Current Source Enable | 0: Disable<br>1: Enable | Valid | Valid |
| **LUT3_x Function Select** | | | | | |
| 94 | reg<1184> | LUT3_3 or DFF6 with RSTB/SETB Select | 0: LUT3_3<br>1: DFF6 with RSTB/SETB | Valid | Valid |
| | reg<1185> | LUT3_2 or DFF5 with RSTB/SETB Select | 0: LUT3_2<br>1: DFF5 with RSTB/SETB | Valid | Valid |
| | reg<1186> | LUT3_1 or DFF4 with RSTB/SETB Select | 0: LUT3_1<br>1: DFF4 with RSTB/SETB | Valid | Valid |
| | reg<1187> | LUT3_0 or DFF3 with RSTB/SETB Select (Two consecutive DFFs if reg<1471>=1 for SM) | 0: LUT3_0<br>1: DFF3 with RSTB/SETB | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **LUT2_x Function Select** | | | | | |
| 94 | reg<1188> | LUT2_3 or PGEN Select | 0: LUT2_3<br>1: PGEN | Valid | Valid |
| | reg<1189> | LUT2_2 or DFF2 Select | 0: LUT2_2<br>1: DFF2 | Valid | Valid |
| | reg<1190> | LUT2_1 or DFF1 Select | 0: LUT2_1<br>1: DFF1 | Valid | Valid |
| | reg<1191> | LUT2_0 or DFF0 Select | 0: LUT2_0<br>1: DFF0 | Valid | Valid |
| **LUT4_x Function Select** | | | | | |
| 95 | reg<1192> | LUT4_1 or DLY/CNT1(16bits) Select | 0: LUT4_1<br>1: DLY/CNT1(16bits) | Valid | Valid |
| | reg<1193> | LUT4_0 or DLY/CNT0(16bits) Select | 0: LUT4_0<br>1: DLY/CNT0(16bits) | Valid | Valid |
| **LUT3_x Function Select** | | | | | |
| 95 | reg<1194> | LUT3_9 or DLY/CNT6(8bits) Select | 0: LUT3_9<br>1: DLY/CNT6(8bits) | Valid | Valid |
| | reg<1195> | LUT3_8 or DLY/CNT5(8bits) Select | 0: LUT3_8<br>1: DLY/CNT5(8bits) | Valid | Valid |
| | reg<1196> | LUT3_7 or DLY/CNT4(8bits) Select | 0: LUT3_7<br>1: DLY/CNT4(8bits) | Valid | Valid |
| | reg<1197> | LUT3_6 or DLY/CNT3(8bits) Select | 0: LUT3_6<br>1: DLY/CNT3(8bits) | Valid | Valid |
| | reg<1198> | LUT3_5 or DLY/CNT2(8bits) Select | 0: LUT3_5<br>1: DLY/CNT2(8bits) | Valid | Valid |
| | reg<1199> | LUT3_4 or DFF7 with RSTB/SETB Select | 0: LUT3_4<br>1: DFF7 with RSTB/SETB | Valid | Valid |
| **LUT2_1 / DFF1** | | | | | |
| 96 | reg<1200> | LUT2_1 <0> | | Valid | Valid |
| | reg<1201> | LUT2_1 <1> / DFF1 Initial Polarity Select | 0: Low<br>1: High | Valid | Valid |
| | reg<1202> | LUT2_1 <2> / DFF1 Output Select | 0: Q output<br>1: QB output | Valid | Valid |
| | reg<1203> | LUT2_1 <3> / DFF1 or Latch Select | 0: DFF function<br>1: Latch function | Valid | Valid |
| **LUT2_0 / DFF0** | | | | | |
| 96 | reg<1204> | LUT2_0 <0> | | Valid | Valid |
| 96 | reg<1205> | LUT2_0 <1> / DFF0 Initial Polarity Select | 0: Low<br>1: High | Valid | Valid |
| | reg<1206> | LUT2_0 <2> / DFF0 Output Select | 0: Q output<br>1: QB output | Valid | Valid |
| | reg<1207> | LUT2_0 <3> / DFF0 or Latch Select | 0: DFF function<br>1: Latch function | Valid | Valid |
| **LUT2_3 / PGEN** | | | | | |
| 97 | reg<1211:1208> | LUT2_3<3:0> or PGEN 4bit counter data<3:0> | | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **LUT2_2 / DFF2** | | | | | |
| 97 | reg<1212> | LUT2_2 <0> | | Valid | Valid |
| | reg<1213> | LUT2_2 <1> / DFF2 Initial Polarity Select | 0: Low<br>1: High | Valid | Valid |
| | reg<1214> | LUT2_2 <2> / DFF2 Output Select | 0: Q output<br>1: QB output | Valid | Valid |
| | reg<1215> | LUT2_2 <3> / DFF2 or Latch Select | 0: DFF function<br>1: Latch function | Valid | Valid |
| **LUT3_0 / DFF3** | | | | | |
| 98 | reg<1219:1216> | LUT3_0 <3:0> | | Valid | Valid |
| | reg<1220> | LUT3_0 <4> / DFF3 Initial Polarity Select | 0: Low<br>1: High | Valid | Valid |
| | reg<1221> | LUT3_0 <5> / DFF3 RSTB or SETB Select | 0: RSTB from Matrix Output<br>1: SETB from Matrix Output | Valid | Valid |
| | reg<1222> | LUT3_0 <6> / DFF3 Output Select | 0: Q output<br>1: QB output | Valid | Valid |
| | reg<1223> | LUT3_0 <7> / DFF3 or Latch Select | 0: DFF function<br>1: Latch function | Valid | Valid |
| **LUT3_1 / DFF4** | | | | | |
| 99 | reg<1227:1224> | LUT3_1 <3:0> | | Valid | Valid |
| | reg<1228> | LUT3_1 <4> / DFF4 Initial Polarity Select | 0: Low<br>1: High | Valid | Valid |
| | reg<1229> | LUT3_1 <5> / DFF4 RSTB or SETB Select | 0: RSTB from Matrix Output<br>1: SETB from Matrix Output | Valid | Valid |
| | reg<1230> | LUT3_1 <6> / DFF4 Output Select | 0: Q output<br>1: QB output | Valid | Valid |
| | reg<1231> | LUT3_1 <7> / DFF4 or Latch Select | 0: DFF function<br>1: Latch function | Valid | Valid |
| **LUT3_2 / DFF5** | | | | | |
| 9A | reg<1235:1232> | LUT3_2 <3:0> | | Valid | Valid |
| | reg<1236> | LUT3_2 <4> / DFF5 Initial Polarity Select | 0: Low<br>1: High | Valid | Valid |
| | reg<1237> | LUT3_2 <5> / DFF5 RSTB or SETB Select | 0: RSTB from Matrix Output<br>1: SETB from Matrix Output | Valid | Valid |
| | reg<1238> | LUT3_2 <6> / DFF5 Output Select | 0: Q output<br>1: QB output | Valid | Valid |
| 9A | reg<1239> | LUT3_2 <7> / DFF5 or Latch Select | 0: DFF function<br>1: Latch function | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **LUT3_3 / DFF6** | | | | | |
| 9B | reg<1243:1240> | LUT3_3 <3:0> | | Valid | Valid |
| | reg<1244> | LUT3_3 <4> / DFF6 Initial Polarity Select | 0: Low<br>1: High | Valid | Valid |
| | reg<1245> | LUT3_3 <5> / DFF6 RSTB or SETB Select | 0: RSTB from Matrix Output<br>1: SETB from Matrix Output | Valid | Valid |
| | reg<1246> | LUT3_3 <6> / DFF6 Output Select | 0: Q output<br>1: QB output | Valid | Valid |
| | reg<1247> | LUT3_3 <7> / DFF6 or Latch Select | 0: DFF function<br>1: Latch function | Valid | Valid |
| **LUT3_4 / DFF7** | | | | | |
| 9C | reg<1251:1248> | LUT3_4 <3:0> | | Valid | Valid |
| | reg<1252> | LUT3_4 <4> / DFF7 Initial Polarity Select | 0: Low<br>1: High | Valid | Valid |
| | reg<1253> | LUT3_4 <5> / DFF7 RSTB or SETB Select | 0: RSTB from Matrix Output<br>1: SETB from Matrix Output | Valid | Valid |
| | reg<1254> | LUT3_4 <6> / DFF7 Output Select | 0: Q output<br>1: QB output | Valid | Valid |
| | reg<1255> | LUT3_4 <7> / DFF7 or Latch Select | 0: DFF function<br>1: Latch function | Valid | Valid |
| **LUT3_10 / Pipe Delay** | | | | | |
| 9D | reg<1259:1256> | LUT3_10 <3:0> / Pipe Delay OUT0 Select | | Valid | Valid |
| | reg<1263:1260> | LUT3_10 <7:4> / Pipe Delay OUT1 Select | | Valid | Valid |
| 9E | reg<1265:1264> | Select the Edge Mode of Programmable Delay & Edge Detector | 00: Rising Edge Detector<br>01: Falling Edge Detector<br>10: Both Edge Detector<br>11: Both Edge Delay | Valid | Valid |
| | reg<1267:1266> | Delay Value Select for Programmable Delay & Edge Detector (VDD=3.3V, typical) | 00: 125ns<br>01: 250ns<br>10: 375ns<br>11: 500ns | Valid | Valid |
| | reg<1269:1268> | Power down enable between temp output and crystal oscillator | 00: No matrix PD<br>01: matrix PD for crystal oscillator<br>10: matrix PD for temp sensor<br>11: matrix PD for both xosc & temp sensor | Valid | Valid |
| | reg<1270> | LUT3_10 or Pipe Delay Select | 0: LUT3_10<br>1: Pipe Delay | Valid | Valid |
| | reg<1271> | Pipe Delay OUT1 Polarity Select | 0: Non-inverted<br>1: Inverted | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **DLY/CNT2** | | | | | |
| 9F | reg<1273:1272> | DLY2 Mode Select or Asynchronous CNT2 Reset | 00: On both Falling and Rising Edges (for Delay & Counter Reset)<br>01: on Falling Edge only (for Delay & Counter Reset)<br>10: on Rising Edge only (for Delay & Counter Reset)<br>11: No Delay on either Falling or Rising Edges / High Level Reset | Valid | Valid |
| | reg<1276:1274> | DLY/CNT2 Clock Source Select | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter1 Overflow | Valid | Valid |
| | reg<1277> | DLY/CNT2 Output Selection if DLY/CNT2 Mode Selection is "11". | 0: Default Output<br>1: Edge Detector Output | Valid | Valid |
| | reg<1279:1278> | DLY/CNT2 Mode Selection | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode | Valid | Valid |
| **DLY/CNT3** | | | | | |
| A0 | reg<1281:1280> | DLY3 Mode Select or Asynchronous CNT3 Reset | 00: On both Falling and Rising Edges (for Delay & Counter Reset)<br>01: on Falling Edge only (for Delay & Counter Reset)<br>10: on Rising Edge only (for Delay & Counter Reset)<br>11: No Delay on either Falling or Rising Edges / High Level Reset | Valid | Valid |
| | reg<1284:1282> | DLY/CNT3 Clock Source Select | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter2 Overflow | Valid | Valid |
| | reg<1285> | DLY/CNT3 Output Selection if DLY/CNT3 Mode Selection is "11". | 0: Default Output<br>1: Edge Detector Output | Valid | Valid |
| | reg<1287:1286> | DLY/CNT3 Mode Selection | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **DLY/CNT4** | | | | | |
| A1 | reg<1289:1288> | DLY4 Mode Select or Asynchronous CNT4 Reset | 00: On both Falling and Rising Edges (for Delay & Counter Reset)<br>01: on Falling Edge only (for Delay & Counter Reset)<br>10: on Rising Edge only (for Delay & Counter Reset)<br>11: No Delay on either Falling or Rising Edges / High Level Reset | Valid | Valid |
| | reg<1292:1290> | DLY/CNT4 Clock Source Select | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter3 Overflow | Valid | Valid |
| | reg<1293> | DLY/CNT4 Output Selection if DLY/CNT4 Mode Selection is "11". | 0: Default Output<br>1: Edge Detector Output | Valid | Valid |
| | reg<1295:1294> | DLY/CNT4 Mode Selection | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode | Valid | Valid |
| **DLY/CNT5** | | | | | |
| A2 | reg<1297:1296> | DLY5 Mode Select or Asynchronous CNT5 Reset | 00: On both Falling and Rising Edges (for Delay & Counter Reset)<br>01: on Falling Edge only (for Delay & Counter Reset)<br>10: on Rising Edge only (for Delay & Counter Reset)<br>11: No Delay on either Falling or Rising Edges / High Level Reset | Valid | Valid |
| | reg<1300:1298> | DLY/CNT5 Clock Source Select | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter4 Overflow | Valid | Valid |
| | reg<1301> | DLY/CNT5 Output Selection if DLY/CNT5 Mode Selection is "11". | 0: Default Output<br>1: Edge Detector Output | Valid | Valid |
| | reg<1303:1302> | DLY/CNT5 Mode Selection | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **DLY/CNT6** | | | | | |
| A3 | reg<1305:1304> | DLY6 Mode Select or Asynchronous CNT6 Reset | 00: On both Falling and Rising Edges (for Delay & Counter Reset)<br>01: on Falling Edge only (for Delay & Counter Reset)<br>10: on Rising Edge only (for Delay & Counter Reset)<br>11: No Delay on either Falling or Rising Edges / High Level Reset | Valid | Valid |
| | reg<1308:1306> | DLY/CNT6 Clock Source Select | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12, 011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter5 Overflow | Valid | Valid |
| | reg<1309> | DLY/CNT6 Output Selection if DLY/CNT6 Mode Selection is "11". | 0: Default Output<br>1: Edge Detector Output | Valid | Valid |
| | reg<1311:1310> | DLY/CNT6 Mode Selection | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode | Valid | Valid |
| **DLY/CNT0** | | | | | |
| A4 | reg<1313:1312> | DLY0 Mode Select or Asynchronous CNT0 Reset (16bits) | 00: On both Falling and Rising Edges (for Delay & Counter Reset)<br>01: on Falling Edge only (for Delay & Counter Reset)<br>10: on Rising Edge only (for Delay & Counter Reset)<br>11: No Delay on either Falling or Rising Edges / High Level Reset | Valid | Valid |
| | reg<1316:1314> | DLY/CNT0 Clock Source Select (16bits) | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter6 Overflow | Valid | Valid |
| | reg<1317> | CNT0/FSM0's Q are Set to data or Reset to 0s Selection (16bits) | 0: Reset to 0s<br>1: Set to data (Reg<1583:1576, 1591:1584>) | Valid | Valid |
| | reg<1319:1318> | DLY/CNT0 Mode Selection (16bits) | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **DLY/CNT1** | | | | | |
| A5 | reg<1321:1320> | DLY1 Mode Select or Asynchronous CNT1 Reset (16bits) | 00: On both Falling and Rising Edges (for Delay & Counter Reset)<br>01: on Falling Edge only (for Delay & Counter Reset)<br>10: on Rising Edge only (for Delay & Counter Reset)<br>11: No Delay on either Falling or Rising Edges / High Level Reset | Valid | Valid |
| | reg<1324:1322> | DLY/CNT1 Clock Source Select (16bits) | 000: Internal OSC clock<br>001: OSC/4<br>010: OSC/12<br>011: OSC/24<br>100: OSC/64<br>101: 25MHz OSC clock<br>110: External Clock<br>111: Counter0 Overflow | Valid | Valid |
| | reg<1325> | CNT1/FSM1's Q are Set to data or Reset to 0s Selection (16bits) | 0: Reset to 0s<br>1: Set to data (Reg<1599:1592, 1607:1600>) | Valid | Valid |
| | reg<1327:1326> | DLY/CNT1 Mode Selection (16bits) | 00: Delay mode<br>01: One Shot<br>10: Freq. Detect<br>11: Counter mode | Valid | Valid |
| **DLY/CNTx One-Shot / Freq. Detect Output Polarity** | | | | | |
| A6 | reg<1328> | Reserved | | Valid | Valid |
| | reg<1329> | Select the Polarity of DLY/CNT6's One Shot / Freq. Detect Output | 0: Default Output<br>1: Inverted Output | Valid | Valid |
| | reg<1330> | Select the Polarity of DLY/CNT5's One Shot / Freq. Detect Output | 0: Default Output<br>1: Inverted Output | Valid | Valid |
| | reg<1331> | Select the Polarity of DLY/CNT4's One Shot / Freq. Detect Output | 0: Default Output<br>1: Inverted Output | Valid | Valid |
| | reg<1332> | Select the Polarity of DLY/CNT3's One Shot / Freq. Detect Output | 0: Default Output<br>1: Inverted Output | Valid | Valid |
| | reg<1333> | Select the Polarity of DLY/CNT2's One Shot / Freq. Detect Output | 0: Default Output<br>1: Inverted Output | Valid | Valid |
| | reg<1334> | Select the Polarity of DLY/CNT1's One Shot / Freq. Detect Output | 0: Default Output<br>1: Inverted Output | Valid | Valid |
| | reg<1335> | Select the Polarity of DLY/CNT0's One Shot / Freq. Detect Output | 0: Default Output<br>1: Inverted Output | Valid | Valid |
| **Oscillator** | | | | | |
| A7 | reg<1337:1336> | OSC Clock Pre-divider for 25MHz | 00: Div1<br>01: Div2<br>10: Div4<br>11: Div8 | Valid | Valid |
| | reg<1338> | OSC Fast Start-Up Enable for 25KHz/2MHz | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1340:1339> | OSC Clock Pre-divider for 25KHz/2MHz | 00: Div1<br>01: Div2<br>10: Div4<br>11: Div8 | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| A7 | reg<1341> | Force 25MHz Oscillator ON | 0: Auto Power ON (If any CNT/DLY use 25MHz source)<br>1: Force Power ON | Valid | Valid |
| | reg<1342> | Oscillator (25KHz: Ring OSC, 2M: RC-OSC) Select | 0: 25KHz Ring OSC<br>1: 2MHz RC-OSC | Valid | Valid |
| | reg<1343> | Force 25KHz/2MHz Oscillator ON | 0: Auto Power ON (if any CNT/DLY use 25K/2MHz source)<br>1: Force Power ON | Valid | Valid |
| A8 | reg<1346:1344> | Internal OSC 25KHz/2MHz Frequency Divider Control for matrix input <28> | 000: OSC/1<br>001: OSC/2<br>010: OSC/3<br>011: OSC/4<br>100: OSC/8<br>101: OSC/12<br>110: OSC/24<br>111: OSC/64 | Valid | Valid |
| | reg<1349:1347> | Internal OSC 25KHz/2MHz Frequency Divider Control for matrix input <27> | 000: OSC/1<br>001: OSC/2<br>010: OSC/3<br>011: OSC/4<br>100: OSC/8<br>101: OSC/12<br>110: OSC/24<br>111: OSC/64 | Valid | Valid |
| | reg<1350> | OSC Clock 25KHz/2MHz to matrix input <28> enable | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1351> | OSC Clock 25KHz/2MHz to matrix input <27> enable | 0: Disable<br>1: Enable | Valid | Valid |
| A9 | reg<1354:1352> | ASM_reg_init<2:0> for ASM state default setup bits | | Valid | Valid |
| | reg<1355> | External oscillator pin selection for 25KHz/2MHz | 0: PIN20<br>1: PIN18 | Valid | Valid |
| | reg<1356> | OSC Clock 25 MHz to matrix input <29> enable | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1357> | External Clock Source Select instead of 25MHz | 0: Internal Oscillator<br>1: External Clock from Pin17 | Valid | Valid |
| | reg<1358> | External Clock Source Select instead of 25KHz/2MHz | 0: Internal Oscillator<br>1: External Clock from Pin18 or Pin 20 | Valid | Valid |
| | reg<1359> | Reserved | | Valid | Valid |
| ASM 8-to-1 MUX's 3 selection bits | | | | | |
| AA | reg<1362:1360> | ASM_state0_dec8x1_EN1 | | Valid | Valid |
| | reg<1363> | Reserved | | Valid | Valid |
| | reg<1366:1364> | ASM_state0_dec8x1_EN0 | | Valid | Valid |
| | reg<1367> | Reserved | | Valid | Valid |
| AB | reg<1370:1368> | ASM_state1_dec8x1_EN0 | | Valid | Valid |
| | reg<1371> | Reserved | | Valid | Valid |
| | reg<1374:1372> | ASM_state0_dec8x1_EN2 | | Valid | Valid |
| | reg<1375> | Reserved | | Valid | Valid |
| AC | reg<1378:1376> | ASM_state1_dec8x1_EN2 | | Valid | Valid |
| | reg<1379> | Reserved | | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| AC | reg<1382:1380> | ASM_state1_dec8x1_EN1 | | Valid | Valid |
| | reg<1383> | Reserved | | Valid | Valid |
| AD | reg<1386:1384> | ASM_state2_dec8x1_EN1 | | Valid | Valid |
| | reg<1387> | Reserved | | Valid | Valid |
| | reg<1390:1388> | ASM_state2_dec8x1_EN0 | | Valid | Valid |
| | reg<1391> | Reserved | | Valid | Valid |
| AE | reg<1394:1392> | ASM_state3_dec8x1_EN0 | | Valid | Valid |
| | reg<1395> | Reserved | | Valid | Valid |
| | reg<1398:1396> | ASM_state2_dec8x1_EN2 | | Valid | Valid |
| | reg<1399> | Reserved | | Valid | Valid |
| AF | reg<1402:1400> | ASM_state3_dec8x1_EN2 | | Valid | Valid |
| | reg<1403> | Reserved | | Valid | Valid |
| | reg<1406:1404> | ASM_state3_dec8x1_EN1 | | Valid | Valid |
| | reg<1407> | Reserved | | Valid | Valid |
| B0 | reg<1410:1408> | ASM_state4_dec8x1_EN1 | | Valid | Valid |
| | reg<1411> | Reserved | | Valid | Valid |
| | reg<1414:1412> | ASM_state4_dec8x1_EN0 | | Valid | Valid |
| | reg<1415> | Reserved | | Valid | Valid |
| B1 | reg<1418:1416> | ASM_state5_dec8x1_EN0 | | Valid | Valid |
| | reg<1419> | Reserved | | Valid | Valid |
| | reg<1422:1420> | ASM_state4_dec8x1_EN2 | | Valid | Valid |
| | reg<1423> | Reserved | | Valid | Valid |
| B2 | reg<1426:1424> | ASM_state5_dec8x1_EN2 | | Valid | Valid |
| | reg<1427> | Reserved | | Valid | Valid |
| | reg<1430:1428> | ASM_state5_dec8x1_EN1 | | Valid | Valid |
| | reg<1431> | Reserved | | Valid | Valid |
| B3 | reg<1434:1432> | ASM_state6_dec8x1_EN1 | | Valid | Valid |
| | reg<1435> | Reserved | | Valid | Valid |
| | reg<1438:1436> | ASM_state6_dec8x1_EN0 | | Valid | Valid |
| | reg<1439> | Reserved | | Valid | Valid |
| B4 | reg<1442:1440> | ASM_state7_dec8x1_EN0 | | Valid | Valid |
| | reg<1443> | Reserved | | Valid | Valid |
| | reg<1446:1444> | ASM_state6_dec8x1_EN2 | | Valid | Valid |
| | reg<1447> | Reserved | | Valid | Valid |
| B5 | reg<1450:1448> | ASM_state7_dec8x1_EN2 | | Valid | Valid |
| | reg<1451> | Reserved | | Valid | Valid |
| | reg<1454:1452> | ASM_state7_dec8x1_EN1 | | Valid | Valid |
| | reg<1455> | Reserved | | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **Filter / Edge Detector** | | | | | |
| B6 | reg<1457:1456> | Select the edge mode of Edge Detector_1 | 00: Rising Edge<br>01: Falling Edge<br>10: Both Edge<br>11: Delay | Valid | Valid |
| | reg<1458> | Filter_1/Edge Detector_1 output Polarity Select | 0: Filter_1 output<br>1: Filter_1 output inverted | Valid | Valid |
| | reg<1459> | Filter_1or Edge Detector_1 Select<br>(Typ. 30 ns @VDD=3.3 V) | 0: Filter_1<br>1: Edge Detector_1 | Valid | Valid |
| | reg<1461:1460> | Select the edge mode of Edge Detector_0 | 00: Rising Edge<br>01: Falling Edge<br>10: Both Edge<br>11: Delay | Valid | Valid |
| | reg<1462> | Filter_0/Edge Detector_0 output Polarity Select | 0: Filter_0 output<br>1: Filter_0 output inverted | Valid | Valid |
| | reg<1463> | Filter_0 or Edge Detector_0 Select<br>(Typ. 47 ns @VDD=3.3 V) | 0: Filter_0<br>1: Edge Detector_0 | Valid | Valid |
| **VREF / Bandgap** | | | | | |
| B7 | reg<1464> | Reserved | | Valid | Valid |
| | reg<1465> | Reserved | | Valid | Valid |
| | reg<1466> | Bandgap OK for ACMP Output Delay Time Select, the start Time is "resetb_core go to High" | 0: 500 uS<br>1: 50 uS | Valid | Valid |
| | reg<1467> | Reserved | | Valid | Valid |
| | reg<1468> | Reserved | | Valid | Valid |
| | reg<1469> | Reserved | | Valid | Valid |
| | reg<1470> | Reserved | | Valid | Valid |
| | reg<1471> | Two consecutive DFFs enable for SM | 0: Disable<br>1: Enable | Valid | Valid |
| B8 | reg<1474:1472> | Power divider (VDD/3, VDD/4) ON/OFF | 0XX: Power divider off (if there is no use of VDD/3, VDD/4 @ ACMP negative in)<br>100: Reservedb<br>X10: Reserved<br>XX1:Reserved | Valid | Valid |
| | reg<1475> | VDD Bypass Enable when device power is 1.8 V | 0: Regulator Auto ON<br>1: Regulator OFF (VDD Bypass) | Valid | Valid |
| | reg<1476> | Force Bandgap ON | 0: Auto-Mode<br>1: Enable (if chip is Power Down, the Bandgap will Power Down even if it is Set to 1). | Valid | Valid |
| | reg<1477> | NVM Power Down | 0: None (Or Programming Enable)<br>1: Power Down (Or Programming Disable) | Valid | Valid |
| | reg<1478> | Reserved | | Valid | Valid |
| | reg<1479> | GPIO Quick Charge Enable | 0: Disable<br>1: Enable | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| B9 | reg<1482:1480> | VREF2 Output Source Select | 000: ACMP2 VREF<br>001: ACMP3 VREF<br>100: VDD/2<br>101: VDD/3<br>110: VDD/4<br>111: Hi-Z | Valid | Valid |
| | reg<1483> | VREF2 Output Active Buffer Control | 0: Disabled (Bypass Active Buffer)<br>1: Enabled | Valid | Valid |
| | reg<1486:1484> | VREF1 Output Source Select | 000: ACMP0 VREF<br>001: ACMP1 VREF<br>100: VDD/2<br>101: VDD/3<br>110: VDD/4<br>111: Hi-Z | Valid | Valid |
| | reg<1487> | VREF1 Output Active Buffer Control | 0: Disabled (Bypass Active Buffer)<br>1: Enabled | Valid | Valid |
| BA | reg<1488> | Reserved | | Valid | Valid |
| | reg<1489> | Wake time Selection in Wake Sleep Mode | 0: short wake time<br>1: normal wake time | Valid | Valid |
| | reg<1490> | ACMP0 Wake & Sleep function Enable | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1491> | ACMP1 Wake & Sleep function Enable | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1492> | ACMP2 Wake & Sleep function Enable | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1493> | ACMP3 Wake & Sleep function Enable | 0: Disable<br>1: Enable | Valid | Valid |
| | reg<1494> | Wake Sleep Output State When WS Oscillator is Power Down if DLY/CNT0 Mode Selection is "11" | 0: Low<br>1: High | Valid | Valid |
| | reg<1495> | Wake Sleep Ratio Control Mode Selection if DLY/CNT0 Mode Selection is "11" | 0: Default Mode<br>1: Wake Sleep Ratio Control Mode | Valid | Valid |
| BB | reg<:1503:1496> | Reserved | | Valid | Valid |
| BC | reg<:1511:1504> | Reserved | | Valid | Valid |
| BD | reg<:1519:1512> | Reserved | | Valid | Valid |
| BE | reg<:1527:1520> | Reserved | | Valid | Valid |
| BF | reg<:1535:1528> | Reserved | | Valid | Valid |
| **LUT / DLY/CNT Control Data** | | | | | |
| C0 | reg<1543:1536> | LUT3_5 <7:0> or DLY/CNT2 Control Data | 1 - 256 (Delay Time = [Counter Control Data + 1] / Freq) | Valid | Valid |
| C1 | reg<1551:1544> | LUT3_6 <7:0> or DLY/CNT3 Control Data | 1 - 256 (Delay Time = [Counter Control Data + 1] / Freq) | Valid | Valid |
| C2 | reg<1559:1552> | LUT3_7 <7:0> or DLY/CNT4 Control Data | 1 - 256 (Delay Time = [Counter Control Data + 1] / Freq) | Valid | Valid |
| C3 | reg<1567:1560> | LUT3_8 <7:0> or DLY/CNT5 Control Data | 1 - 256 (Delay Time = [Counter Control Data + 1] / Freq) | Valid | Valid |
| C4 | reg<1575:1568> | LUT3_9 <7:0> or DLY/CNT6 Control Data | 1 - 256 (Delay Time = [Counter Control Data + 1] / Freq) | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| C5 | reg<1583:1576> | LUT4_0 <15:0> or DLY/CNT0 (16bits, <15:0> = <1591:1576>) Control Data | 1 - 16384 (Delay Time = [Counter Control Data + 2] / Freq) | Valid | Valid |
| C6 | reg<1591:1584> | | | Valid | Valid |
| C7 | reg<1599:1592> | LUT4_1 <15:0> or DLY/CNT1 (16bits, <15:0> = <1607:1592>) Control Data | 1 - 16384 (Delay Time = [Counter Control Data + 2] / Freq) | Valid | Valid |
| C8 | reg<1607:1600> | | | Valid | Valid |
| C9 | reg<1615:1608> | PGEN pattern data <15:0> = <1623:1608> | | Valid | Valid |
| CA | reg<1623:1616> | | | Valid | Valid |
| **ACMP0** | | | | | |
| CB | reg<1628:1624> | ACMP0-INVoltageSelect: | 00000: 50 mV 00001: 100 mV<br>00010: 150 mV 00011: 200 mV<br>00100: 250 mV 00101: 300 mV<br>00110: 350 mV 00111: 400 mV<br>01000: 450 mV 01001: 500 mV<br>01010: 550 mV 01011: 600 mV<br>01100: 650 mV 01101: 700 mV<br>01110: 750 mV 01111: 800 mV<br>10000: 850 mV 10001: 900 mV<br>10010: 950 mV 10011: 1 V<br>10100: 1.05 V 10101: 1.1 V<br>10110: 1.15 V 10111: 1.2 V<br>11000: VDD/3 11001: VDD/4<br>11010: EXT_VREF(PIN12)<br>11011: EXT_VREF(PIN7)<br>11100: EXT_VREF(PIN12)/2<br>11101:EXT_VREF(PIN7)/2 | Valid | Valid |
| | reg<1630:1629> | ACMP0PositiveInputDivider | 00: 1.0X<br>01: 0.5X<br>10: 0.33X<br>11: 0.25X | Valid | Valid |
| | reg<1631> | ACMP0 Low Bandwidth (MAX: 1MHz) Enable | 0: OFF<br>1:ON | Valid | Valid |
| **ACMP1** | | | | | |
| CC | reg<1636:1632> | ACMP1-INVoltageSelect: | 00000: 50 mV 00001: 100 mV<br>00010: 150 mV 00011: 200 mV<br>00100: 250 mV 00101: 300 mV<br>00110: 350 mV 00111: 400 mV<br>01000: 450 mV 01001: 500 mV<br>01010: 550 mV 01011: 600 mV<br>01100: 650 mV 01101: 700 mV<br>01110: 750 mV 01111: 800 mV<br>10000: 850 mV 10001: 900 mV<br>10010: 950 mV 10011: 1 V<br>10100: 1.05 V 10101: 1.1 V<br>10110: 1.15 V 10111: 1.2 V<br>11000: VDD/3 11001: VDD/4<br>11010: EXT_VREF(PIN12)<br>11011: EXT_VREF(PIN12)<br>11100: EXT_VREF(PIN12)/2<br>11101: EXT_VREF(PIN12)/2 | Valid | Valid |
| | reg<1638:1637> | ACMP1PositiveInputDivider | 00: 1.0X<br>01: 0.5X<br>10: 0.33X<br>11: 0.25X | Valid | Valid |
| | reg<1639> | ACMP1 Low Bandwidth (MAX: 1MHz) Enable | 0: OFF<br>1: ON | Valid | Valid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **ACMP2** | | | | | |
| CD | reg<1644:1640> | ACMP2-INVoltageSelect: | 00000: 50 mV 00001: 100 mV<br>00010: 150 mV 00011: 200 mV<br>00100: 250 mV 00101: 300 mV<br>00110: 350 mV 00111: 400 mV<br>01000: 450 mV 01001: 500 mV<br>01010: 550 mV 01011: 600 mV<br>01100: 650 mV 01101: 700 mV<br>01110: 750 mV 01111: 800 mV<br>10000: 850 mV 10001: 900 mV<br>10010: 950 mV 10011: 1 V<br>10100: 1.05 V 10101: 1.1 V<br>10110: 1.15 V 10111: 1.2 V<br>11000: VDD/3 11001: VDD/4<br>11010: EXT_VREF(PIN12)<br>11011: EXT_VREF(PIN14)<br>11100: EXT_VREF(PIN12)/2<br>11101: EXT_VREF(PIN14)/2 | Valid | Valid |
| | reg<1646:1645> | ACMP2PositiveInputDivider | 00: 1.0X<br>01: 0.5X<br>10: 0.33X<br>11: 0.25X | Valid | Valid |
| | reg<1647> | ACMP2 Low Bandwidth (MAX: 1MHz) Enable | 0: OFF<br>1: ON | Valid | Valid |
| **ACMP3** | | | | | |
| CE | reg<1652:1648> | ACMP3-INVoltageSelect: | 00000: 50 mV 00001: 100 mV<br>00010: 150 mV 00011: 200 mV<br>00100: 250 mV 00101: 300 mV<br>00110: 350 mV 00111: 400 mV<br>01000: 450 mV 01001: 500 mV<br>01010: 550 mV 01011: 600 mV<br>01100: 650 mV 01101: 700 mV<br>01110: 750 mV 01111: 800 mV<br>10000: 850 mV 10001: 900 mV<br>10010: 950 mV 10011: 1 V<br>10100: 1.05 V 10101: 1.1 V<br>10110: 1.15 V 10111: 1.2 V<br>11000: VDD/3 11001: VDD/4<br>11010: EXT_VREF(PIN12)<br>11011: EXT_VREF(PIN14)<br>11100: EXT_VREF(PIN12)/2<br>11101: EXT_VREF(PIN14)/2 | Valid | Valid |
| | reg<1654:1653> | ACMP3PositiveInputDivider | 00: 1.0X<br>01: 0.5X<br>10: 0.33X<br>11: 0.25X | Valid | Valid |
| | reg<1655> | ACMP3 Low Bandwidth (MAX: 1MHz) Enable | 0: OFF<br>1: ON | Valid | Valid |

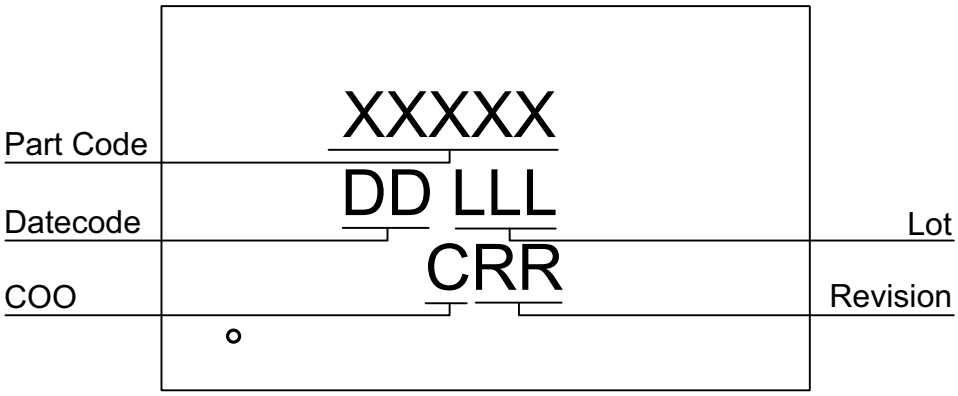
| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **Misc.** | | | | | |
| CF | reg<1656> | Reserved | | Valid | Valid |
| | reg<1657> | Switch from “Matrix OUT: OSC 25MHz PD” to “Matrix OUT: OSC 25MHz Force On” | 0: OSC PD<br>1: OSC Force On (Matrix Output <59>) | Valid | Valid |
| | reg<1658> | Switch from “Matrix OUT: OSC 25KHz/2MHz PD” to “Matrix OUT: OSC 25KHz/2MHz Force On” | 0: OSC PD<br>1: OSC Force On (Matrix Output <58>) | Valid | Valid |
| | reg<1659> | Reserved | | Valid | Valid |
| CF | reg<1660> | Reserved | | Valid | Valid |
| | reg<1661> | Reserved | | Valid | Valid |
| | reg<1662> | I²C reset bit with reloading NVM into Data register (TBD) | 0: Keep existing condition<br>1: Reset execution | Valid | Valid |
| | reg<1663> | IO Latching Enable During I²C Write Interface | 0: Disable<br>1: Enable | Valid | Valid |
| D0 | reg<1671:1664> | RAM 8 outputs for ASM-state0 | | Valid | Valid |
| D1 | reg<1679:1672> | RAM 8 outputs for ASM-state1 | | Valid | Valid |
| D2 | reg<1687:1680> | RAM 8 outputs for ASM-state2 | | Valid | Valid |
| D3 | reg<1695:1688> | RAM 8 outputs for ASM-state3 | | Valid | Valid |
| D4 | reg<1703:1696> | RAM 8 outputs for ASM-state4 | | Valid | Valid |
| D5 | reg<1711:1704> | RAM 8 outputs for ASM-state5 | | Valid | Valid |
| D6 | reg<1719:1712> | RAM 8 outputs for ASM-state6 | | Valid | Valid |
| D7 | reg<1727:1720> | RAM 8 outputs for ASM-state7 | | Valid | Valid |
| D8 | reg<1735:1728> | User configurable RAM / OTP Byte 0 | | Valid | Valid |
| D9 | reg<1743:1736> | User configurable RAM / OTP Byte 1 | | Valid | Valid |
| DA | reg<1751:1744> | User configurable RAM / OTP Byte 2 | | Valid | Valid |
| DB | reg<1759:1752> | User configurable RAM / OTP Byte 3 | | Valid | Valid |
| DC | reg<1767:1760> | User configurable RAM / OTP Byte 4 | | Valid | Valid |
| DD | reg<1775:1768> | User configurable RAM / OTP Byte 5 | | Valid | Valid |
| DE | reg<1783:1776> | User configurable RAM / OTP Byte 6 | | Valid | Valid |
| DF | reg<1791:1784> | User configurable RAM / OTP Byte 7 | | Valid | Valid |
| E0 | reg<1799:1792> | Reserved | | Invalid | Invalid |
| E1 | reg<1807:1800> | Reserved | | Invalid | Invalid |
| E2 | reg<1815:1808> | Reserved | | Invalid | Invalid |
| E3 | reg<1823:1816> | Reserved | | Invalid | Invalid |
| E4 | reg<1831:1824> | 8-bit Pattern ID Byte 1 (From NVM): ID[39:32] | | Valid | Valid |
| E5 | reg<1832> | NVM Data Read Disable (From NVM): ID[24] for BANK0/1/2 only | 0: Disable (Programmed data can be read.), 1: Enable (Programmed data can't be read.) | Valid | Invalid |
| | reg<1833> | Reserved | | Valid | Invalid |
| | reg<1835:1834> | Reserved | | Valid | Invalid |
| | reg<1839:1836> | Reserved | | Valid | Invalid |
| E6 | reg<1847:1840> | 8-bit Pattern ID Byte 0 (From NVM): ID[23:16] | | Valid | Valid |
| E7 | reg<1855:1848> | Reserved | | Valid | Invalid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| E8 | reg<1863:1856> | Reserved | | Valid | Invalid |
| E9 | reg<1867:1864> | I²C Control Code Bit [3:0] | Value for slave address | Valid | Invalid |
| | reg<1868> | Reserved | | Valid | Valid |
| | reg<1869> | Reserved | | Valid | Valid |
| | reg<1870> | Reserved | | Valid | Valid |
| | reg<1871> | BANK0/1/2 I²C-write protection bit | 0: writable<br>1: Non-writable | Valid | Invalid |
| EA | reg<1879:1872> | CNT4 Counted Value | | Valid | Invalid |
| EB | reg<1887:1880> | CNT0 (16bits) = <1895:1880> Counted Value | | Valid | Invalid |
| EC | reg<1895:1888> | | | Valid | Invalid |
| ED | reg<1903:1896> | CNT6 Counted Value | | Valid | Invalid |
| EE | reg<1911:1904> | CNT1 (16bits) = <1919:1904> Counted Value | | Valid | Invalid |
| EF | reg<1919:1912> | | | Valid | Invalid |
| **Matrix Input** | | | | | |
| F0 | reg<1920> | Matrix Input 0 | GND | Valid | Invalid |
| | reg<1921> | Matrix Input 1 | Pin2 Digital Input | Valid | Invalid |
| | reg<1922> | Matrix Input 2 | Pin3 Digital Input | Valid | Invalid |
| | reg<1923> | Matrix Input 3 | Pin4 Digital Input | Valid | Invalid |
| | reg<1924> | Matrix Input 4 | Pin5 Digital Input | Valid | Invalid |
| | reg<1925> | Matrix Input 5 | Pin6 Digital Input | Valid | Invalid |
| | reg<1926> | Matrix Input 6 | Pin7 Digital Input | Valid | Invalid |
| | reg<1927> | Matrix Input 7 | PIN10 Digital Input | Valid | Invalid |
| F1 | reg<1928> | Matrix Input 8 | LUT2_0 / DFF0 Output | Valid | Invalid |
| | reg<1929> | Matrix Input 9 | LUT2_1 / DFF1 Output | Valid | Invalid |
| | reg<1930> | Matrix Input 10 | LUT2_2 / DFF2 Output | Valid | Invalid |
| | reg<1931> | Matrix Input 11 | LUT2_3 / PGEN Output | Valid | Invalid |
| | reg<1932> | Matrix Input 12 | LUT3_0 / DFF3 Output | Valid | Invalid |
| | reg<1933> | Matrix Input 13 | LUT3_1 / DFF4 Output | Valid | Invalid |
| | reg<1934> | Matrix Input 14 | LUT3_2 / DFF5 Output | Valid | Invalid |
| | reg<1935> | Matrix Input 15 | LUT3_3 / DFF6 Output | Valid | Invalid |
| F2 | reg<1936> | Matrix Input 16 | LUT3_4 / DFF7 Output | Valid | Invalid |
| | reg<1937> | Matrix Input 17 | LUT3_5 / CNT_DLY2(8bit) Output | Valid | Invalid |
| | reg<1938> | Matrix Input 18 | LUT3_6 / CNT_DLY3(8bit) Output | Valid | Invalid |
| | reg<1939> | Matrix Input 19 | LUT3_7 / CNT_DLY4(8bit) Output | Valid | Invalid |
| | reg<1940> | Matrix Input 20 | LUT3_8 / CNT_DLY5(8bit) Output | Valid | Invalid |
| | reg<1941> | Matrix Input 21 | LUT3_9 / CNT_DLY6(8bit) Output | Valid | Invalid |
| | reg<1942> | Matrix Input 22 | LUT4_0 / CNT_DLY0(16bit) Output | Valid | Invalid |
| | reg<1943> | Matrix Input 23 | LUT4_1 / CNT_DLY1(16bit) Output | Valid | Invalid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| F3 | reg<1944> | Matrix Input 24 | LUT3_10 / Pipe Delay (1st stage) Output | Valid | Invalid |
| | reg<1945> | Matrix Input 25 | Pipe Delay Output0 | Valid | Invalid |
| | reg<1946> | Matrix Input 26 | Pipe Delay Output1 | Valid | Invalid |
| | reg<1947> | Matrix Input 27 | Fixed "L" output because it is OSC clock. | Valid | Invalid |
| | reg<1948> | Matrix Input 28 | Fixed "L" output because it is OSC clock. | Valid | Invalid |
| | reg<1949> | Matrix Input 29 | Fixed "L" output because it is OSC clock. | Valid | Invalid |
| | reg<1950> | Matrix Input 30 | Filter0 / Edge Detect0 Output | Valid | Invalid |
| | reg<1951> | Matrix Input 31 | Filter1 / Edge Detect1 Output | Valid | Invalid |
| F4 | reg<1952> | Matrix Input 32 | Virtual Input <0> | Valid | Valid |
| | reg<1953> | Matrix Input 33 | Virtual Input <1> | Valid | Valid |
| | reg<1954> | Matrix Input 34 | Virtual Input <2> | Valid | Valid |
| F4 | reg<1955> | Matrix Input 35 | Virtual Input <3> | Valid | Valid |
| | reg<1956> | Matrix Input 36 | Virtual Input <4> | Valid | Valid |
| | reg<1957> | Matrix Input 37 | Virtual Input <5> | Valid | Valid |
| | reg<1958> | Matrix Input 38 | Virtual Input <6> | Valid | Valid |
| | reg<1959> | Matrix Input 39 | Virtual Input <7> | Valid | Valid |
| F5 | reg<1960> | Matrix Input 40 | RAM_0 Output for ASM-state | Valid | Invalid |
| | reg<1961> | Matrix Input 41 | RAM_1 Output for ASM-state | Valid | Invalid |
| | reg<1962> | Matrix Input 42 | RAM_2 Output for ASM-state | Valid | Invalid |
| | reg<1963> | Matrix Input 43 | RAM_3 Output for ASM-state | Valid | Invalid |
| | reg<1964> | Matrix Input 44 | RAM_4 Output for ASM-state | Valid | Invalid |
| | reg<1965> | Matrix Input 45 | RAM_5 Output for ASM-state | Valid | Invalid |
| | reg<1966> | Matrix Input 46 | RAM_6 Output for ASM-state | Valid | Invalid |
| | reg<1967> | Matrix Input 47 | RAM_7 Output for ASM-state | Valid | Invalid |
| F6 | reg<1968> | Matrix Input 48 | Pin12 Digital Input | Valid | Invalid |
| | reg<1969> | Matrix Input 49 | Pin13 Digital Input | Valid | Invalid |
| | reg<1970> | Matrix Input 50 | Pin14 Digital Input | Valid | Invalid |
| | reg<1971> | Matrix Input 51 | Pin15 Digital Input | Valid | Invalid |
| | reg<1972> | Matrix Input 52 | Pin16 Digital Input | Valid | Invalid |
| | reg<1973> | Matrix Input 53 | Pin17 Digital Input | Valid | Invalid |
| | reg<1974> | Matrix Input 54 | Pin18 Digital Input | Valid | Invalid |
| | reg<1975> | Matrix Input 55 | Pin19 Digital Input | Valid | Invalid |
| F7 | reg<1976> | Matrix Input 56 | Pin20 Digital Input | Valid | Invalid |
| | reg<1977> | Matrix Input 57 | ACMP_0 Output | Valid | Invalid |
| | reg<1978> | Matrix Input 58 | ACMP_1 Output | Valid | Invalid |
| | reg<1979> | Matrix Input 59 | ACMP_2 Output | Valid | Invalid |
| | reg<1980> | Matrix Input 60 | ACMP_3 Output | Valid | Invalid |
| | reg<1981> | Matrix Input 61 | Programmable Delay with Edge Detector Output | Valid | Invalid |
| | reg<1982> | Matrix Input 62 | Resetb_core | Valid | Invalid |
| | reg<1983> | Matrix Input 63 | VDD | Valid | Invalid |
| **Reserved** | | | | | |
| F8 | reg<1991:1984> | Reserved | | Valid | Invalid |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| F9 | reg<1999:1992> | Reserved | | Valid | Invalid |
| FA | reg<2007:2000> | Reserved | | Valid | Invalid |
| FB | reg<2015:2008> | Reserved | | Valid | Valid |
| FC | reg<2023:2016> | Reserved | | Valid | Invalid |
| FD | reg<2031:2024> | Reserved | | Valid | Invalid |
| FE | reg<2039:2032> | Reserved | | Valid | Valid |
| FF | reg<2047:2040> | Reserved | | Valid | Valid |

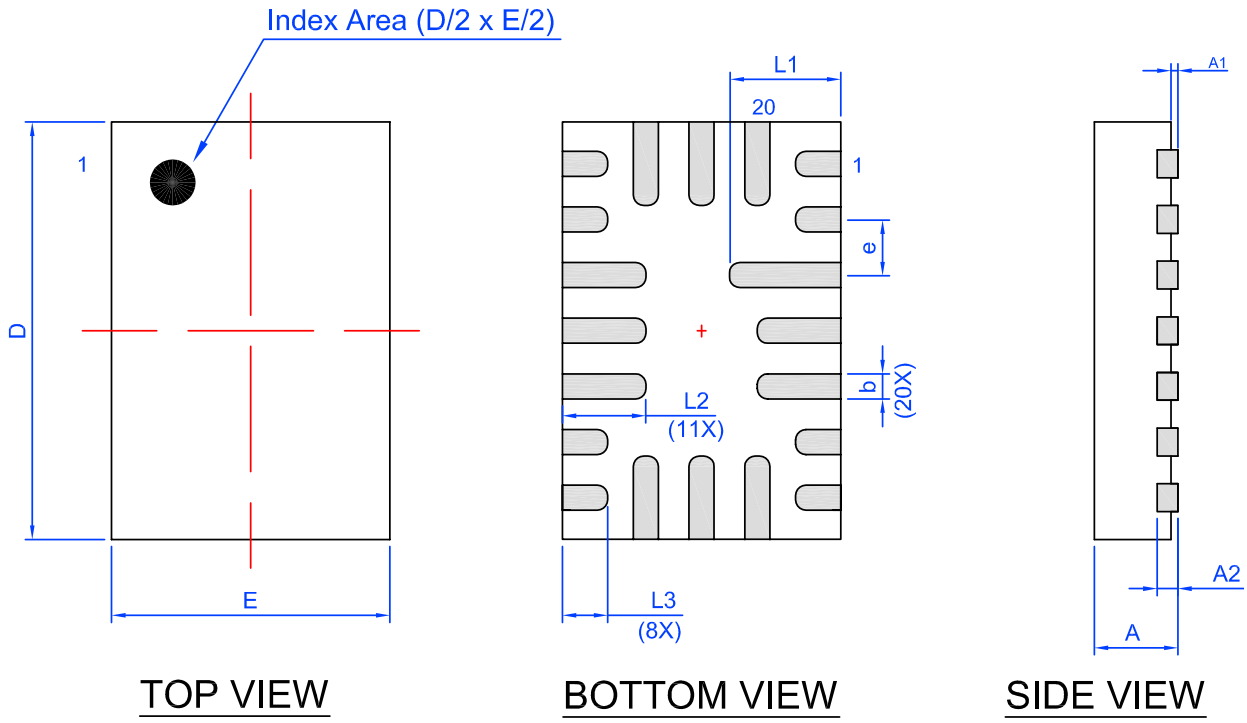
## 22.0 Package Top Marking System Definition




XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

## 23.0 Package Drawing and Dimensions

**STQFN 20L 2x3mm 0.4P COL Package**
**JEDEC MO-220, Variation WECE**
**IC Net Weight: 0.015 g**




Unit: mm

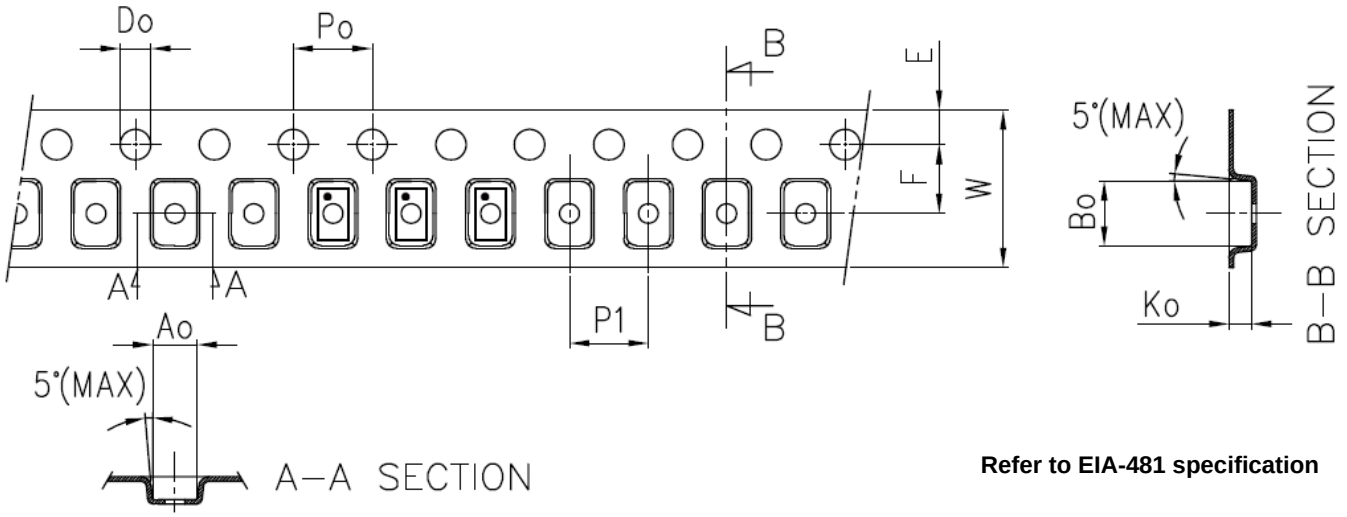
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|---|---|---|---|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.005 | - | 0.050 | E | 1.95 | 2.00 | 2.05 |
| A2 | 0.10 | 0.15 | 0.20 | L1 | 0.75 | 0.80 | 0.85 |
| b | 0.13 | 0.18 | 0.23 | L2 | 0.55 | 0.60 | 0.65 |
| e | 0.40 BSC | | | L3 | 0.275 | 0.325 | 0.375 |

## 24.0 Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 20L 2x3 mm 0.4P COL | 20 | 2 x 3 x 0.55 | 3,000 | 3,000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

### 24.1 Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STQFN 20L 2x3 mm 0.4P COL | 2.2 | 3.15 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |



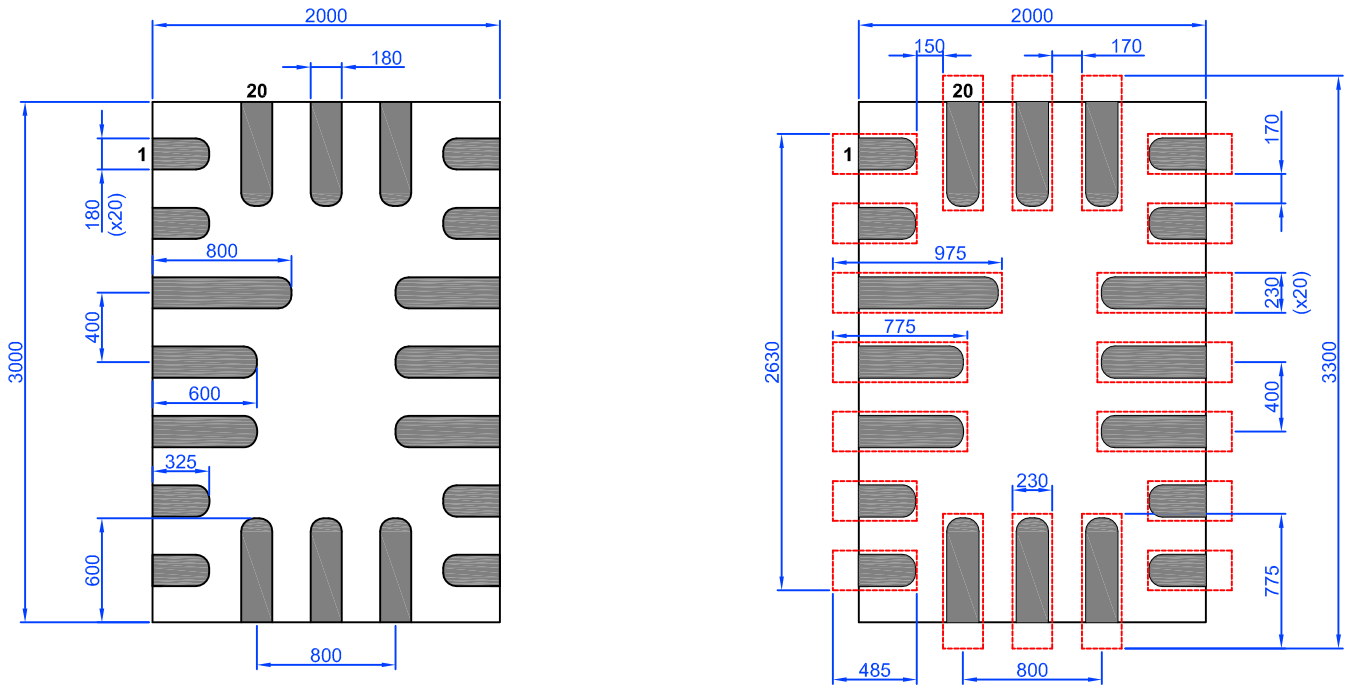

**Refer to EIA-481 specification**

## 25.0 Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

**Units: µm**




## 26.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 $mm^3$ (nominal). More information can be found at www.jedec.org.

## 27.0 Revision History

| Date | Version | Change |
|---|---|---|
| 4/21/2016 | 1.02 | Clarified text in Crystal Oscillator section<br>Reorganized I2C and ASM Electrical Spec |
| 3/21/2016 | 1.01 | Updated subsection I2C Serial Command Register Protection |
| 3/16/2016 | 1.00 | Production Release |

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GreenFET1 / GreenFET3: MOSFET Drivers and ultra-small, low RDSon Load Switches
GreenCLK1 / GreenCLK2 / GreenCLK3: Crystal replacement technology

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Стандарт Электрон Связь

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