9-4131; Rev. 0; 9/91

MAXIM

15-Bit ADC with Parallel Interface

General Description

The MAX135 is a CMOS 15-bit, binary-output analog-to-digital converter (ADC). Multi-slope integration provides low-noise and high-resolution conversions in less time than standard integrating ADCs: The MAX135 is tested at 16 conversions per second, but operates at up to 6 times that rate. The MAX135 uses Super LSBs with data averaging to achieve 18-bit resolution.

Supply current is 125µA maximum during normal operation and only 10µA maximum in sleep mode. Low conversion noise allows tested operation at only 300mV full scale (15µV per LSB). A simple 8-bit parallel data bus and three control lines easily interface to all common microprocessors, and twos-complement output coding simplifies bipolar measurements.

High resolution and compact size make the MAX135 ideal for data loggers, numerical control systems, weigh scales, data-acquisition systems, and panel meters. The MAX135 comes in 28-pin DIP and SO packages in both commercial and extended temperature grades.

Applications

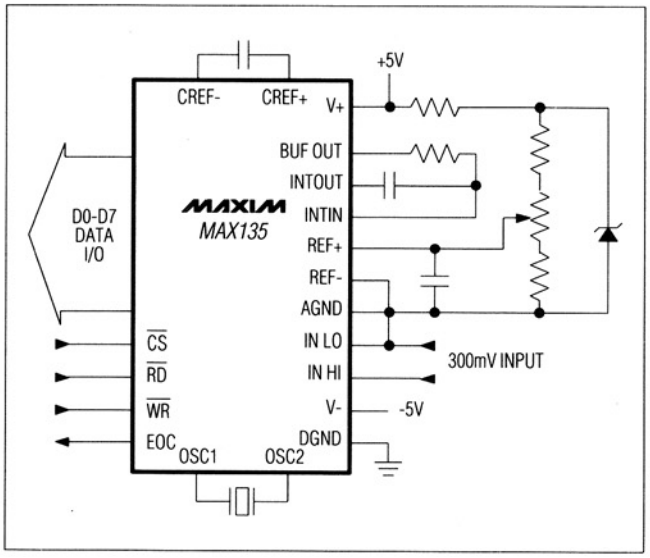
Data Acquisition

Battery-Powered Instruments

Control Applications

Analog-Signal Measurement
Pressure, Flow, Temperature, Voltage, Current, Resistance, Weight

Functional Diagram



Features

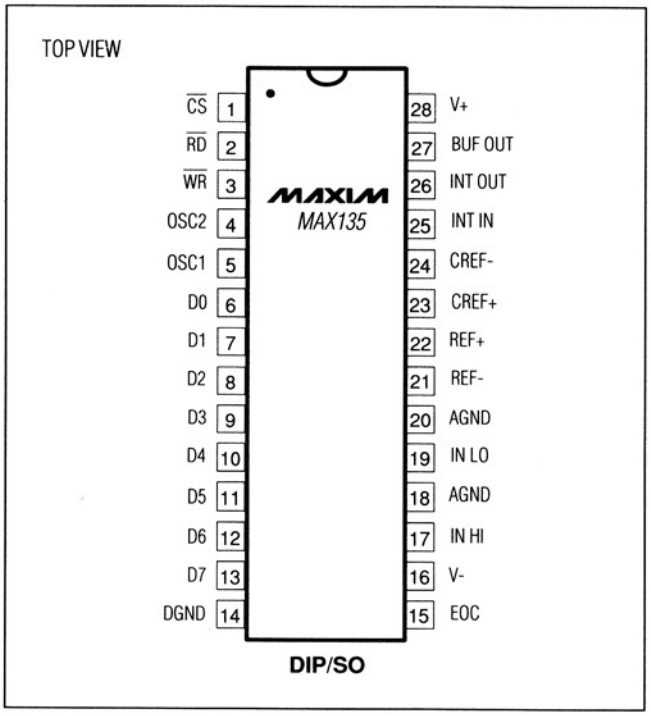
- ♦ **15-Bit, Multi-Slope Integrating ADC**
- ♦ **15µV Resolution at 16 Conv/Sec**
- ♦ **Low Supply Current**
  - **125µA Max (Normal Operation)**
  - **10µA Max (Sleep-Mode Operation)**
- ♦ **±0.005% Accuracy at 16 Conv/Sec**
- ♦ **3 Super Bits for 18-Bit Resolution**
- ♦ **Low Noise - Operates at 300mV Full Scale**
- ♦ **Easy µP Interface - 8-Bit Parallel Data Bus**
- ♦ **±10pA Input Leakage Current**
- ♦ **Small 28-Pin DIP and SO Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX135CPI	0°C to +70°C	28 Plastic DIP
MAX135CWI	0°C to +70°C	28 Wide SO
MAX135C/D	0°C to +70°C	Dice*
MAX135EPI	-40°C to +85°C	28 Plastic DIP
MAX135EWI	-40°C to +85°C	28 Wide SO

* *Contact factory for dice specifications.*

Pin Configuration



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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

15-Bit ADC with Parallel Interface

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V+ to DGND ..... -0.3V < V+ < +6.0V
- V- to DGND ..... +0.3V < V- < -9.0V
- V+ to V- ..... +15V

Analog Input Voltage (any input) ..... V+ to V-
Digital Input Voltage ..... (DGND - 0.3V) to (V+ + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
- 28-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 786mW
- 28-Pin Wide SO (derate 12.50mW/°C above +70°C) . 688mW

Operating Temperature Ranges:
- MAX135C_ _ ..... 0°C to +70°C
- MAX135E_ _ ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF- = 0V, REF+ = 545mV, RINT = 402kΩ, CINT = 0.0047µF, CREF = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution		(Note 1)				20,000	LSB
Zero Error		IN HI = 0V	T_A = +25°C			±2	LSB
			T_A = T_{MIN} to T_{MAX}			±5	
Nonlinearity		(Notes 2, 3)	T_A = +25°C			±2	LSB
Rollover Error		(Note 4)	T_A = +25°C			±3	LSB
			T_A = T_{MIN} to T_{MAX}			±10	
Conversion Time				63			ms
Input Voltage Range		IN HI to IN LO				±300	mV
Leakage Current		IN HI, IN LO	T_A = +25°C			±10	pA
			T_A = T_{MIN} to T_{MAX}			±250	
Common-Mode Rejection		IN HI = IN LO	V_{CM} = ±500mV		3	10	LSB
			V_{CM} = ±3.5V		70		
Common-Mode Range		IN HI = IN LO			±3.5		V
Read Zero (50Hz/60Hz Range)						±2000	LSB
Noise (Zero-Reading Mode)		IN HI = IN LO	T_A = +25°C		1.5		LSB
Zero-Reading Drift		(Note 3)				0.1	LSB/°C
Scale Factor Temp. Coefficient		(Note 3)				5	ppm/°C
Positive Supply Rejection		FS change, V- = -5.0V, +4.5V ≤ V+ ≤ +5.5V				2	LSB
Negative Supply Rejection		FS change, V+ = 5.0V, -4.5V ≤ V- ≤ -5.5V				2	LSB
Positive Supply Current	I+				60	125	µA
Negative Supply Current	I-				-35	-65	
Digital Ground Supply Current					-25	-60	
Positive Sleep-Mode Current	I+				4	10	µA
Negative Sleep-Mode Current	I-				-4	-10	
Digital Ground Sleep-Mode Current					0	±2	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF- = 0V, REF+ = 545mV, RINT = 402kΩ, CINT = 0.0047µF, CREF = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SECTION						
Output High	V_{OH}	D0-D7, I_{OUT} = -1mA	3.5	4.3		V
		DO-D7, I_{OUT} = -100µA	4.0	4.5		
		EOC, I_{OUT} = -100µA	4.0			
Output Low	V_{OL}	D0-D7, I_{OUT} = 1.6mA		0.2	0.4	V
		EOC, I_{OUT} = 100µA			0.4	
Input High	V_{IH}	Referred to DGND, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.4			V
Input Low	V_{IL}	Referred to DGND, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$			0.8	V
Input Current	I_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, D0-D7 when three-stated		±10	±500	nA
Input Capacitance	C_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, D0-D7 when three-stated		5		pF

TIMING CHARACTERISTICS

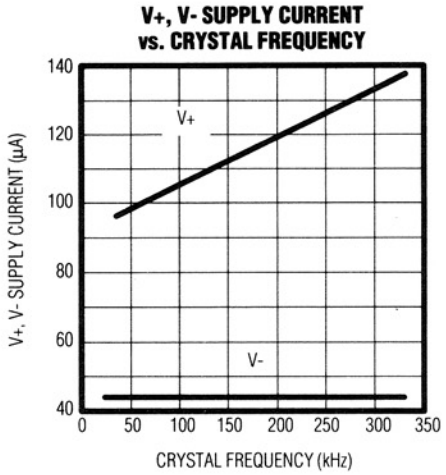
(Test circuit of Figures 1 and 2, V+ = 5V, V- = -5V, DGND = AGND = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1		0			ns
$\overline{WR}$ Data-Setup Time	t_2		200	<100		ns
$\overline{WR}$ Pulse Width	t_3		200	<100		ns
Data Hold after $\overline{WR}$	t_4		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_5		0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_6		0			ns
$\overline{RD}$ to Data Valid	t_7		480	240		ns
Bus-Relinquish Time	t_8		380	190		ns
$\overline{WR}$ to $\overline{RD}$	t_9		300			ns
$\overline{RD}$ to $\overline{WR}$	t_{10}		200			ns
Delay between Write Operations	t_{11}		500	<250		ns

Note 1: 18-bit resolution achieved by averaging multiple conversions.
Note 2: Max deviation from best straight line fit, 1LSB = 15.63µV.
Note 3: Guaranteed by design, not tested.
Note 4: Difference in reading for equal positive and negative inputs near full scale.

15-Bit ADC with Parallel Interface

Typical Operating Characteristic



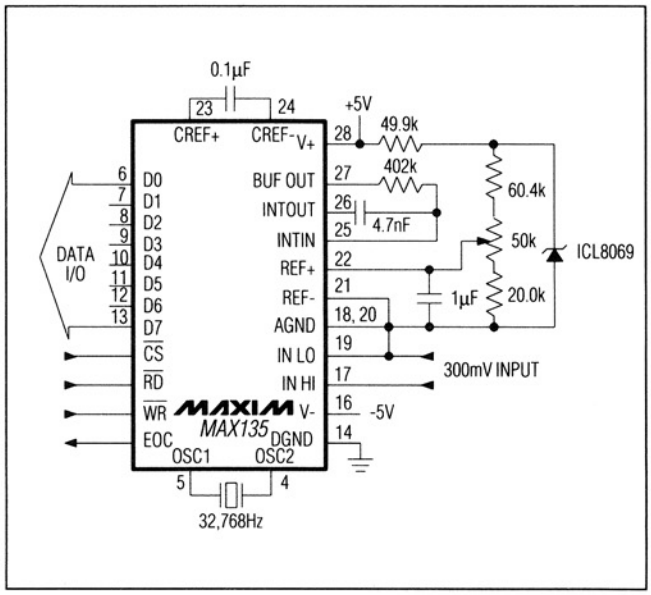


Figure 1. Test and Typical Application Circuit

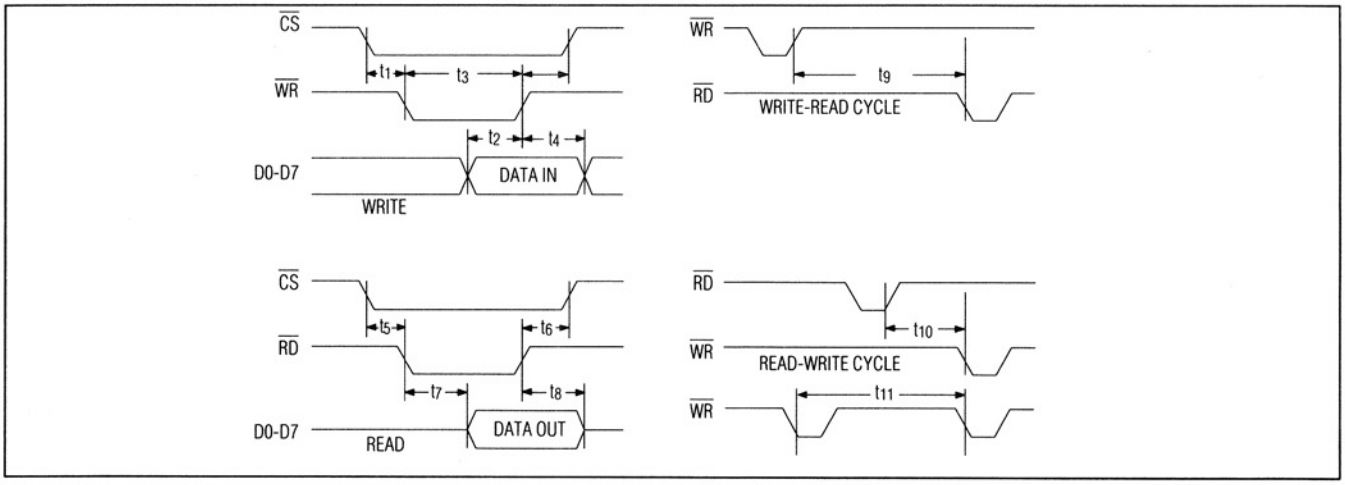


Figure 2. Parallel-Mode Timing

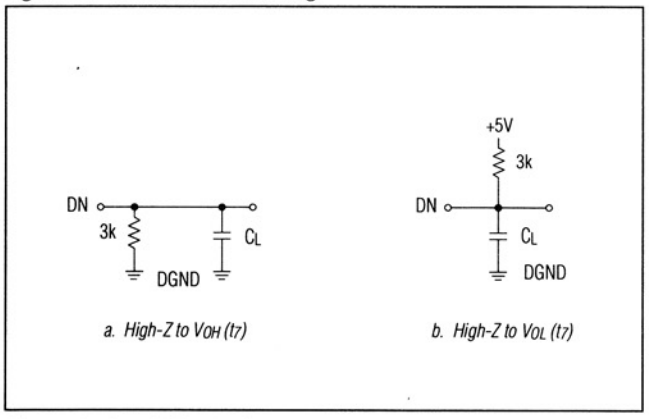


Figure 3. Load Circuits for Access Time

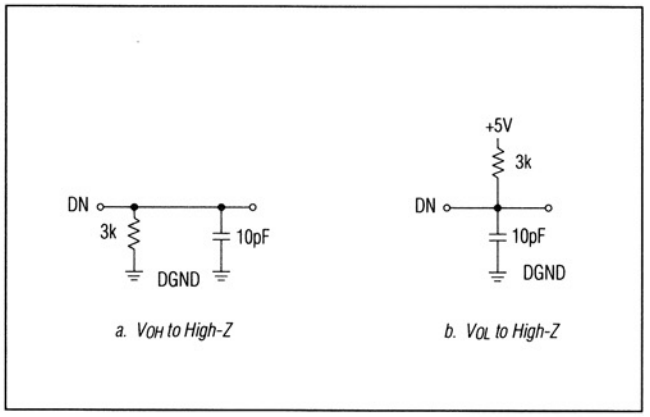


Figure 4. Load Circuits for Bus Relinquish Time

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input low for communication with the MAX135.
2	$\overline{RD}$	$\overline{READ}$ Input low to read data.
3	$\overline{WR}$	$\overline{WRITE}$ Input latches data on the rising edge.
4	OSC2	Oscillator Output 2 normally connected to a 32,768Hz crystal.
5	OSC1	Oscillator Input 1 normally connected to a 32,768Hz crystal, or may be connected to an external clock.
6-13	D0-D7	Three-State Data Inputs/Outputs. See Tables 1 and 2.
14	DGND	Digital Ground - power-supply return
15	EOC	End-of-Conversion pin goes high at conversion end.
16	V-	Negative Supply Input - typically -5V
17	IN HI	Positive Analog Input voltage connection
18, 20	AGND	Analog Ground
19	IN LO	Negative Analog Input voltage connection
21	REF-	Negative Reference Input
22	REF+	Positive Reference Input
23	CREF+	Reference Capacitor - positive connection
24	CREF-	Reference Capacitor - negative connection
25	INTIN	Integrator Input - external component connection
26	INTOUT	Integrator Output - external component connection. To minimize noise, this pin should drive the outside foil (negative end) of the integrator capacitor.
27	BUF OUT	Buffer Amplifier Output drives the integrator resistor.
28	V+	Positive Supply, +5V

15-Bit ADC with Parallel Interface

Application Information

Figure 1 shows the basic MAX135 application circuit. The component values are selected for 16 conversions per second. Keep the analog lines and components away from the digital input/output (I/O) lines to prevent capacitive coupling to the analog circuitry.

Increasing Speed

Applications with greater conversion rates require different components; the *Components* section describes how to determine the correct values. Ground planes and shielding are essential for stable readings on faster conversion rates. When operating at crystal frequencies specified in Table 1 that are greater than 32,768Hz, use either the 50Hz or 60Hz mode; however, the 50Hz mode will improve performance due to a longer integration period. When operating in 50Hz mode, both the integrator capacitor and the reference voltage must be appropriately selected. For fast conversion rates where resolution is not important, use fewer digits as a quick solution. If maximum resolution is important, a trailing average of the data will provide highest resolution.

Increasing Resolution

For applications where resolution is important and speed is not, achieve additional resolution by using bits LSB/2, LSB/4, and LSB/8 found in the status register. When averaged, these bits can yield up to ±18-bit resolutions. For maximum resolution, use a trailing average of at least 100 readings.

Components

The MAX135 requires an integrator resistor (RINT) and capacitor (CINT), a reference capacitor (CREF), and a crystal. A 32,768Hz crystal frequency is used to test the MAX135. The crystal frequency, reference voltage, and integrator current dictate the values of RINT and CINT.

Integrator Resistor

The integrator resistor sets the maximum integrator output current for the integrate phase. A 402kΩ metal-film resistor is recommended for use with reference voltages between 345mV and 655mV. Best linearity is achieved when the integration current (IINT) does not exceed 2.5µA. For other reference voltages, select RINT as follows:

$$RINT = \frac{VREF}{2.5\mu A < IINT < 0.5\mu A}, \qquad IINT = \frac{VREF}{RINT}$$

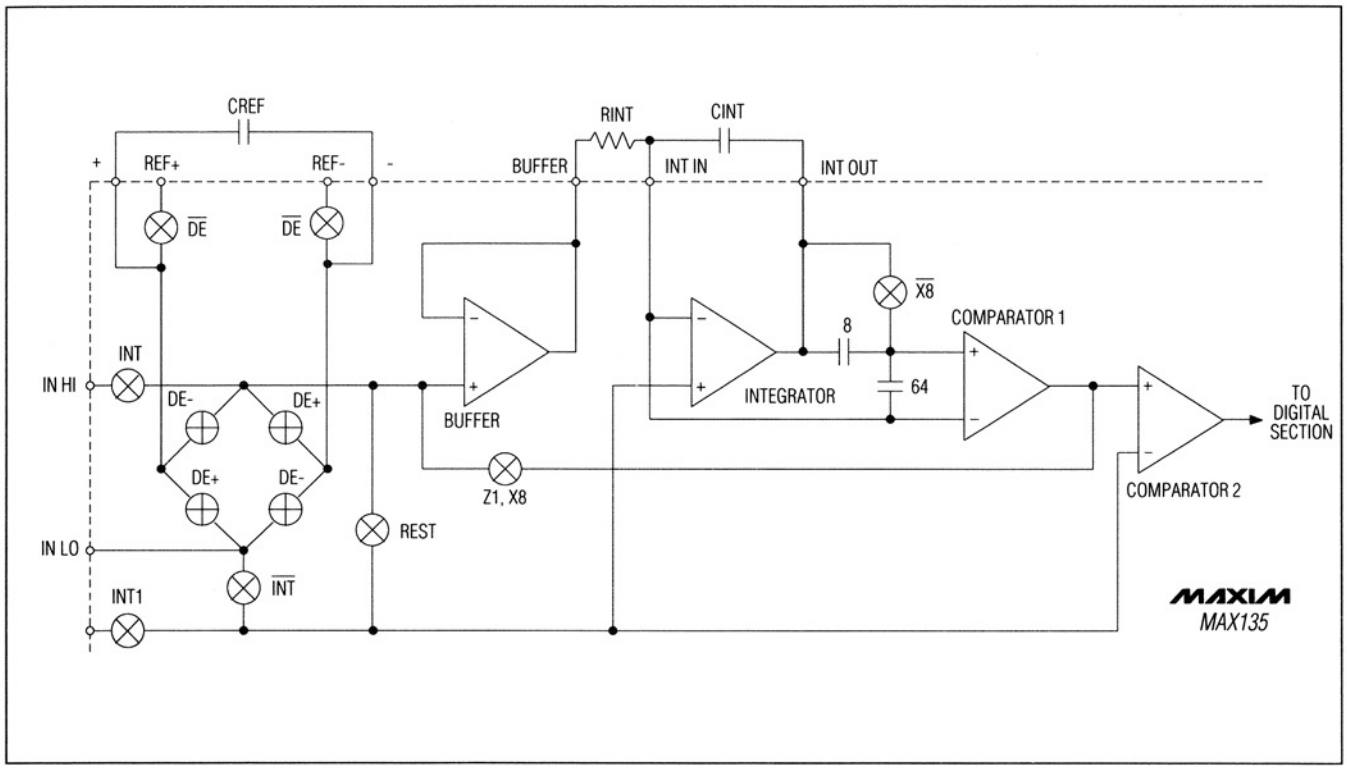


Figure 5. Analog Section Block Diagram

Integrator Capacitor

The oscillator frequency, integrator resistor, and integrator capacitor set the maximum integrator output-voltage swing for full-scale reading. The voltage swing is about 3V for a 402kΩ integrator resistor and a 4.7nF integrator capacitor when the clock frequency is 32,768Hz. If different clock frequencies are used, select CINT using the following equations:

$$tINT = \left(\frac{1}{f_{OSC}}\right) \times \begin{pmatrix} 545 \text{ for } 60Hz \\ \text{or} \\ 655 \text{ for } 50Hz \end{pmatrix}$$

$$CINT = \frac{(V_{IN(FS)}/RINT) \times tINT}{3.5V > V_{SWING} > 1V}$$

The integrator capacitor's dielectric absorption directly affects integral nonlinearity. High-quality metal-film capacitors are recommended in the following order of preference: polypropylene, polystyrene, polycarbonate, and polyester (Mylar). A polyester capacitor will generate some integral nonlinearity.

Reference Capacitor

The reference capacitor value must be small enough to fully charge from a discharged state on power-up in the desired time, and large enough so the charge does not droop excessively during a conversion. The reference capacitor is normally 0.1µF for all oscillator frequencies. For applications that require a physically smaller capacitor, the equation below will maintain CREF proportionality.

$$CREF = \frac{0.0033}{f_{OSC}}$$

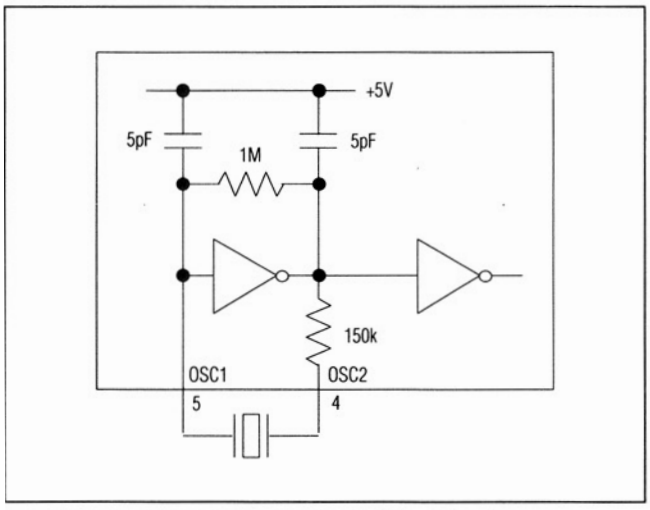


Figure 6. MAX135 Internal Oscillator Drive Circuitry

The reference capacitor must have low leakage, since it stores the reference voltage while floating during the deintegrate phase. Any leakage or charge loss during this phase changes the scale factor. Polypropylene, polystyrene, polycarbonate, and polyester metal-film capacitors are recommended, in this order, for low-leakage characteristics.

Crystal Frequency

The crystal frequency sets the conversion rate . Table 1 lists the crystal frequencies and integrator capacitors for 50Hz and 60Hz operation at particular conversion rates. These crystal frequencies complete a conversion in an integral number of line cycles. Figure 6 shows the internal oscillator drive circuitry used with external crystals.

Table 1. Crystal Frequencies and Integrator Capacitors for 50Hz to 60Hz Operation

Conv/ Sec	Hz	CINT/60Hz (pF)	CINT/50Hz (pF)	R kΩ
16	32,768	4700	6800	402
32	65,536	2700	3300	402
48	98,304	1800	2000	402
64	131,072	1200	1500	402
80	163,840	1000	1200	402
96	196,608	820	1000	402

NOTE: CAPACITOR VALUES ARE FOR A 2.5V INTEGRATOR SWING.

Two manufactures of miniature quartz resonators are:

Micro Crystal
702 West Algonquin Road
Arlington Heights, Illinois 60005

Seiko Instruments USA Inc.
2990 West Lomita Boulevard
Torrance, California 90505

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Reference Voltage Selection

For 300mV full scale, when the 60Hz mode is selected, the reference voltage is 523mV. If 50Hz is selected, the reference voltage is 629mV for 300mV full scale.

$$\text{Volts / LSB} = \frac{V_{IN(FS)}}{20{,}000}$$

$$\text{VREF} = \frac{(545 \text{ counts}) \times 64 \times V_{IN(FS)}}{20{,}000} \quad \text{60Hz operation}$$

or

$$\text{VREF} = \frac{(655 \text{ counts}) \times 64 \times V_{IN(FS)}}{20{,}000} \quad \text{50Hz operation}$$

Note: $V_{IN(FS)}$ = full-scale input voltage.

The ICL8069 is a 1.25V 50µA supply current reference, making it idealy suited for generating the MAX135's reference. Figure 7 shows how 1.25V can be divided for the desired reference voltage.

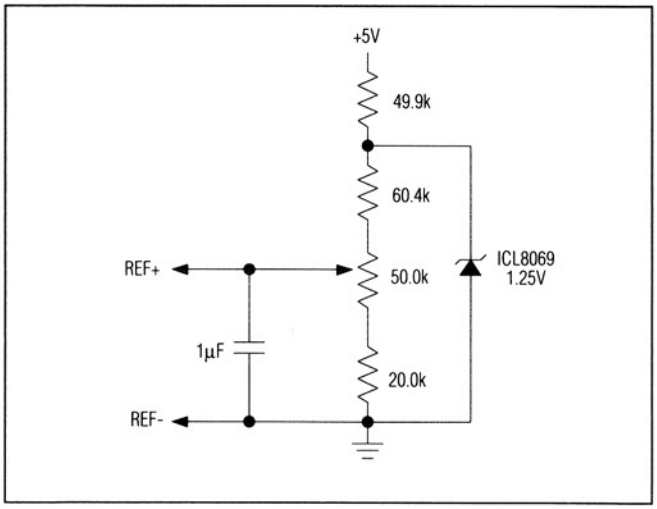

Figure 7. Dividing an ICL8069 to generate the MAX135's reference voltage.

Digital Interface

The MAX135 implements an 8-bit, bidirectional data bus with CHIP SELECT ($\overline{CS}$), READ ($\overline{RD}$), and WRITE ($\overline{WR}$). $\overline{CS}$ allows access to the I/O data bits and control lines. $\overline{WR}$ latches data into the command input register. $\overline{RD}$ sets the MAX135 data I/O lines to drive the data bus.

Initialize the ADC immediately after power-up to insure correct operation.

The MAX135 has four internal registers: the command input register, output register 0, output register 1, and the output status register. Table 2 defines their bit locations. Use $\overline{WR}$ to write to the command input register. Once the register bits RS0 and RS1 are set to the desired register address and the $\overline{WR}$ command is initiated, the designated register can be read. When $\overline{RD}$ is low, the designated register data is available on the data bus. When $\overline{RD}$ is high, the outputs go three-state and all I/O output lines return to input lines.

Table 2: MAX135 Register Map of Input and Output Data

		Data Bit							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command Input Register	1	Start Convert	50Hz Mode	Sleep Mode	Read Zero	Don't Care	RS0	RS1	Don't Care
	0	Returns to 0 at EOC	60Hz Mode	Run	Read IN HI	Don't Care	See Table 3		Don't Care
Output Register 0 RS1 = 0, RS0 = 0		B7	B6	B5	B4	B3	B2	B1	B0 LSB
Output Register 1 RS1 = 0, RS0 = 1	1	- Polarity	B14	B13	B12	B11	B10	B9	B8
	0	+ Polarity							
Output Status Register RS1 = 1, RS0 = 0	1	Collision	EOC	Integrating Input	Sleep	Always Low		Super LSBs	
	0	No Collision	Converting	Not Integrating	Run		LSB/2	LSB/4	LSB/8

Table 3: Register Set-Bit Definitions

RS1	RS0	Definitions
0	0	Selects register 0; outputs data bits B0-B7
0	1	Selects register 1; outputs data bits B8-B14, polarity
1	0	Selects register 2; outputs status bits, LSB/8, LSB/4, LSB/2, CB, EOC
1	1	Invalid data

Input Register

Register Set Bits

Data pins D1 and D2 (RS1 and RS0) in the command input register determine the data to be read on the data bus. These bits select which register outputs data to the bus. Table 3 defines the bit values that determine the register in use.

Read-Zero Bit

The MAX135 performs a read-zero conversion on command - a calibration process that removes zero offset. The read-zero bit, when set to 1, internally shorts the inputs; when a start-conversion command is given, the zero error is converted. Subtract the results from the standard external measurement conversion when the read-zero conversion ends. If the read-zero bit is set to 0, the converter measures the voltage between IN HI and IN LO once a start bit is given.

An average of multiple read-zero measurements determines the most accurate read zero.

Sleep Bit

With the sleep bit set to 1 and 1 written to D5, the low-power sleep mode starts when EOC = 1. In sleep mode, the supply current is typically under 5µA, the oscillator shuts down, and data can be read. When sleep mode is released, the analog circuitry needs time to stabilize before the next conversion starts. Accomplish this by writing a separate instruction to emerge from sleep mode, and waiting at least one conversion cycle before writing a start instruction.

50Hz/60Hz

With a 32,768Hz crystal, the 50Hz/60Hz bit sets the integration period equal to one line cycle for 50Hz/60Hz environments. When D6 is set to 0, the integrator count is an integer multiple of 60Hz (32,768Hz/60Hz = 546 counts). When D6 is set to 1, the integrator count is an integer multiple of 50Hz (32,768Hz/50Hz = 655 counts). Achieve the highest AC rejection by adjusting the integration period for 50Hz or 60Hz.

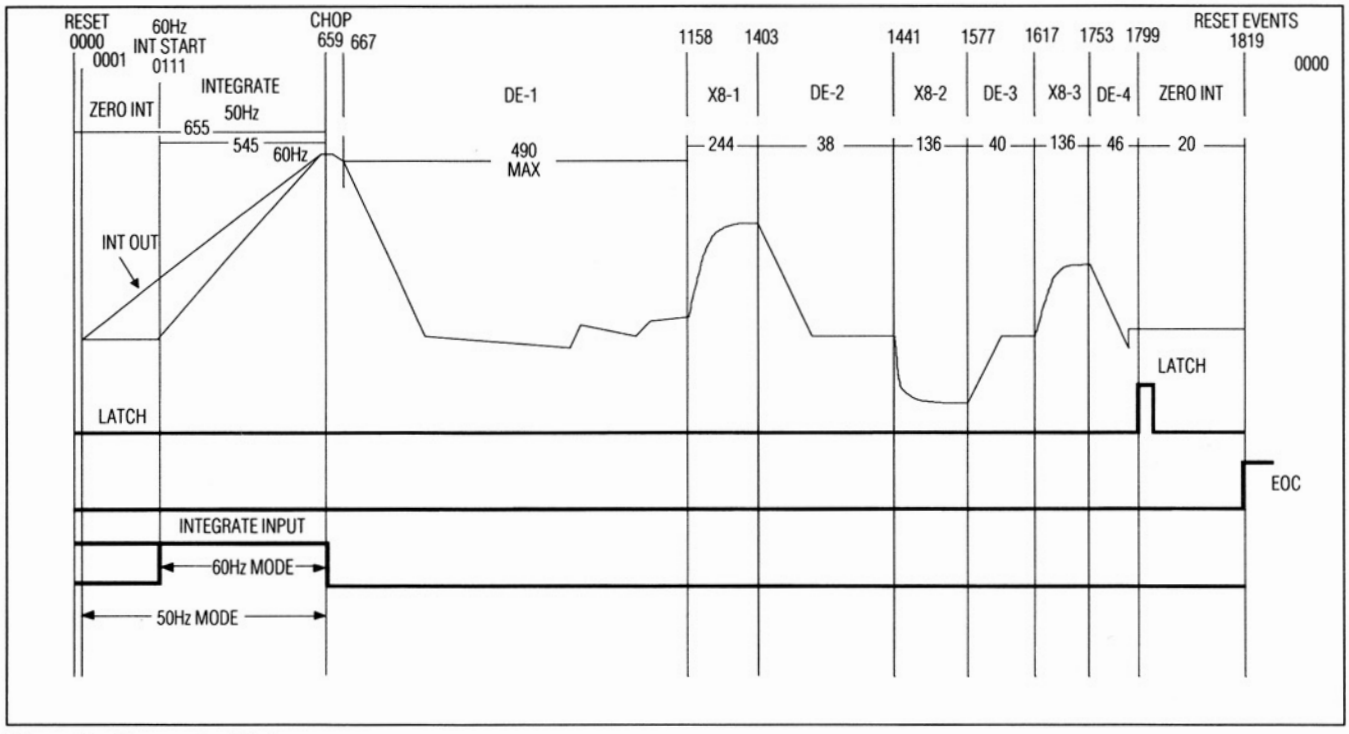

Figure 8. Conversion Timing

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Start Bit

The start bit initiates a conversion when set to 1 in the command input register. The MAX135 immediately starts a conversion, stops at conversion end, and waits for the next start-bit command. Send a start instruction to initiate each conversion.

To initiate a continuous data stream, write a separate start command for each conversion in one of three ways:

1. Wait longer than a known conversion time and write another start command.
2. Poll either the EOC status register bit or the EOC line to determine conversion end and start time for the next conversion. EOC becomes 1 at conversion end at count 0000 of the conversion counter (Figure 8).
3. Set the start bit to 1 before conversion end. The internal conversion counter is then checked for its count. If the count is 0000 (EOC = 1), a new conversion starts and the conversion counter is set to 0001. The start bit resets to 0 after 5 clock cycles. The MAX135 will not check the start bit again until the conversion counter returns to a 0000 count. This means a start command can be given any time after the 0005 internal conversion count; the next conversion starts when the counter returns to 0000.

Output Registers

Register 0

Register 0 contains the low-byte (bits B0-B7) conversion data. New data is available after EOC goes high. Access register 0 by setting RS0 and RS1 to 0. Output data is the sum of system offset (read zero) plus the results of the external input voltage measurement.

Register 1

Register 1 contains the high-byte (bits B8-B15) data. Data is in a twos-complement format, where the polarity bit is a 1 for negative polarity data. Access register 1 by setting control bits RS0 = 1 and RS1 = 0 when writing to the command input register.

Status Register

LSB/2, LSB/4, LSB/8 Bits (Super LSBs)

The LSB/2, LSB/4, and LSB/8 bits enhance resolution. At each conversion end they are updated and read back from the status register. When using these three bits, 18 bits of resolution are available. When using the 17 bits plus sign, average the readings to stabilize the result.

Integrate Bit

The integrate (INT) bit is set to 1 at the beginning of an integration and becomes 0 at the end. Poll INT to determine the earliest time the analog input can be changed without affecting the conversion.

End-of-Conversion Bit

The end-of-conversion (EOC) bit signals conversion status. If EOC is 1, the conversion is complete and the ADC waits in zero-integrate mode at count 0000 for the next start instruction. . A conversion cycle has 1820 counts. EOC becomes 1 at count 0000 and 0 at count 0001.

Collision Bit

The collision bit warns the microprocessor that the register's data was changed during the read cycle. Once the status register is read, the collision bit resets to 0. Collisions do not occur if a conversion's read cycle is completed before the next conversion begins.

Analog Section

Sequence Counter and Results Counter

A binary sequence counter controls the sequencing or timing of the conversion phases. In integrate phase, both start and stop occur at preset counts. The deintegrate phases start at predetermined counts, and terminate when the comparator detects zero crossing at the integrator output.

The results counter accumulates counts during all deintegrate phases. It is an up/down binary counter, with the deintegrate polarity determining count direction. In the first deintegrate phase, the results counter counts by 64s. Since the second deintegrate phase deintegrates a residual voltage multiplied by 8, the results counter increments or decrements by 8s during this phase. It increments or decrements by 1s during the third deintegrate phase, and by 1/8s during the fourth deintegrate phase. The results counter's contents transfers to the results register at each conversion end.

Differential Reference Inputs

The reference inputs accept voltages anywhere within the converter's power-supply voltage range.

The main source of rollover error is common-mode voltage, which is caused by the reference capacitor losing or gaining charge to stray capacitance. A positive signal with a large common-mode voltage can cause the reference capacitor to gain charge (increase voltage). In contrast, the reference capacitor will lose charge (decrease voltage) when deintegrating a negative input signal. The rollover error is a direct result of the difference in reference for positive or negative input voltages. Use an optimum reference capacitor to hold rollover error under one-half count for worst-case conditions (see *Components* section). A common-mode voltage near or at AGND minimizes rollover error caused by these sources.

Differential Input

Acceptable differential input voltages are dictated by the input amplifier's common-mode range (specifically from 1.5V below the positive supply to 1.5V above the negative supply). For optimum performance, the input voltage at IN HI and IN LO should not come within 2V of either the positive or negative supply. Do not saturate the integrator output, since the integrator also swings with the common-mode voltage.

Conversion Phases

For this section of an explanation of conversion phases refer to figures 5, and 8.

Integrate Phase

The MAX135 integrates the input signal by connecting the noninverting input of the integrator to IN LO and the buffer input to IN HI. The integration period is 545 counts for 60Hz mode and 655 counts for 50Hz mode.

Deintegrate Phase

The voltage polarity on the integrator capacitor at the end of integrate phase determines the polarity of the first deintegration phase. The first deintegrate phase ends when the comparator detects the integrator capacitor discharge. The MAX135 then goes into a rest phase, where both the buffer input and the integrator's noninverting input connect to AGND, integrating the system offset.

Near the end of the maximum allowable deintegration period, the integrator capacitor's voltage polarity is again sampled, resulting in either a positive or negative deintegrate cycle.

Rest Phase

A rest phase follows each deintegrate phase. Rest phase starts when the integrator crosses zero and ends when the maximum count for that deintegrate phase is reached.

Times-Eight Phase

When a zero crossing is detected at the end of the deintegrate phase , deintegration continues until the next clock cycle. This causes the integrator to overshoot zero crossing slightly, leaving a small residual voltage on the integrator capacitor. The times-eight (X8) phase inverts and multiplies this residual by a factor of 8.

Second Deintegrate Phase

The second deintegrate phase deintegrates the residual voltage on the integrator capacitor that has been through the X8 phase. Since the voltage across the integrator capacitor has been multiplied by 8, each clock cycle of deintegration corresponds to 1/8 of one clock cycle during the first deintegration.

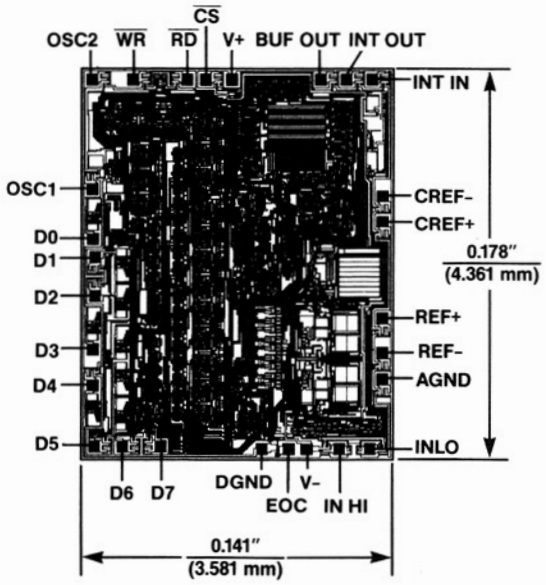
Additional Times-Eight and Deintegrate Phases

At the end of the second and third deintegrate phases, the device X8 multiplies the residual voltage left on the integrator capacitor. A deintegration occurs after each of these X8 multiplications, resulting in a second, third, and fourth deintegrate phase. Each time the integrator capacitor's residual voltage is multiplied by 8, the following deintegrate phase has 8X finer resolution.

Zero-Integrate Phase

The zero-integrate phase zeros out the integrator to prepare for the next integration (Figure 8). This phase occurs at the beginning and end of each conversion. At power-up or in the hold mode prior to a conversion, the MAX135 continues to zero integrate until a conversion starts. When a conversion starts in 60Hz mode, another 111 clocks of zero integrate are completed before a conversion begins. In 50Hz mode, only one additional zero integrate is performed before the conversion starts. An additional 20 clocks of zero integrate occur at each conversion end.

Chip Topography



15-Bit ADC with Parallel Interface

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