LatticeEC™ Advanced Evaluation Board – Revision C

User's Guide

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Introduction

The LatticeEC Advanced Evaluation Board provides a convenient platform to evaluate, test, and debug designs with the support of LatticeEC advanced interface capabilities. The board provides easy access to PCI, DDR SDRAM, FCDRAM and SPI4.2 interfaces. The information in this document pertains only to boards marked as 'Rev C'. This marking is located on the front of the board, beneath the Lattice logo.

Features

- Required voltages supplied by PCI or one external 5V DC supply
- ispVM® System programming support
- SPI3 Flash device included for non-volatile configuration storage
- ispDOWNLOAD® cable included
- 5V AC adapter included
- PCI edge connector (120-pin) for 32-bit PCI interface
- SODIMM socket supporting 16-bit, 200MHz 200-pin DDR SDRAM
- Onboard FCRAM
- SPI4.2 interface via VHDM connectors
- Prototyping area with access to over 150 I/O pins
- SMA connectors included (10) for high-speed clock and data interfacing

Figure 1. LatticeEC Advanced Evaluation Board

Electrical, Mechanical and Environmental Specifications

The nominal board dimensions are 9 inches by 4.2 inches. The environmental specifications are as follows:

- Operating temperature: 0ºC to 55ºC
- Storage temperature: -40ºC to 75ºC
- Humidity: < 95% without condensation
- 5V DC input (+/- 10%) up to 4A, or 3.3V input from PCI backplane

Additional Resources

Additional resources related to this board can be downloaded from the web at www.latticesemi.com/boards. Click on the appropriate evaluation board, then see the blue "Resources" box on the right of the screen for items such as: updated documentation, software, sample designs, IP evaluation bitstreams, and more.

Table 1. Embedded Functions

Description	Source	LatticeEC Pin	Notes
33.33MHz clock	On-Board oscillator	F6 / AF14	3.3V TTL Output

The 3.3V oscillator socket accepts both full-size and half-size oscillators and can route to different clock inputs, depending on its position within the socket. The 16-pin socket will allow connection to PLL clock pin F6 when the bottom of the oscillator is aligned to socket pins 8 and 9. When the top of the oscillator is aligned to socket pins 1 and 16, the clock is provided to primary clock pin AF14.

LatticeEC Device

This board features a LatticeEC FPGA with a 1.2V DC core. It can accommodate all pin compatible LatticeEC devices in the 672-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeECP/EC Family Data Sheet on the Lattice web site at www.latticesemi.com.

Note: The connection tables listed in this document refer to the LFEC20E device. Available I/Os and associated sysIO™ banks may differ for other densities within this device family.

Programming Headers

Two programming headers are provided on the evaluation board, providing access to the LatticeEC JTAG port or the SPI Flash device. The pinouts for the headers are provided in Table 2.

Table 2. JTAG Programming Headers

Function	JP6 (1x10)	JP8 (2x5)
Vcc (3.3V)	1	6
TDO	2	7
TDI / SFLASH_D	3	5
ISPEN_N / SFLASH_S_N	4	10
DONE	5	9
TMS	6	3
TCK / SFLASH_C	8	1
INITN	10	8
GND	7, 9	2, 4

Note: When using a 1x8 download cable, connect to the 1x10 header by justifying the alignment to pin 1 (V_{CC}).

A jumper installed on JP7 provides a connection between the configuration clock (CCLK) and a general-purpose I/O. JP7 must be installed to program the SPI Serial Flash through the LatticeEC device using JTAG; the jumper must be removed to configure the LatticeEC device from SPI Flash (see the section in this document entitled SPI Flash Download via JTAG). This evaluation board utilizes DOUT as the GPIO. When designing your own board choose the pin that is listed in Lattice technical note TN1078, *SPI Serial Flash Programming Using ispJTAG on LatticeECP/EC FPGAs* for your particular density and package

Power Setup

For stand-alone board operation (i.e. outside of a PCI backplane), the evaluation board may be supplied with a single 5V DC power supply. On-board regulators will provide the supply voltages necessary for each component. The adjustable voltage supply (V_{CCADJ}) is set by the potentiometer located at R32 within the approximate range of 1.22V to 3.26V.

The 5V DC power may be applied using the power jack at J22 or the banana jacks at J21 (5V DC) and J20 (GND). The requirements for power jack J22 are listed in Table 3.

Table 3. Power Jack J22 Specifications

Polarity	Positive Center
Inside Diameter	0.1" (2.5mm)
Outside Diameter	0.218" (5.5mm)
Current Capacity	4A

Power may also be supplied directly for each individual supply rail using banana jack connectors. To enable this mode of operation, the appropriate fuses must be removed. All power sources must be regulated to the specifications in Table 4. No special power sequencing is required for the evaluation board.

Table 4. Individual Control of Supplies

Supply	Jack	Fuse	Requirement
3.3V	J18	F3 (1.5A)	+/- 0.3V
2.5V / 2.6V	J16	F1 (3A)	+/- 10%
1.2V	J17	F2 (3A)	+/- 5%
VCC_ADJ	J19	F4 (1.5A)	User-Defined

When the evaluation board is inserted into a PCI backplane, all onboard power will be derived from the PCI 3.3V power rail. The onboard 3.3V regulator (U5) will then be automatically be disabled, allowing power to be supplied directly from the PCI host system.

Jumper J32 allows the adjustment of the 2.5V power supply for 2.6V operation. This may be necessary for compatibility with high-speed DDR memory modules. A jumper in position 1-2 provides a nominal 2.5V supply. To increase the voltage to 2.6V, place the jumper in position 2-3.

Jumpers JP2, JP3, JP4, and JP5 allow the user to select the voltage (V_{CCIO}) applied to the eight I/O banks of the FPGA, as shown in Table 5.

Note: Care must be exercised to insure that only one voltage is strapped to each bank and certain restrictions apply depending on which features of the board are being used.

Table 5. V_{CCIO} Selection Jumper

	JP2	JP3	JP4	JP5
	3.3V	1.2V	2.5V / 2.6V	Adjustable
VCCIO 0 (Bank0)	O O	O O	O O	O O
VCCIO 1	O O	O O	O O	O O
VCCIO 2	O O	O O	O O	O O
VCCIO 3	O O	O O	O O	O O
VCCIO 4	O O	O O	O O	O O
VCCIO 5	O O	O O	O O	O O
VCCIO 6	O O	O O	O O	O O
VCCIO 7 (Bank7)	O O	O O	O O	O O

Note: Shown with factory default settings.

Depending on the optional devices installed, some sysIO banks may have restrictions.

Table 6. sysIO Bank Considerations

Bank	Setting
0	2.5V only (FCRAM interface)
1	2.5V/2.6V if DDR SDRAM installed in socket J11
2	2.5V if SPI4.2 interface used
3	2.5V if SPI4.2 interface used, 3.3V if SPI3 configuration mode used[1].
4	3.3V when PCI interface used
5	3.3V when PCI interface used
6	Any
7	Any

1. The LatticeEC Advanced Evaluation Board connects 2.5V to the V_{CCIO} of Bank 3 to maximize functionality of the board with the SPI4.2 interface in the same bank as the sysCONFIG™ port. For optimum sysIO compatibility, 3.3V V_{CCIO} is recommended for the sysCONFIG port when interfacing to SPI3 Flash memory devices.

The following tables detail the various standards supported by the LatticeEC FPGA Input/Output (sysIO) structures. More information can be found in Lattice technical note number TN1056, *LatticeECP/EC sysIO Usage Guide*, available on the Lattice web site at www.latticesemi.com.

Table 7. Mixed Voltage Support

	Input sysIO Standards					Output sysIO Standards				
V_{CCIO}	1.2V	1.5V	1.8V	2.5V	3.3V	1.2V	1.5V	1.8V	2.5V	3.3V
1.2V	Yes			Yes	Yes	Yes				
1.5V	Yes	Yes		Yes	Yes		Yes			
1.8V	Yes		Yes	Yes	Yes			Yes		
2.5V	Yes			Yes	Yes				Yes	
3.3V	Yes			Yes	Yes					Yes

For example, if V_{CCIO} is connected to 3.3V, the input threshold for any pin within that sysIO bank may be configured as 1.2V, 2.5V or 3.3V. Outputs are driven to the levels present on V_{CCIO}.

Table 8. sysIO Standards Supported per Bank

Description	Top Side Banks 0-1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
Types of I/O Buffers	Single-ended	Single-ended and Differential	Single-ended	Single-ended and Differential
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I, III HSTL18_I, II, III SSTL18D Class I, SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I, III, HSTL18D Class I, III PCI33 LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I, III HSTL18 Class I, II, III SSTL18D Class I, SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I, III HSTL18D Class I, III PCI33 LVDS LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I, III HSTL18 Class I, II, III SSTL18D Class I, SSTL25D Class I, II, SSTL33D Class I, II HSTL15D Class I, III HSTL18D Class I, III PCI33 LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I, III HSTL18 Class I, II, III SSTL18D Class I, SSTL25D Class I, II, SSTL33D_I, II HSTL15D Class I, III HSTL18D Class I, III PCI33 LVDS LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]
Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
Clock Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
PCI Support	PCI33 with clamp	PCI33 no clamp	PCI33 with clamp	PCI no clamp
LVDS Output Buffers		LVDS (3.5mA) Buffers		LVDS (3.5mA) Buffers

1. These differential standards are implemented by using complementary LVCMOS driver with external resistor pack.

PCI

The LatticeEC Evaluation Board is designed to interface directly to PCI 2.2 compatible systems using the PCI edge connector. All necessary signals required for 32-bit PCI operation are provided to the connector, as shown in Tables 9 and 10.

Table 9. PCI Connections – Solder Side

J23	Description	LatticeEC Pin	sysIO Bank
6	PCI_INTA_N	AB12	5
7	PCI_INTC_N	Y12	5
15	PCI_RST_N	AC13	5
17	PCI_GNT_N	AB13	4
20	PCI_AD30	AD14	4
22	PCI_AD28	AB14	4
23	PCI_AD26	Y14	4
25	PCI_AD24	AE15	4
26	PCI_IDSEL	AC15	4
28	PCI_AD22	AA15	4
29	PCI_AD20	AF16	4
31	PCI_AD18	AD16	4
32	PCI_AD16	AB16	4
34	PCI_FRAME_N	Y16	4
36	PCI_TRDY_N	AE17	4
38	PCI_STOP_N	AC17	4
43	PCI_PAR	Y17	4
44	PCI_AD15	AE18	4
46	PCI_AD13	AC18	4
47	PCI_AD11	AA18	4
49	PCI_AD9	AF19	4
52	PCI_CBE0_N	AA19	4
54	PCI_AD6	AE20	4
55	PCI_AD4	AF21	4
57	PCI_AD2	AF22	4
58	PCI_AD0	AF23	4
60	PCI_REQ64_N	AA13	4

Table 10. PCI Connections – Component Side

J6	Description	LatticeEC Pin	sysIO Bank
7	PCI_INTB_N	AA12	5
8	PCI_INTD_N	AF13	5
9	PCI_PRSNT1_N	AE13	5
11	PCI_PRSNT2_N	AD13	5
16	PCI_CLK	W1	6
18	PCI_REQ_N	AA13	4
20	PCI_AD31	AE14	5
21	PCI_AD29	AC14	4
23	PCI_AD27	AA14	4
24	PCI_AD25	AF15	4
26	PCI_CBE3_N	AD15	4
27	PCI_AD23	AB15	4
29	PCI_AD21	Y15	4
30	PCI_AD19	AE16	4
32	PCI_AD17	AC16	4
33	PCI_CBE2_N	AA16	4
35	PCI_IRDY_N	AF17	4
37	PCI_DEVSEL_N	AD17	4
40	PCI_PERR_N	AB17	4
42	PCI_SERR_N	AA17	4
44	PCI_CBE1_N	AF18	4
45	PCI_AD14	AD18	4
47	PCI_AD12	AB18	4
48	PCI_AD10	Y18	4
52	PCI_AD8	AE19	4
53	PCI_AD7	AF20	4
55	PCI_AD5	AA20	4
56	PCI_AD3	AE21	4
58	PCI_AD1	AE22	4
60	PCI_ACK64_N	AF24	4

SPI 4.2

Provided for SPI 4.2 interfaces are two 6x10 backplane connectors. Connector J15 includes necessary data pairs and control signals for transmit data, while J14 has been configured for receive data. Standard 100-ohm differential termination is provided for all applicable receive signal pairs.

Table 11. SPI4.2 Transmit Connections

J15	Description	LatticeEC Pin	sysIO Bank
A1	SPI4_TDAT_P0	AA26	3
A2	SPI4_TDAT_P2	U25	3
A3	SPI4_TDAT_P4	T26	3
A4	SPI4_TDAT_P6	T21	3
A7	SPI4_TDAT_P8	R23	3
A8	SPI4_TDAT_P10	P26	3
A9	SPI4_TDAT_P12	P22	3
A10	SPI4_TDAT_P14	N22	3
B1	SPI4_TDAT_N0	AB26	3
B2	SPI4_TDAT_N2	U24	3
B3	SPI4_TDAT_N4	T25	3
B4	SPI4_TDAT_N6	U21	3
B7	SPI4_TDAT_N8	T24	3
B8	SPI4_TDAT_N10	R26	3
B9	SPI4_TDAT_N12	P23	3
B10	SPI4_TDAT_N14	N23	3
C5	SPI4_TSCLK	AC24	3
C6	SPI4_TSTAT0	AC26	3
C10	SPI4_TCTL_P	N24	3
D6	SPI4_TSTAT1	AC25	3
D10	SPI4_TCTL_N	N25	3
E1	SPI4_TDAT_P1	U22	3
E2	SPI4_TDAT_P3	U26	3
E3	SPI4_TDAT_P5	T23	3
E4	SPI4_TDAT_P7	R22	3
E5	SPI4_TDCLK_P	AA25	3
E7	SPI4_TDAT_P9	R24	3
E8	SPI4_TDAT_P11	P24	3
E9	SPI4_TDAT_P13	P21	3
E10	SPI4_TDAT_P15	M26	3
F1	SPI4_TDAT_N1	U23	3
F2	SPI4_TDAT_N3	V26	3
F3	SPI4_TDAT_N5	T22	3
F4	SPI4_TDAT_N7	R21	3
F5	SPI4_TDCLK_N	AB25	3
F7	SPI4_TDAT_N9	R25	3
F8	SPI4_TDAT_N11	P25	3
F9	SPI4_TDAT_N13	N21	3
F10	SPI4_TDAT_N15	N26	3

Table 12. SPI4.2 Receive Connections

J14	Description	LatticeEC Pin	sysIO Bank	Notes
A1	SPI4_RDAT_P14	L21	2	100-ohm LVDS termination
A2	SPI4_RDAT_P12	L24	2	100-ohm LVDS termination
A3	SPI4_RDAT_P10	K22	2	100-ohm LVDS termination
A4	SPI4_RDAT_P8	K26	2	100-ohm LVDS termination
A7	SPI4_RDAT_P6	G25	2	100-ohm LVDS termination
A8	SPI4_RDAT_P4	H26	2	100-ohm LVDS termination
A9	SPI4_RDAT_P2	G22	2	100-ohm LVDS termination
A10	SPI4_RDAT_P0	D25	2	100-ohm LVDS termination
B1	SPI4_RDAT_N14	M21	2	100-ohm LVDS termination
B2	SPI4_RDAT_N12	L25	2	100-ohm LVDS termination
B3	SPI4_RDAT_N10	K21	2	100-ohm LVDS termination
B4	SPI4_RDAT_N8	L26	2	100-ohm LVDS termination
B7	SPI4_RDAT_N6	F25	2	100-ohm LVDS termination
B8	SPI4_RDAT_N4	J26	2	100-ohm LVDS termination
B9	SPI4_RDAT_N2	F21	2	100-ohm LVDS termination
B10	SPI4_RDAT_N0	D26	2	100-ohm LVDS termination
C1	SPI4_RCTL_P	M23	2	100-ohm LVDS termination
C5	SP4_RSTAT0	C25	2	
C6	SPI4_RSCLK	D23	2	
D1	SPI4_RCTL_N	M22	2	100-ohm LVDS termination
D5	SPI4_RSTAT1	C26	2	
E1	SPI4_RDAT_P15	M24	2	100-ohm LVDS termination
E2	SPI4_RDAT_P13	L23	2	100-ohm LVDS termination
E3	SPI4_RDAT_P11	J20	2	100-ohm LVDS termination
E4	SPI4_RDAT_P9	K24	2	100-ohm LVDS termination
E6	SPI4_RDCLK_P	H24	2	100-ohm LVDS termination
E7	SPI4_RDAT_P7	J25	2	100-ohm LVDS termination
E8	SPI4_RDAT_P5	J24	2	100-ohm LVDS termination
E9	SPI4_RDAT_P3	G21	2	100-ohm LVDS termination
E10	SPI4_RDAT_P1	G23	2	100-ohm LVDS termination
F1	SPI4_RDAT_N15	M25	2	100-ohm LVDS termination
F2	SPI4_RDAT_N13	L22	2	100-ohm LVDS termination
F3	SPI4_RDAT_N11	K20	2	100-ohm LVDS termination
F4	SPI4_RDAT_N9	K23	2	100-ohm LVDS termination
F6	SPI4_RDCLK_N	H23	2	100-ohm LVDS termination
F7	SPI4_RDAT_N7	K25	2	100-ohm LVDS termination
F8	SPI4_RDAT_N5	H25	2	100-ohm LVDS termination
F9	SPI4_RDAT_N3	H21	2	100-ohm LVDS termination
F10	SPI4_RDAT_N1	G24	2	100-ohm LVDS termination

DDR SDRAM

The included 200-pin SODIMM socket provides a built-in 16-bit interface to standard 2.5V DDR SDRAM memory modules. The required V_{REF} and V_{TT} voltages, as well as termination of each signal to $V_{TT,}$ are provided.

Table 13. DDR Interface to SODIMM Socket

J11	Description	LatticeEC Pin	sysIO Bank
5	SODIMM_DQ7	C15	1
6	SODIMM_DQ0	G14	1
7	SODIMM_DQ6	B16	1
8	SODIMM_DQ1	F14	1
11	SODIMM_DQS0	G15	1
12	SODIMM_DM0	F15	1
13	SODIMM_DQ3	D15	1
14	SODIMM_DQ4	E14	1
17	SODIMM_DQ2	E15	1
18	SODIMM_DQ5	C14	1
19	SODIMM_DQ11	F17	1
20	SODIMM_DQ12	D16	1
23	SODIMM_DQ8	G16	1
24	SODIMM_DQ13	C16	1
25	SODIMM_DQS1	A20	1
26	SODIMM_DM1	E16	1
29	SODIMM_DQ10	G17	1
30	SODIMM_DQ15	C17	1
31	SODIMM_DQ9	F16	1
32	SODIMM_DQ14	D17	1
35	SODIMM_CK0	A15	1
37	SODIMM_CK0_N	B15	1
95	SODIMM_CKE1	E17	1
96	SODIMM_CKE0	B17	1
99	SODIMM_A12	D19	1
100	SODIMM_A11	A18	1
101	SODIMM_A9	E18	1
102	SODIMM_A8	B18	1
105	SODIMM_A7	F18	1
106	SODIMM_A6	D18	1
107	SODIMM_A5	F19	1
108	SODIMM_A4	C18	1
109	SODIMM_A3	G18	1
110	SODIMM_A2	A19	1
111	SODIMM_A1	G19	1
112	SODIMM_A0	B19	1
115	SODIMM_A10	E20	1
116	SODIMM_BA1	B20	1
117	SODIMM_BA0	B21	1
118	SODIMM_RAS_N	A21	1

Table 13. DDR Interface to SODIMM Socket (Continued)

J11	Description	LatticeEC Pin	sysIO Bank
119	SODIMM_WE_N	B22	1
120	SODIMM_CAS_N	A22	1
121	SODIMM_S0_N	A23	1
122	SODIMM_S1_N	A24	1

FCRAM

Included with the evaluation board is a 256Mb (8Mb x 4 x 8-bit) FCRAM device. All necessary voltages and signal terminations are supplied.

Table 14. FCRAM Connections

U1	Description	LatticeEC Pin	sysIO Bank
2	FCRAM_DQ0	A14	0
5	FCRAM_DQ1	B14	0
8	FCRAM_DQ2	A13	0
11	FCRAM_DQ3	B13	0
21	FCRAM_A14	A11	0
22	FCRAM_A13	B11	0
23	FCRAM_FN	C11	0
24	FCRAM_CS_N	D11	0
26	FCRAM_BA0	A10	0
27	FCRAM_BA1	B10	0
28	FCRAM_A10	C10	0
29	FCRAM_A0	D10	0
30	FCRAM_A1	A9	0
31	FCRAM_A2	B9	0
32	FCRAM_A3	C9	0
35	FCRAM_A4	G10	0
36	FCRAM_A5	F10	0
37	FCRAM_A6	E10	0
38	FCRAM_A7	G11	0
39	FCRAM_A8	F11	0
40	FCRAM_A9	E11	0
41	FCRAM_A11	G12	0
42	FCRAM_A12	E12	0
44	FCRAM_PD_N	F13	0
45	FCRAM_CLK	A2	0
46	FCRAM_CLK_N	A3	0
51	FCRAM_DQS	F12	0
56	FCRAM_DQ4	D12	0
59	FCRAM_DQ5	C12	0
62	FCRAM_DQ6	B12	0
65	FCRAM_DQ7	A12	0

Proto Area

For general purpose I/Os, numerous test points are provided for direct access. The test points are labeled according to the associated I/O pin location and are listed in Table 15.

Table 15. LatticeEC Pins Accessible at Test Points

A4 (0)	C8 (0)	F7 (0)	K3 (7)	N6 (6)	U1[1] (6)	AA11 (5)	AE11 (5)
A5 (0)	D1[2] (7)	F8 (0)	K4 (7)	P1[1] (6)	U2 (6)	AB4 (6)	AE12 (5)
A6 (0)	D2 (7)	F9 (0)	K5 (7)	P2 (6)	U3 (6)	AB6 (5)	AE2 (5)
A7 (0)	D4 (0)	G1[2] (7)	K6 (7)	P3 (6)	U4 (6)	AB7 (5)	AE3 (5)
A8 (0)	D6 (0)	G2 (7)	L1 (7)	P4 (6)	U5 (6)	AB8 (5)	AE5 (5)
A16 (1)	D7 (0)	G3 (7)	L2 (7)	P5 (6)	V1[1] (6)	AB9 (5)	AE6 (5)
A17 (1)	D8 (0)	G4 (7)	L3 (7)	P6 (6)	V2 (6)	AB10 (5)	AE7 (5)
B1[2] (7)	D9 (0)	G6 (7)	L4 (7)	R1[1] (6)	W2 (6)	AB11 (5)	AE8 (5)
B3 (0)	E1[2] (7)	G7 (0)	L5 (7)	R2 (6)	W21 (3)	AC4 (6)	AE9 (5)
B4 (0)	E2 (7)	G8 (0)	L6 (6)	R3 (6)	W22 (3)	AC5 (5)	AF2 (6)
B5 (0)	E3 (7)	G9 (0)	L7 (6)	R4 (6)	Y8 (5)	AC6 (5)	AF3 (5)
B6 (0)	E4 (7)	H1[2] (7)	M1 (7)	R5 (6)	Y9 (5)	AC7 (5)	AF5 (5)
B7 (0)	E6 (0)	H4 (7)	M2 (7)	R6 (6)	Y10 (5)	AC8 (5)	AF6 (5)
B8 (0)	E7 (0)	J1[2] (7)	M3 (7)	T1[1] (6)	Y11 (5)	AC9 (5)	AF7 (5)
C1[2] (7)	E8 (0)	J4 (7)	M4 (7)	T2 (6)	AA6 (5)	AC10 (5)	AF8 (5)
C4 (0)	E9 (0)	J5 (7)	M5 (6)	T3 (6)	AA7 (5)	AC11 (5)	AF9 (5)
C5 (0)	F1[2] (7)	J6 (7)	M6 (6)	T4 (6)	AA8 (5)	AC12 (5)	AF10 (5)
C6 (0)	F2 (7)	K1 (7)	N4 (6)	T5 (6)	AA9 (5)	AC23 (3)	AF11 (5)
C7 (0)	F3 (7)	K2 (7)	N5 (6)	T6 (6)	AA10 (5)	AE10 (5)	AF12 (5)

Note: sysIO Bank indicated in parenthesis.

1. Also connected to SW1. See Table 16 for details.
2. Also connected to LEDs. See Table 18 for details.

Switches

Switch 1 (SW1) on the left side of the board is an eight-switch block that is part of the prototyping area. The pull-up resistors associated with SW1 are wired to 2.5V, but any I/O voltage up to 3.3V may be used. A switch in the down position produces a low (0), the up position produces a high (1). Table 16 shows the connections to the LatticeEC I/O pins.

Table 16. SW1 Connections

Switch	I/O Ball	sysIO Bank
SW1(1)	V1	6
SW1(2)	U1	6
SW1(3)	T1	6
SW1(4)	R1	6
SW1(5)	P1	6
SW1(6)	M1	7
SW1(7)	L1	7
SW1(8)	K1	7

SW2 is a momentary switch that the user can define for any purpose, such as a global reset. SW2 is wired to I/O ball E23 (bank 4) and applies a low logic level when depressed.

SW3 is a momentary switch that, when pressed, forces the FPGA to start its programming cycle.

SW4, when in position 1 (up), connects the download cable to the SPI Flash so that the user can program the Flash. When SW4 is in position 2 (down) the SPI Flash is connected to the LatticeEC FPGA; pressing and releasing SW3 (assuming the configuration switch, SW5, is properly set) will configure the FPGA. The FPGA may be accessed via the ispJTAG, using J6, no matter which position SW4 is in.

SW5 determines which type of device the FPGA expects to receive programming information from and whether the FPGA will be master or slave during the transfer. Table 17 lists the possible configuration modes. A switch in the down position produces a low (0), the up position produces a high (1).

Table 17. LatticeEC Configuration Settings

SW5-1	SW5-2	SW5-3	Configuration Mode
0	0	0	SPI3 Flash
0	0	1	SPIX Flash
1	0	0	Master Serial
1	0	1	Slave Serial
1	1	0	Master Parallel
1	1	1	Slave Parallel
X	X	X	ispJTAG (always available)

LEDs

Eight user-definable LEDs are provided on the upper left side of the board above SW1. These LEDs are each wired to a separate general purpose I/O as defined in Table 18. The current limiting resistors associated with these LEDs are wired to 2.5V but any I/O voltage up to 3.3V may be used. The LED will light when its associated I/O pin is driven low.

Table 18. LEDs

LED	I/O Ball	sysIO Bank
D1	B1	7
D2	C1	7
D3	D1	7
D4	E1	7
D5	F1	7
D6	G1	7
D7	H1	7
D8	J1	7

Miscellaneous

Ten SMA connectors are provided for clocks or general purpose, user-definable signals. The center pin is wired to an I/O pin and the outer case is soldered to ground. Table 19 details to which I/O pin each SMA connector is wired.

Table 19. SMA Connectors

Location	I/O Ball	sysIO Bank	Description
J2	Y1	6	GP I/O (T)
J3	Y2	6	GP I/O (C)
J4	V6	6	PLL FB T, GP I/O
J5	W6	6	PLL FB C, GP I/O
J7	N2	7	PCLKT, GP I/O
J8	N1	7	PCLKC, GP I/O
J9	AE4	5	GP I/O (T)
J10	AF4	5	GP I/O (C)
J12	W24	3	PLL IN T, GP I/O
J13	W23	3	PLL IN C, GP I/O

Note: T and C can be used as a differential pair.

One RJ-45 female connector is provided for general-purpose interfacing to the LatticeEC device. The connections are listed in Table 20.

Table 20. RJ-45 Connections

J1	LatticeEC Pin	sysIO Bank	Description
1	AA1	6	GP I/O (T), LDQS45
2	AB1	6	GP I/O (C)
3	Y4	6	GP I/O (T)
4	Y3	6	GP I/O (C)
5	W4	6	GP I/O (C)
6	W3	6	GP I/O (T)
7	AB2	6	GP I/O (C)
8	AC1	6	GP I/O (T)

Download Procedures

Requirements:

- PC with ispVM System v.14.3 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable).

  Note: An option to install these drivers is included as part of the ispVM System setup.

- ispDOWNLOAD Cable (pDS4102-DL2A, HW7265-DL3A, HW-USB-1A, etc.)

JTAG Download

The LatticeEC device can be configured easily via its JTAG port. The device is SRAM-based, so the it must remain powered on to retain its configuration when programmed in this fashion.

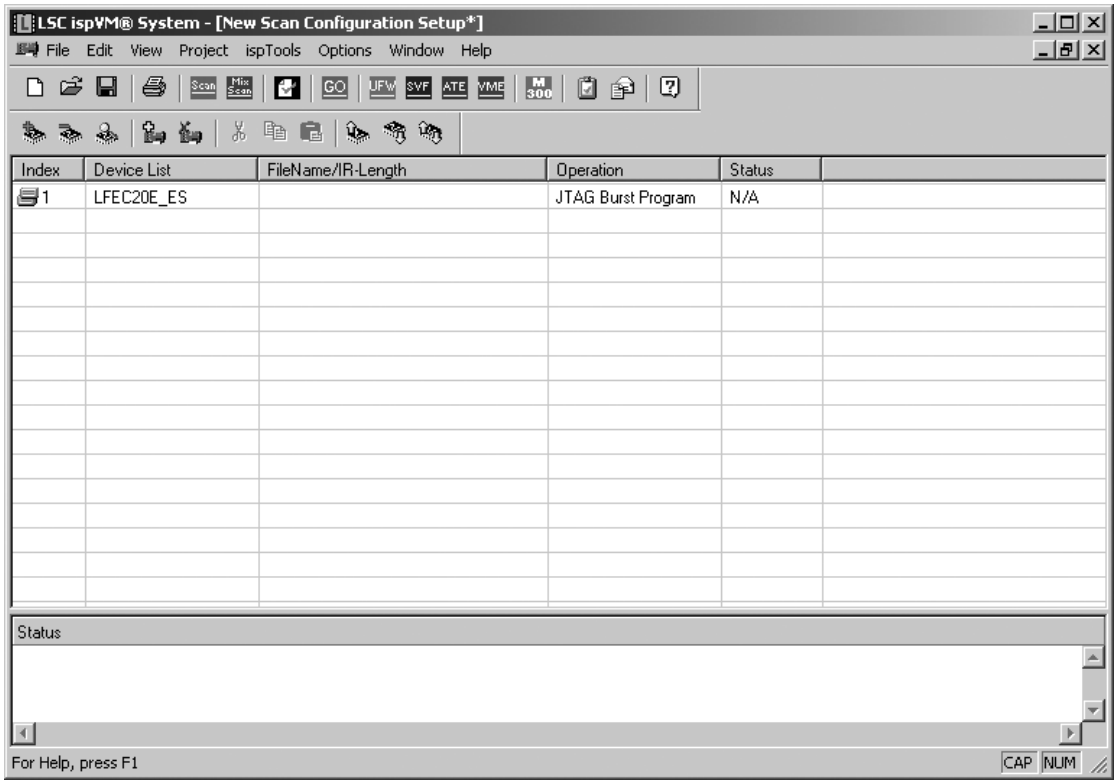
1. Connect the ispDOWNLOAD cable to the appropriate header. JP6 is used for the 1x10 cable, while JP8 is used for the 2x5 version.

Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP/EC FPGA device and render the board inoperable.*

When using a 1x8 download cable, connect to the 1x10 header by justifying the alignment to pin 1 (V_{CC}).

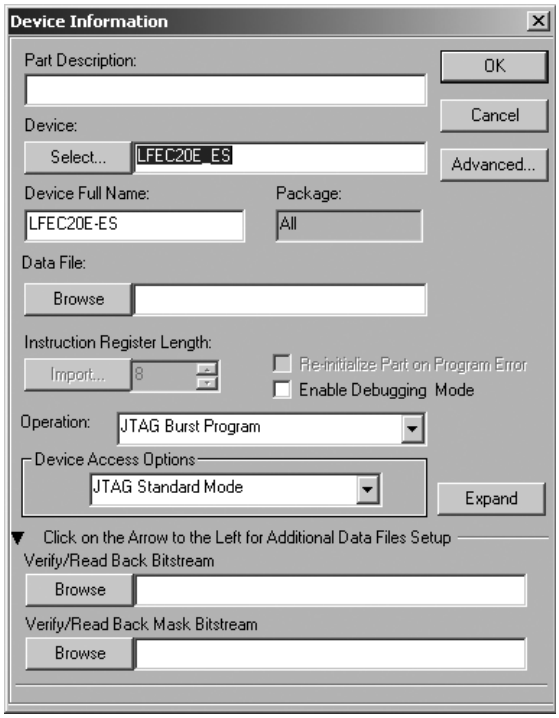
2. Connect the LatticeEC Evaluation Board to an external 5V supply.
3. Start the ispVM System software.
4. Press the 'SCAN' button located in the toolbar. The LatticeEC device should be automatically detected. The resulting screen should be similar to Figure 2.

Figure 2. ispVM System Interface



5. Double-click the device to open the device information dialog, as shown in Figure 3. In the device information dialog, click the Browse button located under 'Data File'. Locate the desired bitstream file (.bit). Click OK to both dialog boxes.

Figure 3. Device Information Dialog



6. Click the green 'GO' button. This will begin the download process into the device.
7. Upon successful download, the device will be operational.

SPI Flash Download

For non-volatile storage of configuration memory, the LatticeEC device features an interface compatible with low-cost SPI3 Flash memory devices. ispVM System has the capability to program the SPI3 Flash device directly. During the LatticeEC power-up cycle, the data stored in the SPI3 Flash device is automatically read into configuration memory.

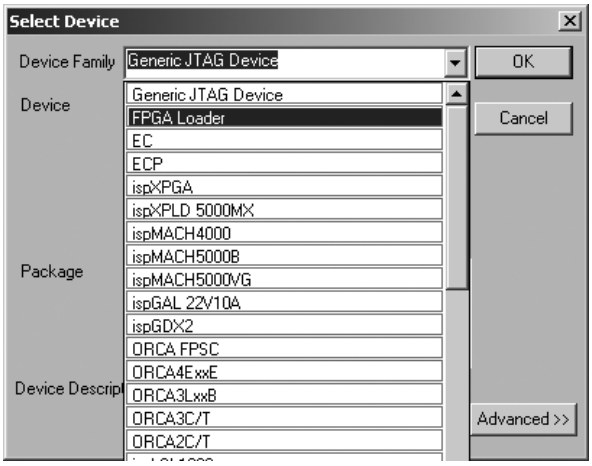
1. Set switch SW5 to "000". This enables SPI3 mode by setting the CFG pins of the LatticeEC device.
2. Set switch SW4 to position 1 (up) to enable the SPI3 connections from the programming headers directly to the SPI3 device.
3. Connect the ispDOWNLOAD cable to the appropriate header. JP6 is used for the 1x10 cable, while JP8 is used for the 2x5 version.

   Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP/EC FPGA device and render the board inoperable.*

   When using a 1x8 download cable, connect to the 1x10 header by justifying the alignment to pin 1 (V_{CC}).
4. Connect the evaluation board to an external 5V supply.
5. Start the ispVM System software.
6. Create a new chain file (File->New).

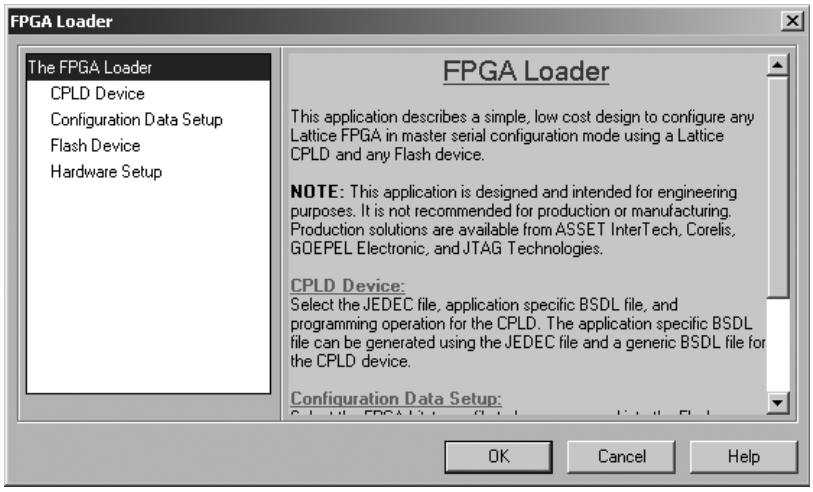
7. Insert a new device into the chain (Edit->Add Device).
8. In the resulting Device Information dialog, shown in Figure 4, press the 'Select' button.

Figure 4. Device Selector Dialog



9. Use the pull-down menu to in the 'Device Family' field to choose the device 'FGPA Loader'. Press OK. The resulting dialog should resemble Figure 5.

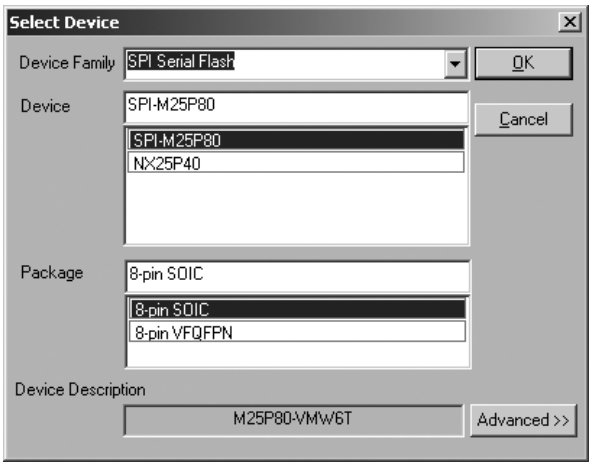
Figure 5. FPGA Loader Setup



10. Choose the 'Flash Device' page and press the 'Select' button.
11. Select the 'SPI Serial Flash' family and choose the device SPI-M25P80, as shown in Figure 6. Press OK.

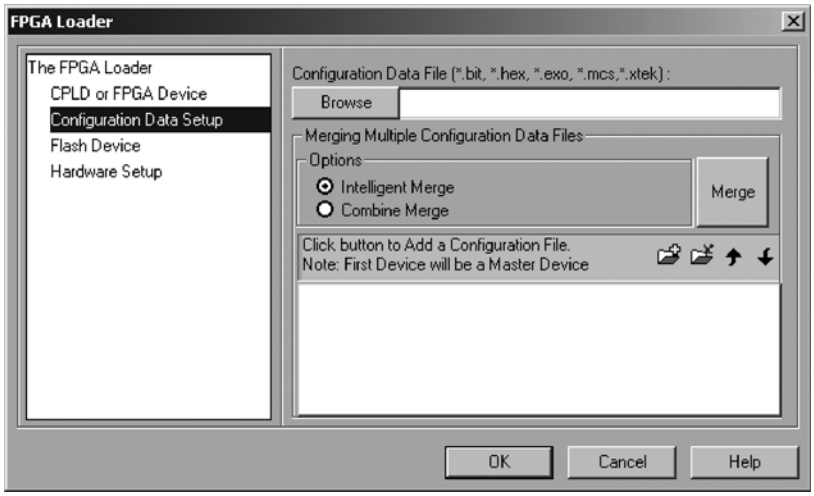
    Note: It may be necessary to select an alternate SPI3 Flash device, as the part number is subject to change.

Figure 6. SPI Device Selection



12. Choose the 'Configuration Data Setup' page, as shown in Figure 14.

Figure 7. Configuration Data Setup Page



13. Click the 'Browse' button near the top of the window. Browse to the desired bitstream (.bit) file, created by the Lattice ispLEVER® design tool.
14. Press OK to exit the FPGA Loader setup.
15. Click the green 'GO' button. This will begin the download process into the Flash device.
16. Once the download is complete, toggle switch SW4 to position 2 to restore the SPI3 Flash connections to the LatticeEC device.
17. Cycle the board power. The data should automatically transfer from the Flash to the FPGA.

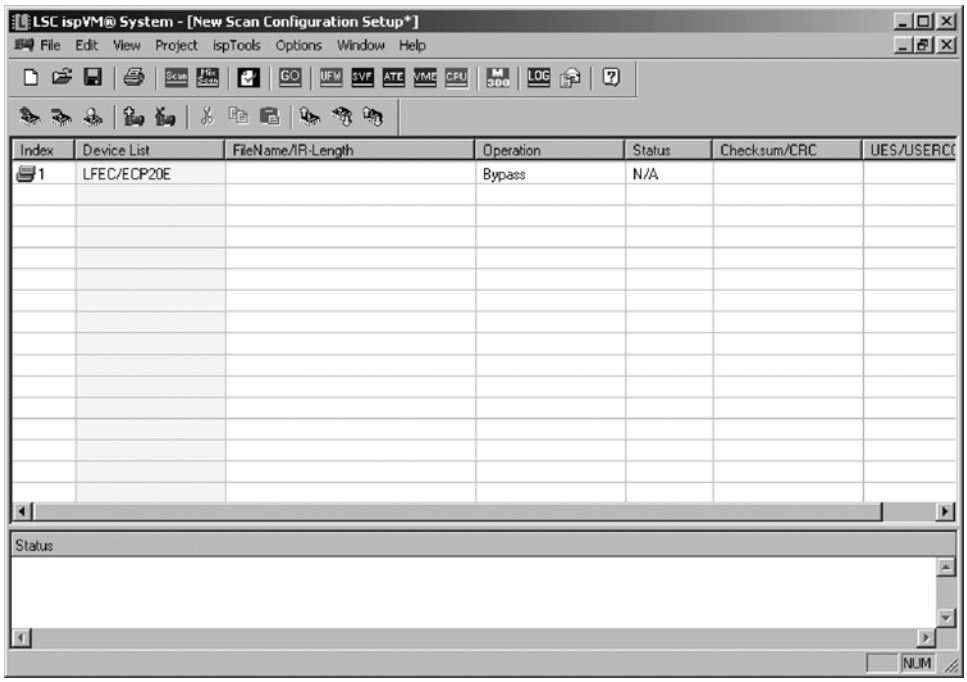
SPI Flash Download via JTAG

The LatticeEC device is capable of programming the SPI FLASH device from its JTAG port.

1. Install a jumper on JP7. This provides the CCLK to GPIO connection, as described in Lattice technical note TN1078, *SPI Serial Flash Programming Using ispJTAG on LatticeECP/EC FPGAs*.
2. Ensure that SW2 is set to position 2 (down) and that SW5 is set to "000" to select the SPI configuration mode.
3. Connect the LatticeEC Evaluation Board to an external 5V supply.
4. Connect the ispDOWNLOAD cable to the appropriate header. JP6 is used for the 1x10 cable, while JP8 is used for the 2x5 version.

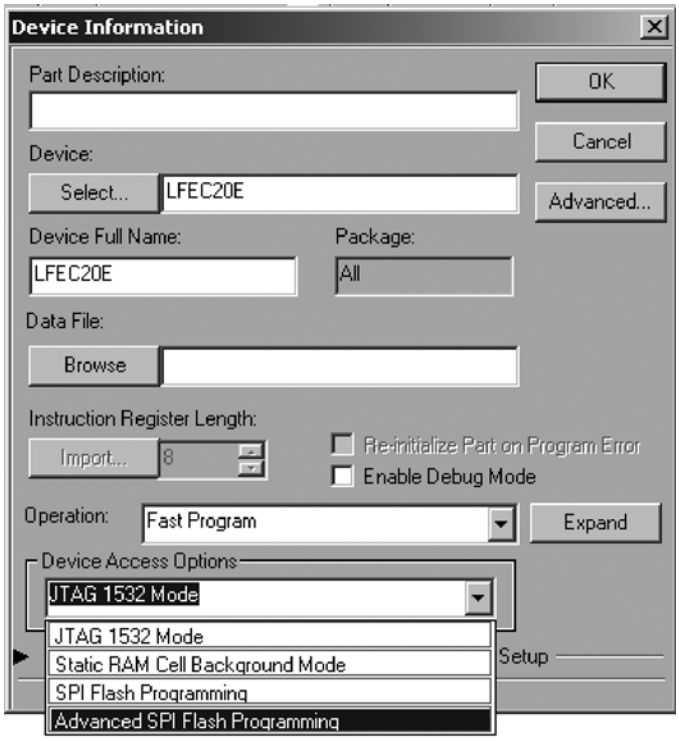
   Note: When using a 1x8 download cable, connect to the 1x10 header by justifying the alignment to pin 1 (Vcc).
5. Start the ispVM System software.
6. Press the 'SCAN' button located in the toolbar. The LatticeEC device should be automatically detected. The resulting screen should appear similar to Figure 8.

Figure 8. ispVM System Interface



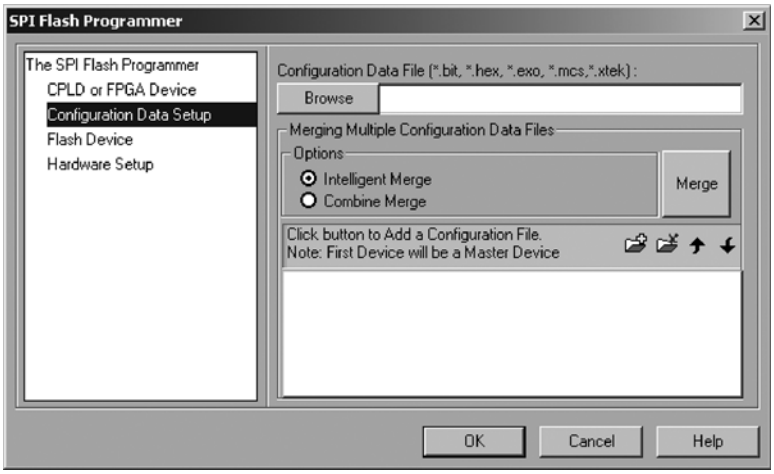
7. Double-click the device to open the device information dialog, as shown in Figure 9. In the device information dialog, set the 'Device Access Options' setting to 'Advanced SPI Flash Programming'. The SPI Flash Programmer dialog should immediately appear, as shown in Figure 10.

Figure 9. Setting the Device Access Options



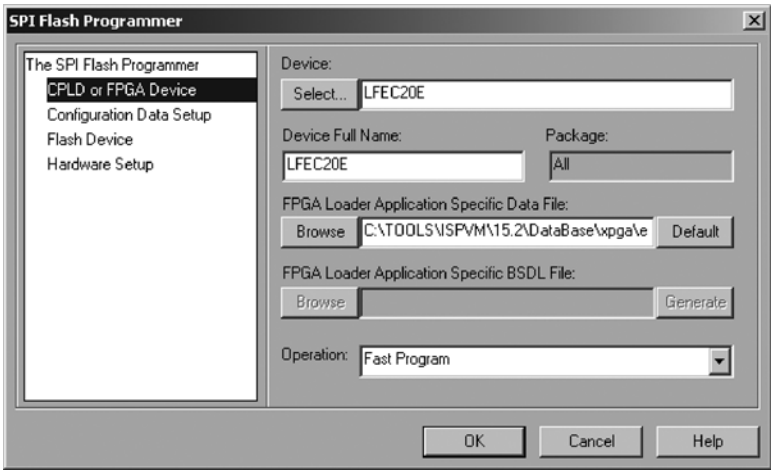
Note: Selection of the 'Advanced SPI Flash Programming' option allows the user to specify a data file other than the ispVM System default. This is necessary for the LatticeEC Advanced Evaluation Board.

Figure 10. SPI Flash Programmer



8. Choose the 'CPLD or FPGA Device' page, as shown in Figure 11.

Figure 11. FPGA Device Setup

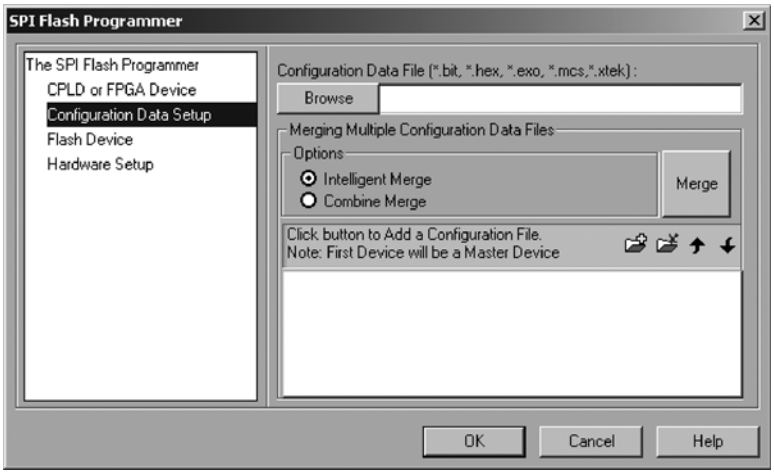


9. Click the 'Browse' button to select an alternate Application Specific Data File. Choose the 'ec20_adv_revc_spi_loader.bit' file.

Note: This file is available in the Design Files section of the LatticeEC Advanced Evaluation Board on the Lattice web site (www.latticesemi.com).

10. Select the 'Configuration Data Setup' page, as shown in Figure 12.

Figure 12. Configuration Data Setup



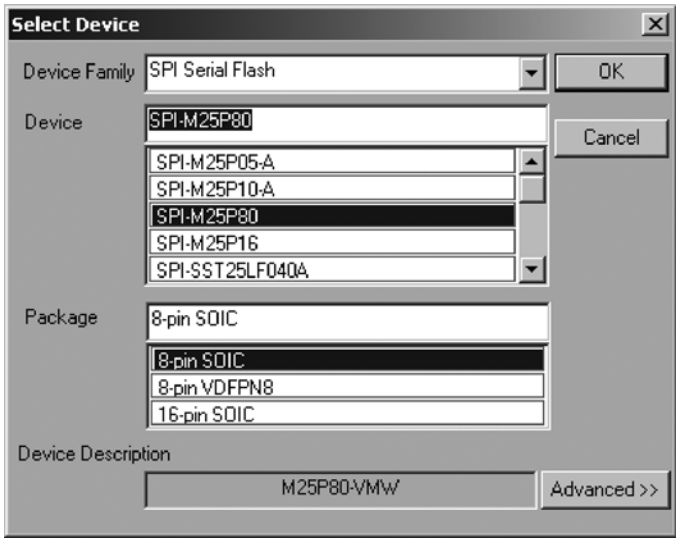
11. Browse to the desired data file to program into the Flash device.

12. Choose the 'Flash Device' page and press the 'Select' button.

13. Select the 'SPI Serial Flash' family and choose the device SPI-M25P80, as shown in Figure 13. Press OK.

    Note: It may be necessary to select an alternate SPI Flash device, as the part number is subject to change.

Figure 13. SPI Device Selection



14. Press OK to exit the FPGA Loader setup.
15. Click the green 'GO' button. This will begin the download process into the Flash device.
16. Remove the jumper at JP7.
17. Cycle the board power. The data should automatically transfer from the Flash to the FPGA.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeEC20 Evaluation Board - Advanced	LFEC20E-H-EV	
LatticeECP20 Evaluation Board - Advanced	LFECP20E-H-EV	

Technical Support Assistance

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e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
December 2006	02.2	Updated PCI Connections – Solder Side table. Correction for PCI_AD24: connects to ball AE15.
March 2007	02.3	Added Ordering Information section.
April 2007	02.4	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.

Appendix A. Schematics

Figure 14. Evaluation Board Block Diagram

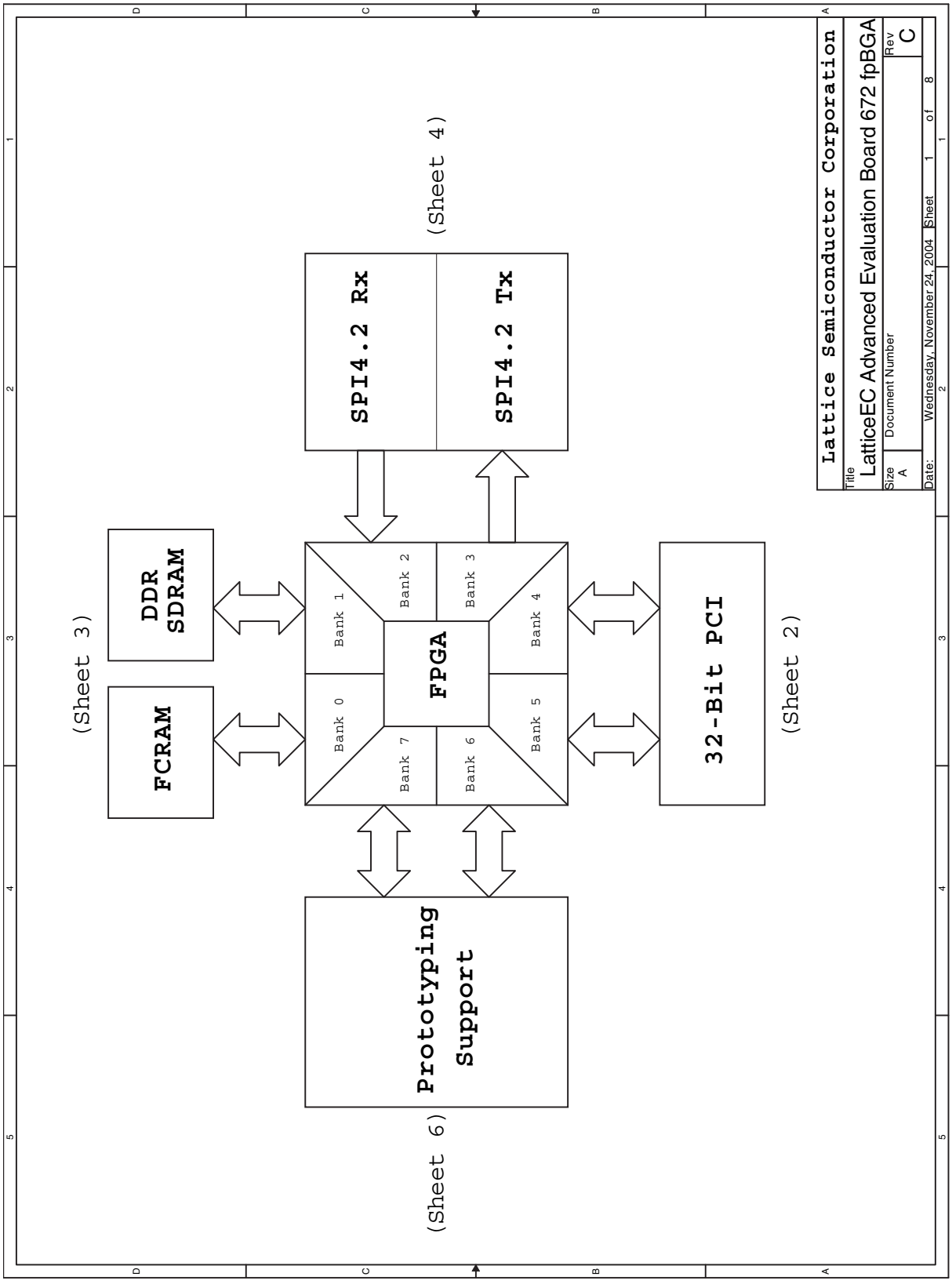


Figure 15. 32-Bit PCI Interface

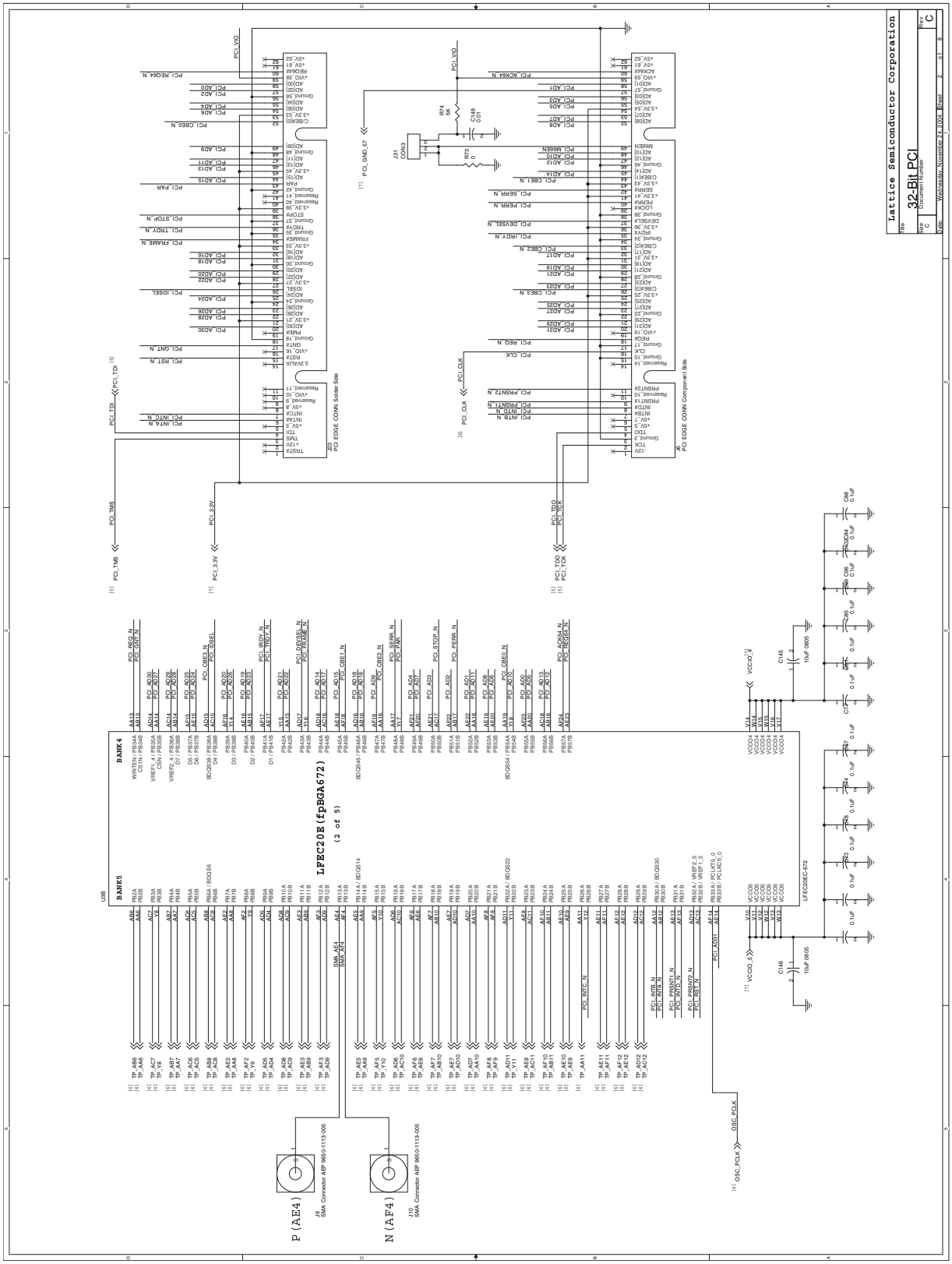


Figure 16. DDR SDRAM and FCRAM

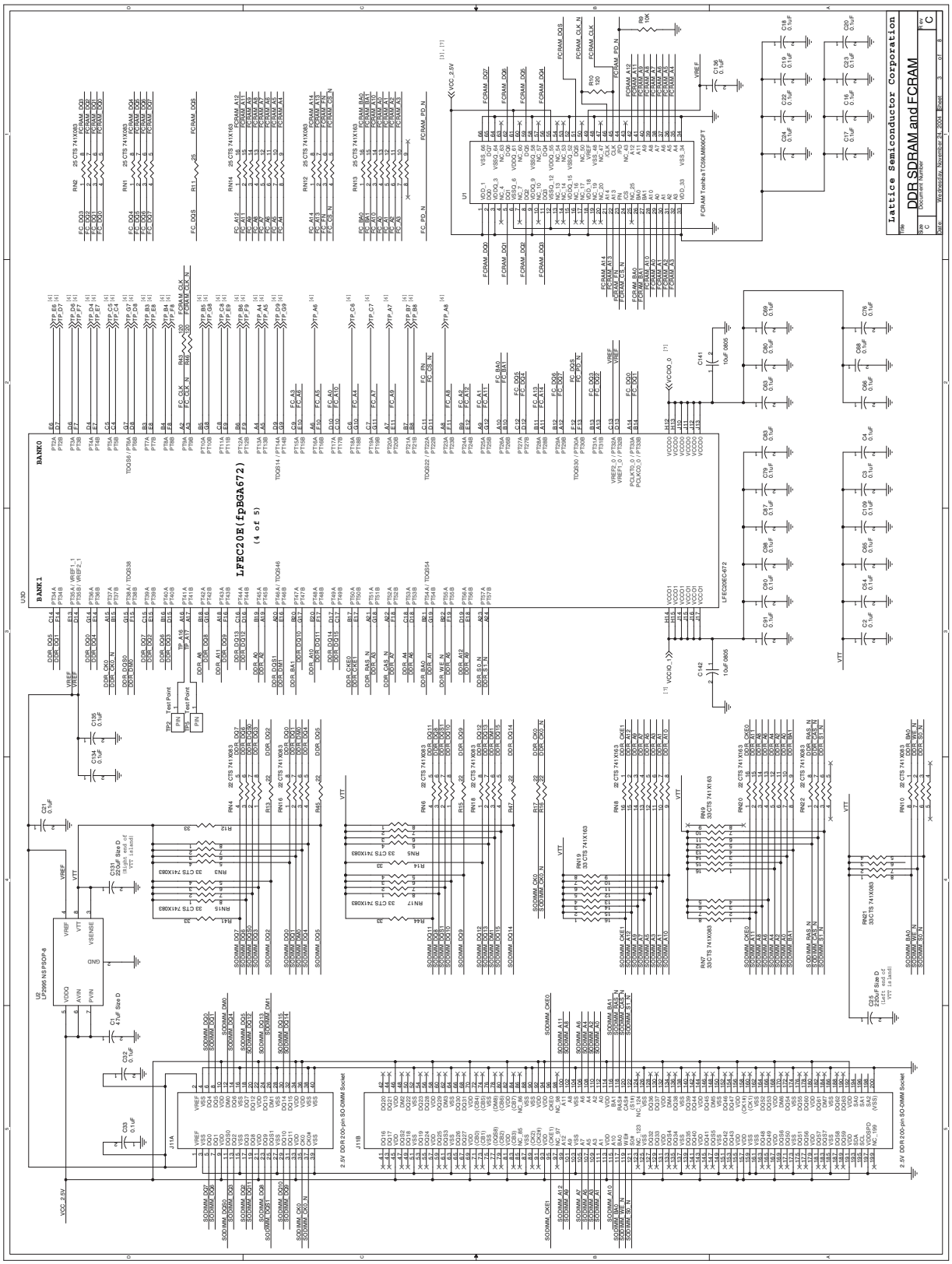


Figure 17. SPI 4.2

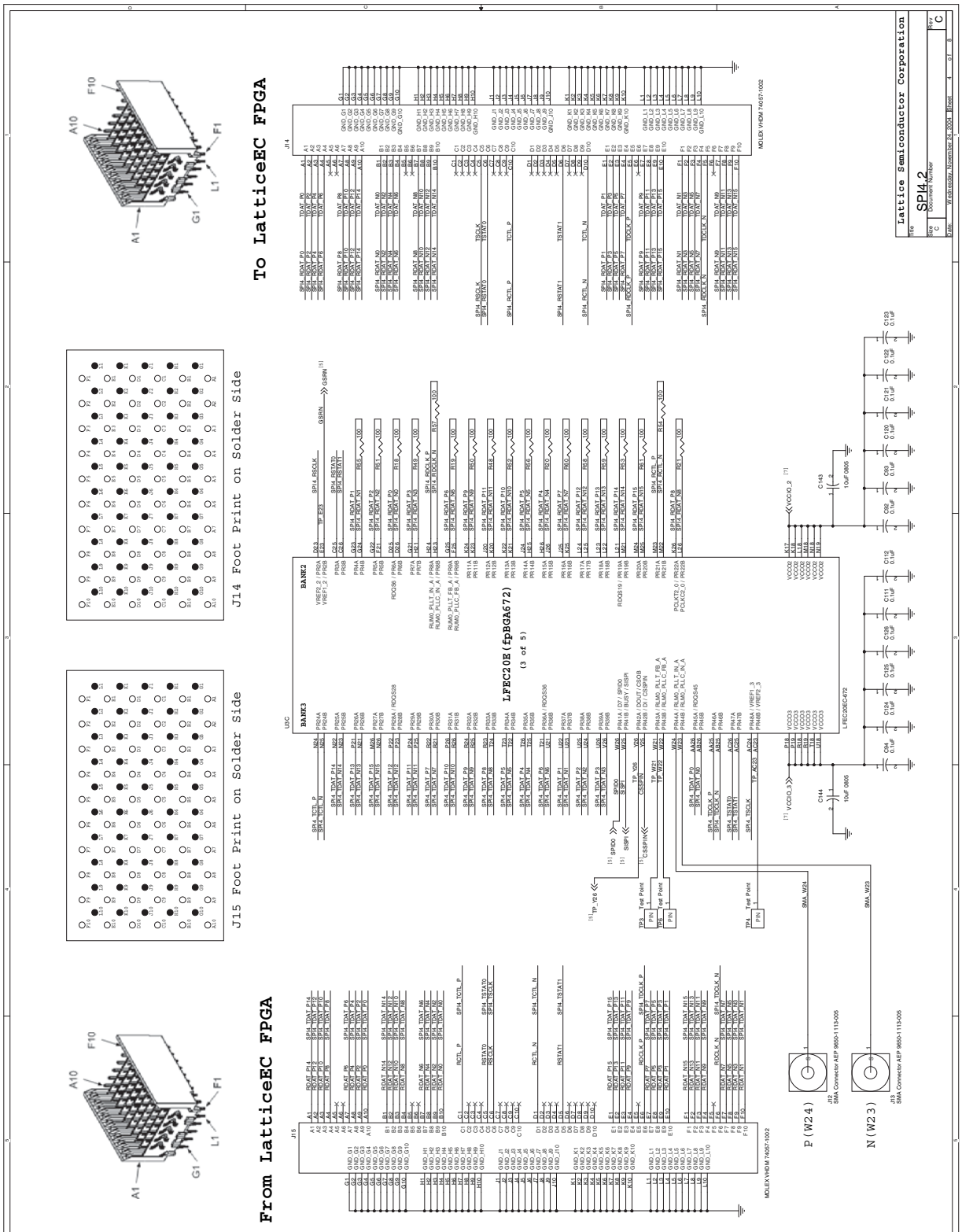


Figure 18. JTAG and FPGA Programming

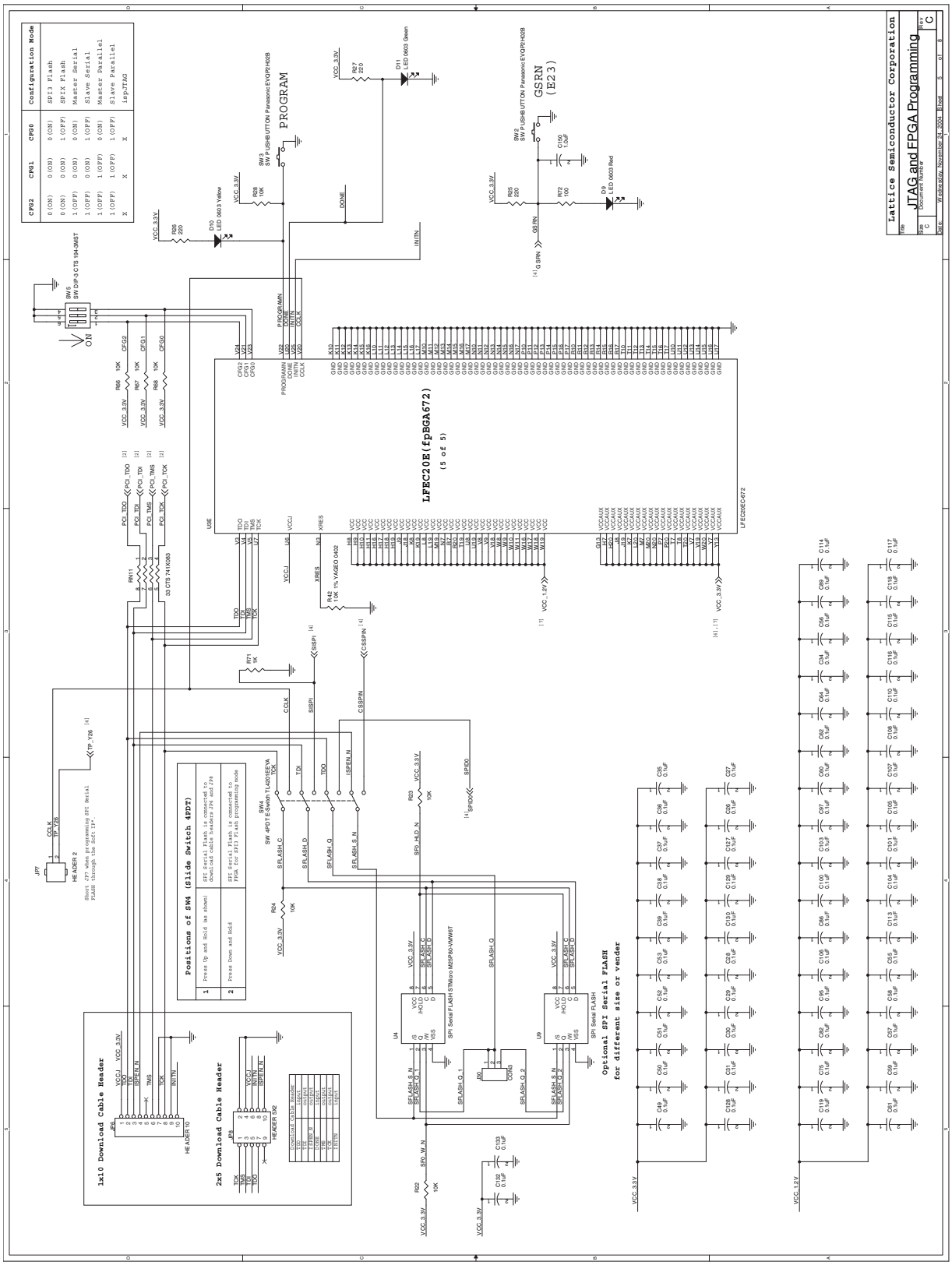


Figure 19. Prototyping Support

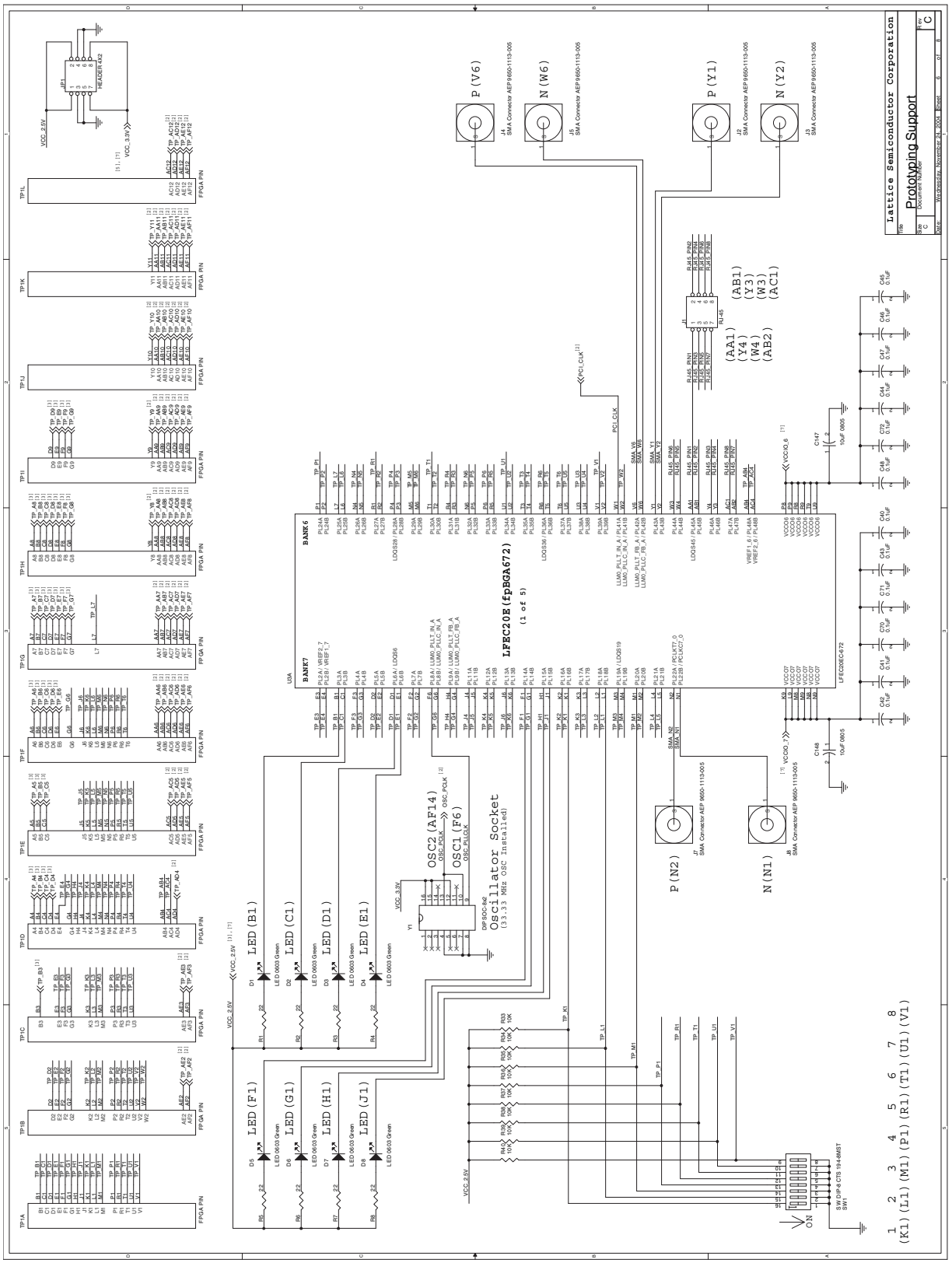


Figure 20. Power

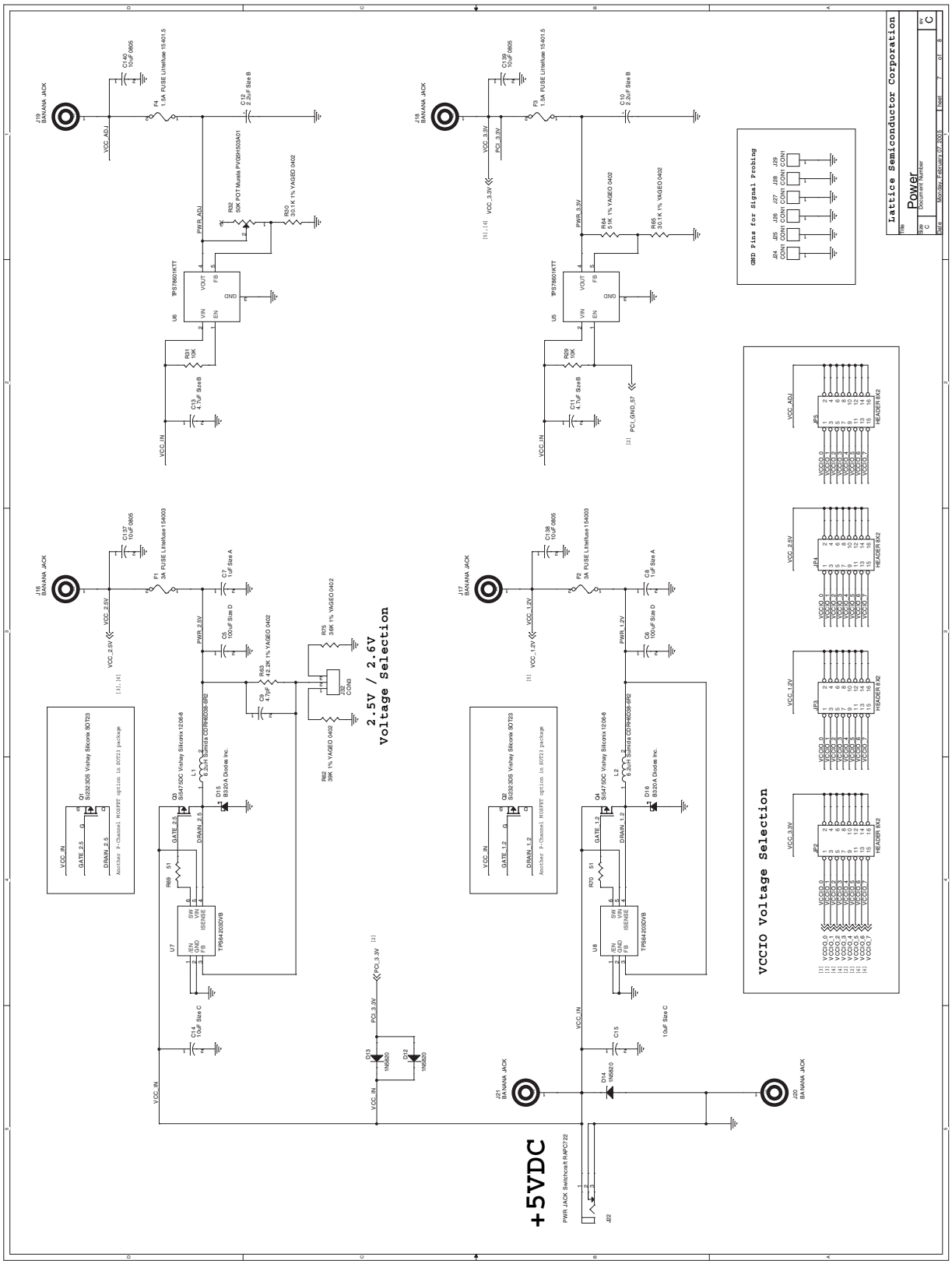
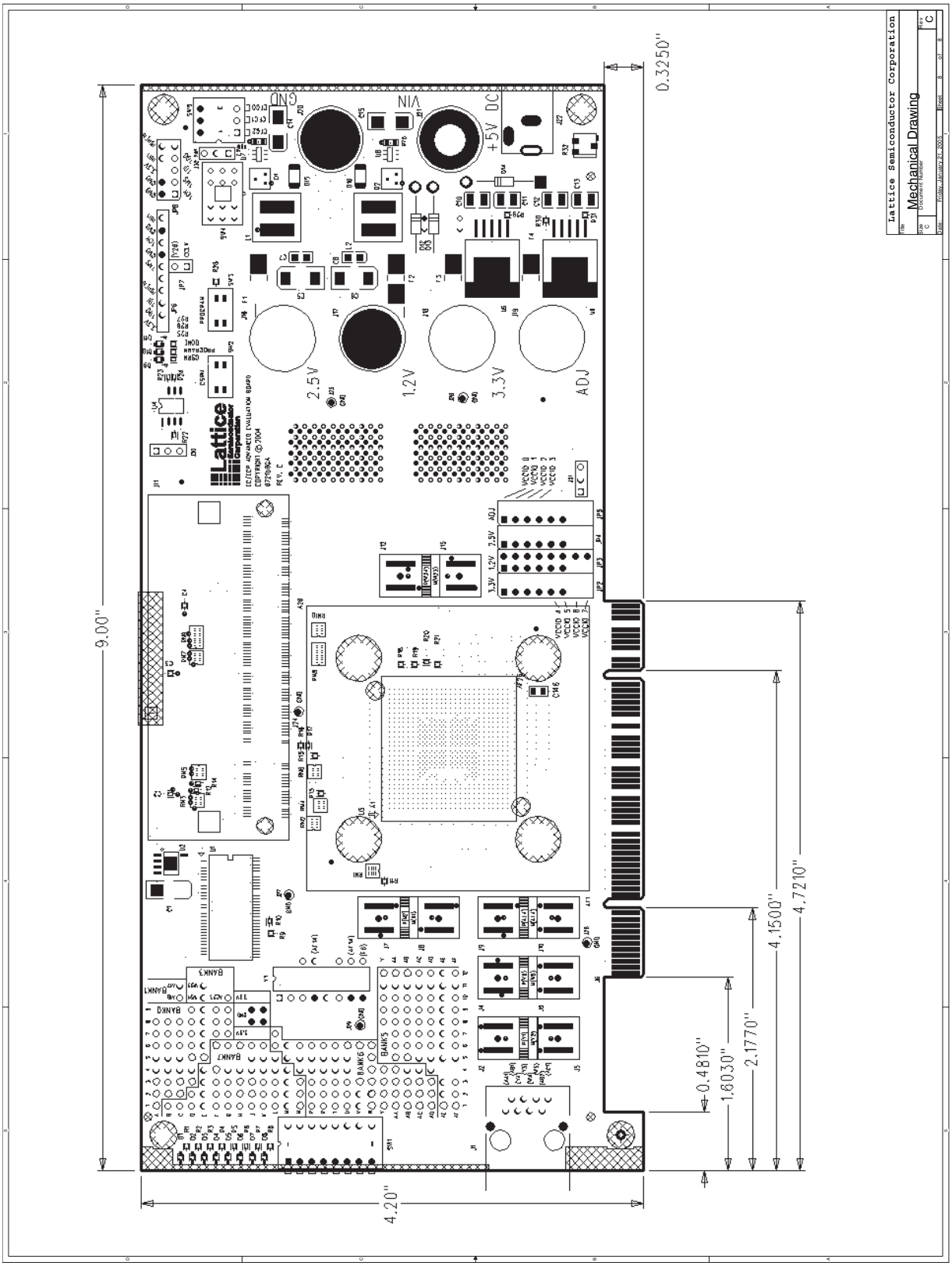


Figure 21. Mechanical Drawing



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