DESCRIPTION

Demonstration circuit 540 is a general purpose data acquisition board featuring the LTC1604 and LTC1608 (version B) Analog to Digital converters. These two devices are pin compatible, and in terms of performance, almost indistinguishable up to 333 Ksps, the maximum conversion rate of the LTC1604. The LTC1608 has a maximum conversion rate of 500 Ksps, and may also offer performance advantages below 333 Ksps as the longer acquisition time relative to the LTC1604 may permit use of a slower settling drive amplifier.

Both devices are 16 bit ADCs with +/- 2.5V fully differential inputs. Both exhibit 90 dB Sinad, and -100 dB spurious free dynamic range (with a 5kHz input signal).

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
ADC Input Voltage Range		±2.5V
ADC Common Mode Input Voltage Range		$V_{SS} < A_{IN}^-, A_{IN}^+ < V_{DD}$
SNR	100 kHz input (typical)	90 dB
THD	100 kHz input (typical)	-94 dB
SFDR	100 kHz input (typical)	96 dB
-3 dB bandwidth	Source impedance <50 ohms	5 MHz
Power consumption (LTC1604)	V_{DD} (5V)	30 mA max
	V_{SS} (-5V)	40 mA max
Power consumption (LTC1608)	V_{DD} (5V)	35 mA max
	V_{SS} (-5V)	49 mA max

OPERATING PRINCIPLES

The LTC1604 and the LTC1608 are 16 Bit Successive Approximation converters with no pipeline delay. Devices with this level of performance require careful implementation of the PCB design in order to deliver full performance. This demo circuit provides in addition to a functioning board mounted device, an example of a well implemented 4 layer PCB. The performance can be evaluated using a data collection tool such as a logic analyzer or Linear Technology's DATS data collection system. As a reference design, it demonstrates proper placement of bypassing, signal

routing, and interconnection of analog and digital grounds at the converter.

Other placement schemes involving components on the bottom side, and different geometries in the various planes may also work, but must be implemented with forethought about the effects of via placement with respect to underlying planes, the effects of lead inductance, parasitic capacitance between planes, planes and pads etcetera. Transmission line effects and the associated mirrored current flow through underlying planes must be well thought out. If time for a complete understanding of the effects of the various parasitics is not available, the layout of the area surrounding the ADC on the demo board should be duplicated to the letter. A two layer board is generally not advisable. If you intend to put a two layer design into production, use the back side as a complete uninterrupted ground plane, or contact the factory for assistance. If you intend to implement a board with 6, 8 or more layers, the 4 layer design can be used as a model, but do not use those other layers for power planes. There is typically about 150 pF/sq inch between layers in multilayer PCBs. (6 mil K=4) Most difficulties in getting a high performance ADC to perform to spec are related to layout. See the Layout Tips section at the end of this document for additional layout guidance.

The DC540 demo board requires in addition to the analog inputs, and power (+/-5V), an external TTL or CMOS logic level clock at the desired conversion rate. The output data lines are buffered to permit driving a short cable. A long flat cable may result in degraded SNR. The board also incorporates an optional input buffer/amplifier using the LT1469. This should be placed in the signal path if a high impedance source is used, or if gain is required. Consult the included schematic and layout if you intend to modify the function of this amplifier. As populated this amplifier provides 19.1 dB of differential gain. These amplifiers are unity gain stable, and can be configured for unity gain by removing R15, or for other gains by changing R15 (100Ω) to other values.

Gain in dB is 20*log(1+(804/R15))

Other circuitry incorporated on the Demo Board allows experimentation with various low pass filter networks between the amplifier and the ADC. The circuitry as populated is a second order network, with a first pole at 800 kHz, and a second pole at 10 MHz. This second pole is intended primarily to attenuate reverse transfer of high frequency sampling spikes that may result in envelope detection in the amplifier input stage, or may produce disturbances that do not settle out in the time available to the amplifier. The worst case settling time is at the maximum conversion rate with a converter that has the maximum permissible conversion time.

This is 200 ns with the LT1608* at 500 Ksps, although typically the amplifier will have 550 nsec to settle.

*Also, 200 ns worst case for the LT1604 at 333 Ksps.

The LTC1608 at 333 Ksps would only require that the amplifier settle in 1.2 µs.

The settling time published for the LT1469 is 900 ns, but this is for a large step. In response to a small disturbance, it may settle within 200 ns.

The pole at 800 kHz is intended to limit the input noise bandwidth. Although the amplifier may be rolled-off at a lower frequency, the unity gain bandwidth of the amplifier extends to 40-50 MHz, and peaks over a broad range in the neighborhood of 20 MHz. While the full power (-3dB) bandwidth of the converter is typically 5 MHz, thereafter the converter input has a first order roll-off. The effective noise bandwidth may be as high as 20 MHz considering the peaking. If this full noise bandwidth from the LT1469 were present at the ADC input, the SNR would be reduced slightly. The input network may be modified if desired to produce a true second order response, or with components removed to evaluate the performance with fewer components. This network is not intended as an anti-aliasing filter.

QUICK START PROCEDURE

Demonstration Circuit 540 can be used to evaluate the performance of the LTC1604 and LTC1608 relatively easily; however, high quality clock and signal generators are required to achieve data sheet performance. Various methods can be used to evaluate the performance of the ADC, including the use of Linear Technology's DATS system. Other approaches may involve third party parallel data acquisition, incorporation into prototype systems involving real signals, or with evaluation boards from FPGA or DSP vendors, or may simply be directly or indirectly fed to a high performance DAC:

NOTE: If the Linear Technology DATS system has not been made available to you, you must collect and process the data samples using appropriate data collection tools followed by mathematical tools of your choice. If you need or want to perform Fourier Transforms on the digital data, and do not have a means to do this, consult Linear Technology sales force or Field Applications Engineers to inquire about qualifying for a DATS system. If you want to perform testing with complex multi-tone or band limited random noise tests similar to Noise Power Ratio measurements, you may need to use a DAC followed by a spectrum analyzer to get meaningful results.

1. The following are the default jumper positions for this board: These may or may not be appropriate for your intended evaluation.

   JP4-7 Direct (no buffer)

   J5 RD-GND

   JP2 MSB Normal

2. With power off, connect power supplies to +5V, +3V and -5V. (The +3V connection is not necessary if OVDD is jumpered to +5V.) The +3V supply additionally may be anywhere from 2.7V, to 5V

3. If DATS is used, apply power to DATS (or the data collection system) before turning on the power to the DC540 and use a 3.3V supply for OVDD.

4. Connect the desired input signals, and a logic level sample CLOCK of a frequency of your choice. Clock frequencies above the rated maximum conversion rate may produce very erratic results, or may cause the converter to operate at a sub-multiple of the applied clock rate. Note that the clock input is terminated with 50 ohms. If you have a clock produced by standard or programmable logic families, and it is not driving a cable, remove R1.

5. The resistors R16 and R17 terminate signal inputs with 50Ω. These 0603 resistors are rated at 63mW. If you drive these inputs with a signal other than a ground referenced ±2.5V signal, these resistors should be removed. At high frequencies the on board buffer amplifier input network, 50 ohms followed by 1000 pF to ground, is close to 50 ohms to reduce reflections. This input network has a corner frequency of 1.5 MHz. If you have a single ended signal, you can apply it to a single input, either one, but you must either apply a short to the other input, or a 50 ohm terminator if R16 and R17 are removed. If you use the amplifier as populated, a single ended input to either input will result in a differential drive to the ADC with the common mode reduced by 22 dB relative to the differential component. All Buffer/Direct jumpers should be in the same position, although, if the amplifiers are configured for unity gain, you could have one input Buffered, and the other input Direct.

6. Note that you can perform 2 frequency experiments with this board by applying a different signal to each input.

7. Figure 1 shows the recommended experimental set-up.

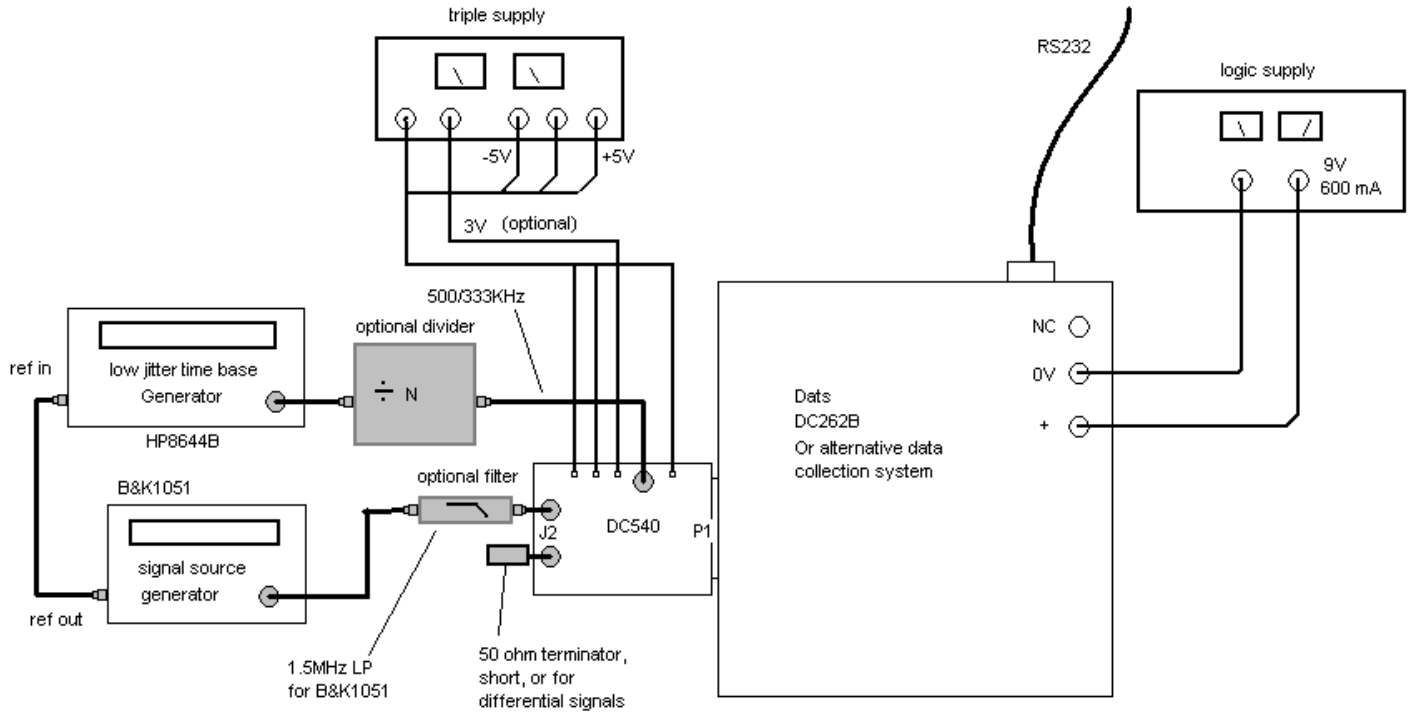

Figure 1. Proper Measurement Equipment Setup

RECOMMENDED INITIAL TEST AS A REALITY CHECK

ADC demo circuits are typically tested at the rated conversion rate with the input signal at one of the rated frequencies. The LTC1608 Demo Board is tested with a B&K 1051 generator, at 98.7548828 kHz.

Typically, the test is performed at –1 dBfs* using non-windowed data. This frequency is exactly coherent, centered in Bin 809 (a prime number) in the case of a 4096 point FFT. The use of a prime number of cycles maximizes the number of distinct codes that are exercised within the transform. In the case of a 4096 point FFT, no more than about 6% of the codes are exercised. Averaging 16-20 transforms would statistically exercise almost all codes. (as would a 64K transform)

*-1 dBfs = 1.57 V_{RMS}, or +21.88 dBm into 50 ohms or ±29204 counts

The B&K 1051 is a very low distortion generator, but it has some noise extending out to several MHz, so the use of a 1-1.5MHz low pass filter is required to get the published SNR.

The clock source used is typically an HP 8644B sine generator followed by a PECL divider with level shifters based on low noise bipolar transistors with an f_T of 9 GHz. The HP8644 generator has very low phase noise, but must be used at several MHz to avoid the conversion of the noise in the input stage of the divider into phase noise.

The use of 5 MHz, or 10 MHz from the HP8644B followed by a divide by 10 or 20 respectively is recommended for the LTC1608.

The LTC1604, is tested at 333 kHz, with 100.0788574 kHz (Bin 1231, also prime).

Using a 3.33000 MHz signal followed by a divide by 10.

The HP8644 has 5/10 MHz reference output, and the B&K 1051 must by synchronized to this reference to provide output frequencies that are accurate enough to use a non-windowed FFT.

If you have similar equipment, this configuration can be used to validate the Demo Board performance before undertaking testing with other signal sources.

SAMPLE CLOCK SOURCES

If you use a sample clock that is produced by a timing generator incorporated in a microcontroller, and, you are digitizing recurring waveform signals with frequencies and amplitudes that are a significant percentage of the sample clock frequency, make sure that the sample clock is deterministic and with low phase jitter. Some microcontrollers that use a timing processor, or make use of fractional divide ratios to produce flexible timing functions, will compromise the performance of the ADC. A non-deterministic sample clock will translate the slew rate of a higher frequency higher amplitude recurring signal to appear as broadband noise, degrading the SNR. This noise component looks in the time domain like random noise that is amplitude modulated by the input frequency. Modulated random noise still appears random in a spectral plot. It is worse however than the noise floor would suggest as it has a higher crest factor due to the modulation.

If you use a PLL based clock and do not see very good results digitizing frequencies that are at a significant fraction of the sampling frequency, or above (undersampling), you may want to do a reality check of the performance with a low phase noise sample clock source. We have seen parts dismissed as no better than lower performance parts simply because the clock source was the limiting factor. Similarly, if you intend to use a PLL as your eventual clock source, it is recommended that you evaluate the ADC performance with the "clock source under consideration".

If you use logic dividers to produce a 500 kHz clock signal from a higher frequency oscillator, make sure that the logic producing the clock, or any buffering is powered from a quiet supply. Power supply dependent propagation delay in low power CMOS will translate power supply noise into phase noise. If you intend to use low power CMOS logic to produce your sample clock, and intend to operate this off a logic supply that may have even typical digital noise levels, you should verify performance with the digital noise in place. If your master time base is operating off a well filtered supply, and you intend to use programmable logic as a means of producing your sample clock, you may want to consider re-timing the sample clock after division using a single fast D type flip flop powered from a well decoupled supply, and clocked from the original oscillator. High speed FPGAs and CPLDs that have maximum clock rates above 200 MHz may be fine as is.

POOR EQUIPMENT

If you do not have the high quality generators necessary for a non-windowed FFT, you may still be able to perform useful tests that may represent the performance of the ADC.

If you want to examine the output of the ADC in the frequency domain, and do not have an accurate signal generator, or if you intend to use real world signals that are not coherent with the sample window (an exact integral number of cycles of the waveform within a rectangular window) you can use one of various raised cosine window functions, either with Linear's DATS system, which offers a number of windowing algorithms, or with a mathematical tool. If the ADC is digitizing essentially random real world signals that typically fall off with frequency (such as vibration), you can use

poorer clock sources, as phase noise will not degrade results significantly if there is little high frequency content. If you are converting pre-sampled signals such as the output of Multiplexers or CCDs, clock jitter will be of little concern as long as the aperture does not fall outside the window where your external signal source has settled.

ALTERNATE EVALUATION TECHNIQUES

Alternatively, you can feed the output of the ADC to a DAC, and observe the result with a spectrum analyzer. This has the advantage that it may be used with incoherent signals such as for Noise Power Ratio measurements. The DAC in this case must have better performance then the ADC, or you must accommodate the shortcomings of the DAC either by decimating before the DAC, or by accounting for the DAC's properties in your evaluation.

In the case where you use a DAC with either of these ADCs, the DAC is likely to compromise the result in one way or another. For example, if you were to use the LTC1668, a 50 Msps 16-bit DAC, the spurs generated by the DAC may dominate those of the ADC. This DAC which is fast enough to re-construct the output from a 16-bit ADC running at 50 Msps, does not have sufficiently accurate gain to match the slower speed LTC1608, and may also elevate the noise floor of the LTC1608 results. It is best suited to AC signals. For DC or lower frequency applications, lower speed DACs such as the LTC1597 having high DC accuracy, do not necessarily produce good AC performance above a few kHz. The LTC1597 with a composite output stage can produce low distortion (-95 db THD) results up to about 30 kHz.

In any case where the output is fed into a DAC, the resulting clock ± data product frequencies must be discounted, either by post filtering, or by ignoring them on the spectrum analyzer. If you are dealing with real world signals such as vibration, you could even listen to the result, possibly after some frequency translation.

Feeding the analog input of the ADC with a low frequency ramp and observing the output truncated before a lower resolution DAC generates a sawtooth waveform. This can be used to find missing codes, however the ramp generator performance will typically compromise any attempt to gauge linearity. A common pitfall associated with this evaluation method is that the major carries are obscured by the step in the sawtooth waveform. If you use an adder to shift the point that the wrapping occurs by say 128 counts, you can see the major carries properly. If a DAC is used to generate the ramps, the use of a filter after the ramp generator is mandatory.

If you use instead, a low amplitude sinusoid of some frequency that is easy to generate with low distortion, and possibly decimate the output such that the DAC generates a lower frequency signal, you can evaluate performance with AC signals well above audio, possibly with an oscilloscope or with an audio spectrum analyzer. If you use a low amplitude signal near 100 kHz, (101 kHz for example), with a 500 kHz sample clock, divided by 5 to drive the DAC, the DAC will produce a waveform that is the difference frequency between the input and 100 kHz. In the case of 101 kHz, this would appear as 1 kHz at the output of the DAC. Note: A spectrum analyzer will also see the 100 kHz ±1 kHz products, as well as repeated products around every harmonic of the 100 kHz, out to hundreds of MHz in the case of the LTC1668. If you were to use the LTC1597, a 100 kHz update rate is about as high as you can expect to go and still get good results generating frequencies in the audio range.

If you use a lower resolution DAC with the least significant bits, these techniques can be used with a low amplitude signal to exaggerate the DNL of the ADC without the DAC being the limiting factor.

If you use the LTC1597, with the data rate decimated (or re-sampled) to the extent that the resulting signals are below a few kHz, full amplitude signals can be translated and observed. The LTC1668 can reproduce pretty much any AC

waveform acquired by the LTC1608, but there will be a gain error.

High frequency dithering and over-sampling techniques can mitigate the non-linearities of the DAC and more faithfully reproduce the ADC output. The ADC output is over-sampled by (up to 100x) using interpolation filtering (e.g. an FIR followed by a simpler filter (e.g. CIC)) to produce a 50 Msps data rate into the LTC1668 DAC. Super imposing a high frequency dither onto the ADC input and subsequently analog low pass filtering the clock and higher frequency data products out of the DAC reduces the DAC non-linearities by the ratio of over-sampling to post filter bandwidth. The low pass filtered DAC output can then be examined with a high performance spectrum analyzer.

These DAC based methods are arguably only worthwhile if you have signals that are not well suited to FFT based analysis. Incoherent signals such as noise power ratio measurements fall into this category. DAC based evaluation is required for continuous sampling not generally possible with computationally intensive Fourier transform based evaluation techniques.

Using a low amplitude sinusoidal signal rather than a ramp to evaluate an ADC permits multiplying the amplitude of the DIGITAL signals by shifting right. For example the 8 LSBs of the ADC feed the 8 MSBs of the DAC. By varying the DC bias, you can produce a situation where the AC waveform crosses a major carry in the ADC, and will produce some observable distortion in the waveform output by the DAC, but attributable to the ADC alone. This technique minimizes the effect of the DAC, and will show the weaknesses of any ADC, as well as many signal generators, so be careful with your interpretation. You are exaggerating DNL by a factor of 256, and you are exaggerating frequency instability by a factor of 100.

This technique is obviously not suitable for evaluating the dynamics of high amplitude, high frequency input signals.

If you are interested in high amplitude waveforms near Nyquist, you can produce a waveform at the output of a DAC that is the difference frequency from Nyquist ($f_{NYQUIST}$ = 250 kHz for 500 Ksps) . If you feed the ADC with 249 kHz for example, by inverting every other sample (by XORing every other sample) you will see at the output of the DAC, the 1 kHz difference frequency. This also exaggerates the frequency instability of either of your signals.

NOISE POWER RATIO MEASUREMENTS

This technique involves feeding the ADC with band limited noise, typically originating in a noise diode, amplified, fed through a wide bandpass filter, and followed with a deep notch filter placed in the center of the pass band. The quality of the ADC can be related to the depth of the notch as represented in the output data. In a poor converter, inter-modulation products will fill in the notch. As this technique uses random frequency content, it cannot be evaluated very effectively in the digital domain unless very large FFTs are performed. Feeding the output to a DAC however permits evaluation with a spectrum analyzer and the phenomena associated with the Fourier transform called leakage, does not occur. If the notch is large enough, a large windowed transform can be used, but the depth of the notch must exceed the SFDR of the converter over the transform window.

GENERATORS

Using a non-synthesized function generator with the above evaluation techniques will produce a very graphic picture of how poor these generators are in terms of frequency stability. These techniques that translate a higher frequency down to the range that can be reproduced with a lower speed high resolution DAC will make a mediocre generator look terrible. Poor generators also have insufficient frequency stability to be usable with a non-windowed FFT. Windowing may produce better looking results, but phase noise, and amplitude modulation will produce artifacts around the fun-

damental. In most cases, even with good generators, you must use low pass filtering to resolve the harmonics that are due to the ADC alone. Many poor generators also have low frequency artifacts that may require a band pass filter to suppress.

REAL WORLD SIGNALS

With complex signals, especially non periodic signals, correlating the ADC performance in terms of THD, SFDR and SNR with a single or intermodulation distortion performance two tone test, is difficult. As a result, many or even most customers want to examine signals that they are familiar with, or that are typical of what they get from a real world source. To make matters more difficult, often converters from different vendors are rated under different conditions, making a comparison of specs difficult.

Converters with similar THD, or even similar individual harmonics may perform differently under scenarios that involve low level signals in the presence of high level interferers. If the signal of interest is a low level signal riding on top of a higher amplitude lower frequency content signal, a converter that has a given level of 3rd harmonic distortion associated with gain compression near the peaks will perform differently than one with the same level of 3rd harmonic due to an abrupt discontinuity at the major carries.

In these cases, Linear Technology's DATS system can be used to collect up to 128K samples that can be imported into Excel or other math software.

MODIFICATIONS

In addition to changes to gain and frequency cutoff in the input circuitry, The LT1469 can be replaced with an alternative amplifier. The maximum practical gain with the LT1468 would be on the order of 19 dB, essentially the gain as configured. Higher gain will simply elevate the noise floor, and is of arguable value.

Lower gain or unity gain with the amplifier as a means of accommodating a higher source impedance may be preferable in many applications.

Other dual amplifiers may be preferable in cases where the converter is operated in the neighborhood of Nyquist (the LT1807) or for lower input referred noise (e.g. LT6201 may be usable up to a gain of 36 dB) or in cases were fast settling, (e.g. recovery from transients) is required (LT1819).

Other modifications that may be entertained are

1) Replacement of the output latches with series termination resistors.
2) Reduction of the 1000 pF input capacitor(s) C14 & C19 if high source impedance or differential signals with higher source impedance, or source impedance imbalance. If you need AC common mode rejection, the value of these capacitors should be reduced to the range of 20-30 pF, to act as RFI suppression (both directions).
3) Changes to this input network, as well as the network between the amplifiers, and ADC, and the feedback network in order to produce higher order roll off.

LAYOUT TIPS

This board is intended to be a link between a digital data collection subsystem, a signal source and a clock source. You will notice that there are essentially three grounds, digital ground, analog ground, and clock ground. All three come together at the ADC. The ground fill that extends from the Clock connector to the neighborhood of the ADC could be viewed as a continuation of the shield around the clock cable, with the output of U5 at the end of that cable.

The top surface area under the ADC is filled with copper, and peppered with vias adjacent to pins 5-8. This is a reflection of how important it is to ground these pins. You will also notice a cluster of vias at each of the Capacitors C9, C10, and C11.

C11 is the most important of these capacitors. If you elect to implement C11 as a group of capacitors of lesser value, note that one of these should be placed as close as possible to pin 4. The others should be positioned such that their ground connections are as close as possible at the expense of some trace length on the REFCOMP node. These capacitors can potentially be on the bottom of the board, and grounded at the same cluster of vias as the local capacitor. You will notice that there is no power plane under the ADC, or in fact, even on the "digital end of this board. All digital ICs (U2, U3, U5, U6) should have local bypassing close to the IC and between the V_{CC} and Gnd pins to return power supply currents directly to the IC ground return.

If you intend to use 6,8 or more layers in your implementation, you should not use these additional layers for power planes, at least not an uninterrupted power plane extending from the digital section. It is suggested that you put as many layers of ground as possible under the ADC, and extending out to the points where all the capacitors are grounded. Although this board was implemented with 74HC575 latches in the data path, it is not always recommended that these be used in actual implementations, as they do not have enough ground pins. The presence of a very noisy bus on the output side of these devices may allow high frequency noise to be reflected back into the ADC. The use of devices such as the 74LVC16373 or it's variants (depending on voltages at OVdd and the destination) is suggested. These later devices have a significant number of ground pins, so ground bounce is much reduced.

You will notice that the bulk bypass on +5V, and -5V are interconnected together with a fat trace before being routed to the ground plane. This is to prevent ripple current from the power supply from developing differentials across the ground plane. This power ground is then taken to an area of ground fill on the bottom of the board.

In an actual implementation, this treatment of the power, digital clock and analog grounds is not always possible, but the same guidelines should be used. Power supply ripple should not develop differential voltages across the ground plane.

Ground current flow between the different subsystems that are interconnected at the ADC should not develop signals (ground loops) between points in the ground where they can be picked up by the ADC or amplified by the front end. One of the tests performed on this and other demo boards is the intentional introduction of AC ground currents. It is a common mistake to characterize an ADC board with inputs shorted to determine if there is a noise problem. Part of the testing should involve shorting the inputs at various points in the signal path, with a realistic, or better yet, worst case grounding scenario. This may mean intentionally injecting significant AC currents into the grounds.

DEBUGGING TIPS

Although this demo board is quite straight forward in that it is essentially just the ADC followed by a latch, achieving data sheet results can be difficult.

Generally this is due to the limitations of generators, poor cabling, or a lack of familiarity with the limitations of the Fourier transform. Even if you use a poor generator, if you follow with a bandpass filter and use windowing, you can often get reasonable results, but, if you don't, check the following;

1) Between the generator and your filter, and between the filter, and the demo board, you must use good coaxial cables, with proper termination. Or you must use twisted pair or twisted shielded pair with full differential signaling.

Failure to use good interconnection practices, using clip leads for example, or poor implementation of the filter will produce a differential signal component at the input of the ADC that is related to ground currents that flow between the Data Collection Device, and the generator. This is made worse in the case where the amplifier section is used to produce voltage gain. High frequency digi-

tal noise currents can sometimes be reduced by the use of ferrites around cables. For lower frequency effects that may elevate the noise floor, transformers or opto-couplers may be used for both the clock and data. Note however, the use of a transformer on the clock requires that the clock be a higher frequency sinusoid, and that it be received by a low noise differential receiver, and subsequently divided down to 500 kHz, or less.

The clock is often regarded as a digital signal, but if the edge rate of the clock signal is low, ground bounce at the point that the clock signal originates can result in jitter, which will degrade SNR.

2) If you have unwanted signals between grounds at your signal generator, and your ADC board, and you cannot interrupt the ground path with a transformer, (If you want response to DC, or frequencies below what is practical with a signal transformer, you can make use of the fully differential nature of the ADC inputs, as well as the LT1469 based differential gain stage. This gain stage will not reject high frequency common mode, but may reject those components that commonly are encountered in the range of 20kHz to a few hundred kHz, as are encountered in the power supplies of equipment that may be involved.

The passive components used on the demo board are not necessarily the best for optimal CMRR. The 1000 pF input capacitors (C14 & C19) should be reduced to less than 100 pF if CMRR in the 20-100kHz region is important. For example, 5% tolerance in these capacitors will result in a reduction of CMRR in the order of 55 dB, vs 90 dB which the amplifier itself may exhibit.

Note also, that the capacitors C17 and C18, which are provisional with the LT1468, may result in some loss of CMRR, for similar reasons. At 40 kHz, 5% tolerance in these capacitors would result in common mode related signal at -80 dB in a unity gain configuration. In a situation with gain, the resulting output from these capacitors is still only -80 dB relative to the common mode, so with approx 20 dB of gain as configured by default, this could be viewed as CMRR of 100 dB.

Capacitors C17 and C18 are provisional for amplifiers that may not be unity gain stable, and which even though producing differential gain, must satisfy the constraint that the common mode be greater than the minimum gain for the amplifier.

In order to use twisted shielded pairs, for example, you should not use 50 ohm through-terminators at the inputs, (although these are often such tight tolerance that you may be able to get away with it) but rather 100 or 120 ohms between the two inputs (depending on the cable).

The use of two RG59U cables will not likely give good results, as the match in terms of impedance, and length is unlikely to produce true differential signaling.

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331