

# Universal Relay Driver

## Features

- ▶ 10 to 450V input voltage range
- ▶ Energy saving hold current mode
- ▶ Adjustable microcontroller supply
- ▶ Low supply current <1.0mA
- ▶ Constant current coil
- ▶ Programmable pull-in current, pull-in time, and hold current
- ▶ Efficient PWM operation using the relay coils' inductance

## Applications

- ▶ Industrial controls
- ▶ Relay timers
- ▶ Solenoid drivers
- ▶ Home automation

## General Description

The Supertex HV9901 is a BiCMOS/DMOS universal relay driver that employs PWM switching techniques. It is designed for efficient and energy-saving operation of a low voltage relay with supply voltages ranging from 10 to 450V DC through utilization of the relay coils' inductance.

The circuit is capable of operating over a wide input voltage range without requiring a change of any external components. For example, this will enable users to use 5.0V coil relays for DC voltages 10 to 450V or AC voltages up to 240V.

The HV9901 has an internal high-voltage regulator to power internal PWM circuitry. Additionally, it includes an adjustable auxiliary regulator with a 1.0mA capability that can be used to supply low power micro controllers.

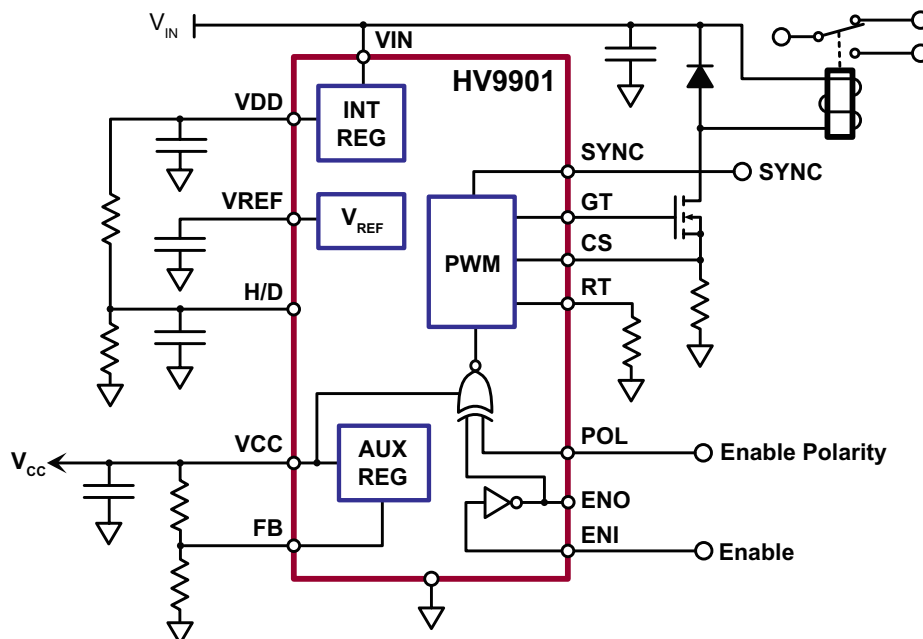
The pull-in current, pull-in time and hold current are all program-mable using only two resistors and a capacitor. The PWM switching frequency can be either:

- Synchronized to an external clock, or
- Synchronized to other HV9901s, where the synchronized frequency is the highest free-running frequency.

The enable (ENI) logic input is used to turn the relay on/off. Enable polarity may be selected via the POL input. Audible noise is prevented using fixed switching frequencies above 20kHz.

**WARNING!!! Galvanic isolation is not provided. Dangerous voltages are present when connected to the AC line. It is the responsibility of the designer to ensure adequate safeguards are in place to protect the end user from electrical shock.**

## Typical Boost Application Circuit



## Ordering Information

Part Number	Package	Packing
HV9901NG-G	16-Lead SOIC (Narrow Body)	45/Tube
HV9901NG-G M901	16-Lead SOIC (Narrow Body)	1000/Reel
HV9901NG-G M934	16-Lead SOIC (Narrow Body)	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

## Absolute Maximum Ratings

Parameter	Value
Input voltage $V_{IN}^1$	-0.5V to +470V
Input voltage to any other pin <sup>1</sup>	-0.3V to $V_{DD} + 0.3V$
Operating temperature range	-40°C to +85°C
Continuous Power dissipation ( $T_A = +25^\circ C$ ) <sup>2</sup>	750mW

**Note:**

- All voltages are referenced to COM.
- For operation above 25°C ambient derate linearly at 7.5 mW/°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Typical Thermal Resistance

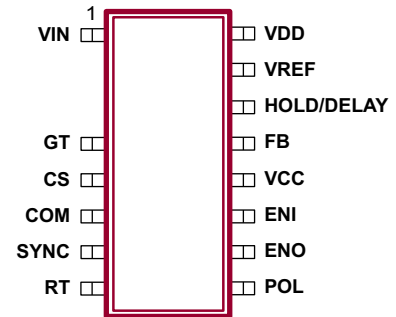
Package	$\theta_{ja}$
16-Lead SOIC	83°C/W

## Electrical Characteristics ( $T_A = +25^\circ C$ unless otherwise noted)

Sym	Parameter	Min	Typ	Max	Units	Conditions
<b>High Voltage Regulator</b>						
$V_{IN}$	Input voltage	10	-	450	V	$I_{CC} = 0$ to 1.0mA load
$I_{IN}$	Supply current	-	-	2.0	mA	No load at $V_{DD}$ . load at $I_{CC} = 1.0mA$ $C_{GT} = 500pF, f_{OSC} = 25KHz$
$V_{DD}$	Internally regulated voltage	8.5	9.0	9.5	V	No load at $V_{DD}$ . $C_{GT} = 500pF,$ $f_{OSC} = 25KHz$
$UV_{ON}$	$V_{DD}$ under voltage lockout, on	7.8	8.2	8.5	V	---
$UV_{HYS}$	$V_{DD}$ under voltage lockout, hysteresis	-	0.5	-	V	---

\* Maximum allowable load current limited by power dissipation and operating ambient temperature.

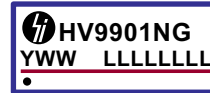
## Pin Configuration



**16-Lead SOIC**  
(top view)

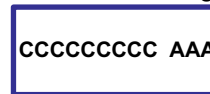
## Product Marking

Top Marking



Y = Last Digit of Year Sealed  
 WW = Week Sealed  
 L = Lot Number  
 C = Country of Origin  
 A = Assembler ID\*

Bottom Marking



— = "Green" Packaging  
 \* May be part of top marking

Package may or may not include the following marks: Si or

**16-Lead SOIC**

**Electrical Characteristics** ( $T_A = +25^\circ\text{C}$  unless otherwise noted)

Sym	Parameter	Min	Typ	Max	Units	Conditions
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**Adjustable Regulator**

$V_{CC}$	Regulator output voltage range	2.0	-	5.5	V	$I_{CC} = 1.0\text{mA}$ load
$I_{CC}$	Regulator output current	0	-	1.0	mA	No load at $V_{DD}^*$
$V_{FB}$	Feedback voltage	0	$V_{REF}$	$V_{DD} - 1.0\text{V}$	V	---
$I_{FB}$	Input bias current	-	25	100	nA	$V_{FB} = V_{REF}$

**Reference**

$V_{REF}$	Bandgap reference voltage	1.20	1.25	1.30	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
	Load regulation	-	-	7.0	mV	$0\text{mA} < I_{REF} < 0.3\text{mA}$
	Line regulation	-	10	15	mV	$8.5\text{V} < V_{DD} < 9.5\text{V}$
$I_{REF(SHORT)}$	Short circuit current	-	-	1.0	mA	---
$I_{REF(SINK)}$	Reference voltage sink current	-	-	20	$\mu\text{A}$	---

**Oscillator**

$f_{OSC}$	PWM oscillator frequency	20	25	35	kHz	$R_T = 1.0\text{M}\Omega$
		80	100	140	kHz	$R_T = 226\text{K}\Omega$
-	Temperature coefficient	-	170	-	ppm/ $^\circ\text{C}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$f_{SYNC}$	Oscillator sync frequency	-	-	150	kHz	---
$I_{SYNC}$	Sync input/output sourcing current	20	-	55	$\mu\text{A}$	---
$I_{SYNC}$	Sync input/output sinking current	1.0	-	-	mA	$V_{SYNC} = 0.1\text{V}$
$V_{SYNC}$	Sync input logic low voltage	-	-	1.0	V	---

**PWM**

$D_{MAX}$	Maximum duty cycle	96.5	-	99.5	%	$R_T = 1.0\text{M}\Omega$
		86.5	-	97.5	%	$R_T = 226\text{K}\Omega$
$t_{BLNK}$	Blanking time	150	215	280	ns	---

**MOSFET Driver Output**

$V_{GTH}$	Gate drive output high	$V_{DD} - 0.3$	-	-	V	$I_{OUT} = 10\text{mA}$
$V_{GTL}$	Gate drive output low	-	-	0.30	V	$I_{OUT} = -10\text{mA}$
$t_R$	Rise time	-	30	50	ns	$C_{GT} = 500\text{pF}$
$t_F$	Fall time	-	30	50	ns	

**Current Sensing**

$V_{CS(HL)}$	Current sense voltage, high limit	0.775	0.833	0.891	V	---
$t_{DELAY(HL)}$	Current limit delay to GT, high limit	-	200	250	ns	50mV overdrive
$I_{CS}$	Input bias current	-	25	1000	nA	POL = Low, ENI = Low
$V_{OS}$	Low limit comparator input offset voltage	-	-	$\pm 60$	mV	---
$t_{DELAY(LL)}$	Current limit delay to GT, low limit	-	200	250	ns	50mV overdrive

## Electrical Characteristics ( $T_A = +25^\circ\text{C}$ unless otherwise noted)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{\text{HOLD/DEL}}$	Hold/delay output voltage	$V_{\text{DD}} - 0.4$	-	-	V	$I_{\text{HOLD/DEL}}$ (sourcing) $-100\mu\text{A}$ POL = Low, ENI = Low
$I_{\text{HOLD/DEL}}$	Hold/delay input bias current	-	25	500	nA	POL = Low, ENI = Low  $2.0\text{V} < V_{\text{CC}} < 5.5\text{V}$
$t_{\text{ENI}}$	Shutdown delay	-	50	100	ns	
$V_{\text{ENI}}$	Enable input voltage - High	$0.7V_{\text{CC}}$	-	$V_{\text{CC}}$	V	
	Enable input voltage - Low	0	-	$0.3V_{\text{CC}}$	V	
$I_{\text{ENI}}$	Enable input current - High	-	1.0	5.0	$\mu\text{A}$	
	Enable input current - Low	-5.0	-1.0	-	$\mu\text{A}$	
$V_{\text{POL}}$	Polarity voltage - High	$0.7V_{\text{CC}}$	-	$V_{\text{CC}}$	V	
	Polarity voltage - Low	0	-	$0.3V_{\text{CC}}$	V	
$I_{\text{POL}}$	Polarity current - High	-	1.0	5.0	$\mu\text{A}$	
	Polarity current - Low	-5.0	-1.0	-	$\mu\text{A}$	
$V_{\text{ENO}}$	Enable output voltage - High	$0.9V_{\text{CC}}$	-	$V_{\text{CC}}$	V	
	Enable output voltage - Low	0	-	$0.1V_{\text{CC}}$	V	

## Enable Logic Truth Table

POL	ENI	ENO	Gate Drive Output
Low	Low	High	$V_{\text{GT}} =$ Oscillating output, duty cycle depends on inductive load
Low	High	Low	$V_{\text{GT}} =$ Low, SYNC = High, oscillator shut down.
High	High	Low	$V_{\text{GT}} =$ Oscillating output, duty cycle depends on inductive load
High	Low	High	$V_{\text{GT}} =$ Low, SYNC = High, oscillator shut down.

## Application Information

$$I_{\text{PULL-IN}} = \frac{V_{\text{CS}}}{R_{\text{SENSE}}} \quad I_{\text{CS(HI)}} = 833\text{mV nom}$$

$$V_{\text{CS(LL)}} = \frac{V_{\text{DD}}}{1 + \frac{R_{\text{HDa}}}{R_{\text{HDb}}}} \quad V_{\text{DD}} = 9.0\text{V nom}$$

$$I_{\text{HOLD}} = \frac{V_{\text{CS(LL)}}}{R_{\text{SENSE}}}$$

$$t_{\text{PULL-IN}} = -(R_{\text{HDa}} R_{\text{HDb}}) C_{\text{HD}} \ln \left( 1 - \frac{V_{\text{CS(HL)}} - V_{\text{DD}}}{V_{\text{CS(LL)}} - V_{\text{DD}}} \right)$$

$$f_{\text{PWM}} \approx 3.23\text{kHz} + \frac{21.8\text{GHz} \cdot \Omega}{R_{\text{OSC}}} \quad (\text{valid for } f_{\text{PWM}} > 23\text{kHz})$$

$$V_{\text{CC}} = 1.25\text{V} \left( 1 + \frac{R_{\text{FBa}}}{R_{\text{FBb}}} \right)$$

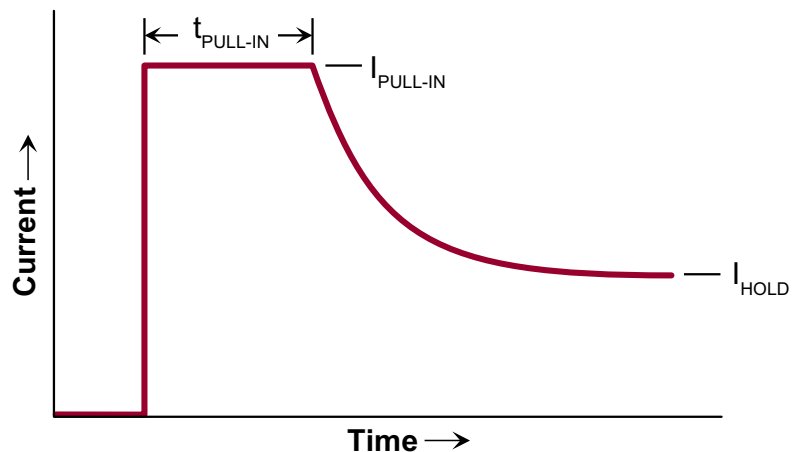


Figure 1

Application Information (cont.)

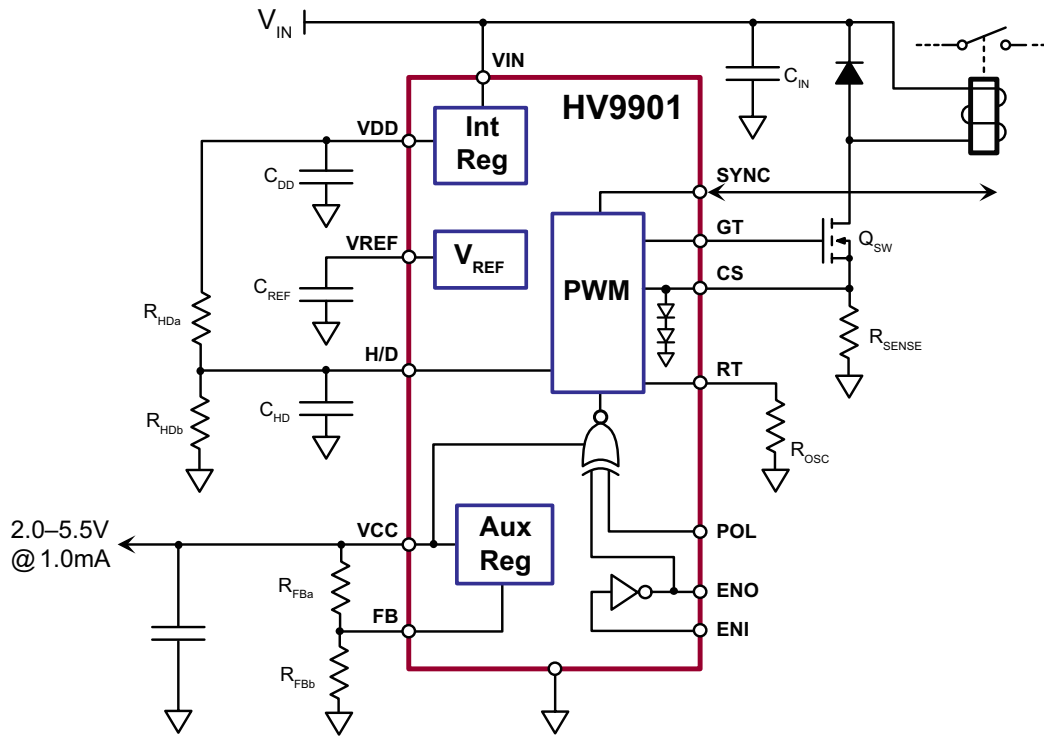
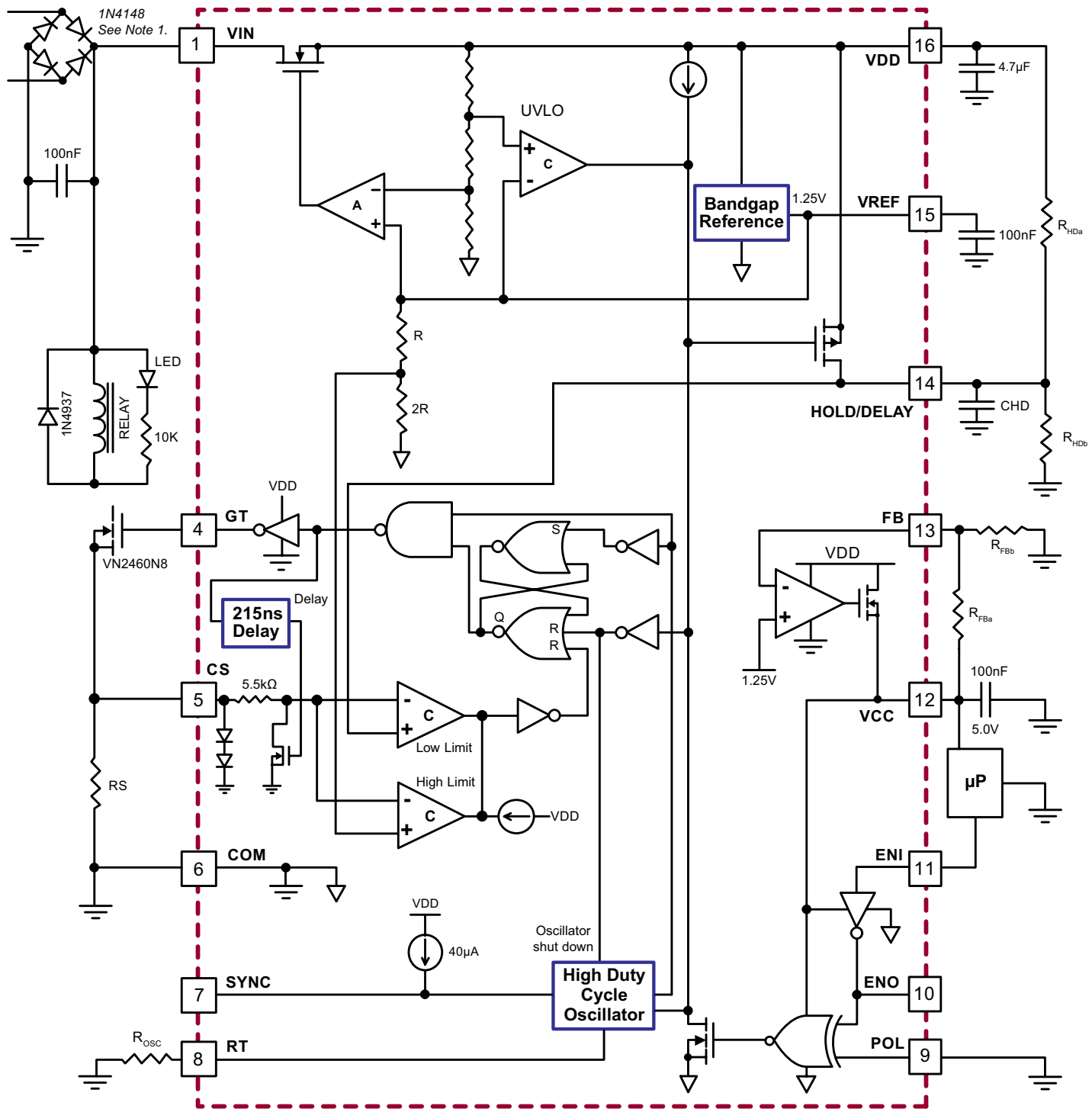


Figure 2

Pin Description

Pin #	Name	Description
1	VIN	Input supply.
2	-	Pin not present
3	-	Pin not present
4	GT	Gate driver output for driving the external switching MOSFET.
5	CS	Current sense input.
6	COM	Common. Connect to circuit ground.
7	SYNC	Open-drain input/output for synchronizing the internal PWM oscillator to other HV9901s or to an external clock.
8	RT	A resistor from this pin to ground sets the PWM switching frequency.
9	POL	Input that determines the polarity of the ENI input. See the truth table.
10	ENO	Enable out. It is the logical inversion of the ENI signal.
11	ENI	Enabled input. Whether ENI is active low or active high is determined by the POL input.
12	VCC	Output of the internal auxiliary regulator. Output voltage is determined by the resistive divider connected to the FB pin.
13	FB	Feedback input for the auxiliary regulator.
14	H/D	HOLD/DELAY input. An RC network connected to this pin controls the pull-in time and the holding current. See the equations on page 4.
15	VREF	Internal reference voltage. Bypass locally with a 10nF capacitor.
16	VDD	Output of the internal regulator. Bypass locally with a 10nF capacitor.

Functional Block Diagram

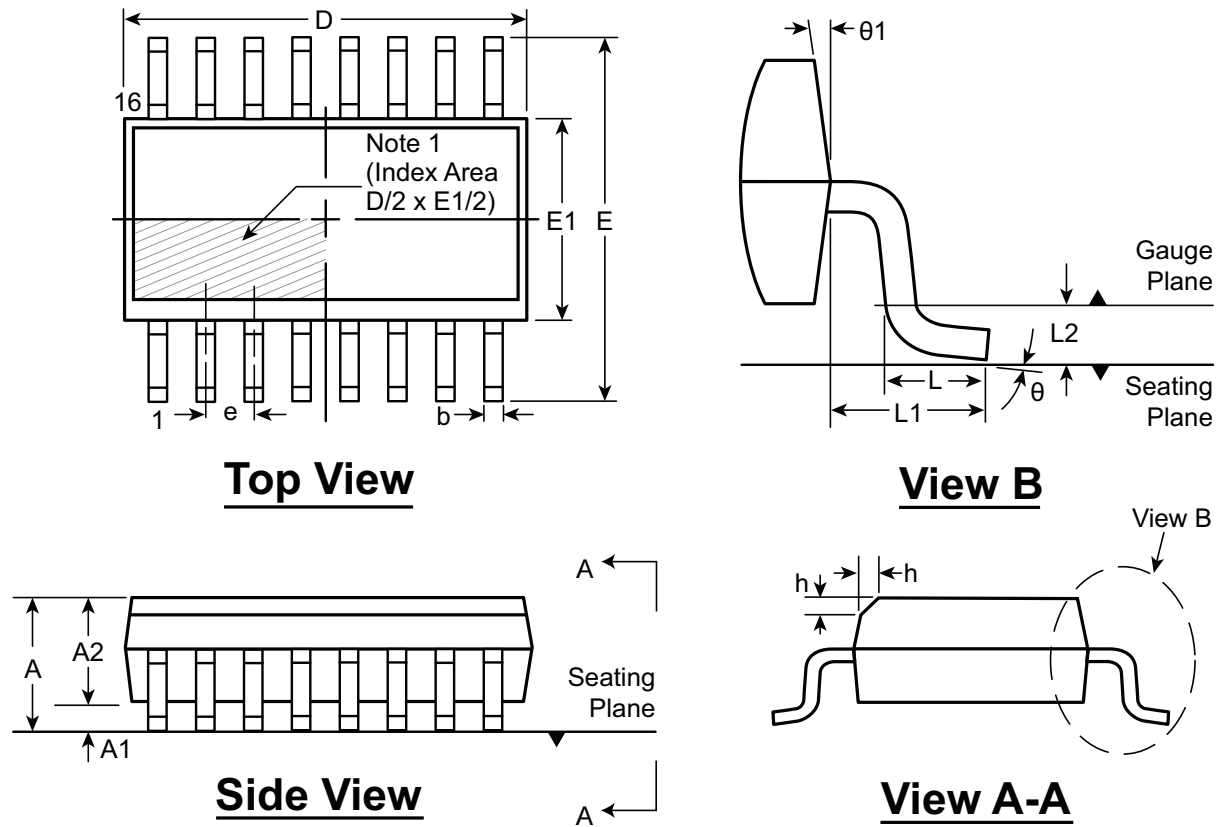


Notes:

1. This diode and bridge rectifier required only for AC operation.
2. For non-isolated AC operation the entire circuit must be floating.
3. All comparators have open drain outputs.

# 16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



**Note:**  
 1. This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	E	E1	e	h	L	L1	L2	□	□1	
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.

\* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-16SONG, Version G041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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