

# 74LVC1G175

Single D-type flip-flop with reset; positive-edge trigger

Rev. 03 — 21 May 2007

Product data sheet

## 1. General description

The 74LVC1G175 is a low-power, low-voltage single positive edge triggered D-type flip-flop with individual data (D) input, clock (CP) input, master reset ( $\overline{\text{MR}}$ ) input, and Q output.

The master reset ( $\overline{\text{MR}}$ ) is an asynchronous active LOW input and operates independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using  $I_{\text{OFF}}$ . The  $I_{\text{OFF}}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

## 2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8B/JESD36 (2.7 V to 3.6 V).
- $\pm 24$  mA output drive ( $V_{\text{CC}} = 3.0$  V)
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V.
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C.

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC1G175GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74LVC1G175GV	-40 °C to +125 °C	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457
74LVC1G175GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G175GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891

### 4. Marking

Table 2. Marking

Type number	Marking code
74LVC1G175GW	YT
74LVC1G175GV	V75
74LVC1G175GM	YT
74LVC1G175GF	YT

### 5. Functional diagram

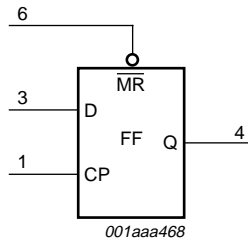


Fig 1. Logic symbol.

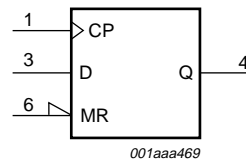


Fig 2. IEC logic symbol.

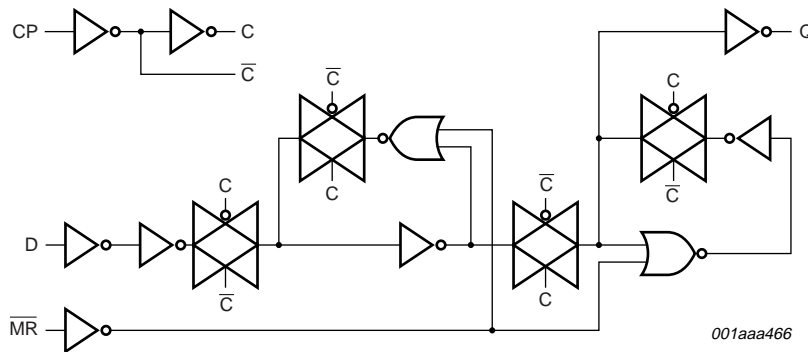
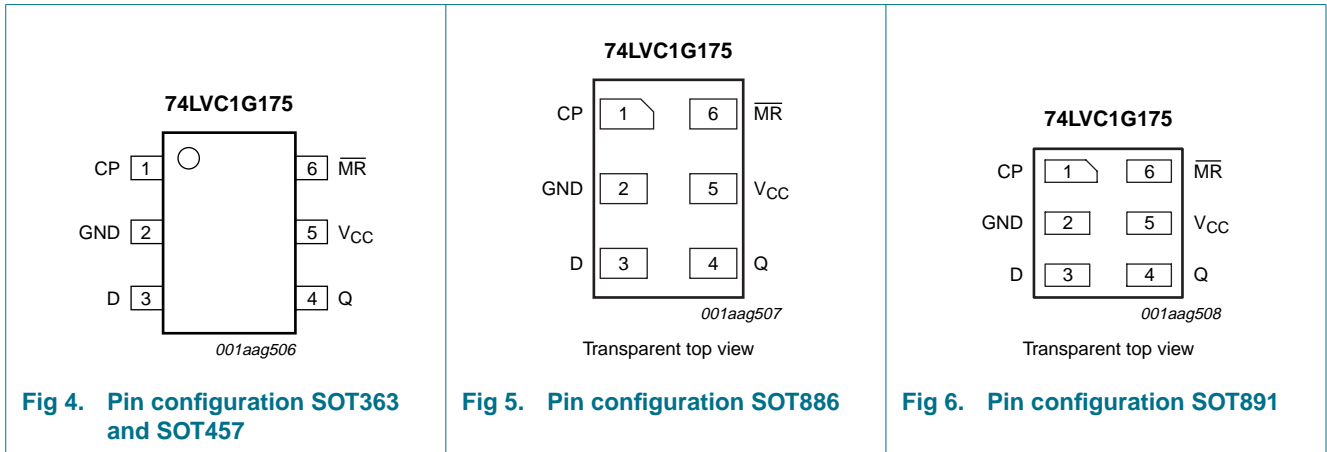


Fig 3. Logic diagram.

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
GND	2	ground (0 V)
D	3	data input
Q	4	flip-flop output
V <sub>CC</sub>	5	supply voltage
MR	6	master reset input (active LOW)

## 7. Functional description

Table 4. Function table<sup>[1]</sup>

Operating mode	Input			Output
	MR	CP	D	Q
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

[1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 ↑ = LOW-to-HIGH CP transition;  
 X = don't care.

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	Active mode	[1][2] -0.5	$V_{CC} + 0.5$	V
		Power-down mode	[1][2] -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	250	mW
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When  $V_{CC} = 0$  V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For SC-88 and SC-74A packages: above 87.5 °C the value of  $P_{tot}$  derates linearly with 4.0 mW/K.  
For XSON6 packages: above 45 °C the value of  $P_{tot}$  derates linearly with 2.4 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	Active mode	0	-	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	-	5.5	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	-	10	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40\text{ °C to }+85\text{ °C}</math><sup>[1]</sup></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}$ ; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}$ ; $V_{CC} = 1.65\text{ V}$	1.2	1.54	-	V
		$I_O = -8\text{ mA}$ ; $V_{CC} = 2.3\text{ V}$	1.9	2.15	-	V
		$I_O = -12\text{ mA}$ ; $V_{CC} = 2.7\text{ V}$	2.2	2.50	-	V
		$I_O = -24\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$	2.3	2.62	-	V
		$I_O = -32\text{ mA}$ ; $V_{CC} = 4.5\text{ V}$	3.8	4.11	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}$ ; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.10	V
		$I_O = 4\text{ mA}$ ; $V_{CC} = 1.65\text{ V}$	-	0.07	0.45	V
		$I_O = 8\text{ mA}$ ; $V_{CC} = 2.3\text{ V}$	-	0.12	0.30	V
		$I_O = 12\text{ mA}$ ; $V_{CC} = 2.7\text{ V}$	-	0.17	0.40	V
		$I_O = 24\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$	-	0.33	0.55	V
		$I_O = 32\text{ mA}$ ; $V_{CC} = 4.5\text{ V}$	-	0.39	0.55	V
$I_I$	input leakage current	$V_{CC} = 0\text{ V to }5.5\text{ V}$ ; $V_I = 5.5\text{ V}$ or GND	[2] -	$\pm 0.1$	$\pm 5$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 5.5\text{ V}$	-	$\pm 0.1$	$\pm 10$	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 1.65\text{ V to }5.5\text{ V}$ ; $I_O = 0\text{ A}$ ; $V_I = 5.5\text{ V}$ or GND	-	0.1	10	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	$V_{CC} = 2.3\text{ V to }5.5\text{ V}$ ; $V_I = V_{CC} - 0.6\text{ V}$ ; $I_O = 0\text{ A}$	[2] -	5	500	$\mu\text{A}$
$C_I$	input capacitance	$V_{CC} = 3.3\text{ V}$ ; $V_I = \text{GND to }V_{CC}$	-	2.5	-	pF

**Table 7. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	0.95	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.7	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	1.9	-	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.0	-	-	V
		I <sub>O</sub> = -32 mA; V <sub>CC</sub> = 4.5 V	3.4	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.10	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.70	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.80	V
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V	-	-	0.80	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 0 V to 5.5 V; V <sub>I</sub> = 5.5 V or GND	-	-	±20	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 1.65 V to 5.5 V; I <sub>O</sub> = 0 A; V <sub>I</sub> = 5.5 V or GND	-	-	40	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>CC</sub> = 2.3 V to 5.5 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	-	5000	μA

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

[2] These typical values are measured at V<sub>CC</sub> = 3.3 V.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit		
			Min	Typ <sup>[1]</sup>	Max	Min	Max			
t <sub>pd</sub>	propagation delay	CP to Q; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	4.9	13.4	1.5	17	ns		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.1	7.1	1.0	9.0	ns		
		V <sub>CC</sub> = 2.7 V	1.0	3.2	7.1	1.0	9.0	ns		
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.1	5.7	0.5	7.5	ns		
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	2.2	4.0	0.5	5.5	ns		
		$\overline{\text{MR}}$ to Q; see <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	4.3	12.9	1.5	17	ns		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.8	7.0	1.0	9.0	ns		
		V <sub>CC</sub> = 2.7 V	1.0	3.0	7.0	1.0	9.0	ns		
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.5	5.8	0.5	7.5	ns		
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	2.0	4.1	0.5	5.5	ns		
		t <sub>w</sub>	pulse width	CP HIGH or LOW; see <a href="#">Figure 7</a>						
				V <sub>CC</sub> = 1.65 V to 1.95 V	6.2	-	-	6.2	-	ns
V <sub>CC</sub> = 2.3 V to 2.7 V	2.7			-	-	2.7	-	ns		
V <sub>CC</sub> = 2.7 V	2.7			-	-	2.7	-	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V	2.7			1.3	-	2.7	-	ns		
V <sub>CC</sub> = 4.5 V to 5.5 V	2.0			-	-	2.0	-	ns		
$\overline{\text{MR}}$ LOW; see <a href="#">Figure 8</a>										
V <sub>CC</sub> = 1.65 V to 1.95 V	6.2			-	-	6.2	-	ns		
V <sub>CC</sub> = 2.3 V to 2.7 V	2.7			-	-	2.7	-	ns		
V <sub>CC</sub> = 2.7 V	2.7			-	-	2.7	-	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V	2.7			1.6	-	2.7	-	ns		
V <sub>CC</sub> = 4.5 V to 5.5 V	2.0			-	-	2.0	-	ns		
t <sub>rec</sub>	recovery time			$\overline{\text{MR}}$ ; see <a href="#">Figure 8</a>						
				V <sub>CC</sub> = 1.65 V to 1.95 V	1.9	-	-	1.9	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.4	-	-	1.4	-	ns		
		V <sub>CC</sub> = 2.7 V	1.3	-	-	1.3	-	ns		
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.2	0.4	-	1.2	-	ns		
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns		
t <sub>su</sub>	set-up time	D to CP; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.9	-	-	2.9	-	ns		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	ns		
		V <sub>CC</sub> = 2.7 V	1.7	-	-	1.7	-	ns		
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.3	0.5	-	1.3	-	ns		
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.1	-	-	1.1	-	ns		

**Table 8. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>h</sub>	hold time	D to CP; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.0	-	-	0.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.3	-	-	0.3	-	ns
		V <sub>CC</sub> = 2.7 V	0.5	-	-	0.5	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.2	0.2	-	1.2	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	-	-	0.5	-	ns
f <sub>max</sub>	maximum frequency	CP; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	80	125	-	80	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	175	-	-	175	-	MHz
		V <sub>CC</sub> = 2.7 V	175	-	-	175	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	175	300	-	175	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V	200	-	-	200	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V <a href="#">[3]</a>	-	14	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

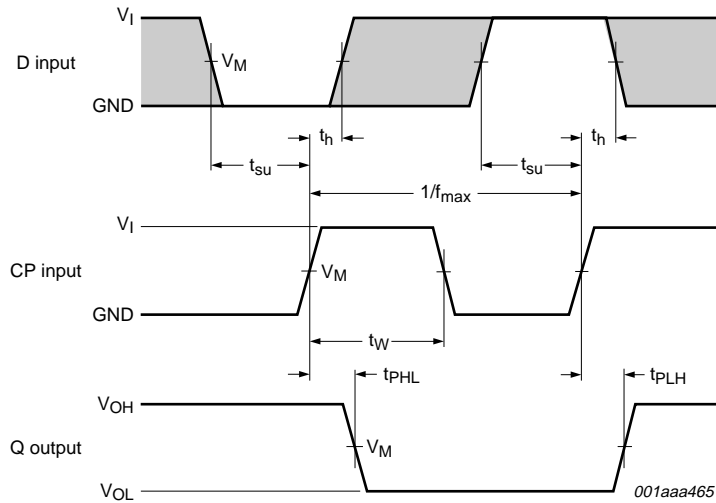
V<sub>CC</sub> = supply voltage in Volts;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

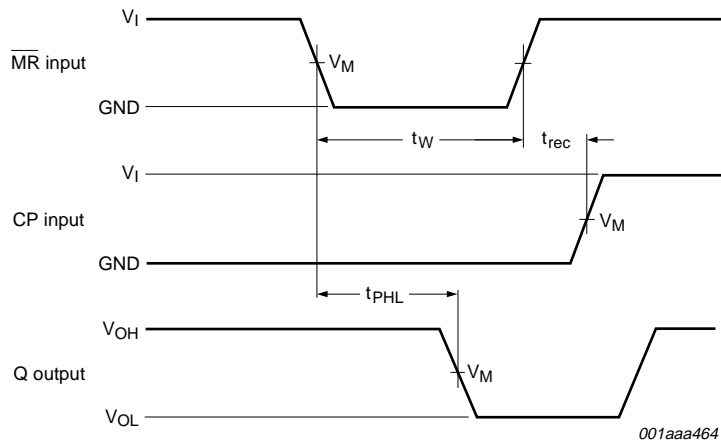


12. Waveforms



Measurement points are given in [Table 9](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage drops that occur with the output load.

**Fig 7. The clock input (CP) to output (Q) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times, and the maximum clock pulse frequency**

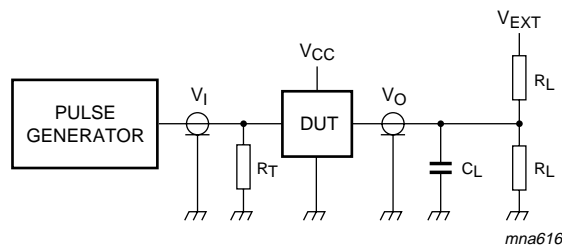


Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage drops that occur with the output load.

**Fig 8. The master reset (MR) input to output (Q) propagation delays, the master reset pulse width, and the MR to CP recovery time**

Table 9. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

Fig 9. Load circuitry for switching times

Table 10. Test data

Supply voltage	Input	Load			$V_{EXT}$
$V_{CC}$	$V_I$	$t_r = t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open

13. Package outline

Plastic surface-mounted package; 6 leads

SOT363

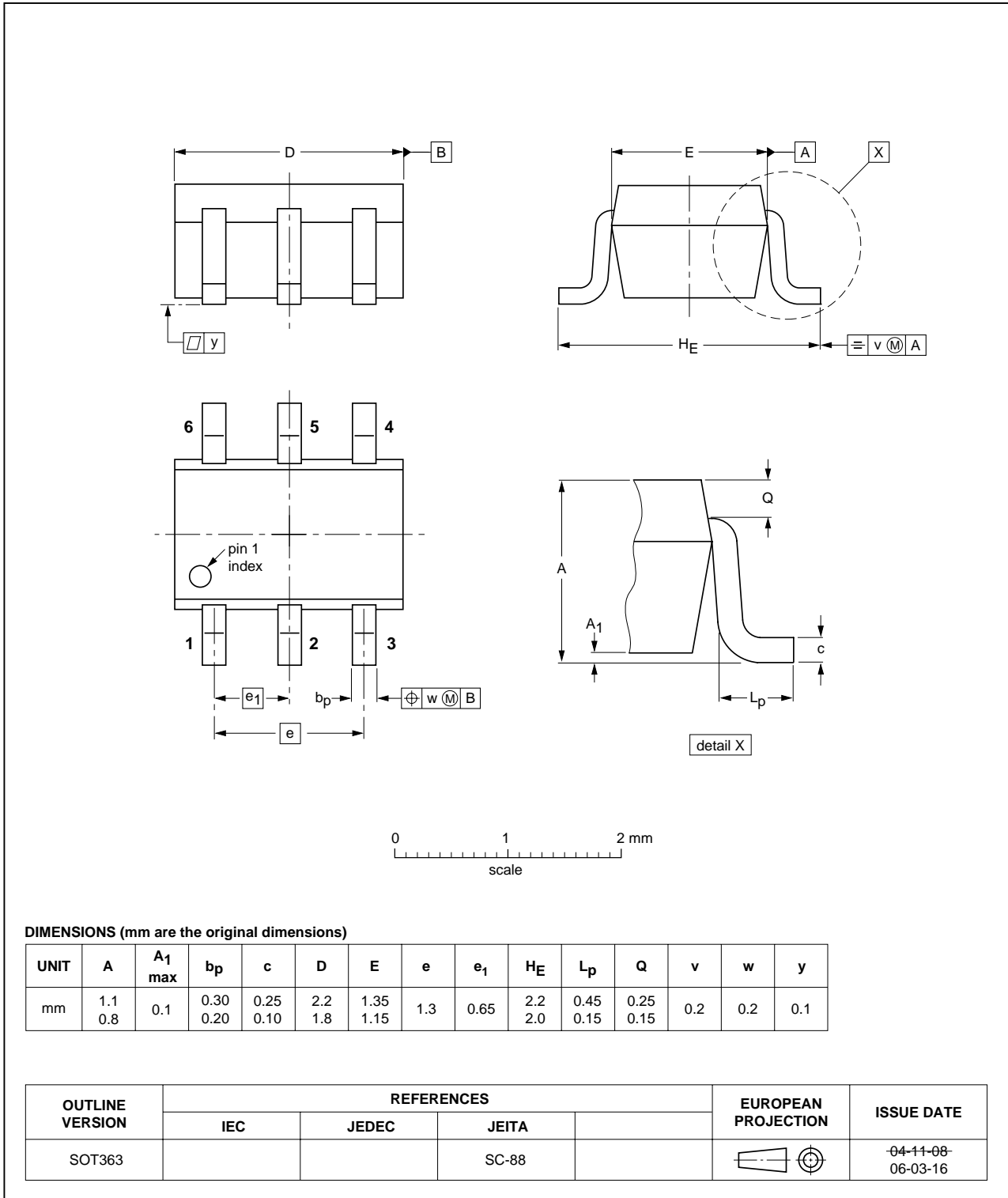


Fig 10. Package outline SOT363 (SC-88)

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

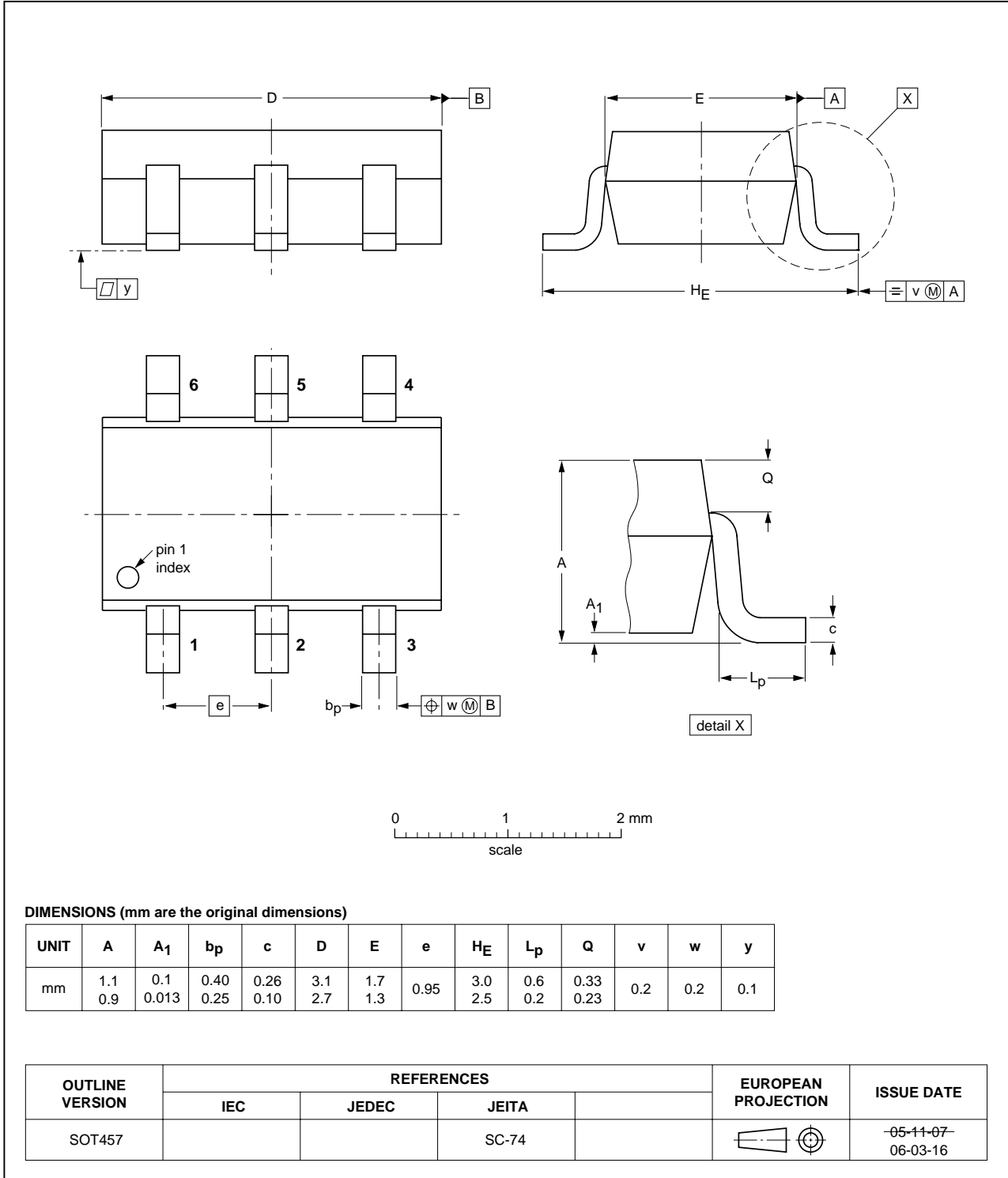


Fig 11. Package outline SOT457 (SC-74)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



Fig 12. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

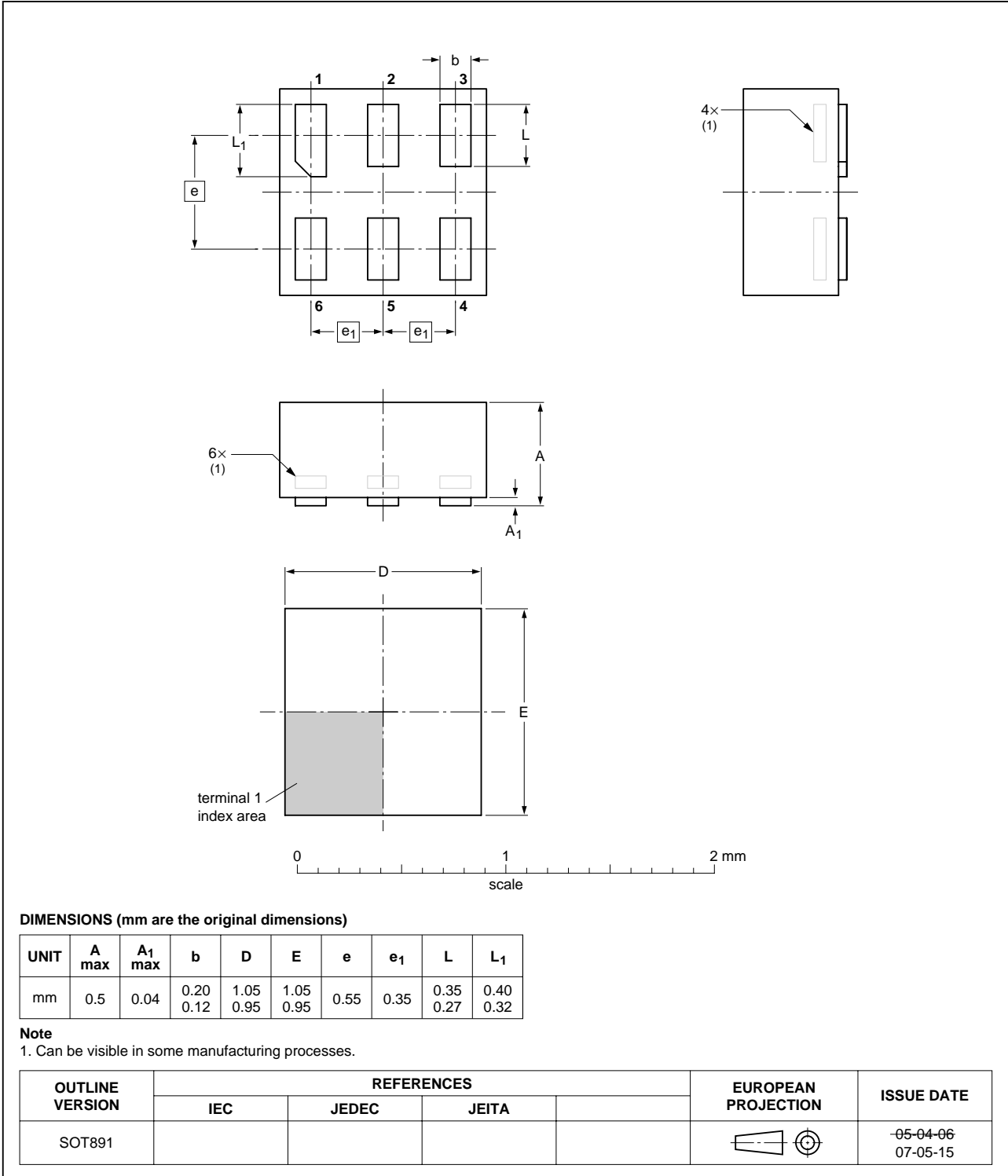


Fig 13. Package outline SOT891 (XSON6)

## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G175_3	20070521	Product data sheet	-	74LVC1G175_2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Added type number 74LVC1G175GF (XSON6/SOT891 package)</li> <li><a href="#">Section 10 "Static characteristics"</a>: Changed: Conditions for input leakage and supply current.</li> </ul>			
74LVC1G175_2	20041018	Product specification	-	74LVC1G175_1
74LVC1G175_1	20040318	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 18. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Marking</b> .....	<b>2</b>
<b>5</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>3</b>
6.1	Pinning .....	3
6.2	Pin description .....	3
<b>7</b>	<b>Functional description</b> .....	<b>3</b>
<b>8</b>	<b>Limiting values</b> .....	<b>4</b>
<b>9</b>	<b>Recommended operating conditions</b> .....	<b>4</b>
<b>10</b>	<b>Static characteristics</b> .....	<b>5</b>
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>7</b>
<b>12</b>	<b>Waveforms</b> .....	<b>9</b>
<b>13</b>	<b>Package outline</b> .....	<b>11</b>
<b>14</b>	<b>Abbreviations</b> .....	<b>15</b>
<b>15</b>	<b>Revision history</b> .....	<b>15</b>
<b>16</b>	<b>Legal information</b> .....	<b>16</b>
16.1	Data sheet status .....	16
16.2	Definitions .....	16
16.3	Disclaimers .....	16
16.4	Trademarks .....	16
<b>17</b>	<b>Contact information</b> .....	<b>16</b>
<b>18</b>	<b>Contents</b> .....	<b>17</b>

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