



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

P-Channel Silicon MOSFET

ATP112 — General-Purpose Switching Device Applications

Features

- ON-resistance $R_{DS(on)1}=33m\Omega$ (typ.)
- 4V drive
- Protection diode in
- Input Capacitance $C_{iss}=1450pF$ (typ.)
- Halogen free compliance

Specifications

Absolute Maximum Ratings at $T_a=25^\circ C$

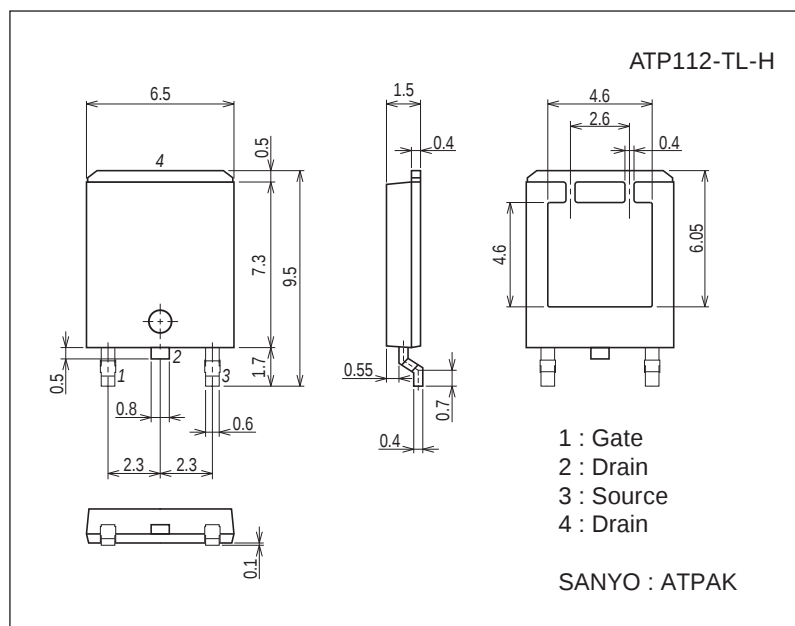
Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		-60	V
Gate-to-Source Voltage	V_{GSS}		± 20	V
Drain Current (DC)	I_D		-25	A
Drain Current ($PW \leq 10\mu s$)	I_{DP}	$PW \leq 10\mu s$, duty cycle $\leq 1\%$	-75	A
Allowable Power Dissipation	P_D	$T_c=25^\circ C$	40	W
Channel Temperature	T_{ch}		150	$^\circ C$
Storage Temperature	T_{stg}		-55 to +150	$^\circ C$
Avalanche Energy (Single Pulse) *1	E_{AS}		50	mJ
Avalanche Current *2	I_{AV}		-13	A

Note : *1 $V_{DD}=-10V$, $L=500\mu H$, $I_{AV}=-13A$ *2 $L \leq 500\mu H$, Single pulse

Package Dimensions

unit : mm (typ)

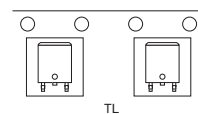
7057-001



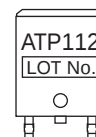
Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

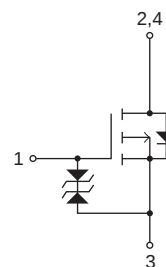
Packing Type: TL



Marking



Electrical Connection

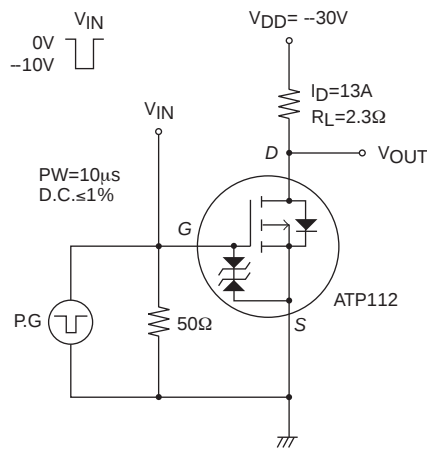


ATP112

Electrical Characteristics at Ta=25°C

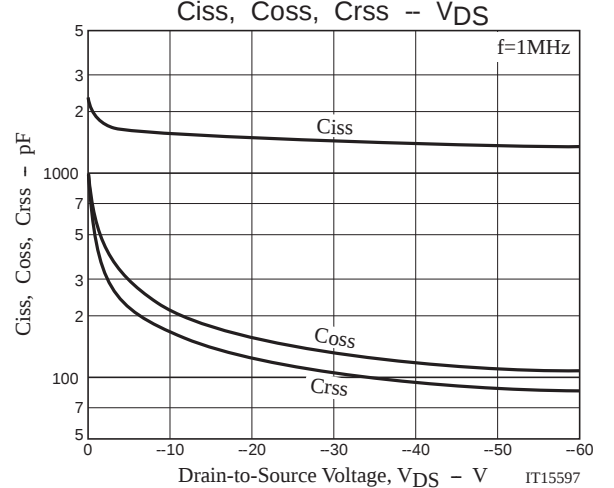
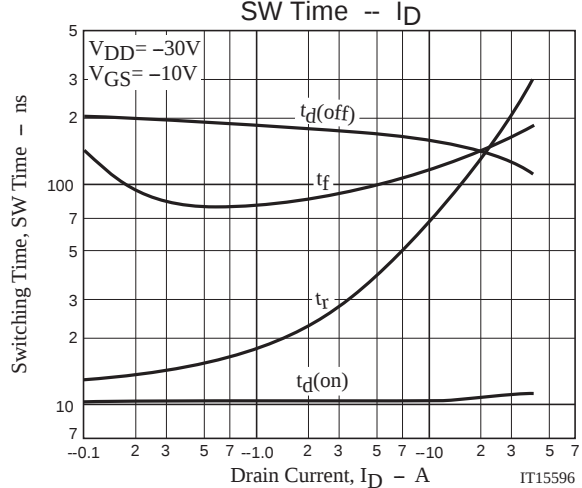
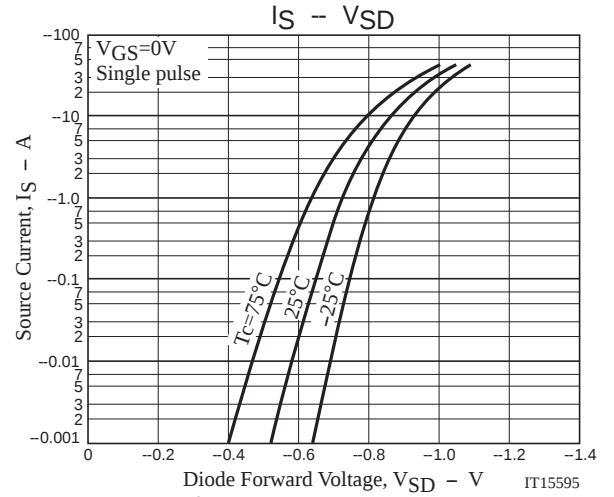
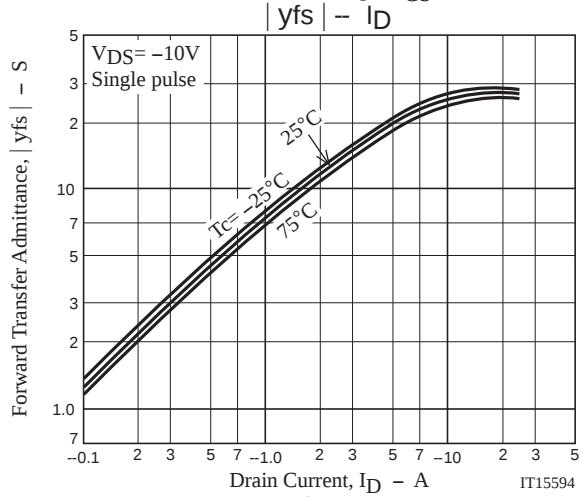
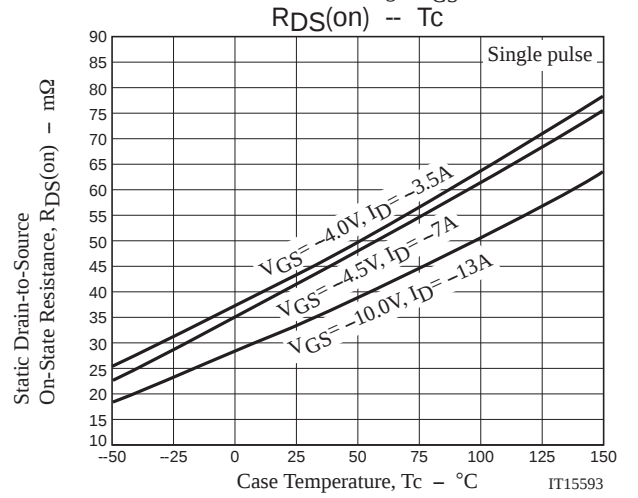
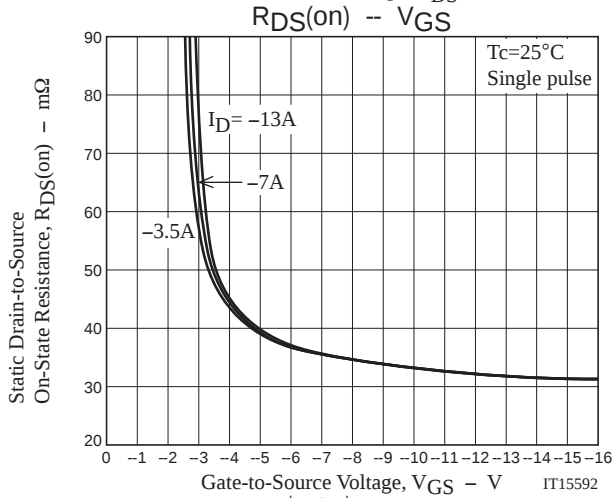
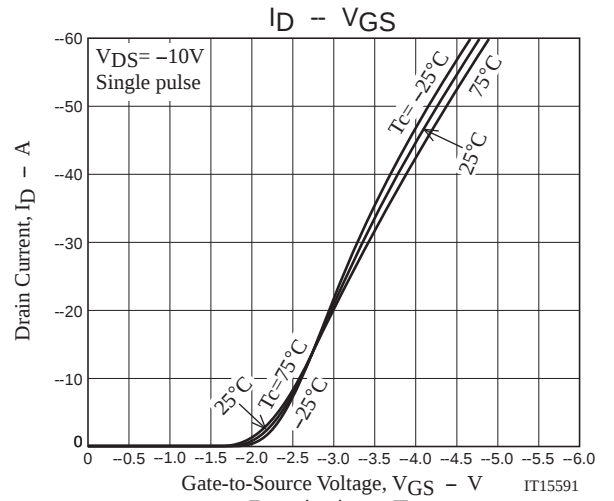
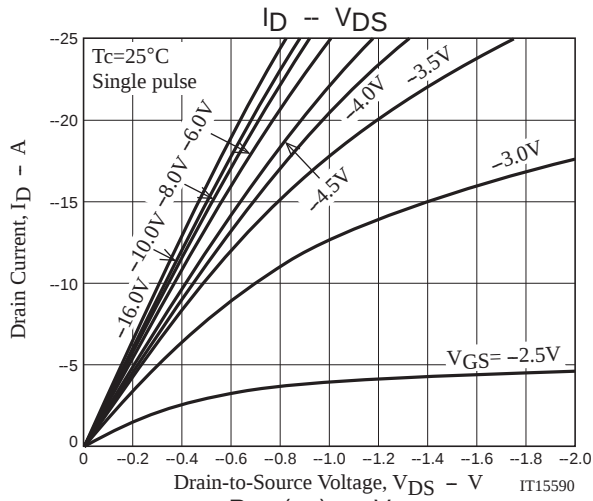
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = -1mA, V_{GS} = 0V$	-60			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60V, V_{GS} = 0V$			-1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 16V, V_{DS} = 0V$			± 10	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = -10V, I_D = -1mA$	-1.2		-2.6	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10V, I_D = -13A$		24		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)1}$	$I_D = -13A, V_{GS} = -10V$		33	43	$m\Omega$
	$R_{DS(on)2}$	$I_D = -7A, V_{GS} = -4.5V$		42	59	$m\Omega$
	$R_{DS(on)3}$	$I_D = -3.5A, V_{GS} = -4V$		45	63	$m\Omega$
Input Capacitance	C_{iss}	$V_{DS} = -20V, f = 1MHz$		1450		pF
Output Capacitance	C_{oss}			155		pF
Reverse Transfer Capacitance	C_{rss}			125		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit.		10		ns
Rise Time	t_r			80		ns
Turn-OFF Delay Time	$t_{d(off)}$			150		ns
Fall Time	t_f			120		ns
Total Gate Charge	Q_g	$V_{DS} = -30V, V_{GS} = -10V, I_D = -25A$		33.5		nC
Gate-to-Source Charge	Q_{gs}			5.3		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			7.9		nC
Diode Forward Voltage	V_{SD}	$I_S = -25A, V_{GS} = 0V$		-0.97	-1.5	V

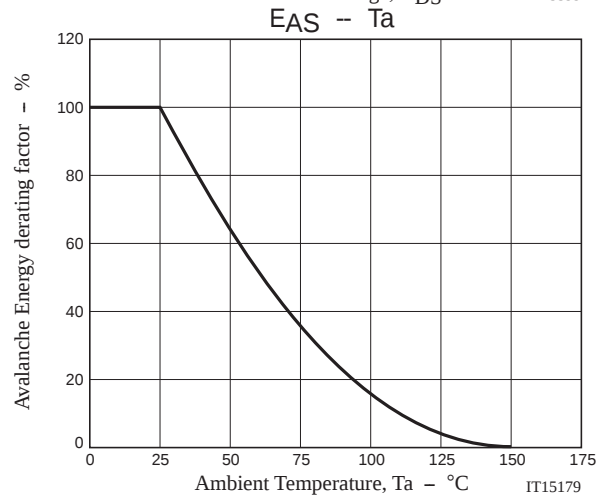
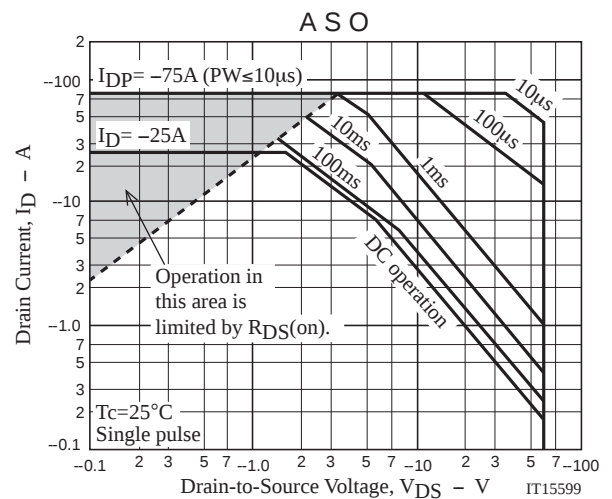
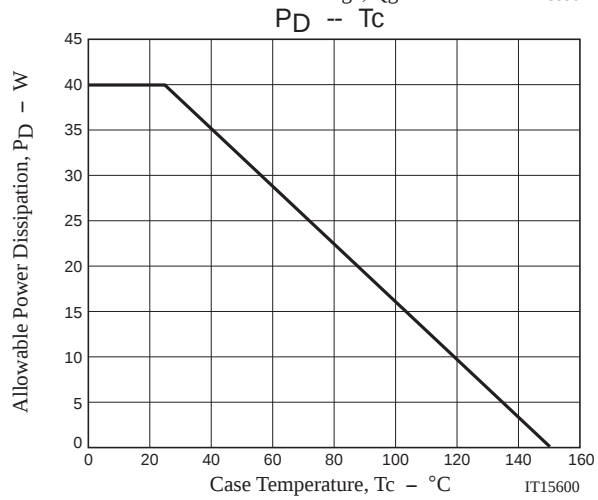
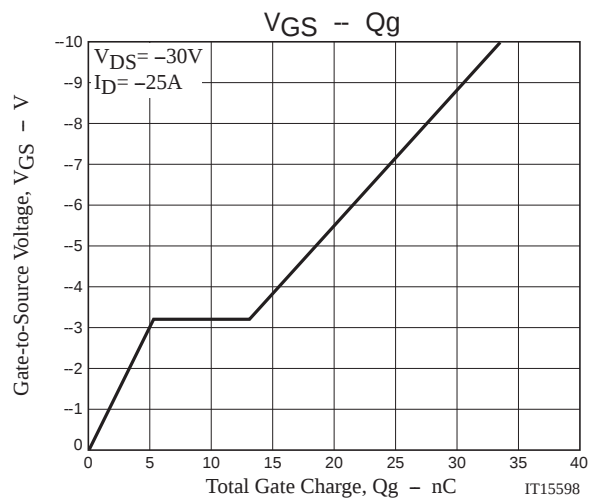
Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
ATP112-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free





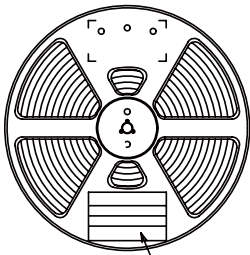
Taping Specification

ATP112-TL-H

1. Packing Format (TL)

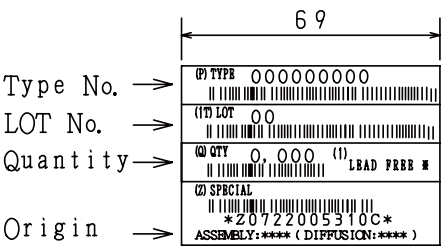
Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3,000	3,000	15,000	1 reels contained Dimensions:mm (external) 340×340×28	5 inner boxes contained Dimensions:mm (external) 355×355×165

Packing method



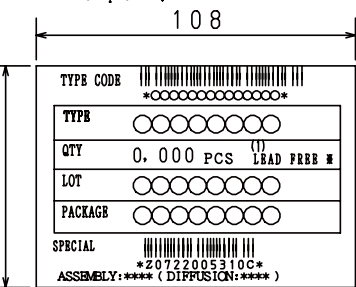
Reel label

Reel label, Inner box label
(unit:mm)



Outer box label

It is a label at the time of factory shipments.
The form of a label may change in physical
distribution process.



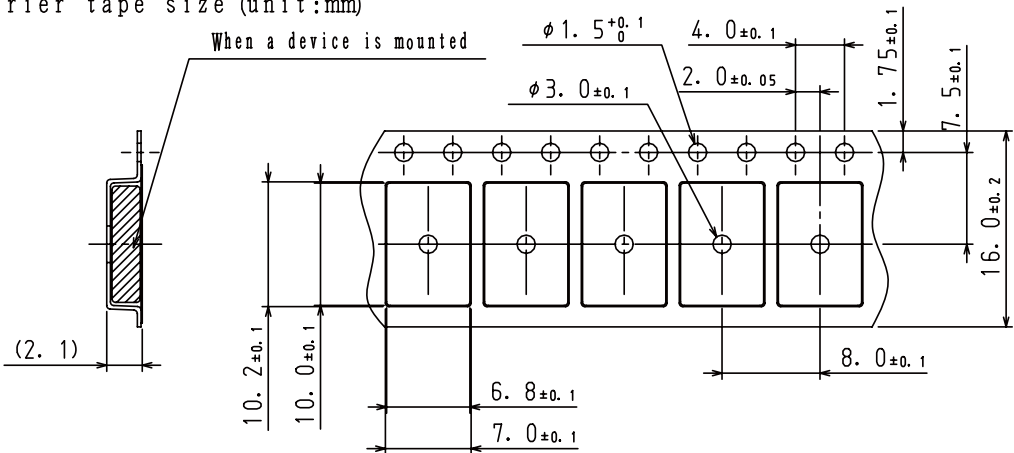
NOTE (1)

The LEAD FREE * description shows that the surface
treatment of the terminal is lead free.

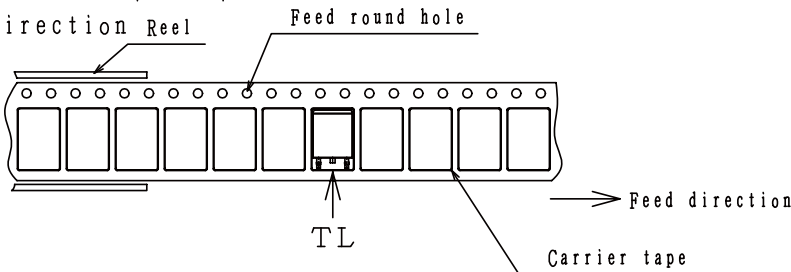
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction Reel

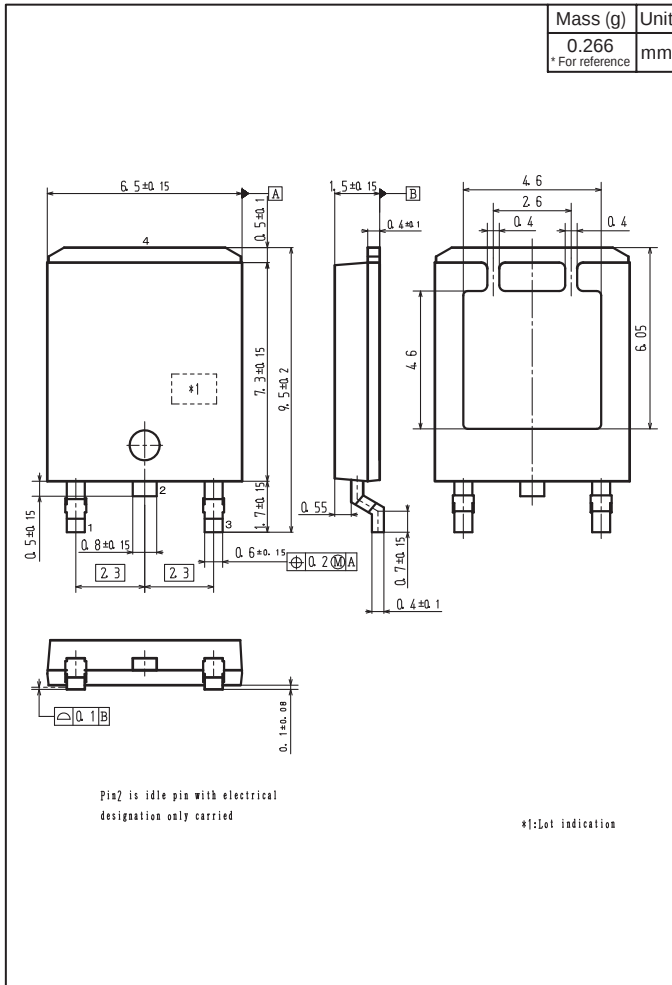


The one electrode terminals on feed hole side...TL

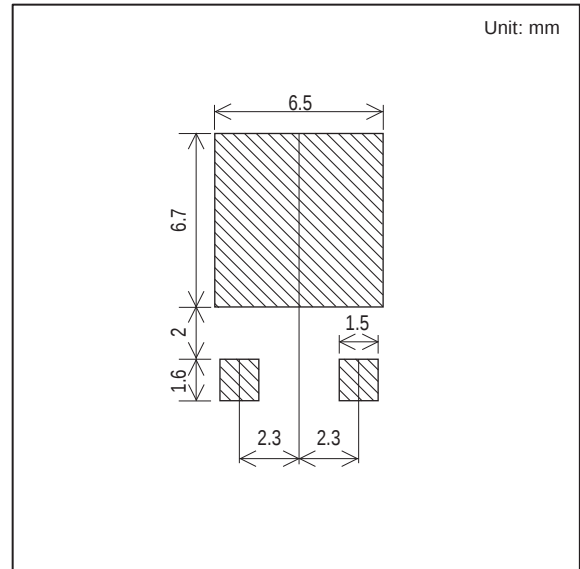
ATP112

Outline Drawing

ATP112-TL-H



Land Pattern Example



Note on usage : Since the ATP112 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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