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FDBL0200N100

N-Channel PowerTrench® MOSFET

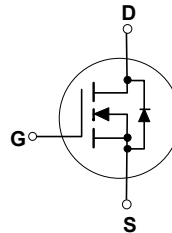
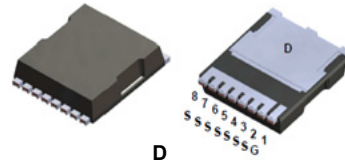
100 V, 300 A, 2.0 mΩ

Features

- Typical $R_{DS(on)}$ = 1.5 mΩ at $V_{GS} = 10V$, $I_D = 80 A$
- Typical $Q_g(tot)$ = 95 nC at $V_{GS} = 10V$, $I_D = 80 A$
- UIS Capability
- RoHS Compliant

Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch



For current package drawing, please refer to the Fairchild website at <http://www.fairchildsemi.com/dwg/PS/PSOF08A.pdf>.

FDBL0200N100 N-Channel PowerTrench® MOSFET

MOSFET Maximum Ratings $T_J = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Rated	Units
V_{DSS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (Note 1)	$T_C = 25^\circ C$	300
	Pulsed Drain Current	$T_C = 25^\circ C$	See Figure 4
E_{AS}	Single Pulse Avalanche Energy (Note 2)	352	mJ
P_D	Power Dissipation	429	W
	Derate Above $25^\circ C$	2.9	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to + 175	$^\circ C$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 3)	0.35	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3a)	43	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3b)	62.5	$^\circ C/W$

Notes:

- 1: Current is limited by silicon.
- 2: Starting $T_J = 25^\circ C$, $L = 0.1mH$, $I_{AS} = 84A$, $V_{DD} = 100V$ during inductor charging and $V_{DD} = 0V$ during time in avalanche.
- 3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design.
 - a) $43^\circ C/W$ when mounted on a $1 in^2$ pad of 2 oz copper
 - b) $62.5^\circ C/W$ when mounted on a minimum pad of 2 oz copper

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDBL0200N100	FDBL0200N100	MO-299A	13"	24mm	2000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

$B_{V_{DS}}$	Drain-to-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 100\text{V}, T_J = 25^\circ\text{C}$	-	-	5	μA
		$V_{GS} = 0\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	-	2	mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	3.1	4.5	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 80\text{A}, T_J = 25^\circ\text{C}$	-	1.5	2.0	$\text{m}\Omega$
		$V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	3.3	4.3	$\text{m}\Omega$

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	6970	9760	pF
C_{oss}	Output Capacitance		-	3950	5530	pF
C_{rss}	Reverse Transfer Capacitance		-	29	41	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	-	0.45	1	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	-	95	133	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V				
Q_{gs}	Gate-to-Source Gate Charge	$V_{DD} = 80\text{V}, I_D = 80\text{A}$	-	31	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge		-	20	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 50\text{V}, I_D = 80\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	-	-	73	ns
$t_{d(on)}$	Turn-On Delay		-	31	50	ns
t_r	Rise Time		-	25	40	ns
$t_{d(off)}$	Turn-Off Delay		-	36	58	ns
t_f	Fall Time		-	9	18	ns
t_{off}	Turn-Off Time		-	-	59	ns

Drain-Source Diode Characteristics

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 80\text{A}, V_{GS} = 0\text{V}$	-	-	1.25	V
		$I_{SD} = 40\text{A}, V_{GS} = 0\text{V}$	-	-	1.2	V
t_{rr}	Reverse-Recovery Time	$I_F = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	115	184	ns
Q_{rr}	Reverse-Recovery Charge	$V_{DD} = 80\text{V}$	-	172	273	nC

Note:

4: The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

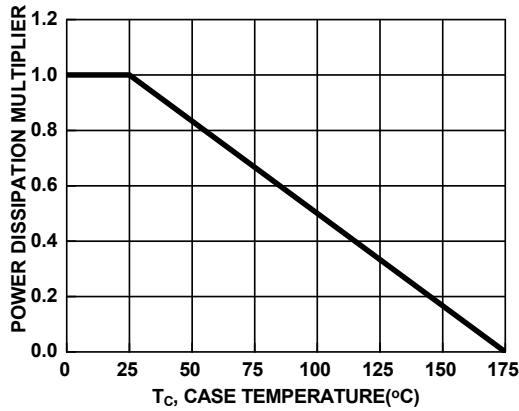


Figure 1. Normalized Power Dissipation vs. Case Temperature

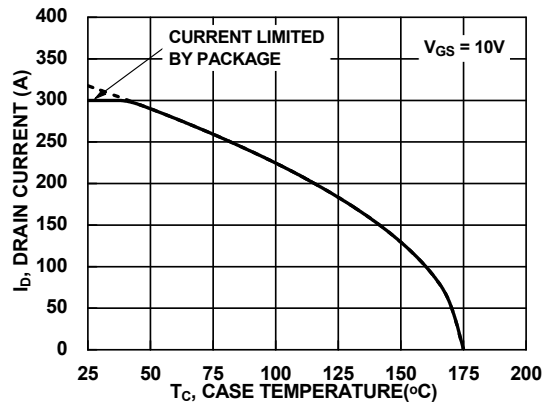


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

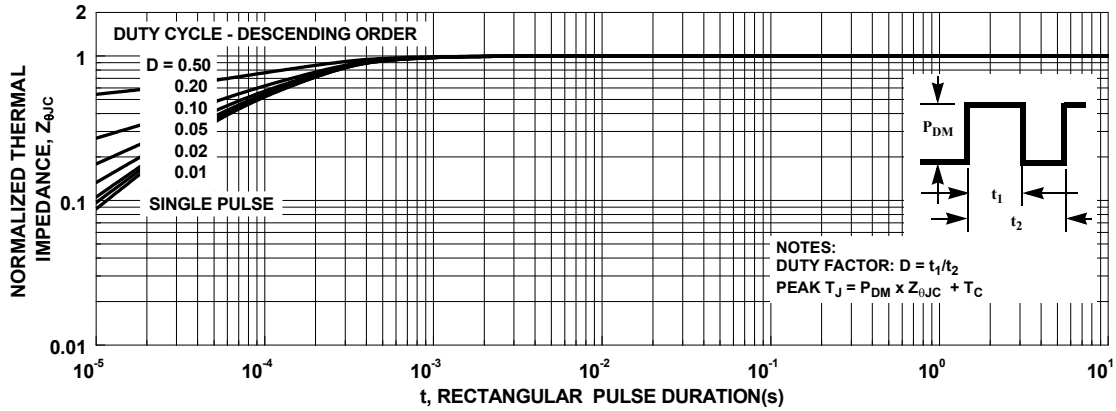


Figure 3. Normalized Maximum Transient Thermal Impedance

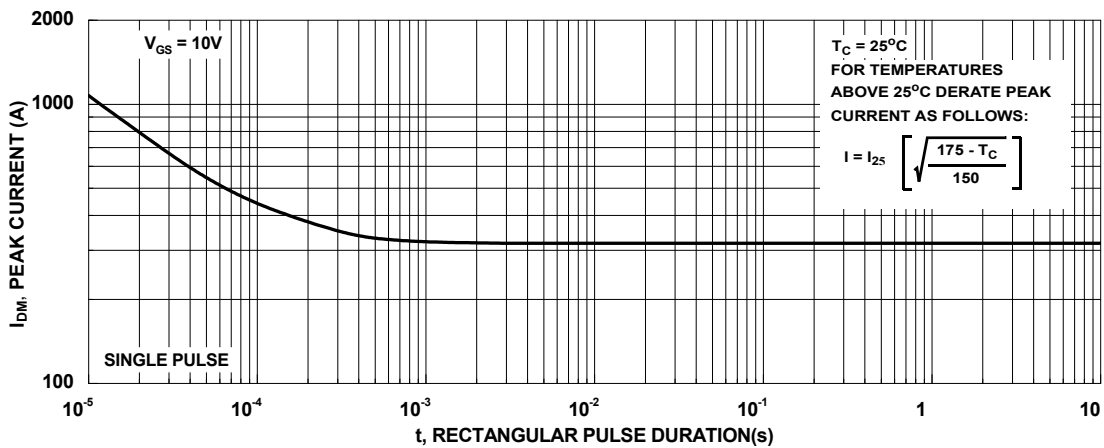


Figure 4. Peak Current Capability

Typical Characteristics

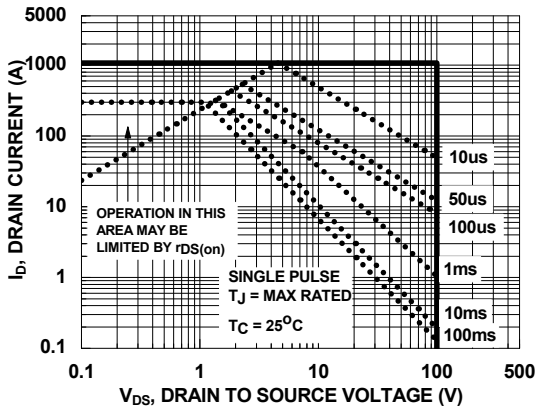
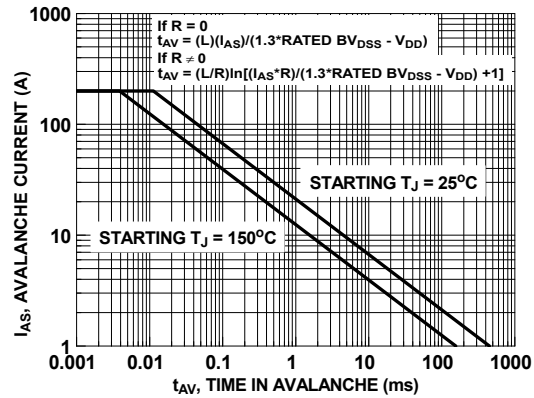


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

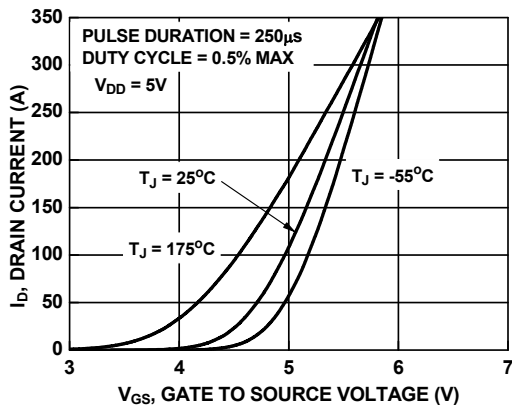


Figure 7. Transfer Characteristics

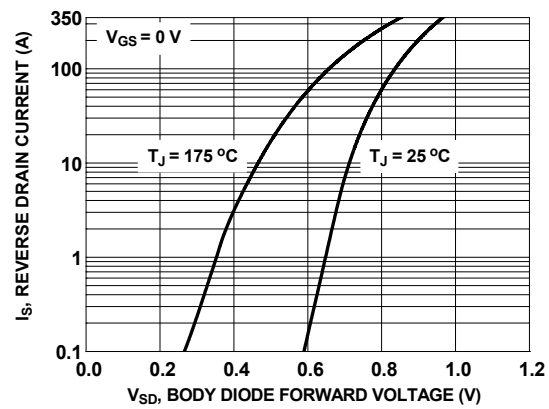


Figure 8. Forward Diode Characteristics

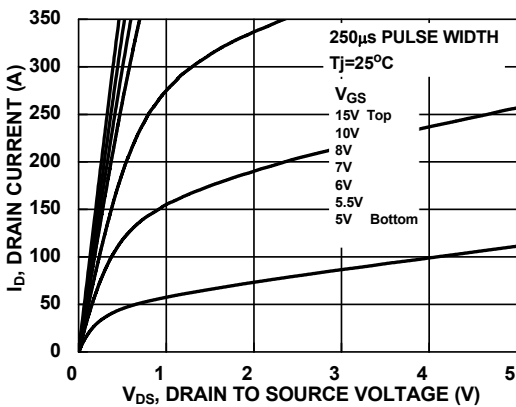


Figure 9. Saturation Characteristics

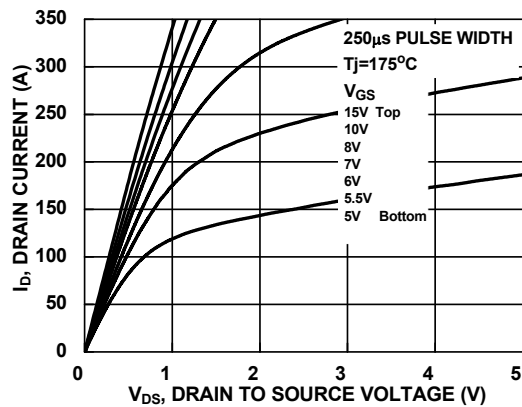


Figure 10. Saturation Characteristics

Typical Characteristics

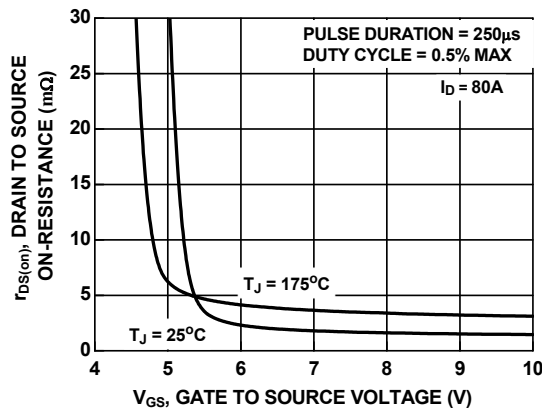


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

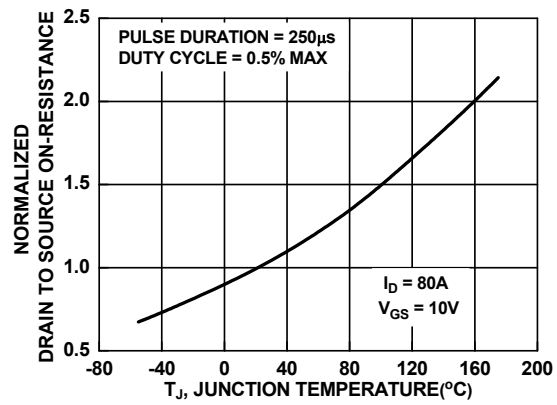


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

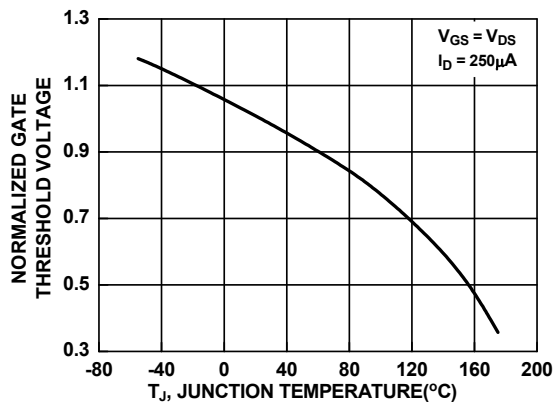


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

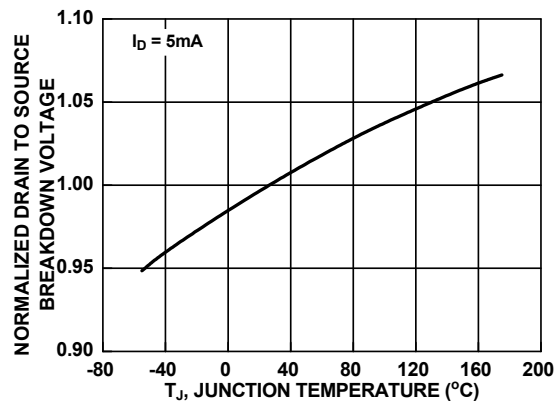


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

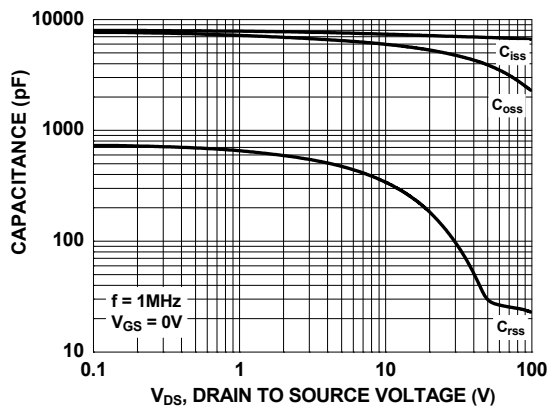


Figure 15. Capacitance vs. Drain to Source Voltage

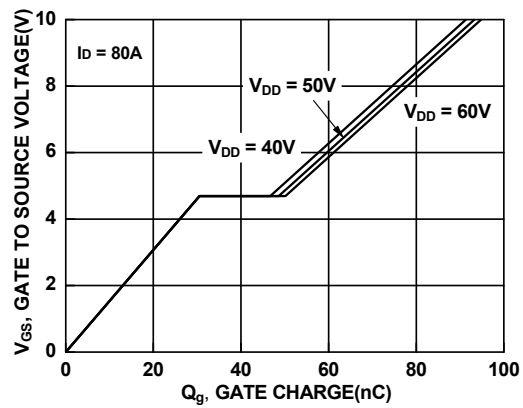
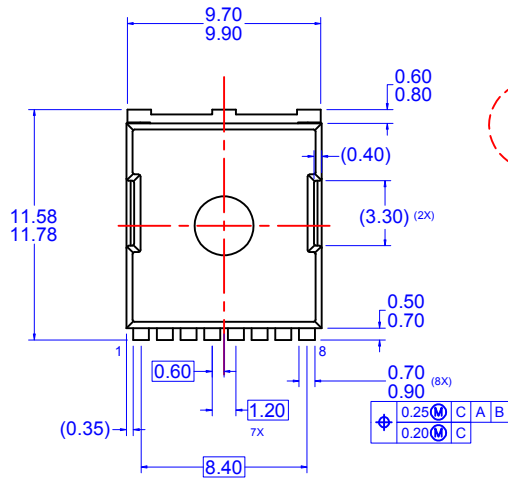
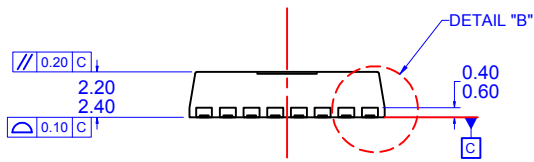
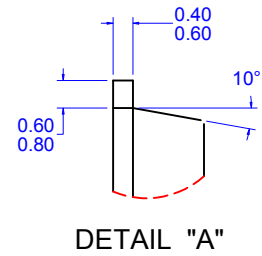
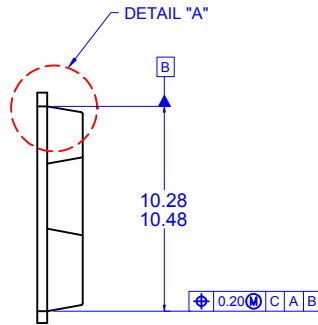


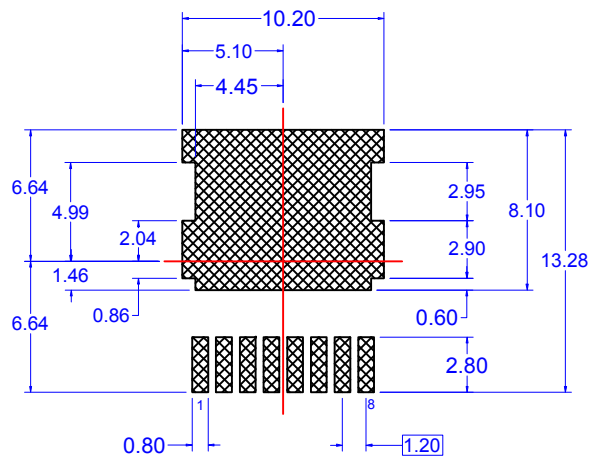
Figure 16. Gate Charge vs. Gate to Source Voltage



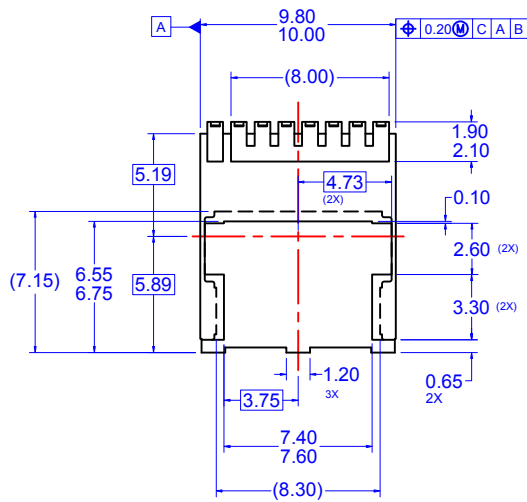
TOP VIEW



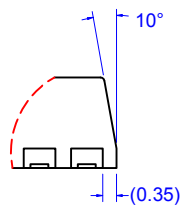
SIDE VIEW



LAND PATTERN RECOMMENDATION



BOTTOM VIEW



DETAIL "B"

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - E) DRAWING FILE NAME: MKT-PSOF08AREV3

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