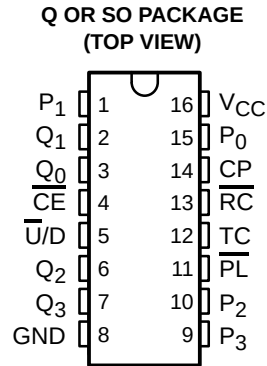


- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- 64-mA Output Sink Current
32-mA Output Source Current



description

The CY74FCT191T is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting. The preset allows the CY74FCT191T to be used in programmable dividers. The count enable input, terminal count output, and ripple-clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION
$\overline{CE}$	Count enable input (active low)
CP	Clock pulse input (active rising edge)
P	Parallel data inputs
$\overline{PL}$	Asynchronous parallel load input (active low)
$\overline{U/D}$	Up/down count control input
Q	Flip-flop outputs
$\overline{RC}$	Ripple clock output (active low)
TC	Terminal count output



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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CY74FCT191T

4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001

ORDERING INFORMATION

T _A	PACKAGE [†]		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	6.2	CY74FCT191CTQCT	FT191-3
	SOIC – SO	Tube	6.2	CY74FCT191CTSOC	FCT191C
		Tape and reel	6.2	CY74FCT191CTSOCT	
	SOIC – SO	Tube	7.8	CY74FCT191ATSOC	FCT191A
		Tape and reel	7.8	CY74FCT191ATSOCT	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

$\overline{RC}$ FUNCTION

INPUTS		OUTPUTS	
$\overline{CE}$	CP	TC [†]	$\overline{RC}$
L		H	
H	X	X	H
X	X	L	H

H = High logic level, L = Low logic level,

X = Don't care,  = Low pulse

[†] TC is generated internally.

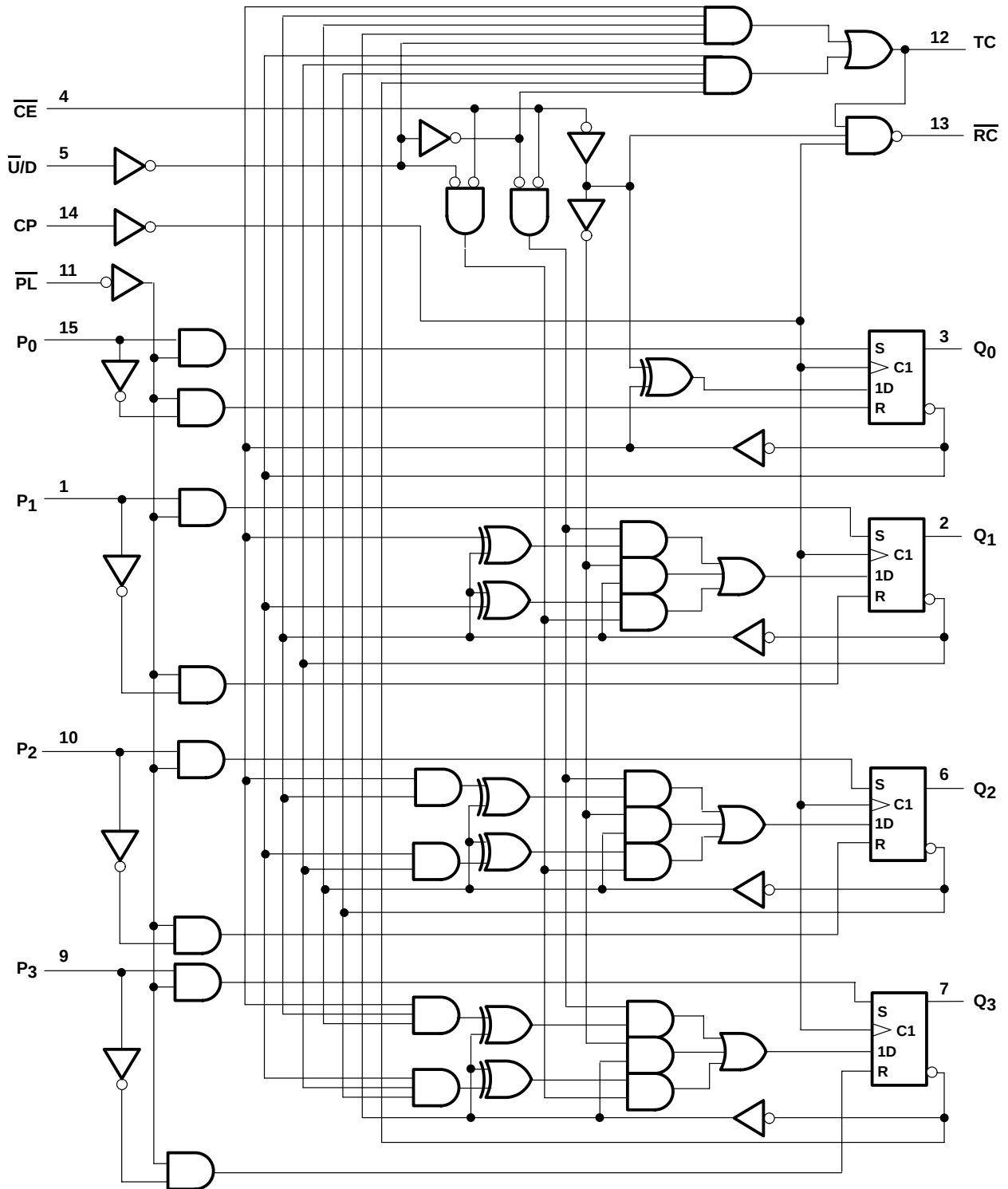
MODE SELECT

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L	↑	Count up
H	L	H	↑	Count down
L	X	X	X	Preset (asynchronous)
H	H	X	X	No change (hold)

H = High logic level, L = Low logic level, X = Don't care,

↑ = Low-to-high clock transition

logic diagram (positive logic)



CY74FCT191T
4-BIT UP/DOWN BINARY COUNTER

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absolute maximum rating over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	90°C/W
SO package	57°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			–32	mA
I_{OL} Low-level output current			64	mA
T_A Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.75\text{ V}$,	$I_{IN} = -18\text{ mA}$		-0.7	-1.2	V
V_{OH}	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -32\text{ mA}$	2			V
	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -15\text{ mA}$	2.4	3.3		
V_{OL}	$V_{CC} = 4.75\text{ V}$,	$I_{OL} = 64\text{ mA}$		0.3	0.55	V
V_H	All inputs			0.2		V
I_I	$V_{CC} = 5.25\text{ V}$,	$V_{IN} = V_{CC}$			5	μA
I_{IH}	$V_{CC} = 5.25\text{ V}$,	$V_{IN} = 2.7\text{ V}$			± 1	μA
I_{IL}	$V_{CC} = 5.25\text{ V}$,	$V_{IN} = 0.5\text{ V}$			± 1	μA
$I_{OS}^\ddagger$	$V_{CC} = 5.25\text{ V}$,	$V_{OUT} = 0\text{ V}$	-60	-120	-225	mA
I_{off}	$V_{CC} = 0\text{ V}$,	$V_{OUT} = 4.5\text{ V}$			± 1	μA
I_{CC}	$V_{CC} = 5.25\text{ V}$, $V_{IN} \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.1	0.2	mA
ΔI_{CC}	$V_{CC} = 5.25\text{ V}$, $V_{IN} = 3.4\text{ V}^\S$, $f_1 = 0$, Outputs open			0.5	2	mA
$I_{CCD}^\P$	$V_{CC} = 5.25\text{ V}$, One bit switching at 50% duty cycle, Preset mode, Outputs open, $MR = V_{CC} = \overline{SR}$, $\overline{PL} = \overline{CE} = \overline{U/D} = CP = \text{GND}$, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.06	0.12	mA/MHz
$I_C^\#$	$V_{CC} = 5.25\text{ V}$, Preset mode, Outputs open, $\overline{PL} = \overline{CE} = \overline{U/D} = CP = \text{GND}$	One bit switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle	$V_{IN} = V_{CC}$ or GND	0.4	0.8	mA
			$V_{IN} = 3.4\text{ V}$ or GND	0.7	1.8	mA
		Four bits switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle	$V_{IN} = V_{CC}$ or GND	1.3	2.6	mA
			$V_{IN} = 3.4\text{ V}$ or GND	2.3	6.6	mA
C_i				5	10	pF
C_0				9	12	pF

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4\text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4\text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

CY74FCT191T

4-BIT UP/DOWN BINARY COUNTER

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

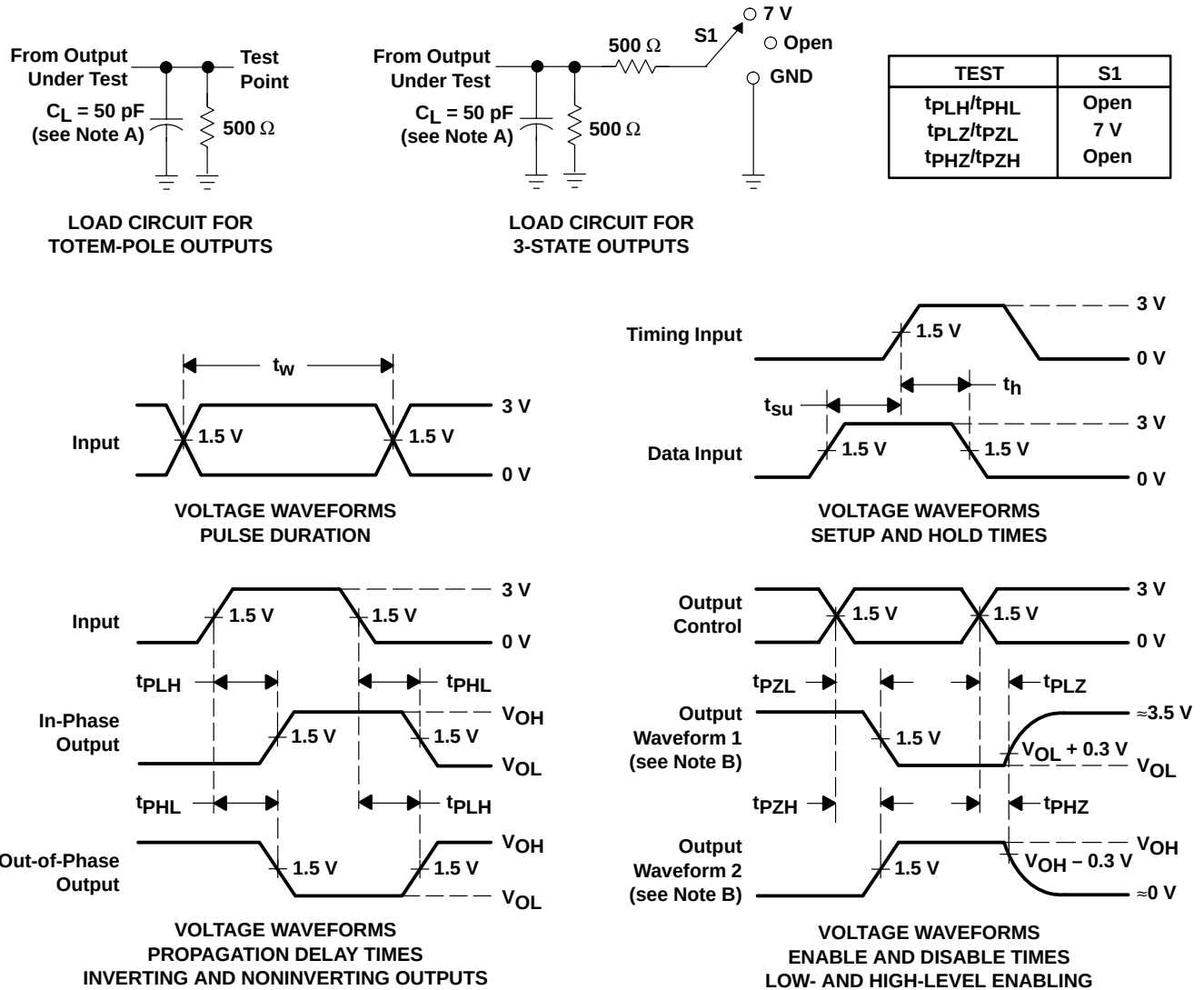
PARAMETER			CY74FCT191AT		CY74FCT191CT		UNIT
			MIN	MAX	MIN	MAX	
t_w Pulse duration	CP	High or Low	4		4		ns
	$\overline{PL}$ low		5.5		5		
t_{su} Setup time	Data before $\overline{PL}\downarrow$	High or Low	4		3.5		ns
	$\overline{CE}$ before $CP\uparrow$	Low	9		7.2		
	$\overline{U/D}$ before $CP\uparrow$	High or Low	10		8		
t_h Hold time	Data after $\overline{PL}\downarrow$	High or Low	1.5		1		ns
	$\overline{CE}$ after $CP\uparrow$	Low	0		0		
	$\overline{U/D}$ after $CP\uparrow$	High or Low	0		0		
t_{rec} Recovery time	$\overline{PL}$ after $CP\uparrow$		5		4.5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT191AT		CY74FCT191CT		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	CP	Q_n	1.5	7.8	1.5	6.2	ns
t_{PHL}			1.5	7.8	1.5	6.2	
t_{PLH}	CP	TC	1.5	11.8	1.5	9.4	ns
t_{PHL}			1.5	11.8	1.5	9.4	
t_{PLH}	CP	$\overline{RC}$	1.5	8.5	1.5	6.8	ns
t_{PHL}			1.5	8.5	1.5	6.8	
t_{PLH}	CE	$\overline{RC}$	1.5	7.2	1.5	6	ns
t_{PHL}			1.5	7.2	1.5	6	
t_{PLH}	$\overline{U/D}$	$\overline{RC}$	1.5	13	1.5	11	ns
t_{PHL}			1.5	13	1.5	11	
t_{PLH}	$\overline{U/D}$	TC	1.5	7.2	1.5	6.1	ns
t_{PHL}			1.5	7.2	1.5	6.1	
t_{PLH}	P_n	Q_n	1.5	9.1	1.5	7.7	ns
t_{PHL}			1.5	9.1	1.5	7.7	
t_{PLH}	$\overline{PL}$	Q_n	2	8.5	2	7.2	ns
t_{PHL}			2	8.5	2	7.2	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CY74FCT191ATSOC	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191A	Samples
CY74FCT191ATSOCE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191A	Samples
CY74FCT191ATSOCG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191A	Samples
CY74FCT191CTQCT	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT191-3	Samples
CY74FCT191CTQCTE4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT191-3	Samples
CY74FCT191CTQCTG4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT191-3	Samples
CY74FCT191CTSOC	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191C	Samples
CY74FCT191CTSOCE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191C	Samples
CY74FCT191CTSOCG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191C	Samples
CY74FCT191CTSOCT	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85	FCT191C	
CY74FCT191CTSOCTG4	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

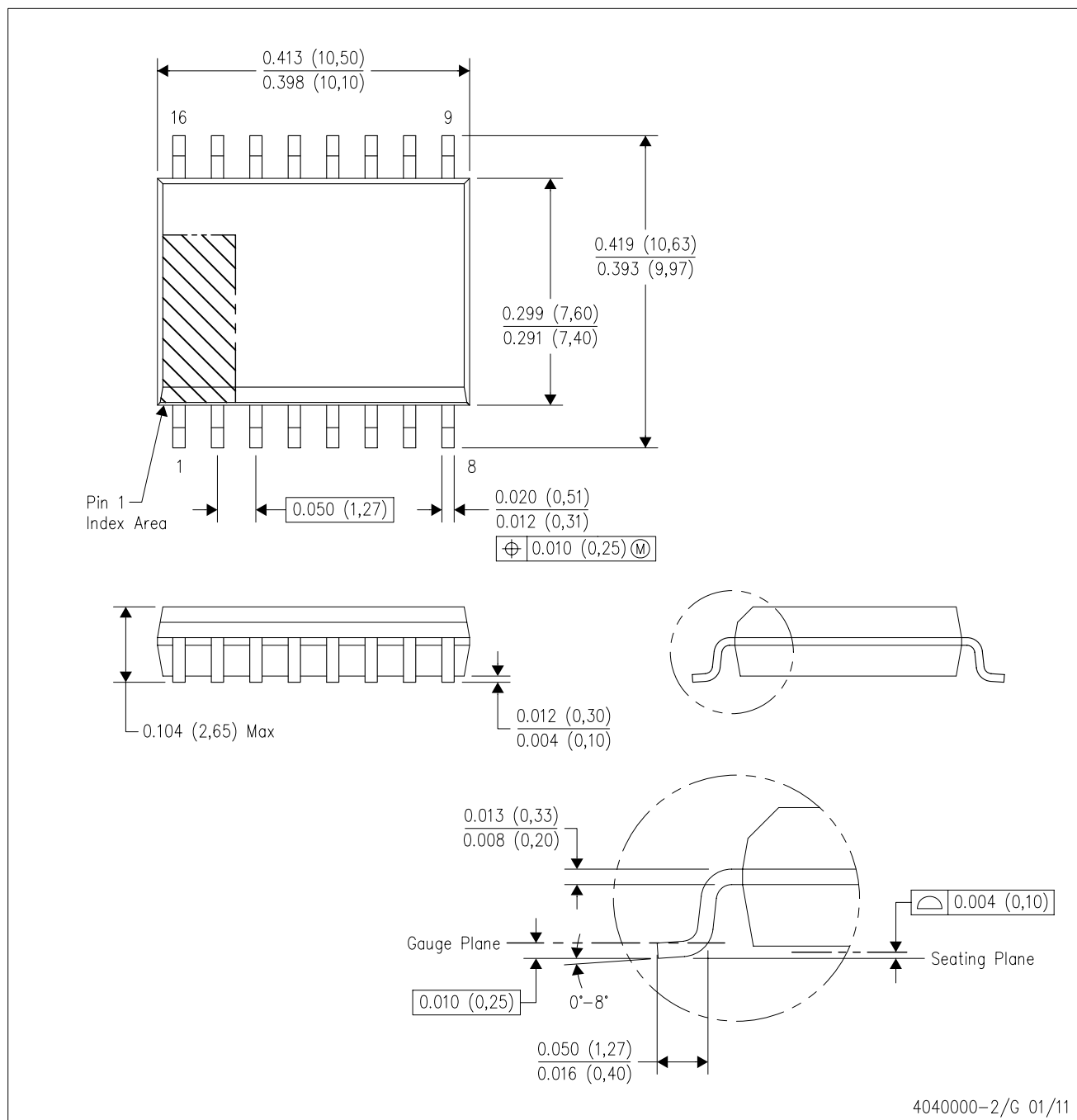
⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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DW (R-PDSO-G16)

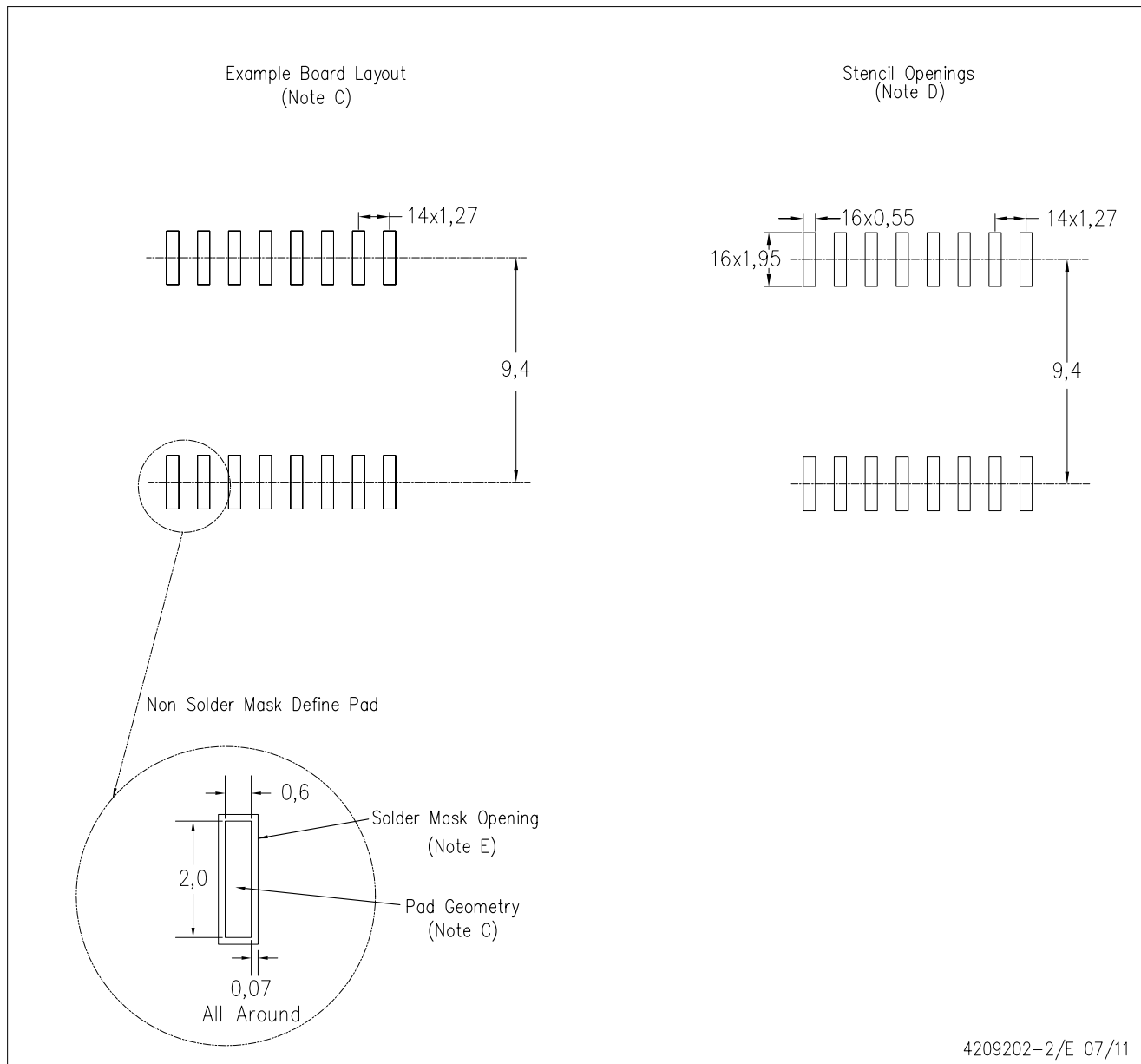
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

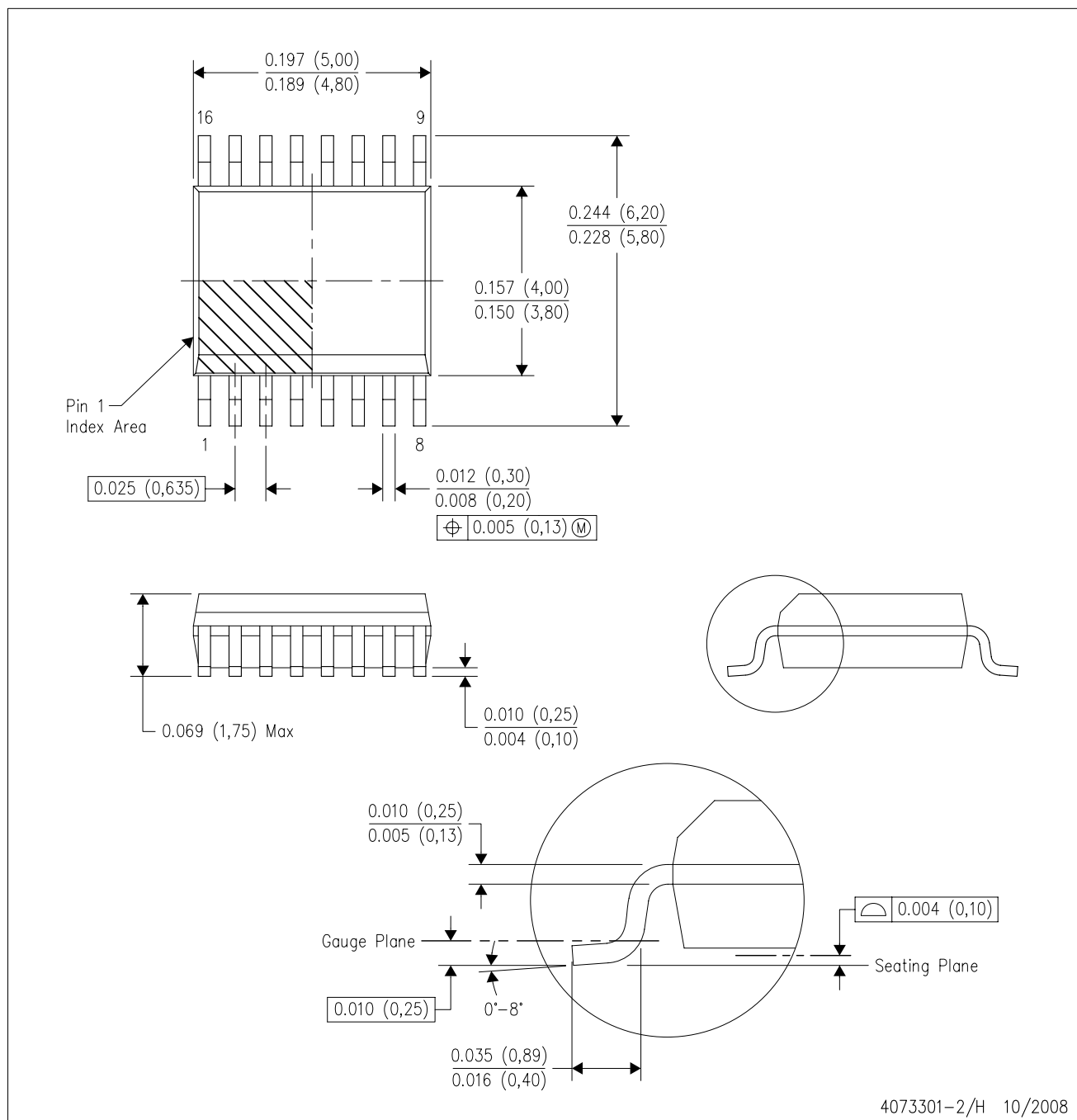
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G16)

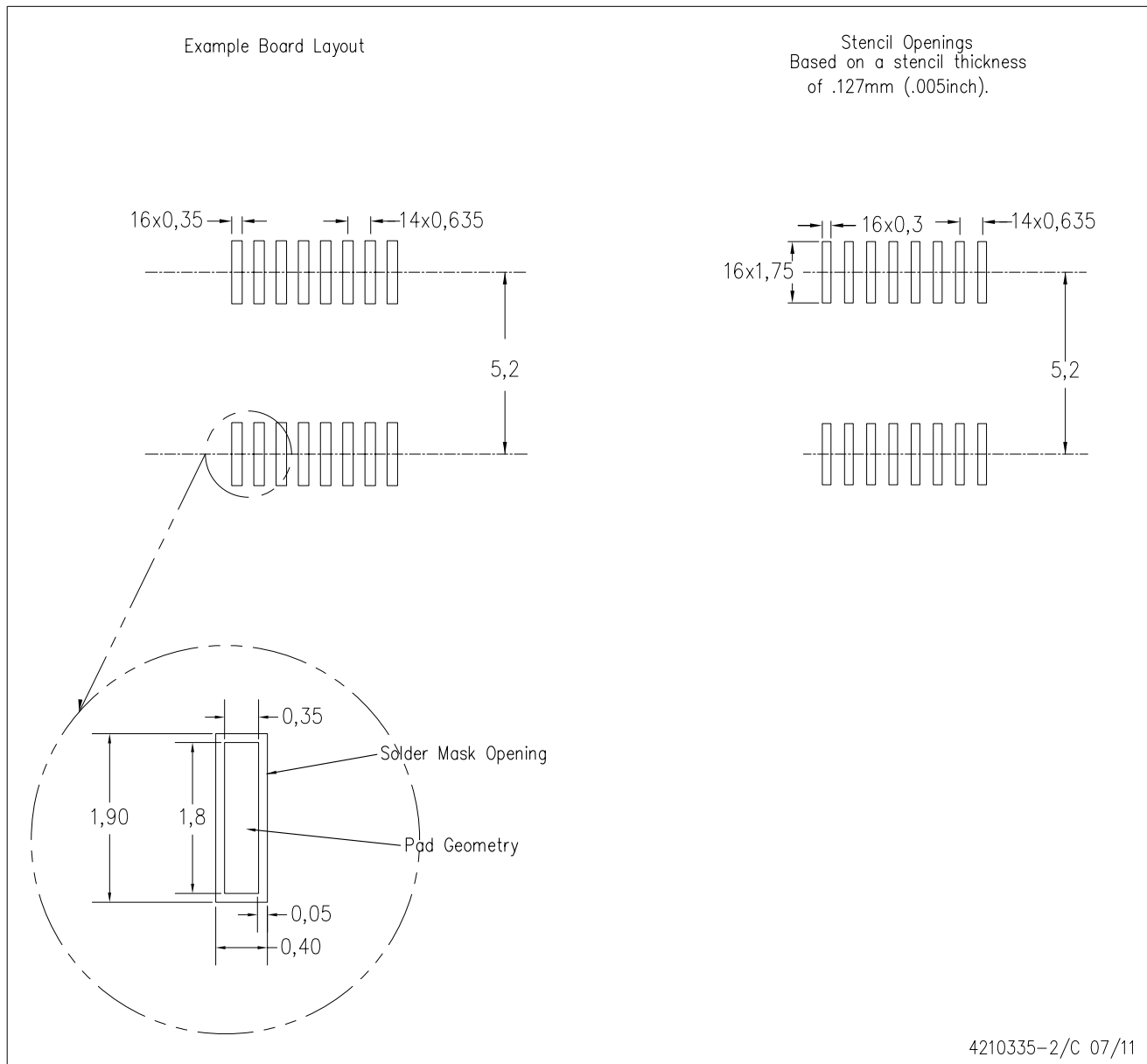
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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