

# AGB1N0CS-GEVK

## Demo 3 Evaluation Board User's Manual



ON Semiconductor®

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### Demo 3 Evaluation Board Overview

The Demo 3 Baseboard is used to connect to headboards and interface with a host PC in order to demonstrate the features of ON Semiconductor's image sensor products.

### Features

- High-Bandwidth USB 3.0 Interface
- Altera Arria II GX FPGA
- HDMI® Transmitter
- 1GB Memory Buffer
- Up to 4-Lane MIPI and HiSPi Interfaces
- CCP and Parallel Interfaces
- I<sup>2</sup>C Control Unit

### Block Diagram

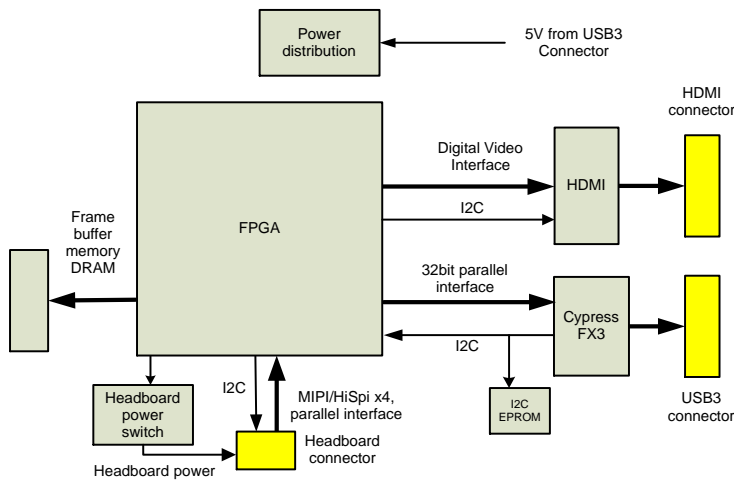


Figure 2. Block Diagram of AGB1N0CS-GEVK

## EVAL BOARD USER'S MANUAL



Top View



Bottom View

Figure 1. AGB1N0CS Evaluation Board

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Top View

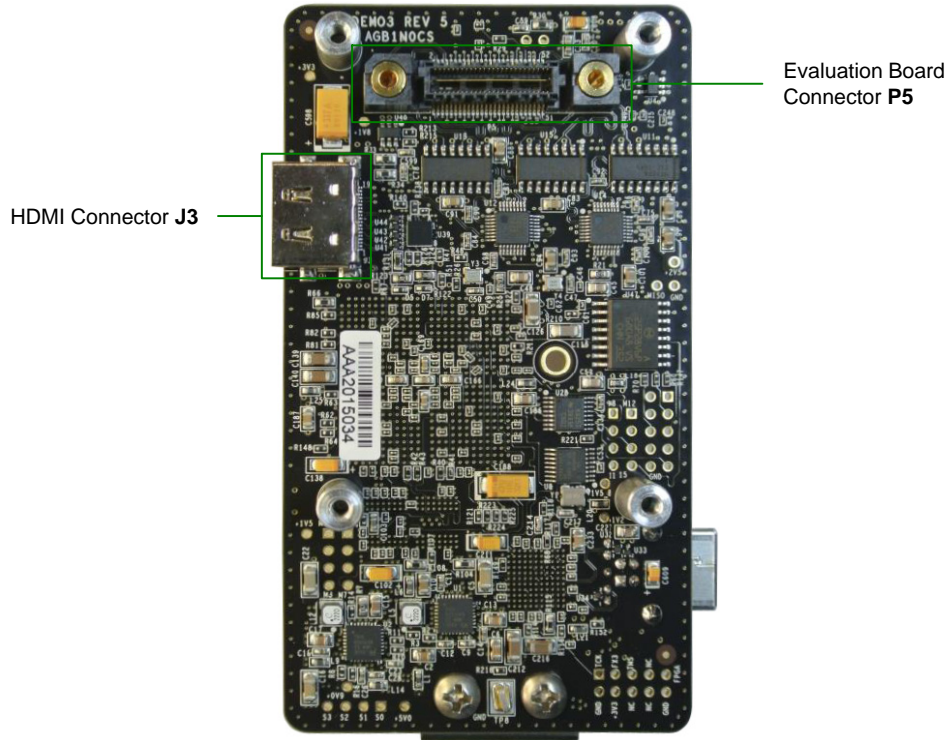


Figure 3. Top View of Demo 3 with Connectors

Bottom View

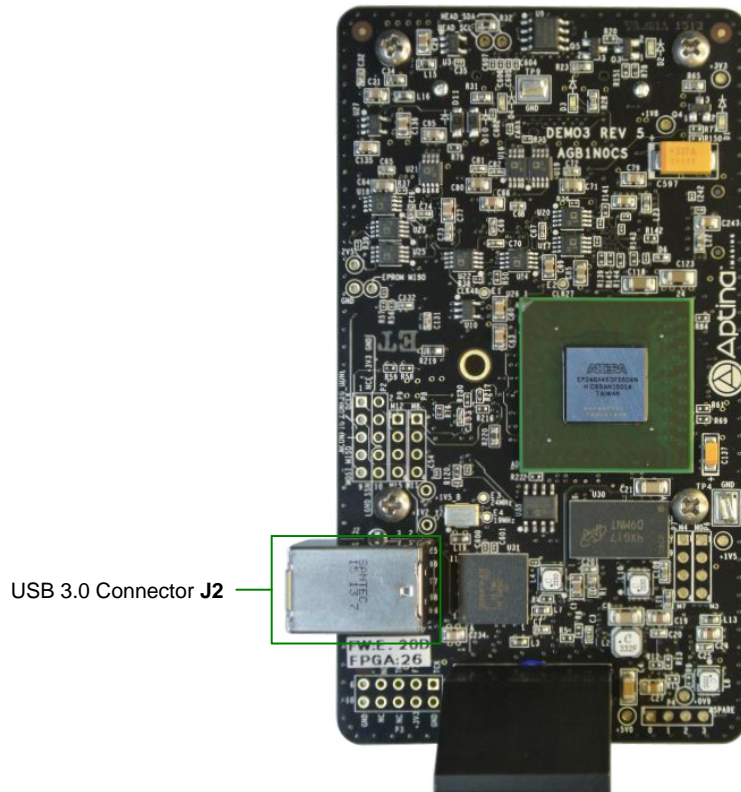


Figure 4. Bottom View of Demo 3 with Test Pins and Connectors

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## Demo 3 Baseboard Function Overview

The Demo 3's FPGA, Altera's EP2AGX45DF25C4N, provides an interface between ON Semiconductor imaging sensors and the Cypress FX3 USB 3.0 controller. An

external SPI EPROM contains the programming file for the FPGA. The EPROM is configurable using the FX3 SPI master interface. The FPGA has a memory controller block that controls data from the on-board DDR3 SDRAM.

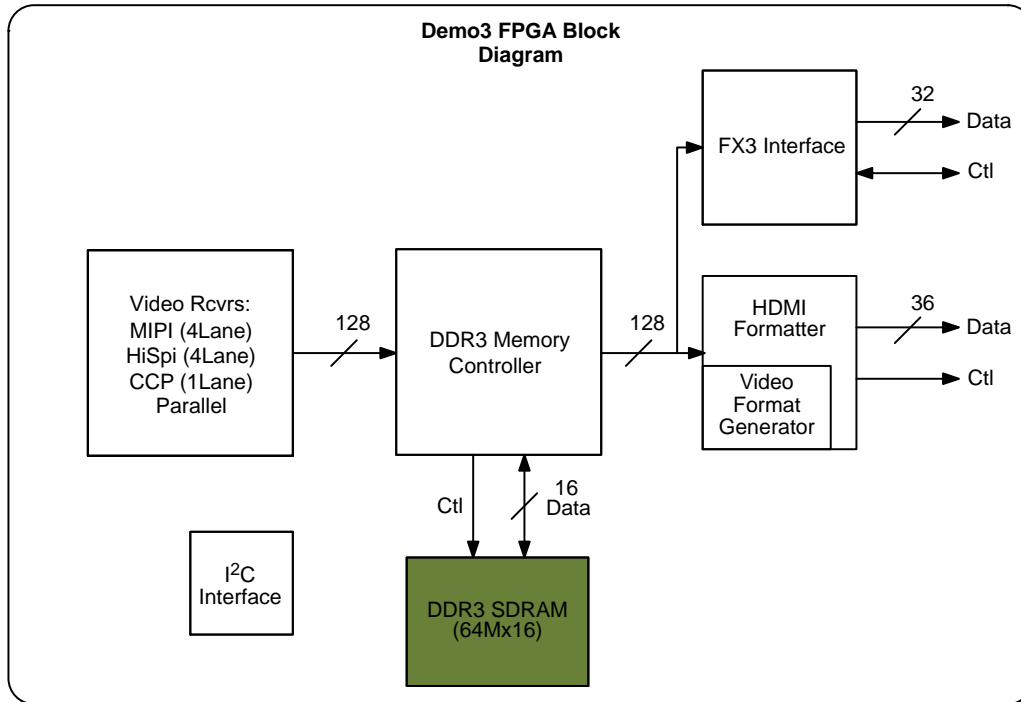


Figure 5. FPGA Block Diagram

### FPGA Frame Buffer

The 1Gb frame buffer using a 64Mbx16 matches data rates between the sensor and FX3 interfaces. It is sized to buffer 3 frames of a 20-Megapixel sensor. There is a triple-buffer to help minimize frame loss. The frame buffer has two principal operating modes that support either self-timed operation or direct interface to the FX3 at HDMI video output of 720p 60 or 1080p 60 frame rates. The frame buffer controller runs at 150 MHz FPGA core clock with peak available bandwidth at 750-Megapixels/second, peak input bandwidth of 400-Megapixels/second, and peak output bandwidth of 200-Megapixels/second. The frame buffer can be configured to operate as a frame capture device, with the entire buffer filled prior to sending data to the FX3 interface.

### Receivers and Data Rates

The FPGA receives data through MIPI, HiSPi, CCP, and parallel interfaces. Each of these receiver blocks has an output FIFO that moves data from the receiver clock to the 150 MHz FPGA core clock.

#### MIPI Receiver:

The MIPI receiver handles 4 lanes of data at a maximum data rate of 768 Mbps/lane. The signal pairs use both single-ended and differential signaling with accordance to the MIPI Alliance Specification for D-PHY v.1.00.00.

#### HiSPi Receiver:

The HiSPi receiver supports high-speed transmission of image sensor data, operating at 1 Gbps per data lane. It is a unidirectional differential serial interface with four data lanes and one DDR clock lane. It supports Streaming-S, Streaming-SP, and Packetized SP protocols that conform to the HiSPi protocol specification v.1.50.00.

#### CCP Receiver:

The CCP receiver is a single-lane data interface that supports 8-, 10-, or 12-bit raw data. It operates with a maximum serial data rate of at least 640 Mbps. The receiver conforms to the SMIA CCP2 1.0 specification.

#### Parallel Receiver:

The parallel receiver allows asynchronous switching between driven and high-Z under pin or register control. The receiver supports 10 or 12 bits of data, running at a pixel rate of at least 125 MHz.

#### HDMI Transmitter

The HDMI transmitter utilizes the ADV7526 chip by Analog Devices to transmit HDMI 34-bit data to the output port. The HDMI interface supports the HDMI 1.4 standard with 12-bit deep color. It supports RGB and YCbCr digital video input. The I<sup>2</sup>C device address is 0x72 and accesses registers inside the HDMI transmitter block.

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## FX3 USB 3.0 Interface

The Cypress FX3 has a 32-bit data interface that is transceived to the differential I/O pins on the transmitters/receivers of the FPGA. The maximum data rate of the interface is 5 Gb/s.

## I<sup>2</sup>C Control Bus

The I<sup>2</sup>C control bus supports 32-bit wide GPIF II data bus and supports 14 configurable control pins. The control bus supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. Operational mode control is done through software configuration using the I<sup>2</sup>C interface from the controller. The I<sup>2</sup>C HDMI chip address is 0x72, and clock generator address is 0xD2. The system EEPROM is 0xA0 and t is configurable up to 0xAx using software.

## Interfacing to Demo 3 Headboard

The headboard connector has a serial sensor data input interface, I<sup>2</sup>C control interface, power input, and parallel image data interface.

## HiSPi Interface

The High Speed Serial Pixel (HiSPi) interface uses four differential data lanes and one differential clock as output and it is unidirectional. In HiSPi mode, 12- or 14-bit compressed, or 16-bit linearized data may be output. Only linear mode is supported on this interface. The HiSPi interface supports three protocols: Streaming–S, Streaming–SP, and Packetized SP.

## MIPI Interface

The MIPI interface implements a serial differential sub-LVDS transmitter that supports multiple formats, error checking, and custom short packets. The interface is designed to MIPI D–PHY v1.0. When the sensor is in software standby system state, the MIPI signals enter ultra low-power state according to their nominal 0 V levels.

## Serial LVDS Interface

The serial LVDS (low-voltage differential signal) interface uses four differential data lanes and one differential clock as output and it is unidirectional. In Serial LVDS mode, 8- or 10-bit compressed, or 12-bit linearized data may be output. Only linear mode is supported on this interface.

## Parallel Interface

The parallel mode interface outputs 10- or 12-bit raw data for linear mode and 10- or 12-bit compressed data in High Dynamic Range, depending on the board. In this mode, FRAME\_VALID and LINE\_VALID signals are output on dedicated pins, along with a synchronized pixel clock two-wire serial interface.

## Two-Wire Serial Interface

Some boards support a two-wire serial interface. The interface supports two modes of operation: 100 kHz for Standard mode, and 400 kHz for High-speed mode.

**Table 1. 52-PIN CONNECTOR TO HEADBOARD FUNCTION DESCRIPTION (P5)**

Pin	Name	Description	DIR	Comment
1	MH_DATA1_P	MIPI/HiSPi Data1+	Out	MIPI/HiSPi Data1+ Signal
2	MH_DATA2_P	MIPI/HiSPi Data2+	Out	MIPI/HiSPi Data2+ Signal
3	MH_DATA1_N	MIPI/HiSPi Data1–	Out	MIPI/HiSPi Data1– Signal
4	MH_DATA2_N	MIPI/HiSPi Data2–	Out	MIPI/HiSPi Data2– Signal
5	S_RESERVED1	General Reserved Signal 1	Out	Signal @ +3.3 V Level
6	MH_DATA3_P	MIPI/HiSPi Data3+	Out	MIPI/HiSPi Data3+ Signal
7	HEAD_MOSI	Master OOT, Slave IN Signal	I/O	Signal @ +3.3 V Level
8	MH_DATA3_N	MIPI/HiSPi Data3–	Out	MIPI/HiSPi Data3– Signal
9	S_DATA1	Parallel Data1	I/O	Parallel Interface Data Bit
10	S_DATA0	Parallel Data0	I/O	Parallel Interface Data Bit
11	S_DATA3	Parallel Data3	I/O	Parallel Interface Data Bit
12	S_DATA2	Parallel Data2	I/O	Parallel Interface Data Bit
13	S_DATA5	Parallel Data5	I/O	Parallel Interface Data Bit
14	S_DATA4	Parallel Data4	I/O	Parallel Interface Data Bit
15	VDDIO_SENSE	Reference Input for I/O Voltage	PWR	Lets Demo3 Set Voltage Level
16	S_DATA6	Parallel Data6	I/O	Parallel Interface Data Bit
17	S_DATA7	Parallel Data7	I/O	Parallel Interface Data Bit
18	S_DATA8	Parallel Data8	I/O	Parallel Interface Data Bit
19	S_DATA9	Parallel Data9	I/O	Parallel Interface Data Bit
20	S_DATA10	Parallel Data10	I/O	Parallel Interface Data Bit
21	S_DATA11	Parallel Data11	I/O	Parallel Interface Data Bit

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**Table 1. 52-PIN CONNECTOR TO HEADBOARD FUNCTION DESCRIPTION (P5)** (continued)

Pin	Name	Description	DIR	Comment
22	S_DATA12	Parallel Data12	I/O	Parallel Interface Data Bit
23	S_DATA13	Parallel Data13	I/O	Parallel Interface Data Bit
24	S_DATA14	Parallel Data14	I/O	Parallel Interface Data Bit
25	S_DATA15	Parallel Data15	I/O	Parallel Interface Data Bit
26	S_SP5	General Control Signal 5	In	Signal @ +3.3 V Level
27	S_SP0	General Control Signal 0	In	Signal @ +3.3 V Level
28	S_SP1	General Control Signal 1	In	Signal @ +3.3 V Level
29	S_LINE_VALID	Serial Line Valid Signal	Out	Checks if Data has Valid Line
30	S_SP3	General Control Signal 3	In	Signal @ +3.3 V Level
31	HEAD_RESET_L	Reset Signal to Headboard	Out	Resets the Headboard Sensor
32	S_SP4	General Control Signal 4	In	Signal @ +3.3 V Level
33	S_SP2	General Control Signal 2	In	Signal @ +3.3 V Level
34	HEAD_SSN	Headboard Slave Signal	In	SPI Slave Signal to Headboard
35	S_FRAME_VALID	Parallel Frame Valid Signal	Out	Checks if Data has Valid Frame
36	S_PIXCLK	Pixel Clock	Out	Parallel Data Pixel Clock
37	HEAD_SDA	I <sup>2</sup> C Data to Sensor	I/O	Signal @ +3.3 V Level
38	+2V8_VAA_HEAD	+2.8 V to V <sub>AA</sub> on Headboard	PWR	For Powering Up the Headboard
39	+5V0_HEAD	+5 V to Headboard	PWR	For Powering Up the Headboard
40	S_RESERVED0	General Reserved Signal 0	In	Signal @ +3.3 V Level
41	HEAD_MISO	Master IN, Slave OUT Signal	I/O	Signal @ +3.3 V Level
42	+1V8_HEAD	+1.8 V to Headboard	PWR	For Powering Up the Headboard


*FPGA, HDMI Chip, USB 3.0 Chip:*

FPGA: Altera Arria II GX (EP2AGX45DF25C4N)

HDMI Chip: Analog Device Low-Power HDMI Transmitter (ADV7526)

USB 3.0 Chip: Cypress FX3 (CYUSB3014-BZX)

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