

Automotive IPD Series

2ch Low Side Switch IC BM2LB150FJ-C

Features

- Built-in overcurrent limiting circuit(OCP)
- Built-in thermal shutdown circuit (TSD)
- Direct control enabled from CMOS logic IC, etc.
- Low On resistance $R_{DS(ON)}$ up to 150 m Ω (when $V_{IN}=5V$, $I_D=0.5A$, $T_j=25$ °C)
- Monolithic power management IC with the control block (CMOS) and power MOS FET mounted on a single chip
- Surface mount package SOP-J8
 AEC-Q100 Qualified (Note 1)
- (Note 1) Grade1

General Description

The BM2LB150FJ-C is an automotive 2ch low side switch IC, which has built-in overcurrent limiting circuit, thermal shutdown circuit, and overvoltage (active clamp) protection circuit.

Applications

2ch low side switch for driving resistive, inductive load, Capacitive load

Product Summary

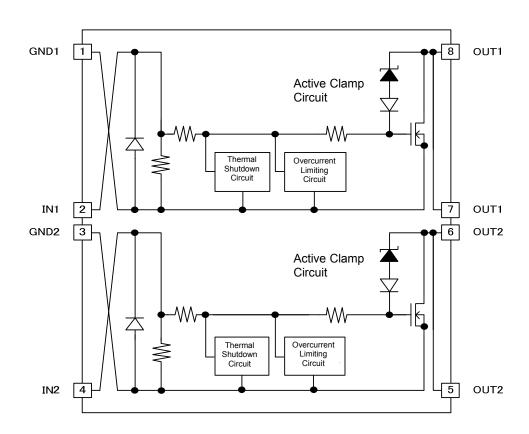
On-state resistance (T _i =25°C, Typ)	150mΩ
Overcurrent limit (T _i =25°C, Typ)	10A
Output clamp voltage (Min)	42V
Active clamp energy (T _i =25°C)	165mJ

Package SOP-J8

W(Typ) x D(Typ) x H(Max) 4.90mm x 6.00mm x 1.65mm



Block Diagram

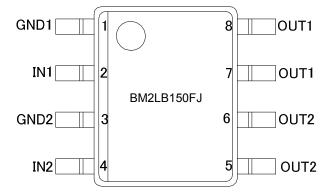


Pin Descriptions

Pin No.	Symbol	Function
1	GND1	GND pin1
2	IN1	Input pin1 (Note1)
3	GND2	GND pin2
4	IN2	Input pin2 (Note1)
5	OUT2	Output pin2
6	OUT2	Output pin2
7	OUT1	Output pin1
8	OUT1	Output pin1

(Note1) Input pin is used to internally connect a pull-down resistor.

Pin Configurations



Absolute Maximum Ratings (T_j =25°C)

Parameter	Symbol	Rating	Unit
Drain-Source voltage in output block	V _{DS}	-0.3 to +42 ^(Note1)	V
Input voltage	V _{IN}	-0.3 to +7	V
Output current (DC)	I _D	6.5(internally limited) (Note2)	Α
Active clamp energy (Single pulse) $T_{j(\text{start})} = 25^{\circ}\text{C}^{\text{(Note3)}}$	E _{AS(25°C)}	165	mJ
Active clamp energy (Single pulse) $T_{j(start)} = 150^{\circ}C^{(Note3)(Note4)}$	E _{AS(150°C)}	60	IIIJ
Operating temperature range	Tj	-40 to +150	°C
Storage temperature range	T _{stg}	-55 to +150	°C
Maximum junction temperature	T _{jmax}	150	°C

(Note1) Please refer to P.12 "Operation Notes", when is used at less than -0.3V.

(Note3) Internally limited by the overcurrent limiting circuit.

(Note3) Min Active clamp energy, using single non-repetitive pulse of 1.0A. $E_{AS} = \frac{1}{2} L I_{AR}^2 \cdot (1 - \frac{V_B}{V_B - V_{CL}})$

$$E_{AS} = \frac{1}{2} LI_{AR}^2 \cdot (1 - \frac{V_B}{V_B - V_{CI}})$$

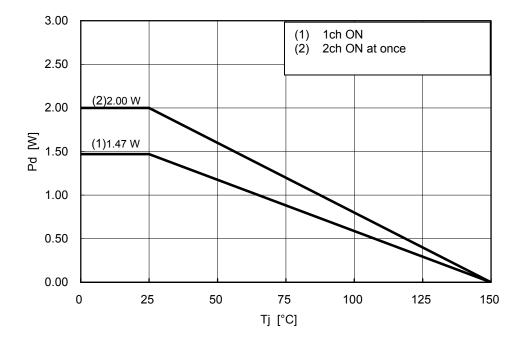
(Note4) Not 100% tested.

Thermal resistance

Parameter	Symbol	Rating	Unit	
Power dissipation (Note5)	(1ch ON)	P _{D(1)}	1.47	W
	(2ch ON at once)	$P_{D(2)}$	2.00	W

 $(Note5) \ When \ mounted \ on \ a \ PCB \ (two-layer \ glass \ epoxy \ board \ measuring \ 76.2 \times 114.3 \ [mm], \ 1.6 \ [mm] \ thick, \ with \ a \ copper \ foil \ area \ of \ 74.2 \times 74.2 \ [mm])$

Heat Dissipation Characteristic



Electrical Characteristics (Unless otherwise specified, −40°C≤T_i≤+150°C and V_{IN}=3.0V to 5.5V)

Parameter	Symbol	Limit		Unit	Conditions		
Farameter	Symbol	Min	Тур	Max	Uniit	Conditions	
Output clamp voltage	V _{CL}	42	48	54	V	V _{IN} =0V,I _D =1mA	
On-state resistance 1 (at 25°C)	R _{ON1}	-	150	190	mΩ	V _{IN} =5V,I _D =0.5A,Tj=25°C	
On-state resistance 1 (at 150°C)	R _{ON2}	-	260	320	mΩ	V _{IN} =5V,I _D =0.5A,Tj=150°C	
On-state resistance 2 (at 25°C)	R _{ON3}	-	200	250	mΩ	V _{IN} =3V,I _D =0.5A, Tj=25°C	
On-state resistance 2 (at 150°C)	R _{ON4}	-	340	420	mΩ	V _{IN} =3V,I _D =0.5A,Tj=150°C	
Leakage current (at 25°C)	V _{IL1}	-	0	4	μΑ	V _{IN} =0V,V _{DS} =18V,Tj=25°C	
Leakage current (at 150°C)	V_{IL_2}	-	2	25	μΑ	V _{IN} =0V,V _{DS} =18V,Tj=150°C	
Turn-ON time	ton	-	-	80	μs	V_{IN} =0V/5V, R_L =15 Ω , V_B =12V, T_j =25°C	
Turn-OFF time	t _{OFF}	-	-	80	μs	V_{IN} =0V/5V, R_L =15 Ω , V_B =12V, T_j =25°C	
Slew rate on	SR _{ON}	-	0.5	1.0	V/µs	V_{IN} =0V/5V, R_L =15 Ω , V_B =12V, T_j =25°C	
Slew rate off	SR _{OFF}	-	1.0	2.0	V/µs	V_{IN} =0V/5V, R_L =15 Ω , V_B =12V, T_j =25 $^{\circ}$ C	
Input threshold voltage	V_{TH}	1.1	-	2.7	V	I _D =1mA	
High-level input current	I _{INH1}	-	150	300	μΑ	V _{IN} =5V	
High-level input current (in abnormal operation)	I _{INH2}	-	250	450	μΑ	V _{IN} =5V	
Low-level input current	I _{INL}	-10	0	10	μA	V _{IN} =0V	
Overcurrent detection current	I _{OCP}	6.5	10.0	13.5	Α	V _{IN} =5V, T _j =25°C	
TSD detection temperature ^(Note1)	T _{jd}	150	175	-	°C	V _{IN} =5V	
TSD release temperature ^(Note1)	T _{jr}	130	-	-	°C	V _{IN} =5V	
TSD hysteresis ^(Note1)	ΔT_{jd}	-	15	-	°C	V _{IN} =5V	

(Note1) Not 100% tested.

Terms

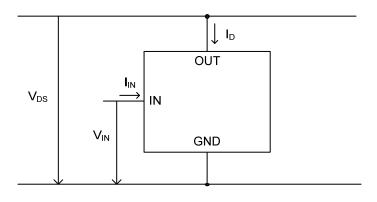


Figure 1. Terms

Measuring circuit

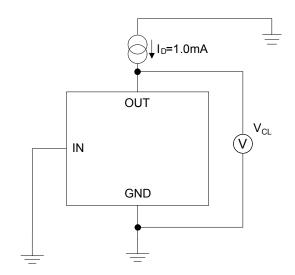


Figure 2. Output clamp voltage measuring circuit

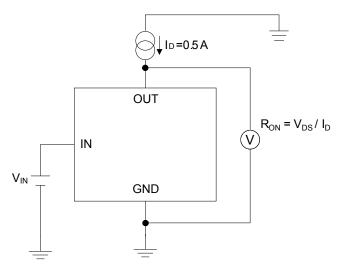


Figure 3. On-state resistance measuring circuit

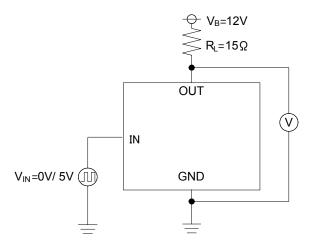


Figure 4. $t_{\text{ON}} \bullet t_{\text{OFF}}$ measuring circuit

I/O Pin Truth Table

Operating Status	Input Signal	Output Level	Output Status	
Normal	Н	L	ON	
Normal	L	Н	OFF	
Overcurrent	Н	Clamp	Current Limiting	
	L	Н	OFF	
Overbook	Н	Н	OFF	
Overheat	L	Н	OFF	

Typical Performance Curves (Unless otherwise specified, Tj=25°C, V_{IN}=5.0V)

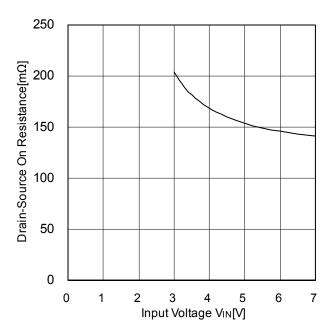


Figure 5. On-state Resistance Characteristics [Input Voltage Characteristics]

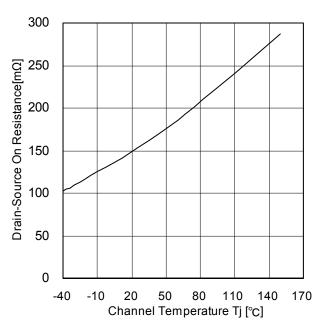


Figure 6. On-state Resistance Characteristics [Temperature Characteristics]

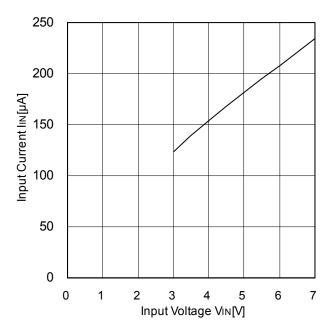


Figure 7. Input Current Characteristics [Input Voltage Characteristics]

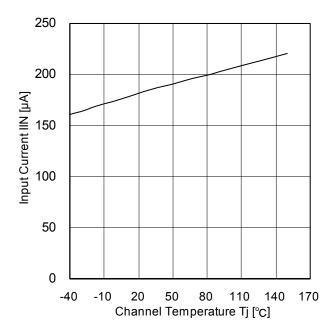


Figure 8. Input Current Characteristics [Temperature Characteristics]

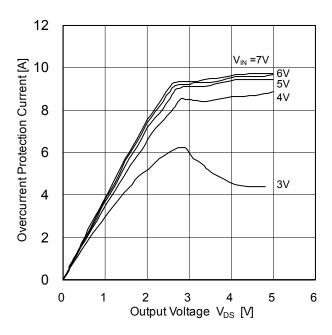


Figure 9. Overcurrent Detection Current Characteristics [Input Voltage Characteristics]

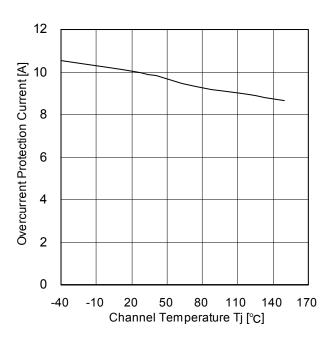


Figure 10. Overcurrent Detection Current Characteristics [Temperature Characteristics]

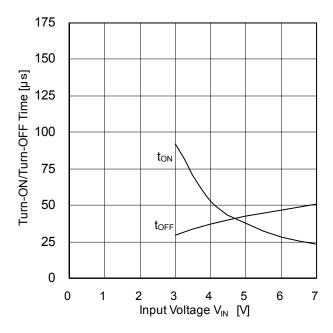


Figure 11. Turn-ON/Turn-OFF Time Characteristics [Input Voltage Characteristics]

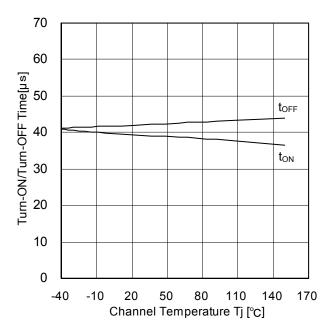


Figure 12. Turn-ON/Turn-OFF Time Characteristics [Temperature Characteristics]

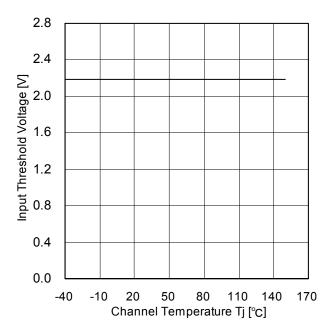


Figure 13. Input Threshold Voltage Characteristics [Temperature Characteristics]

Timing Chart

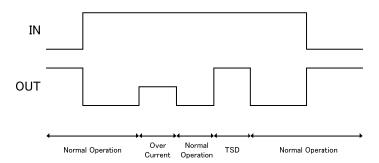


Figure 14. Behavior Sequence

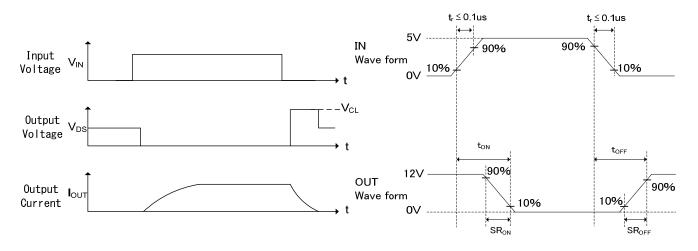
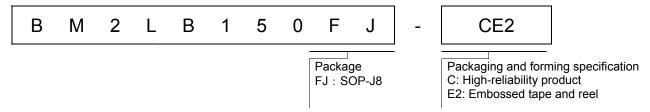


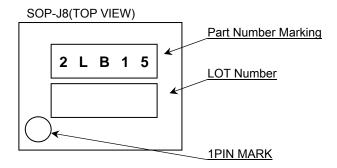
Figure 15. Inductive Load Operation

Figure 16. Switching Time

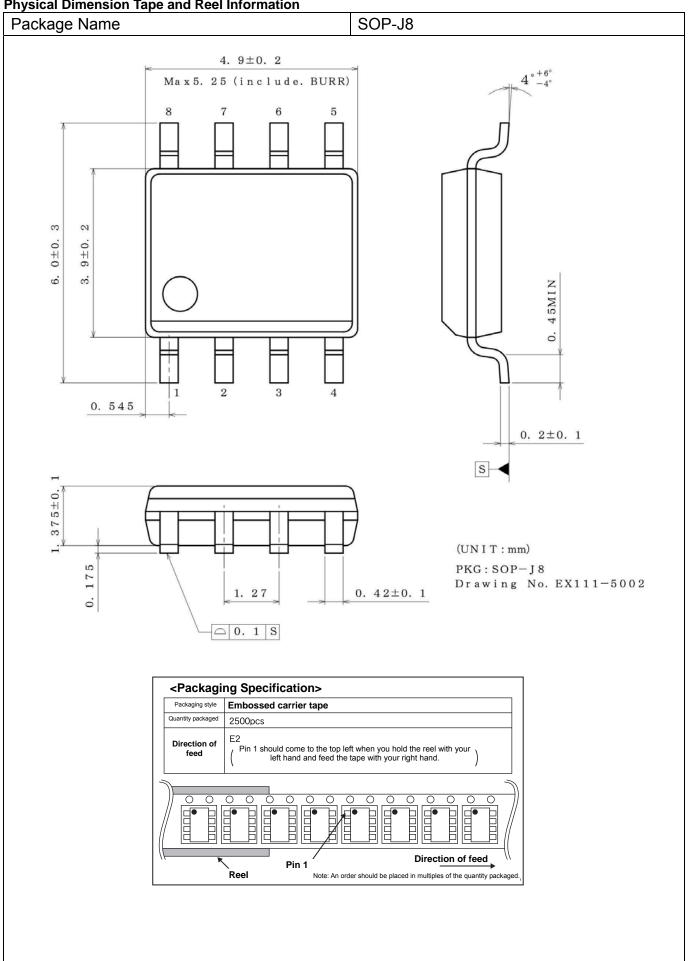
Ordering Information



Marking Diagram



Physical Dimension Tape and Reel Information



Operational Notes

1. Grounding Interconnection Pattern

When a small-signal ground and a high-current ground are used, it is recommended to isolate the high-current grounding interconnection pattern and the small-signal grounding interconnection pattern and establish a single ground at the reference point of a set so that voltage changes due to the resistance and high current of patterned interconnects will not cause any changes in the small-signal ground voltage. Pay careful attention to prevent changes in the interconnection pattern of ground for external components.

The ground lines must be as short and thick as possible to reduce line impedance.

2. Thermal Design

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.

3. Absolute Maximum Ratings

Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

4. Inspections on Set Board

If a capacitor is connected to a low-impedance pin in order to conduct inspections of the IC on a set board, stress may apply to the IC. To avoid that, be sure to discharge the capacitor in each process. In addition, to connect or disconnect the IC to or from a jig in the testing process, be sure to turn OFF the power supply prior to connecting the IC, and disconnect it from the jig only after turning OFF the power supply. Furthermore, in order to protect the IC from static electricity, establish a ground for the IC assembly process and pay utmost attention to transport and store the IC.

5. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

6. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

7. Thermal Shutdown Circuit

This IC has a built-in thermal shutdown circuit as an overheat-protection measure. The circuit is designed to turn OFF output when the temperature of the IC chip exceeds 175°C (Typ) and return the IC to the normal operation when the temperature falls below 150°C (Typ).

The thermal shutdown circuit is a circuit absolutely intended to protect the IC from thermal runaway, not intended to protect or guarantee the IC. Consequently, do not operate the IC based on the subsequent continuous use or operation of the circuit.

8. Overcurrent Limiting Circuit

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

9. Overvoltage (Active Clamp) Protection Function

This IC has a built-in overvoltage protection function in order for the IC to absorb counter-electromotive force energy generated when inductive load is turned OFF. Since the input voltage is clamped at 0V when the active clamp circuit is activated, the thermal shutdown circuit is disabled. Design a thermal solution so that the chip temperature will definitely come to less than 150°C.

10. Counter-electromotive Force

Fully ensure that the counter-electromotive force presents no problems in the operation or the IC.

Operational Notes - continued

11. Negative Current of Output

When supply a negative current from DRAIN terminal in the state that supplied the voltage to IN terminal. The current pass from IN terminal to DRAIN terminal through a parasitic transistor and voltage of IN terminal descend as shown in figure.17 and figure.18.

As shown in figure.17 power MOS is turned on, set the DRAIN terminal is more than -0.3V. Because a negative current may be passed to DRAIN terminal from a power supply of the connection of the IN terminal (MCU, and so on). As shown in figure.18 power MOS is turned off, add a restriction resistance higher than 330 Ω to IN terminal. Because a negative current may be passed to DRAIN terminal from GND of the connection of the IN terminal.

The restriction resistance value, set up in consideration of the voltage descent caused by the IN terminal current.

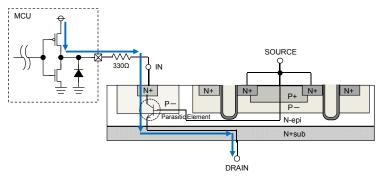


Figure 17. Negative current pass(when power MOS is turned on)

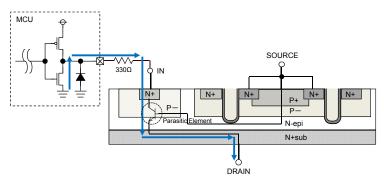


Figure 18. Negative current pass(when power MOS is turned off)

Revision History

Date	Revision	Changes	
09.Jan.2014	001	New Release	
25.Dec.2015	002	 General Description "BM2LB180" → "BM2LB150" Ordering Information is change. "BM2LB180" → "BM2LB150" 	
01.Aug.2016	003	P.1 "Features" Add "AECQ100-012 Grade" P.1 "Applications" Add "Capacitive load" P.1 "Package" Add "W(Typ) x D(Typ) x H(Max)" P.4 "Electrical Characteristics" Turn-ON(OFF) time UNIT change P.12 "Operational Notes" Modify some sentence.	

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JAPAN	USA	EU	CHINA
CLASSⅢ	OL ACOM	CLASS II b	ОГУООШ
CLASSIV	CLASSⅢ	CLASSⅢ	CLASSⅢ

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 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
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 - [d] the Products are exposed to high Electrostatic
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 exceeding the recommended storage time period.
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- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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