NB3V8312C

Ultra-Low Jitter, Low Skew 1:12 LVCMOS/LVTTL Fanout Buffer

The NB3V8312C is a high performance, low skew LVCMOS fanout buffer which can distribute 12 ultra−low jitter clocks from an LVCMOS/LVTTL input up to 250 MHz.

The 12 LVCMOS output pins drive 50 Ω series or parallel terminated transmission lines. The outputs can also be disabled to a high impedance (tri−stated) via the OE input, or enabled when High.

The NB3V8312C provides an enable input, CLK_EN pin, which synchronously enables or disables the clock outputs while in the LOW state. Since this input is internally synchronized to the input clock, changing only when the input is LOW, potential output glitching or runt pulse generation is eliminated.

Separate V_{DD} core and V_{DDO} output supplies allow the output buffers to operate at the same supply as the V_{DD} ($V_{DD} = V_{DDO}$) or from a lower supply voltage. Compared to single−supply operation, dual supply operation enables lower power consumption and output−level compatibility.

The V_{DD} core supply voltage can be set to 3.3 V, 2.5 V or 1.8 V, while the V_{DDO} output supply voltage can be set to 3.3 V, 2.5 V, or 1.8 V, with the constraint that $V_{DD} \geq V_{DDO}$.

This buffer is ideally suited for various networking, telecom, server and storage area networking, RRU LO reference distribution, medical and test equipment applications.

Features

- Power Supply Modes:

V_{DD} (Core)	/ V_{DDO} (Outputs)
3.3 V	/ 3.3 V
3.3 V	/ 2.5 V
3.3 V	/ 1.8 V
2.5 V	/ 2.5 V
2.5 V	/ 1.8 V
1.8 V	/ 1.8 V

- 250 MHz Maximum Clock Frequency
- Accepts LVCMOS, LVTTL Clock Inputs
- LVCMOS Compatible Control Inputs
- 12 LVCMOS Clock Outputs
- Synchronous Clock Enable
- Output Enable to High Z State Control
- 150 ps Max. Skew Between Outputs
- Temp. Range −40°C to +85°C
- 32−pin LQFP and QFN Packages
- These are Pb−Free Devices

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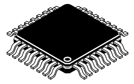
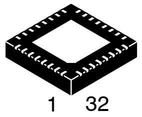


LQFP−32
FA SUFFIX
CASE 873A



QFN32
MN SUFFIX
CASE 488AM

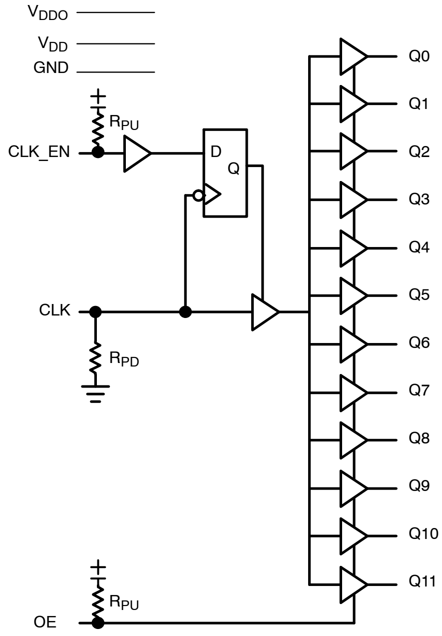


Figure 1. Simplified Logic Diagram

ORDERING AND MARKING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

Applications

- Networking
- Telecom
- Storage Area Network

End Products

- Servers
- Routers
- Switches

August, 2013 − Rev. 0

Publication Order Number:
NB3V8312C/D

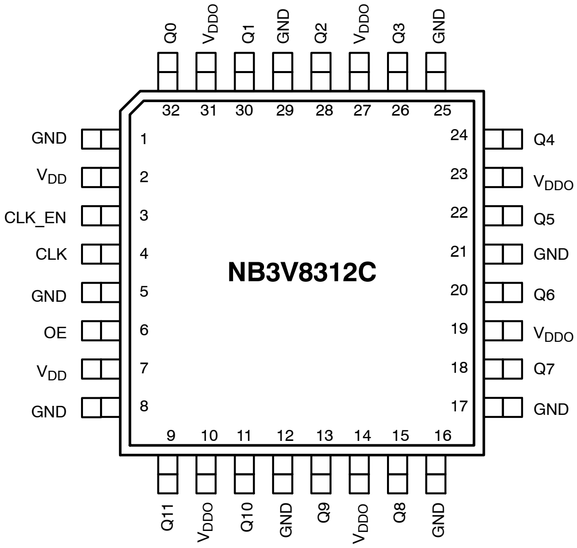


Figure 2. LQFP−32 Pinout Configuration
(Top View)

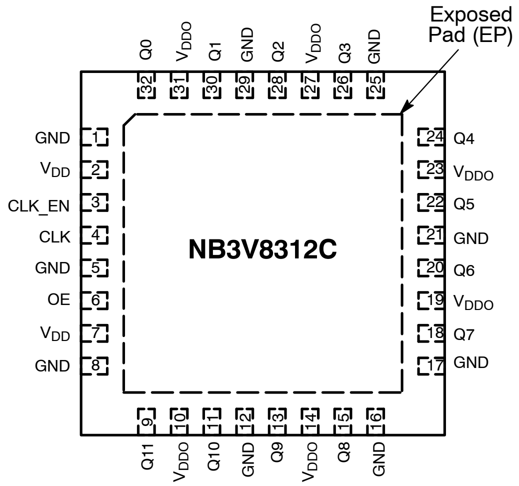


Figure 3. QFN32 Pinout Configuration
(Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Open Default	Description
1, 5, 8, 12, 16, 17, 21, 25, 29	GND	Power		Ground, Negative Power Supply
2, 7	VDD	Power		Positive Supply for Core and Inputs
3	CLK_EN	Input	High	Synchronous Clock Enable Input. When High, outputs are enabled. When Low, outputs are disabled Low. Internal Pullup Resistor.
4	CLK	Input	Low	Single−ended Clock input; LVCMOS/LVTTL. Internal Pull−down Resistor.
6	OE	Input	High	Output Enable. Internal Pullup Resistor.
9, 11, 13, 15, 18, 20, 22, 24, 26, 28, 30, 32	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single−ended LVCMOS/LVTTL outputs
10, 14, 19, 23, 27, 31	VDDO	Power		Positive Supply for Outputs
–	EP	–	–	The Exposed Pad (EP) on the package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is connected to the die and must only be connected electrically to GND on the PC board.

1. All VDD, VDDO and GND pins must be externally connected to a power supply to guarantee proper operation. Bypass each supply pin with 0.01 μF to GND.

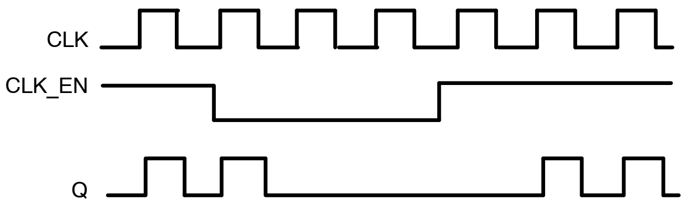


Figure 4. CLK_EN Control Timing Diagram

Table 2. OE, CLK_EN FUNCTION TABLES

Inputs			**Outputs**
OE	**CLK_EN** (Note 2)	**CLK**	**Q[0:11]**
0	X	X	Hi−Z
1	0	X	Low
1	1	0	Low
1	1	1	High

2. The CLK_EN control input synchronously enables or disables the outputs as shown in Figure 4. This control latches on the falling edge of the selected input CLK. When CLK_EN is LOW, the outputs are disabled in a LOW state. When CLK_EN is HIGH, the outputs are enabled as shown. CLK_EN to CLK Set up and Hold times must be satisfied.

Table 3. ATTRIBUTES (Note 3)

Characteristics		Value
Internal Input Pullup (R_{PU}) and Pulldown (R_{PD}) Resistor		50 kΩ
Input Capacitance, C_{IN}		4 pF
Power Dissipation Capacitance, C_{PD} (per Output)		20 pF
R_{OUT}		8 Ω
ESD Protection	Human Body Model Machine Model	> 1.5 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 3)		Level 1
Flammability Rating Oxygen Index		UL−94 code V−0 A 1/8” 28 to 34
Transistor Count		464 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 4)

Symbol	Parameter	Condition		Rating	Unit
V_{DD} / V_{DDO}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Input Voltage			$-0.5 \leq V_I \leq V_{DD} + 0.5$	V
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 5)	0 lfpm 500 lfpm	LQFP−32 LQFP−32	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note 5)	Standard Board	LQFP−32 LQFP−32	12−17	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 5)	0 lfpm 500 lfpm	QFN − 32 QFN − 32	31 27	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note 5)	Standard Board	QFN − 32	12	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
5. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 5. LVCMOS/LVTTL DC CHARACTERISTICS (T_A = −40°C to +85°C)

Symbol	Characteristics		Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage		V_{DD} = 3.465 V	2.0		V_{DD} + 0.3	V
			V_{DD} = 2.625 V	1.7		V_{DD} + 0.3	V
			V_{DD} = 2.0 V	0.65 x V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465 V	−0.3		1.3	V
			V_{DD} = 2.625 V	−0.3		0.7	V
			V_{DD} = 2.0 V	−0.3		0.35 x V_{DD}	V
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465 V or 2.625 V or 2.0 V			150	µA
		OE, CLK_EN				5	
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465 V or 2.625 V or 2.0 V, V_{IN} = 0 V	−5			µA
		OE, CLK_EN		−150			
V_{OH}	Output High Voltage (Note 6)		V_{DDO} = 3.3 V ±5%	2.6			V
			V_{DDO} = 2.5 V ±5%	1.8			
			V_{DDO} = 2.5 V ±5%; I_{OH} = −1 mA	2.0			
			V_{DDO} = 1.8 V ±0.2 V	V_{DD} − 0.4			
			V_{DDO} = 1.8 V ±0.2 V; I_{OH} = −100 µA	V_{DD} − 0.2			
V_{OL}	Output Low Voltage (Note 6)		V_{DDO} = 3. 3V ±5%			0.5	V
			V_{DDO} = 2.5 V ±5%			0.45	
			V_{DDO} = 2.5 V ±5%; I_{OL} = 1 mA			0.4	
			V_{DDO} = 1.8 V ±0.2 V			0.35	
			V_{DDO} = 1.8 V ±0.2 V; I_{OL} = 100 µA			0.2	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Outputs terminated 50 Ω to $V_{DDO}/2$ unless otherwise specified. See Figure 7.

Table 6. POWER SUPPLY DC CHARACTERISTICS, (T_A = −40°C to +85°C)

V_{DD} (Core)	V_{DDO} (Outputs)	Min	Typ	Max	Unit
3.3 V ±5%	3.3 V ±5%			10	mA
3.3 V ±5%	2.5 V ±5%			10	mA
3.3 V ±5%	1.8 V ± 0.2V			10	mA
2.5 V ±5%	2.5 V ±5%			10	mA
2.5 V ±5%	1.8 V ± 0.2V			10	mA
1.8 V ± 0.2 V	1.8 V ± 0.2V			10	mA

Table 7. AC CHARACTERISTICS (T_A = −40°C to +85°C) (Note 7)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{MAX}	Maximum Operating Frequency V_{DD} / V_{DDO}				MHz
	3.3 V ±5% / 3.3 V ±5%	250			
	3.3 V ±5% / 2.5 V ±5%	250			
	3.3 V ±5% / 1.8 V ± 0.2 V	200			
	2.5 V ±5% / 2.5 V ±5%	250			
	2.5 V ±5% / 1.8 V ± 0.2 V	200			
	1.8 V ± 0.2 V / 1.8 V ± 0.2 V	200			
t_{pLH}	Propagation Delay, Low to High; (Note 8) V_{DD} / V_{DDO}				ns
	3.3 V ±5% / 3.3 V ±5%	0.9		2.2	
	3.3 V ±5% / 2.5 V ±5%	1.0		2.3	
	3.3 V ±5% / 1.8 V ± 0.2 V	1.0		3.0	
	2.5 V ±5% / 2.5 V ±5%	1.3		3.1	
	2.5 V ±5% / 1.8 V ± 0.2 V	1.3		3.5	
	1.8 V ± 0.2 V / 1.8 V ± 0.2 V	2.4		4.2	
t_{jit}	Additive Phase Jitter, RMS; V_{DD} / V_{DDO}				fs
	f_C = 100 MHz 3.3 V ±5% / 3.3 V ±5%		30		
	Integration Range: 12 kHz − 20 MHz 3.3 V ±5% / 2.5 V ±5%		40		
	See Figure 5 3.3 V ±5% / 1.8 V ± 0.2 V		50		
	2.5 V ±5% / 2.5 V ±5%		20		
	2.5 V ±5% / 1.8 V ± 0.2 V		100		
	1.8 V ± 0.2 V / 1.8 V ± 0.2 V		130		
$t_{sk(o)}$	Output−to−output skew; (Note 9); Figure 6 V_{DD} / V_{DDO}				ps
	3.3 V ±5% / 3.3 V ±5%			125	
	3.3 V ±5% / 2.5 V ±5%			135	
	3.3 V ±5% / 1.8 V ± 0.2 V			145	
	2.5 V ±5% / 2.5 V ±5%			150	
	2.5 V ±5% / 1.8 V ± 0.2 V			150	
	1.8 V ± 0.2 V / 1.8 V ± 0.2 V			140	
$t_{sk(pp)}$	Part−to−Part Skew; (Note 10) V_{DD} / V_{DDO}				ps
	3.3 V ±5% / 3.3 V ±5%			250	
	3.3 V ±5% / 2.5 V ±5%			250	
	3.3 V ±5% / 1.8 V ± 0.2 V			250	
	2.5 V ±5% / 2.5 V ±5%			250	
	2.5 V ±5% / 1.8 V ± 0.2 V			250	
	1.8 V ± 0.2 V / 1.8 V ± 0.2 V			250	
t_r/t_f	Output rise and fall times V_{DD} / V_{DDO}				ps
	3.3 V ±5% / 3.3 V ±5%	200		700	
	3.3 V ±5% / 2.5 V ±5%	200		700	
	3.3 V ±5% / 1.8 V ± 0.2 V	200		700	
	2.5 V ±5% / 2.5 V ±5%	200		700	
	2.5 V ±5% / 1.8 V ± 0.2 V	200		700	
	1.8 V ± 0.2 V / 1.8 V ± 0.2 V	200		800	
ODC	Output Duty Cycle (Note 11) V_{DD} / V_{DDO}				%
	f ≤ 200 MHz, 3.3 V ±5% / 3.3 V ±5%	45		55	
	f ≤ 150 MHz, 3.3 V ±5% / 2.5 V ±5%	45		55	
	f ≤ 100 MHz, 3.3 V ±5% / 1.8 V ± 0.2 V	45		55	
	f ≤ 150 MHz, 2.5 V ±5% / 2.5 V ±5%	45		55	
	f ≤ 100 MHz, 2.5 V ±5% / 1.8 V ± 0.2 V	45		55	
	f ≤ 100 MHz, 1.8 V ± 0.2 V / 1.8 V ± 0.2 V	45		55	

All parameters measured at f_{MAX} unless noted otherwise.

7. Outputs loaded with 50 Ω to V_{DDO}/2; see Figure 7. CLOCK input with 50% duty cycle; minimum input amplitude = 1.2 V at V_{DD} = 3.3 V, 1.0 V at V_{DD} = 2.5 V, V_{DD}/2 at V_{DD} = 1.8 V.
8. Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.
9. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
10. Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
11. Clock input with 50% duty cycles, rail−to−rail amplitude and t_r/t_f = 500 ps.

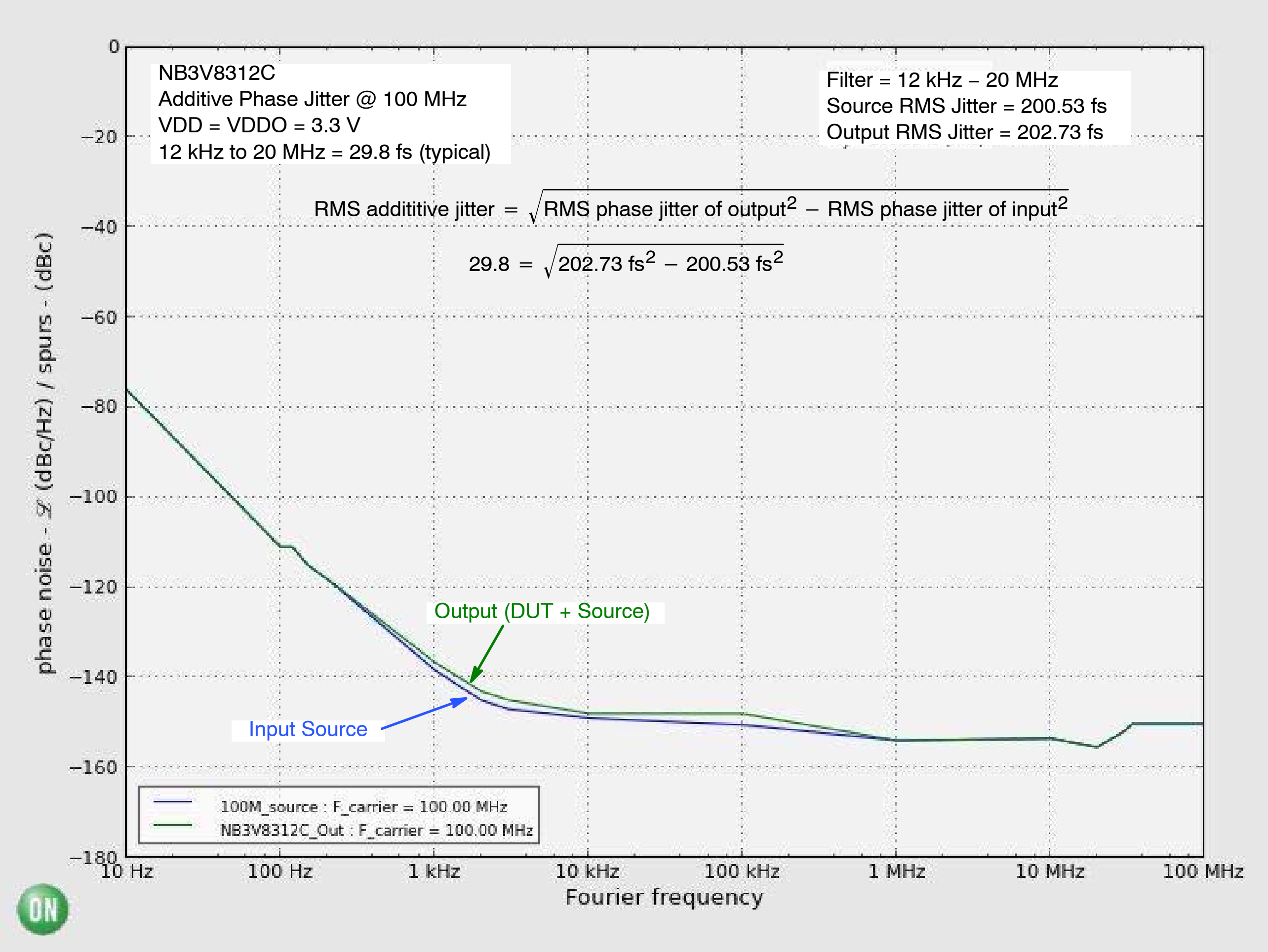


Figure 5. Typical Phase Noise Plot at $f_{carrier}$ = 100 MHz at an Operating Voltage of 3.3 V, Room Temperature

The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 29.8 fs.

The additive phase jitter performance of the fanout buffer is highly dependent on the phase noise of the input source.

To obtain the most accurate additive phase noise measurement, it is vital that the source phase noise be notably lower than that of the DUT. If the phase noise of the source is greater than the device under test output, the source noise will dominate the additive phase jitter calculation and lead to an artificially low result for the additive phase noise measurement within the integration range. The Figure above is a good example of the NB3V8312C source generator phase noise having a significantly higher floor such that the DUT output results in an additive phase jitter of 29.8 fs.

$$\text{RMS addititive jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$29.8 = \sqrt{202.73\ \text{fs}^2 - 200.53\ \text{fs}^2}$$

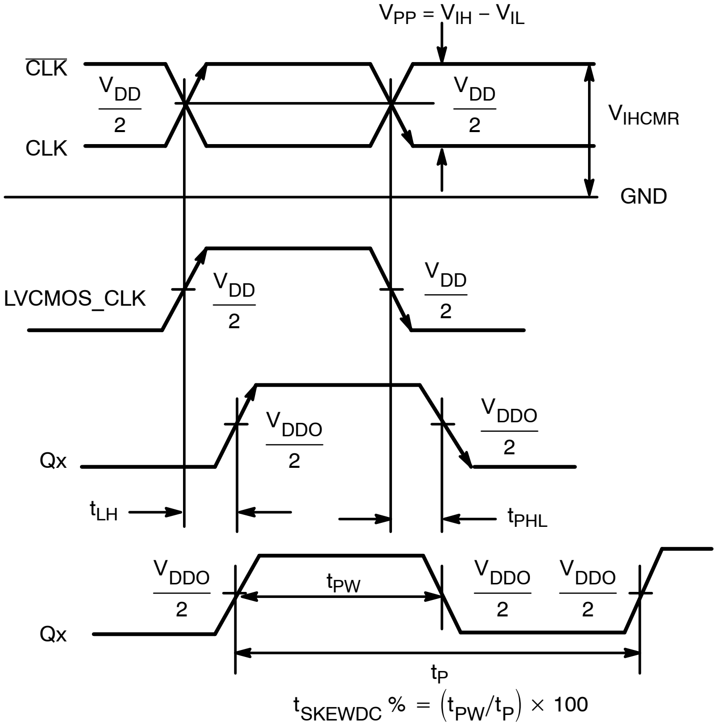


Figure 6. AC Reference Measurement

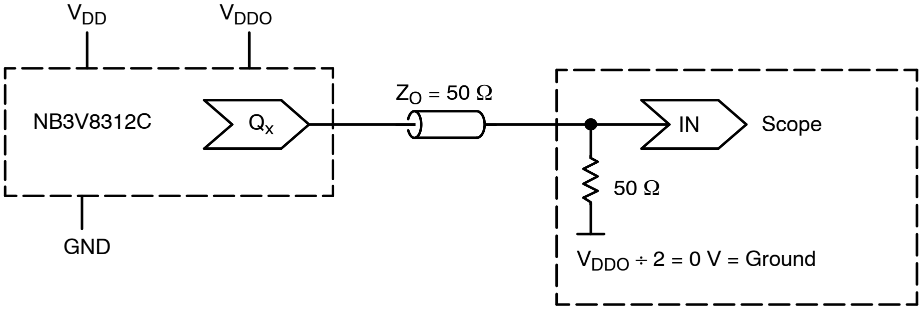
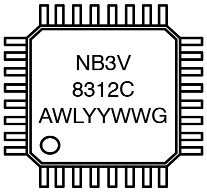


Figure 7. Typical Device Evaluation and Termination Setup – See Table 8

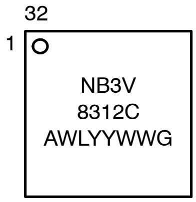
Table 8. TEST SUPPLY SETUP. V_{DDO} SUPPLY MAY BE CENTERED ON 0.0 V (SCOPE GND) TO PERMIT DIRECT CONNECTION INTO “50 Ω TO GND” SCOPE MODULE. V_{DD} SUPPLY TRACKS DUT GND PIN

Spec Condition:	V_{DD} Test Setup	VDDO Test Setup	GND Pin Test Setup
V_{DD} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%	+1.65 ±5%	+1.65 V ±5%	−1.65 V ±5%
V_{DD} = 3.3 V ±5%, V_{DDO} = 2.5 V ±5%	+2.05 V ±5%	+1.25 V ±5%	−1.25 V ±5%
V_{DD} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%	+2.4 V ±5%	+0.9 V ±0.1 V	−0.9 V ±0.1 V
V_{DD} = 2.5 V ±5%, V_{DDO}O = 2.5 V ±5%	+1.25 V ±5%	+1.25 V ±5%	−1.25 V ±5%
V_{DD} = 2.5 V ±5%, V_{DDO} = 1.8 V ±0.2 V	+1.6 V ±5%	+0.9 V ±0.1 V	−0.9 V ±0.1 V
V_{DD} = 1.8 V ±0.2 V, V_{DDO} = 1.8 V ±0.2 V	+0.9 V ±0.1 V	+0.9 V ±0.1 V	−0.9 V ±0.1 V

MARKING DIAGRAMS*



LQFP−32



QFN32

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

(*Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

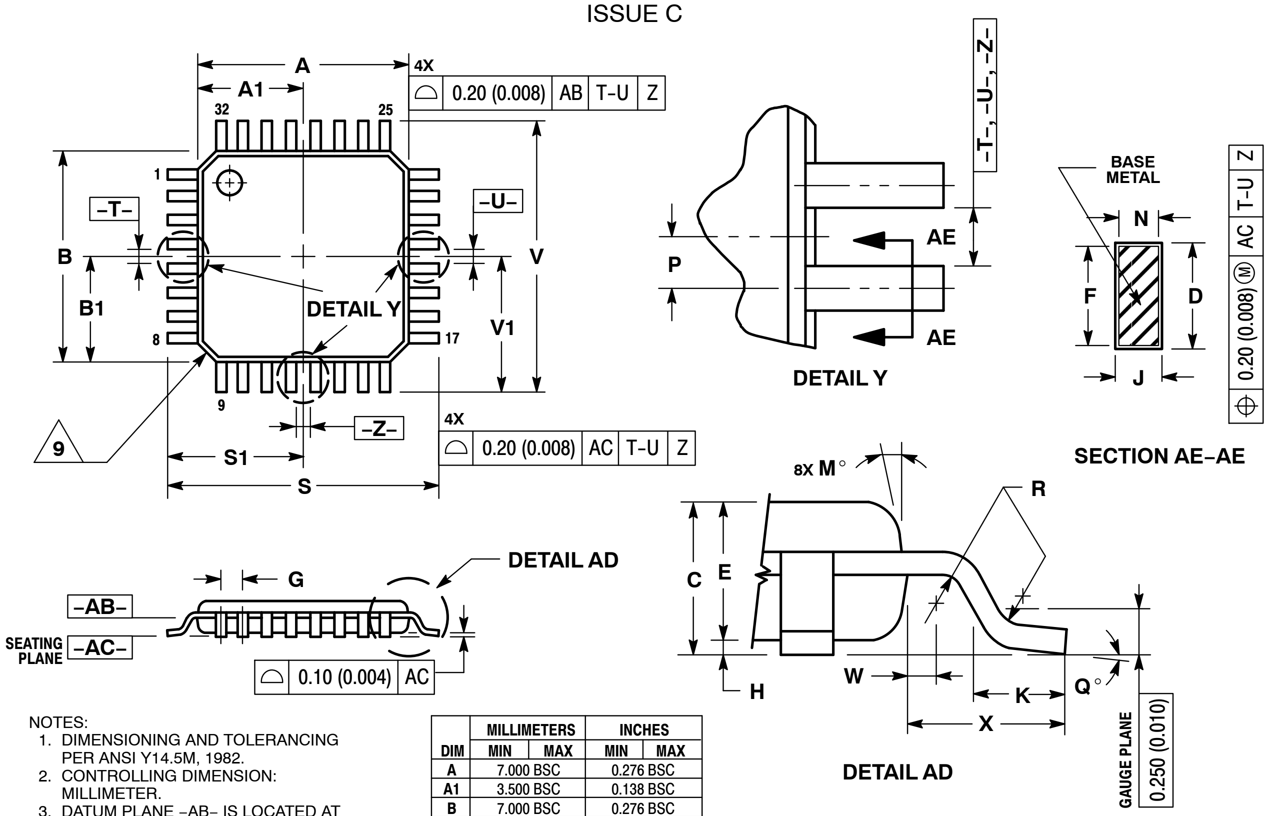
Device	Package	Shipping†
NB3V8312CFAG	LQFP−32 (Pb−Free)	250 Units / Tray
NB3V8312CFAR2G	LQFP−32 (Pb−Free)	2000 / Tape & Reel
NB3V8312CMNG	QFN32 (Pb−Free)	74 Units / Rail
NB3V8312CMNR4G	QFN32 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

32 LEAD LQFP

CASE 873A−02
ISSUE C



NOTES:

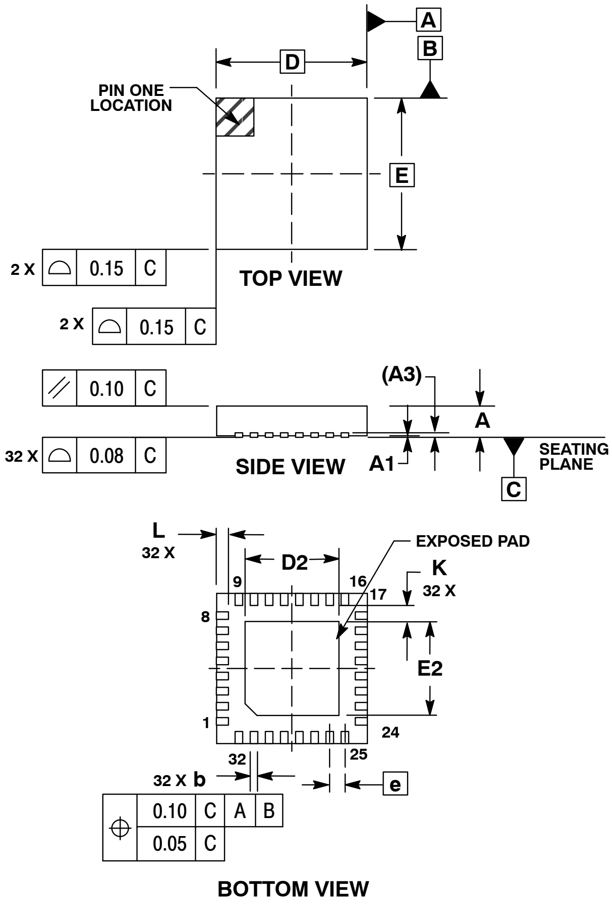
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −AB− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS −T−, −U−, AND −Z− TO BE DETERMINED AT DATUM PLANE −AB−.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE −AC−.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −AB−.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.750	0.018	0.030
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

PACKAGE DIMENSIONS

QFN32 5x5, 0.5P

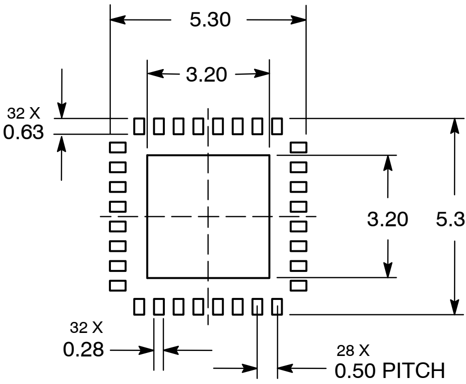
CASE 488AM
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	5.00 BSC		
D2	2.950	3.100	3.250
E	5.00 BSC		
E2	2.950	3.100	3.250
e	0.500 BSC		
K	0.200	---	---
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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