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EVALUATION KIT AVAILABLE

# MAX31790

# 6-Channel PWM-Output Fan RPM Controller

## General Description

The MAX31790 controls the speeds of up to six fans using six independent PWM outputs. The desired fan speeds (or PWM duty cycles) are written through the I²C interface. The outputs drive "4-wire" fans directly, or can be used to modulate the fan's power terminals using an external pass transistor.

Tachometer inputs monitor fan tachometer logic outputs for precise (±1%) monitoring and control of fan RPM as well as detection of fan failure. Six pins are dedicated tachometer inputs. Any of the six PWM outputs can also be configured to serve as tachometer inputs.

The PWM_START inputs select the PWM output status at startup to ensure appropriate fan drive when power is first applied.

To ensure low acoustic impact of fan control, all changes in PWM duty cycle take place at a controlled, programmable rate.

The MAX31790's 3.0V to 5.5V supply voltage range and I²C-compatible interface make it ideal for fan control in a wide range of cooling applications. The MAX31790 is available in a 28-pin TQFN package and operates over the -40°C to +125°C temperature range.

## Features

- ♦ **Controls Up to Six Independent Fans with PWM Drive**
- ♦ **Up to 12 Tachometer Inputs**
- ♦ **Controlled Duty Cycle Rate-of-Change for Best Acoustics**
- ♦ **I²C Bus Interface with Timeout and Watchdog**
- ♦ **3.0V to 5.5V Supply Voltage Range**
- ♦ **1.5mA (typ) Operating Supply Current**

## Applications

Servers

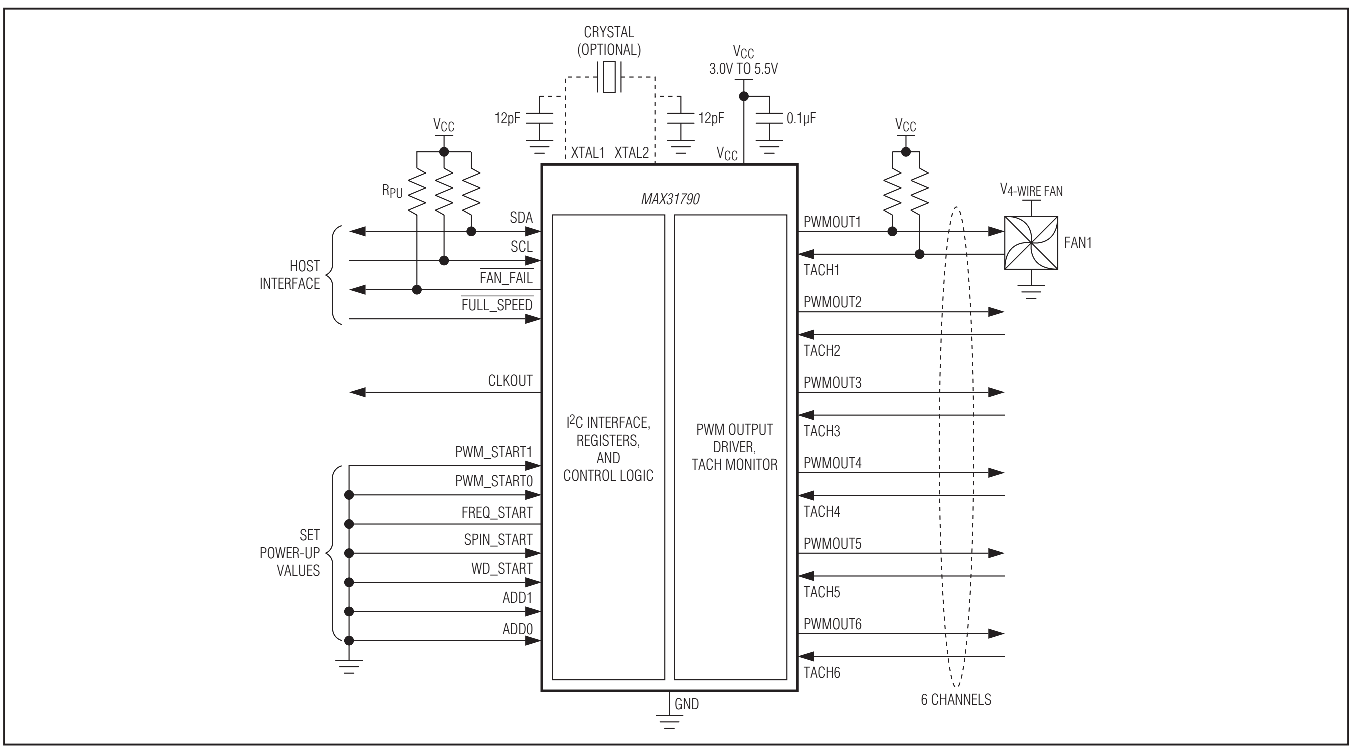
Networking

Telecom

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to: **www.maximintegrated.com/MAX31790.related***

## Typical Operating Circuit



## ABSOLUTE MAXIMUM RATINGS

Voltage Range on $V_{CC}$, SDA, SCL, ADD0, ADD1, $\overline{\text{FAN\_FAIL}}$, PWMOUTn Relative to GND...........-0.3V to +6.0V
Voltage Range on TACHn, WD_START, SPIN_START, FREQ_START, CLKOUT, $\overline{\text{FULL\_SPEED}}$, PWM_STARTn Relative to GND ..............-0.3V to $V_{CC}$ + 0.3V (not to exceed +6.0V)
Input Current at Any Pin.................................................... +5mA
Package Input Current.................................................... +20mA
Continuous Power Dissipation ($T_A$ = +70°C)
TDFN (derate 20.8 mW/°C above +70°C).............1666.7 mW
Operating Temperature Range........................ -40°C to +125°C
Storage Temperature Range............................ -65°C to +150°C
Junction Temperature .....................................................+150°C
ESD Protection (All Pins, HBM) (Note 1)........................ ±2000V
Lead Temperature (soldering, 10s) ................................+300°C
Soldering Temperature (reflow) .....................................+260°C

**Note 1:** Human Body Model, 100pF discharged through a 1.5kΩ resistor.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING CONDITIONS

($T_A$ = -40°C to +125°C, unless otherwise noted.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Operating Supply Voltage | $V_{CC}$ | | 3.0 | 3.3 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | | $V_{CC}$ x 0.7 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | $V_{CC}$ x 0.3 | V |

## ELECTRICAL CHARACTERISTICS

($T_A$ = -40°C to +125°C, typical values are $V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Quiescent Supply Current (Note 4) | $I_{CC}$ | 3.0V < $V_{CC}$ < 3.6V | | 1.5 | 3 | mA |
| | | 4.5V < $V_{CC}$ < 5.5V | | 2.5 | 8 | |
| POR Threshold | $V_{POR}$ | | | 2 | | V |
| Watchdog Timer Accuracy | | $f_{TOSC}$ = 32.768kHz (Note 5) | -0.5 | | +0.5 | s |
| Output Low Voltage (SDA, $\overline{\text{FAN\_FAIL}}$, PWMOUTn, CLKOUT) | | $I_{OL}$ = 3mA | | | 0.4 | V |
| Output High Voltage (CLKOUT) | | $I_{OH}$ = 1mA, $V_{CC}$ = 3.0V | 2.7 | | | V |
| XTAL1 Input Threshold | | | | 0.85 | | V |
| Input Leakage | $I_L$ | (Note 6) | -1 | | +1 | µA |
| Input Capacitance | | All digital inputs | | 5 | | pF |

## FAN CONTROL CHARACTERISTICS

($T_A$ = -40°C to +125°C, typical values are $V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| PWM Resolution | | | 9 | | 9 | Bits |
| PWM Frequency Accuracy | | | -6 | | +6 | % |
| TACH Count Resolution | | | 11 | | 11 | Bits |
| TACH Count Oscillator and CLKOUT Clock | $f_{TOSC}$ | (Note 7) | | 32.768 | | kHz |
| TACH Count Oscillator and CLKOUT Accuracy (Note 7) | $f_{ERR:TOSC}$ | Using internal oscillator: $T_A$ = +25°C, $V_{CC}$ = 3.3V | -0.5 | | +0.5 | % |
| | | Using internal oscillator: 0°C < $T_A$ < +70°C, 3.0V < $V_{CC}$ < 3.6V | -2.5 | | +2.5 | |
| | | Using internal oscillator: -40°C < $T_A$ < +125°C, 3.0V < $V_{CC}$ < 3.6V | -4.0 | | +4.0 | |
| | | Using internal oscillator: -40°C < $T_A$ < +125°C, 3.0V < $V_{CC}$ < 5.5V | -7.0 | | +7.0 | |
| | | Using external crystal | -0.1 | | +0.1 | |
| TACH Minimum Input Pulse Width | $t_{TACHMIN}$ | Pulse width must be greater than this value to be detected | 25 | | 75 | μs |

## I²C AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +3.0V to +5.5V, $T_A$ = -40°C to +125°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (Notes 3, 8) (Figure 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial Clock Frequency | $f_{SCL}$ | | DC | | 400 | kHz |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | 1.3 | | | μs |
| START Condition Hold Time | $t_{HD:STA}$ | | 0.6 | | | μs |
| STOP Condition Setup Time | $t_{SU:STO}$ | 90% of SCL to 10% of SDA | 600 | | | ns |
| Clock Low Period | $t_{LOW}$ | | 1.3 | | | μs |
| Clock High Period | $t_{HIGH}$ | | 0.6 | | | μs |
| START Condition Setup Time | $t_{SU:STA}$ | 90% of SCL to 90% of SDA | 100 | | | ns |
| Data Setup Time | $t_{SU:DAT}$ | 10% of SDA to 10% of SCL | 100 | | | ns |
| Data In Hold Time | $t_{HD:DAT}$ | 10% of SCL to 10% of SDA (Note 9) | 0 | | 0.9 | μs |
| Maximum Receive SCL/SDA Rise Time | $t_R$ | (Note 10) | | 300 | | ns |
| Minimum Receive SCL/SDA Rise Time | $t_R$ | (Note 10) | | 20 + 0.1 x $C_B$ | | ns |

## I2C AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +3.0V to +5.5V, $T_A$ = -40°C to +125°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (Notes 3, 8) (Figure 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Maximum Receive SCL/SDA Fall Time | $t_F$ | (Note 10) | | 300 | | ns |
| Minimum Receive SCL/SDA Fall Time | $t_F$ | (Note 10) | | 20 + 0.1 x $C_B$ | | ns |
| Transmit SDA Fall Time | $t_F$ | 10pF ≤ $C_B$ ≤ 400pF (Note 10) | 20 + 0.1 x $C_B$ | | 250 | ns |
| Pulse Width of Suppressed Spike | $t_{SP}$ | | | 35 | | ns |
| SDA Time Low for Reset of Serial Interface | $t_{TIMEOUT}$ | (Note 11) | 25 | | 45 | ms |

**Note 2:** All voltages referenced to ground. Currents entering the IC are specified as positive.
**Note 3:** Limits are 100% production tested at $T_A$ = +25°C and/or $T_A$ = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.
**Note 4:** SDA = SCL = $V_{CC}$, PWM active with PWM_FREQUENCY = 25kHz.
**Note 5:** The watchdog timer is derived from $f_{TOSC}$ and the watchdog timer accuracy specifications do not include the oscillator's associated error $f_{ERR:TOSC}$.
**Note 6:** Applies to pins SDA, SCL, PWM_STARTn, WD_START, FREQ_START, SPIN_START, ADDn, TACHn, PWMOUTn, $\overline{\text{FULL\_SPEED}}$.
**Note 7:** $f_{TOSC}$ is used to measure fan speed by counting the number of 8192Hz ($f_{TOSC}$/4) clock cycles that take place during a selectable number of tachometer periods.
**Note 8:** All timing specifications are guaranteed by design.
**Note 9:** A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL's falling edge.
**Note 10:** $C_B$—total capacitance of one bus line in pF.
**Note 11:** Holding the SDA line low for a time greater than $t_{TIMEOUT}$ causes the device to reset SDA to the idle state of the serial bus communication (SDA set high).

## EXTERNAL CRYSTAL PARAMETERS

(Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Crystal Oscillator Startup Time | | | | 1 | | s |
| Nominal Frequency | $f_O$ | | | 32.768 | | kHz |
| Series Resistance | ESR | | | | 50 | kΩ |
| Load Capacitance | $C_L$ | | | 12 | | pF |

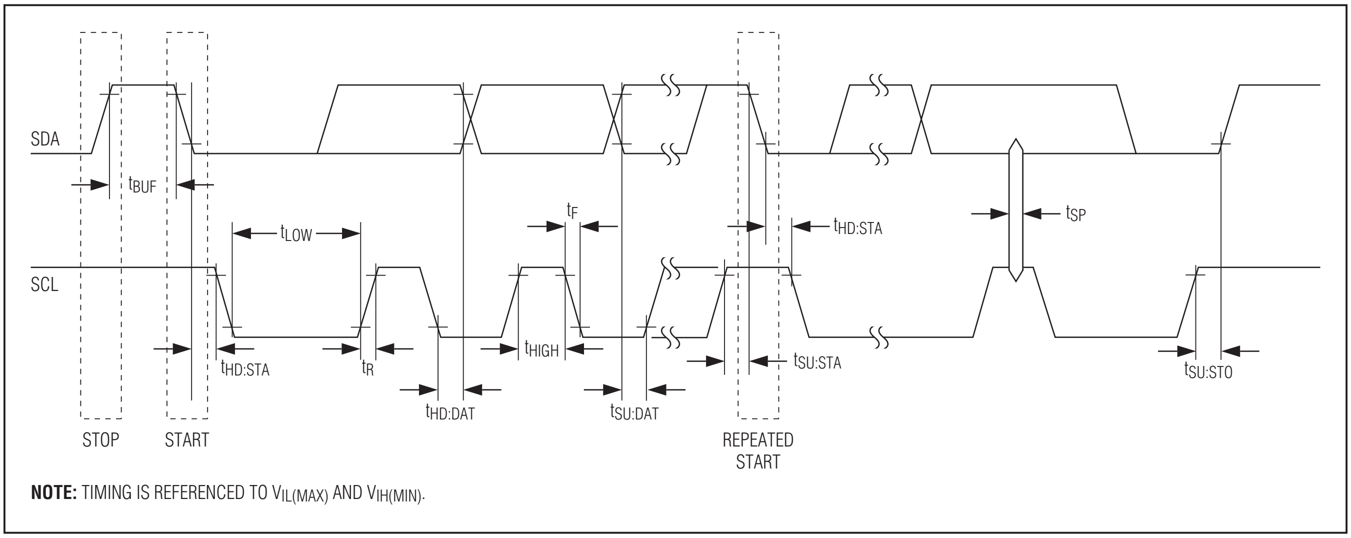
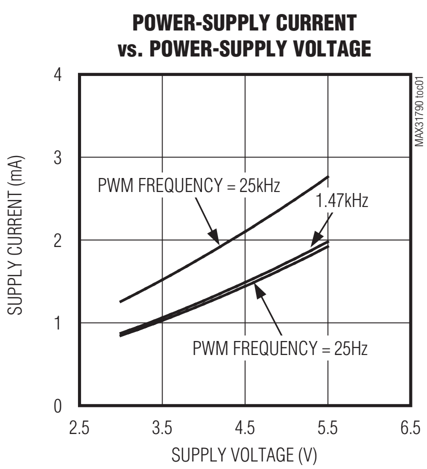
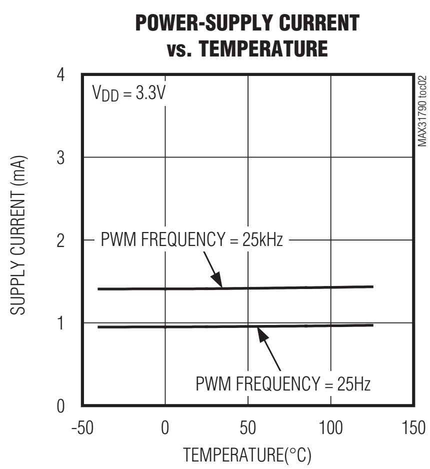



*Figure 1. I²C Timing Diagram*

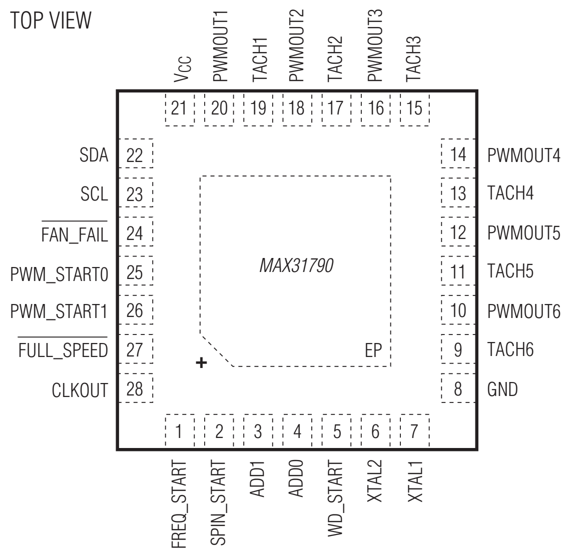
## *Typical Operating Characteristics*

($T_A$ = +25°C, unless otherwise noted.)



## Pin Configuration



**TQFN**
**(4mm x 4mm)**

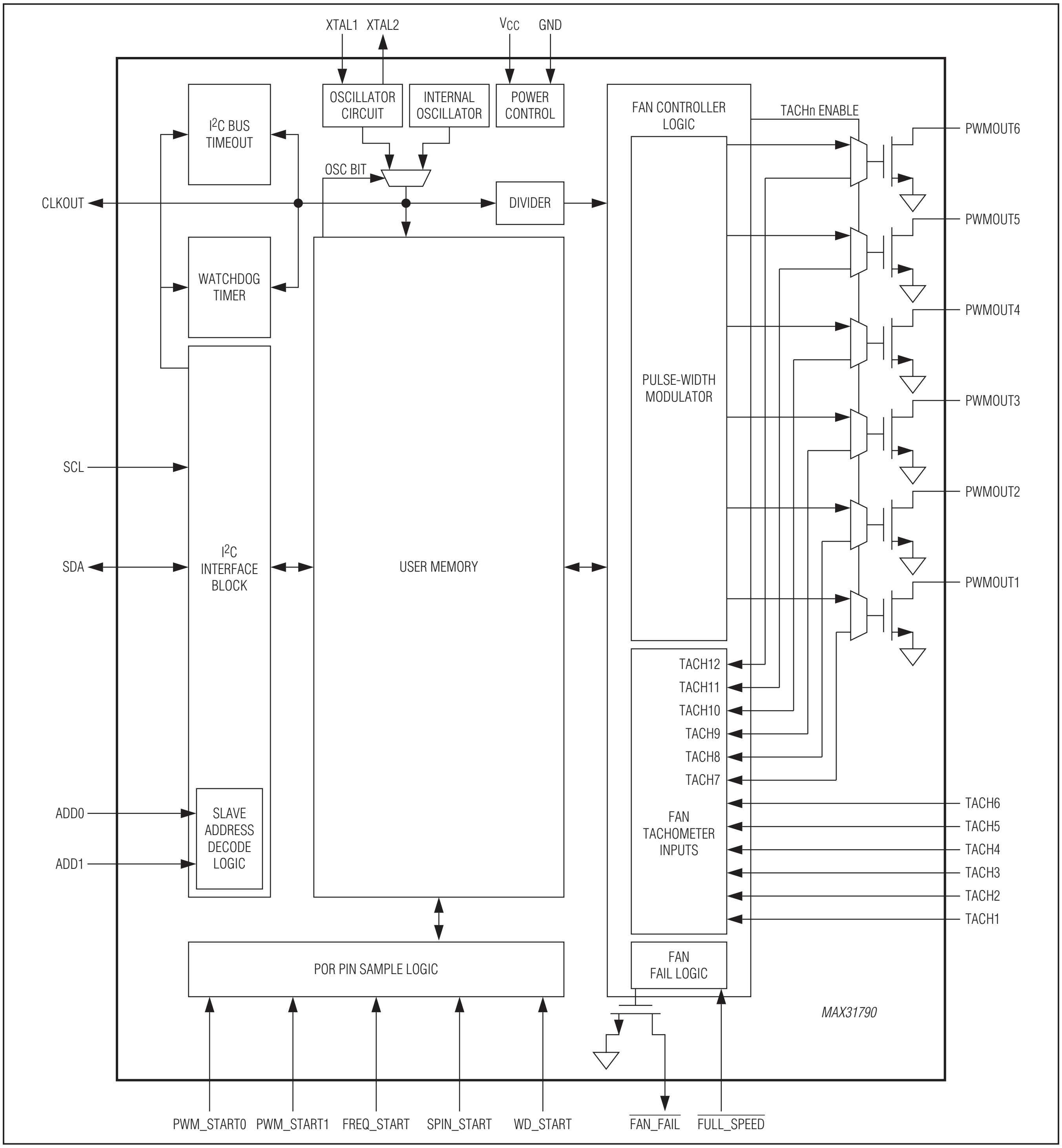
## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | FREQ_START | This input is sampled at power-up and sets the power-up value for the PWM output frequency. See the *Register Map* for values. |
| 2 | SPIN_START | This input is sampled at power-up and sets the initial spin-up behavior. See the *Register Map* for values. |
| 3 | ADD1 | Address Select Inputs. Sampled at the start of every $I^2C$ transaction. One of 16 possible addresses can be selected by connecting ADD0 and ADD1 to GND, $V_{CC}$, SDA, or SCL. |
| 4 | ADD0 | |
| 5 | WD_START | This input is sampled at power-up and sets the initial $I^2C$ watchdog behavior. See the *Register Map* for values. |
| 6 | XTAL2 | Pins for Connecting to Optional 32,768Hz Crystal. The crystal can be used when the best RPM precision is required. At POR the internal oscillator is used, and a nominal 32,768Hz clock is produced at CLKOUT. If a crystal is connected between XTAL1 and XTAL2, the crystal oscillator can be enabled by writing to a register. If no crystal is present, ground XTAL1 and leave XTAL2 unconnected. |
| 7 | XTAL1 | |
| 8 | GND | Ground |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 9 | TACH6 | Logic/Analog Inputs for Tach Signals. If a fan has a logic tach output, it can be used for RPM control. For a 2-wire fan, analog input can be used for fan-failure detection. Also functions as a “locked rotor” input. |
| 11 | TACH5 | |
| 13 | TACH4 | |
| 15 | TACH3 | |
| 17 | TACH2 | |
| 19 | TACH1 | |
| 10 | PWMOUT6 | Open-Drain Output to 4-Wire Fan’s PWM Input or (Less Frequently) to Power Transistor Modulating Fan Power Supply. Can also be used as a tachometer signal input. Can be pulled up as high as 5.5V. |
| 12 | PWMOUT5 | |
| 14 | PWMOUT4 | |
| 16 | PWMOUT3 | |
| 18 | PWMOUT2 | |
| 20 | PWMOUT1 | |
| 21 | $V_{CC}$ | Power-Supply Input. 3.3V nominal. Bypass $V_{CC}$ to GND with a 0.1µF capacitor. |
| 22 | SDA | $I^2C$ Serial-Data Input/Output, Open Drain. Can be pulled up to 5.5V regardless of $V_{CC}$. |
| 23 | SCL | $I^2C$ Serial-Clock Input. Can be pulled up to 5.5V regardless of $V_{CC}$. |
| 24 | $\overline{\text{FAN\_FAIL}}$ | Active-Low, Open-Drain Fan-Failure Output. Active only when fault is present. |
| 25 | PWM_START0 | These inputs are sampled at power-up and set the power-up value for all PWMOUT duty cycles. See the *Register Map* for values. |
| 26 | PWM_START1 | |
| 27 | $\overline{\text{FULL\_SPEED}}$ | When low, this input forces all PWM outputs to 100%. Exception: If a fan has failed and “Duty Cycle = 0 on Failure” has been selected for that fan. |
| 28 | CLKOUT | CMOS Push-Pull 32,768Hz Clock Output. Signal generated from internal oscillator when external crystal is not used. If a crystal is connected between XTAL1 and XTAL2 and enabled, the crystal oscillator generates the output. Output is always active. |
| — | EP | Exposed Pad. Connect to GND. |

### Block Diagram



## Detailed Description

The MAX31790 controls the speeds of up to six fans using six independent PWM outputs. The desired fan speeds (or PWM duty cycles) are written through the I$^2$C interface. The outputs drive "4-wire" fans directly or can be used to control 2-wire or 3-wire fans by modulating the fan's power supply voltage. Modulating the power supply voltage can be achieved by various techniques and are described in the Controlling 2-Wire and 3-Wire Fans section.

The MAX31790 has two main methods for controlling fan speeds: PWM mode and RPM mode. Additional level of control is achieved by the incorporated rate-of-change control that allows the device to control the max rate at which the PWM duty cycle is incremented/decremented.

Tachometer inputs monitor fan tachometer logic outputs for precise (±1%) monitoring and control of fan RPM as well as detection of fan failure. Six pins are dedicated tachometer inputs. Any of the six PWM outputs can also be configured to serve as tachometer inputs, allowing for up to 12 fans to be monitored.

The device can monitor the TACHn inputs and determine when a fan has failed. Failure is detected in various ways depending on the fan control mode. Once a selectable number of fault detections has occurred, the $\overline{\text{FAN\_FAIL}}$ output asserts (if fault detection is not masked for the fan).

Power-on values for PWM duty cycles, PWM frequencies, fan spin-up, and the watchdog are achieved by five pin inputs.

### Fan Control

The device has two main methods for controlling fan speeds: PWM mode and RPM mode.

#### PWM Mode

In PWM mode, the device produces a PWM waveform that drives the fan's PWM speed control input. The fan's speed is proportional to the PWM duty cycle delivered to its PWM input terminal. The duty cycle is set by the fan's associated PWMOUT Target Duty Cycle registers and the actual duty cycle can be read from the corresponding PWMOUT Duty Cycle register. Because the duty cycle ramps to new values at a controlled rate, the values in the two registers can be different. See the Register Descriptions section for details.

#### RPM Mode

In RPM mode, the device monitors tachometer output pulses from the fan and adjusts the PWM duty cycle to force the fan's speed to the desired value. Fan speed is measured by counting the number of internal 8192Hz ($f_{TOSC}$/4) clock cycles that take place during a selectable number of tachometer periods. The number of clock cycles counted (11-bit value) is stored in the associated TACH Count registers and the desired number of cycles is stored in the TACH Target Count registers. See the Register Descriptions section for details.

#### Rate-of-Change Control

Sudden changes in fan speed can be easily heard by users. The device helps reduce the audibility of fan-speed changes by controlling the rate at which the PWM duty cycle is incremented. Three bits in the associated Fan Dynamics register sets the rate at which the duty cycle is incremented/decremented. This allows the time required for an LSB of change in the PWM duty cycle to vary from 0ms to 125ms.

The selected rate of change also applies when the $\overline{\text{FULL\_SPEED}}$ input is asserted or when the fans are forced to 100% due to a fan failure. See the Register Descriptions section for details.

In RPM mode when the fan's speed is near the target speed, that is, when the TACH count is near the TACH target count, the control loop dynamics can often be improved by slowing the rate of change of the PWM duty cycle. This operates as follows: First, set a value for the count "window" and store it in the appropriate Window register. In RPM mode, calculate the difference between the current TACH count and the target TACH count. If the absolute value of this difference is less than the value in the appropriate Window register, the update rate of the PWM duty cycle is slowed to 1 LSB per second. When the current TACH count falls outside of the window, the duty cycle rate of change reverts to the selected value.

#### Spin-Up

When a fan is not spinning, and a low duty cycle waveform is applied to its PWM terminal, it can fail to overcome inertia and start spinning. To overcome this potential problem, a 100% duty cycle waveform can be applied to the fan's PWM input for a short time before a lower duty cycle waveform is applied. This "spin-up" period allows the fan to overcome inertia and begin operating. Spin-up is controlled using the corresponding Fan

Configuration register. Spin-up can be disabled, or it can cause the fan to be driven with a 100% duty cycle until it produces two tachometer pulses, up to a maximum of 0.5s, 1s, or 2s. When spin-up is enabled and the duty cycle is making a transition from 0% to a value that is less than 100% (from 0% to 50%, for example), the duty cycle first goes to 100%. When two tachometer pulses have been detected, or when the maximum spin-up period has elapsed, the duty cycle drops to the target value (50% in this example). The SPIN_START pin sets the spin-up value at power-up.

### Sequential Fan Activation

When multiple high-current fans are activated simultaneously, the startup current can stress the system's power supply. To minimize this effect, the device includes a selectable sequential fan activation feature. When selected, this feature inserts a short minimum delay between the activation times of fans.

The bits for controlling sequential fan activation are located in the Failed Fan Options/Sequential Start register. They select the time delay between fan activations to be one of the following: 0, 250ms, 500ms, 1s, 2s, or 4s. The default time is 500ms per channel.

Sequential fan activation applies to POR, fan failure forcing the fans to full speed, and assertion of the $\overline{\text{FULL\_SPEED}}$ input, which forces all the fans to full speed. In all these cases, all fans are forced to full speed. The sequence operates as follows:

- PWM1 activates. The PWM duty cycle begins to increase at the selected rate of change.
- After the selected delay time has elapsed, PWM2 activates. Again, the PWM duty cycle begins to increase at the selected rate of change.
- The other PWM channels activate in sequence, each delayed by the selected delay time relative to the previous channel. Note that the time delay applies to unused or disabled channels.

### $\overline{\text{FULL\_SPEED}}$ Input

Driving this input low forces all fans to full speed with the exception of any failed fans (if 0% on failure has been selected). This input allows an external temperature switch to provide fail-safe overtemperature protection. In systems with multiple MAX31790s, all $\overline{\text{FAN\_FAIL}}$ outputs can be connected to all $\overline{\text{FULL\_SPEED}}$ inputs, thereby providing full-speed operation if any fan fails, regardless of which MAX31790 controls it. This input is active even in standby mode.

### POR Options

Five inputs allow setup of the device's behavior at power-up. The following inputs are sampled when power is first applied to the device:

**WD_START:** At power-up the watchdog operation is controlled by the WD_START pin. Connect WD_START to $V_{CC}$ to enable, or to GND to disable the watchdog function. When enabled using WD_START, the timeout period is 30s. After power is applied, the watchdog function can be enabled or disabled, and the timeout period can be changed by editing the Global Configuration register.

**SPIN_START:** At power-up, spin-up operation is controlled by the SPIN_START pin. Connect SPIN_START to GND to disable, $V_{CC}$ to enable spin-up for a maximum of 1s, or unconnected to enable spin-up for a maximum of 0.5s. After power is applied, the spin-up function can be enabled or disabled, and the spin-up period can be changed by editing the associated Fan Configuration register.

**PWM_START0, PWM_START1:** At power-up, the PWM output duty cycles are controlled by the PWM_START0 and PWM_START1 pins. Connect PWM_START0/PWM_START1 to GND, $V_{CC}$, or leave unconnected to achieve different duty cycles for all PWM outputs. See the PWMOUT Target Duty Cycle register for the corresponding values and connections. After power is applied, the PWM duty cycles can be changed, by editing that PWM's associated PWMOUT Target Duty Cycle register.

**FREQ_START:** At power-up, all PWM output frequencies are controlled by the FREQ_START pin. Connect FREQ_START to GND for 30Hz, $V_{CC}$ for 25kHz, or unconnected for 1.47kHz. After power is applied, the PWM output frequencies can be changed by editing the PWM Frequency register.

### Watchdog

The device includes an optional $I^2C$ watchdog function that monitors the $I^2C$ bus for transactions. When the watchdog function is enabled, all fans (with the exception of failed fans "0% on fail" selected) are forced to full speed if no $I^2C$ transactions occur within a selected period (5s, 10s, or 30s). Watchdog timing is selected using the Global Configuration register.

### Fan Monitoring

#### Monitoring Tachometer Signals

The TACH inputs accept either tachometer or "locked rotor" output signals from 3-wire or 4-wire fans. When measuring fan speed, the device counts the number of internal 8192Hz ($f_{TOSC}$/4)clock cycles that occur during 1, 2, 4, 8, 16, or 32 tachometer periods. (The speed of each fan is measured once per second.) The number of tachometer periods is selectable for each fan by using the appropriate Fan Dynamics register. Tachometer pulses less than $t_{TACHMIN}$ in duration are ignored to minimize the effect of noise on the tachometer lines. The TACH count for a given RPM can be obtained from the following equation:

$$\text{TACH Count} = \frac{60}{NP \times RPM} \times SR \times 8192$$

where:

NP = number of tachometer pulses per revolution. Most general-purpose brushless DC fans produce two tachometer pulses per revolution.

SR = 1, 2, 4, 8, 16, or 32. This is the number of tachometer periods over which the tachometer clock is counted. See the Speed Range bit information described in the corresponding Fan Dynamics register description.

The tachometer count consists of 11 bits in the TACH Count registers and is available in RPM and PWM modes. In RPM mode, the desired fan count is written to the associated TACH Target Count register. In PWM mode, the desired fan duty cycle is written to the associated PWMOUT Target Duty Cycle register.

Note that the device is intended to be used with 4-wire fans. Modulating a fan's power supply with a PWM waveform, as is sometimes done with 2-wire and 3-wire fans, results in incorrect tachometer counts due to the periodic removal of power from the fan's internal circuitry. Therefore, it is suggested to use PWM mode when interfacing with 2-wire or 3-wire fans.

#### Using PWM Outputs as Tachometer Inputs

Each Fan Configuration register includes a $\overline{\text{PWM}}$/TACH bit that allows the PWMOUT to be configured as a TACH input. In TACH mode, the settings for TACH input enable, locked rotor operation, and TACH pulses counted that have been selected for a given fan channel apply to that channel's TACH input and also to TACH signals sensed by that channel's PWM output.

Figure 2 to Figure 6 show some examples of TACH-PWM connections for various fan configurations

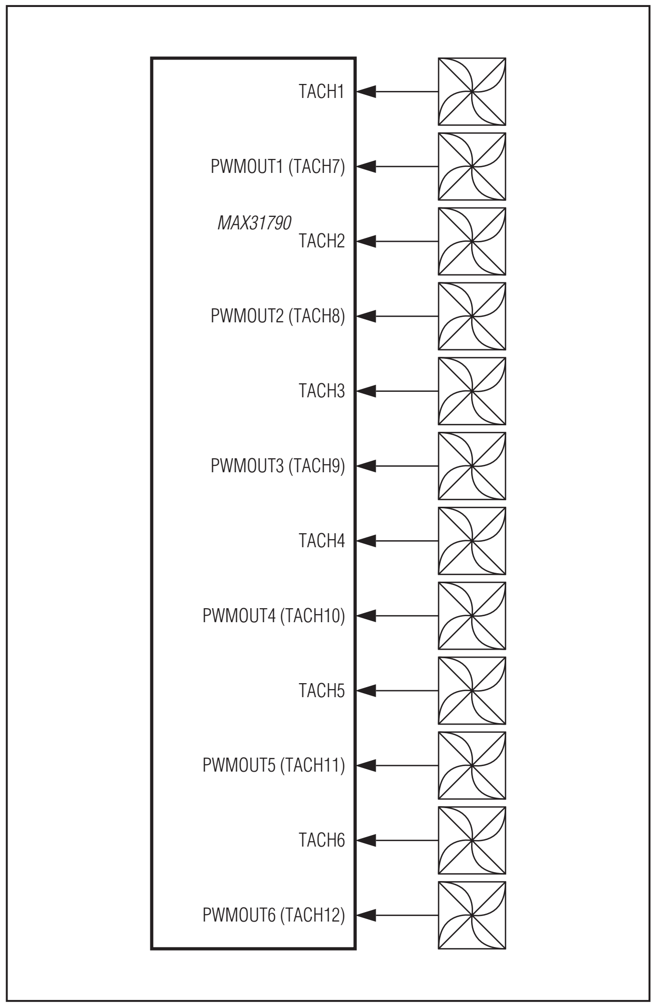



*Figure 2. 12 Fans, 12 TACH Monitors, No PWM*

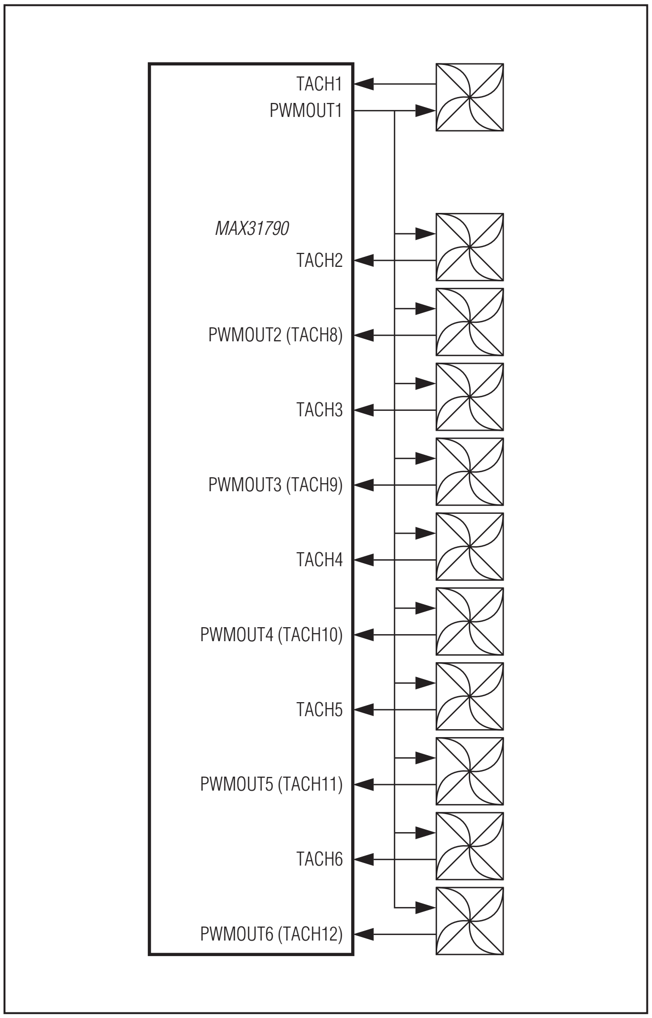



*Figure 3. 11 Fans, 11 TACH Monitors,1 PWM*

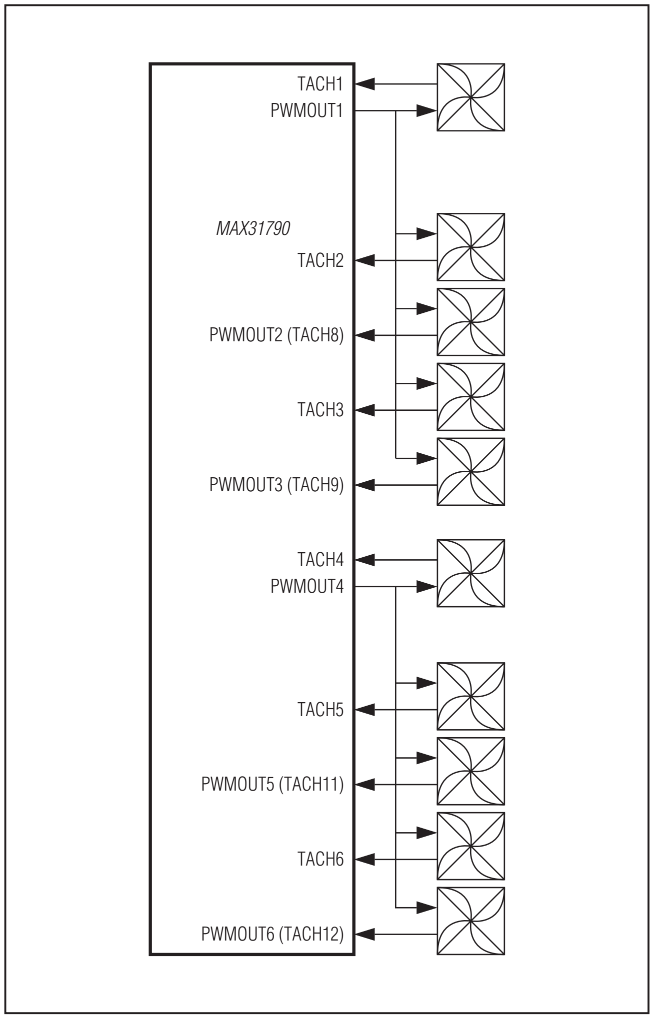



*Figure 4. 10 Fans, 10 TACH Monitors, 2 PWMs*

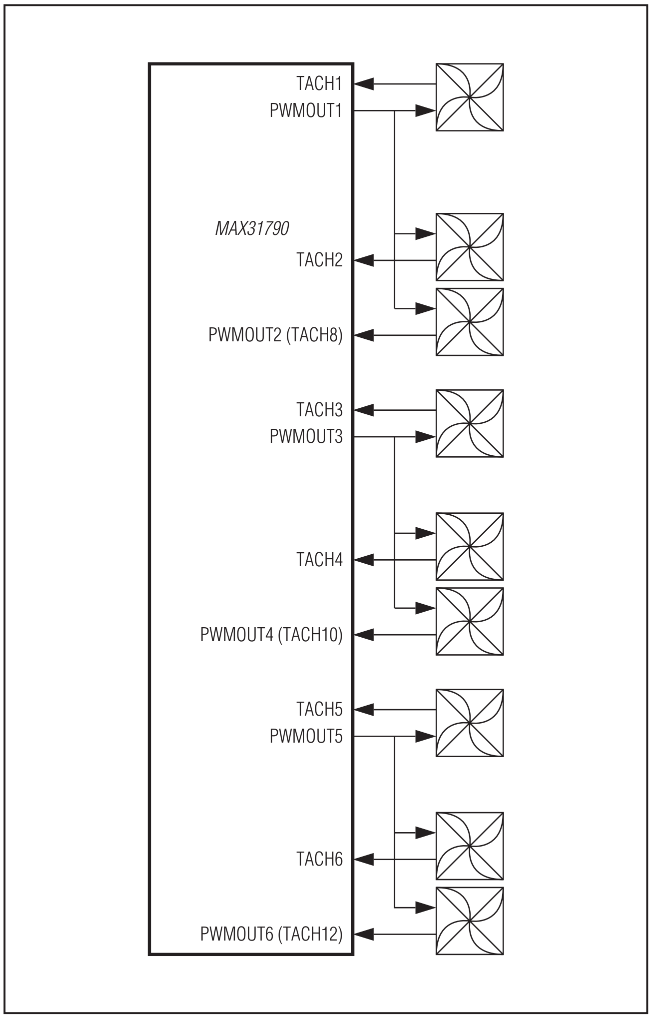



*Figure 5. 9 Fans, 9 TACH Monitors, 3 PWMs*

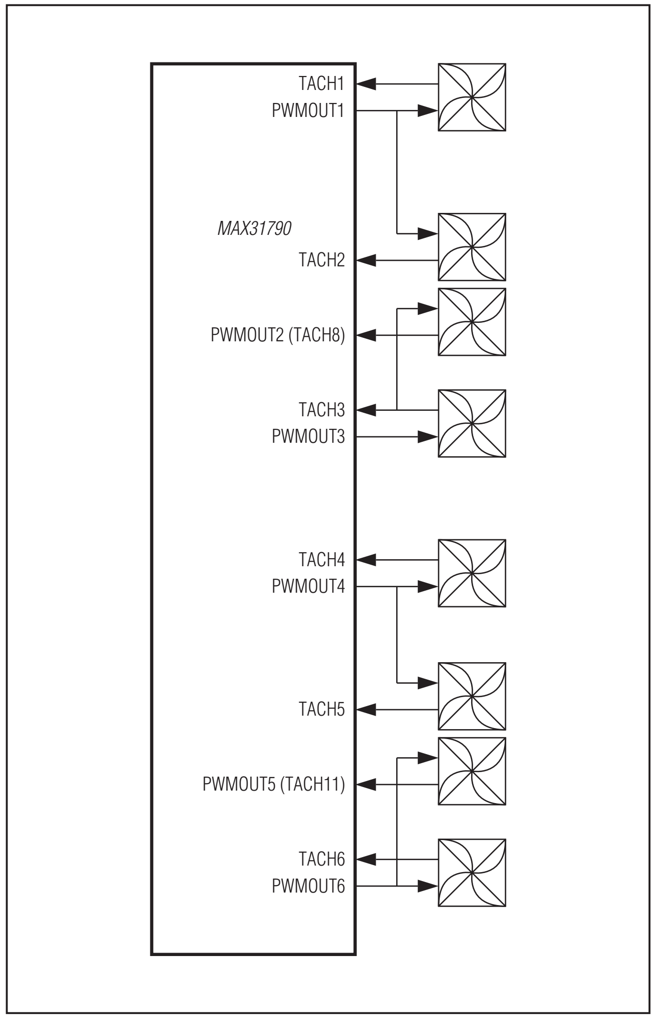



*Figure 6. 8 Fans, 8 TACH Monitors, 4 PWMs*

### Fan Failure

When enabled, the device monitors the TACH inputs to determine when a fan has failed. For fans with tachometer outputs, failure is detected in various ways depending on the fan control mode. In every case, from one to six consecutive fault detections (selected by the Fan Fault Queue bits) are required to decide that the fan has failed. When the selected number of fault detections has occurred, the $\overline{\text{FAN\_FAIL}}$ output asserts (if fault detection is not masked for the fan).

### PWM Mode Failure Detection

In PWM mode, the TACH Target Count register holds the upper limit for tachometer count values. A potential fault condition is identified when the TACH count exceeds the value written to the TACH Target Count register. If the Fan Fault Queue bit value is 1 and the following tachometer count (1 second later) also exceeds the limit value, the fan is considered to have failed. A higher Fan Fault Queue bit value requires a larger number of consecutive values in excess of the limit value. When a PWM output is used as a TACH input, the PWM-mode failure criteria apply. In PWM mode, fan-failure detection is masked when the target duty cycle is set to zero.

### RPM Mode Failure Detection

In RPM mode, a potential fault condition is identified when any of the following three conditions occur: 1) the TACH count exceeds the associated value stored in the TACH Target Count register while the PWM duty cycle is 100%, 2) the TACH count exceeds two times the TACH Target Count register value while the duty cycle is less than 100%, or 3) the TACH count reaches its maximum value of 7FFh. If the Fan Fault Queue bit value is 1 and the TACH Count value also exceeds the limit value, the fan is considered to have failed. A higher Fan Fault Queue value requires a larger number of consecutive values in excess of the limit value. In RPM mode, fan-failure detection is masked when the TACH Target Count register is set to full scale.

### Locked Rotor Mode Failure Detection

Some fans have a locked rotor output that produces a logic-level output to indicate that the fan has stopped spinning. Locked rotor signals can be monitored by setting the $\overline{\text{TACH}}$/Locked Rotor bit in the associated Fan Configuration register. The polarity of the locked rotor signal can be adjusted in this same register. A fan fault is detected when a locked rotor signal has been present for 1 second.

### Failure Indication

Fan failure is indicated in the Fan Fault register and also with the open-drain $\overline{\text{FAN\_FAIL}}$ output after the number of consecutive faults selected by the Fan Fault Queue bits have occurred. The $\overline{\text{FAN\_FAIL}}$ output can be masked using the mask bits in the Fan Fault Mask register.

When a fan has failed, PWM to the affected fan can continue as though the fan is still operational, or the duty cycle can be automatically set to 0 or 100% as determined by the Failed Fan Options bits. See the *Register Descriptions* section for full details.

The failed condition can be cancelled by writing PWM Target duty cycle or TACH target count to the fan's control registers. The new value can be the same as the value already in the register. After writing to the register, the fan-failure detection process begins again. If the fan is still in a failed state, fan failure again is detected.

### Slave Address Byte and Address Pins

The slave address byte consists of a 7-bit slave address plus an R/$\overline{\text{W}}$ bit (Figure 7). The device's slave address is determined by the state of the ADD0 and ADD1 address pins during a START condition of an I²C transaction. The ADD0 and ADD1 pins can be connected to GND, $V_{CC}$, SDA, or SCL. These pins allow up to 16 MAX31790s to reside on the same I²C bus. See Table 1 for a complete list of all 16 possibilities and the corresponding ADD0 and ADD1 pin connections.

For example, the device's slave address byte is 40h when ADD0 and ADD1 pins are grounded during a START condition. I²C communication is described in detail in the *I²C Serial Interface Description* section.

Note: If the state of the ADD0 and ADD1 pins is changing during normal operation, the slave address of the device dynamically changes to reflect the pins states at every START condition. The ADD0 and ADD1 pins cannot change during an I²C transaction.

## Table 1. Slave Address Table

| ADD1 CONNECTION | ADD0 CONNECTION | SLAVE ADDRESS BYTE (HEX) |
|---|---|---|
| GND | GND | 40 |
| GND | SCL | 42 |
| GND | SDA | 44 |
| GND | VCC | 46 |
| SCL | GND | 48 |
| SCL | SCL | 4A |
| SCL | SDA | 4C |
| SCL | VCC | 4E |
| SDA | GND | 50 |
| SDA | SCL | 52 |
| SDA | SDA | 54 |
| SDA | VCC | 56 |
| VCC | GND | 58 |
| VCC | SCL | 5A |
| VCC | SDA | 5C |
| VCC | VCC | 5E |

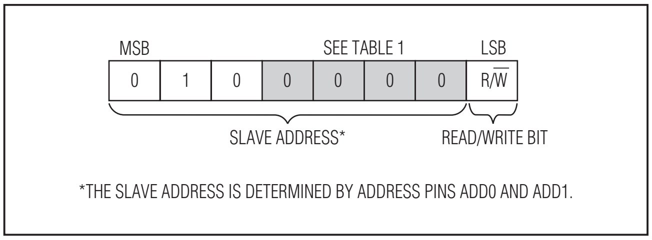



*Figure 7. MAX31790 Slave Address Byte Example*

## Memory Description

The device's control registers are organized in rows of 8 bytes. The I²C master can read or write individual bytes, or can read or write multiple bytes. When writing consecutive bytes, all writes are to the same row. When the final byte in the row is reached, the next byte written is the row's first byte. For example, a write that starts with 02h (Fan 1 Configuration) can write to 02h, 03h, 04h, 05h, 06h, and 07h. If writes continue, the next byte written is 00h, and so on.

Consecutive reads are not subject to the single-row limitation. A read can start at any address and can continue through FFh. If reads continue past FFh, they wrap around to 00h.

"User Bytes" are general-purpose R/W bytes. X denotes the input state at POR.

### Register Map

| R/W | REGISTER | POR STATE | FUNCTION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W | 00h | 0010 0XX0b | Global Configuration | $\overline{\text{Run}}$/Standby<br>0 = Run<br>1 = Standby | Reset:<br>0 = Normal<br>1 = Reset | $\overline{\text{Bus Timeout}}$<br>0 = Enabled | RESERVED | OSC:<br>0 = Internal oscillator<br>1 = External crystal | I²C Watchdog:<br>00b = Disabled<br>01b = 5s<br>10b = 10s<br>11b = 30s | | I²C Watchdog Status<br>1 = Watchdog fault detected |
| R/W | 01h | FREQ_START | PWM Frequency | PWM4-PWM6 Frequency:<br>0000b = 25Hz<br>0001b = 30Hz<br>0010b = 35Hz<br>0011b = 100Hz<br>0100b = 125Hz<br>0101b = 149.7Hz<br>0110b = 1.25kHz<br>0111b = 1.47kHz<br>1000b = 3.57kHz<br>1001b = 5kHz<br>1010b = 12.5kHz<br>1011b = 25kHz | | | | PWM1-PWM3 Frequency:<br>0000b = 25Hz<br>0001b = 30Hz<br>0010b = 35Hz<br>0011b = 100Hz<br>0100b = 125Hz<br>0101b = 149.7Hz<br>0110b = 1.25kHz<br>0111b = 1.47kHz<br>1000b = 3.57kHz<br>1001b = 5kHz<br>1010b = 12.5kHz<br>1011b = 25kHz | | | |
| R/W | 02h | 0XX0 0000b | Fan 1 Configuration | Mode:<br>0 = PWM<br>1 = RPM | Spin-Up<br>00b = No Spin-up<br>01b = 2 TACH counts or 0.5s<br>10b = 2 TACH counts or 1s<br>11b = 2 TACH counts or 2s | | $\overline{\text{Control}}$/Monitor<br>0 = Control<br>1 = Monitor only | TACH Input Enable<br>1 = Enabled | $\overline{\text{TACH}}$/Locked Rotor<br>0 = TACH<br>1 = Locked Rotor | Locked Rotor Polarity<br>0 = Low<br>1 = High | $\overline{\text{PWM}}$/TACH<br>0 = PWM<br>1 = TACH |
| R/W | 03h | 0XX0 0000b | Fan 2 Configuration | Same as Fan 1 Configuration | | | | | | | |
| R/W | 04h | 0XX0 0000b | Fan 3 Configuration | Same as Fan 1 Configuration | | | | | | | |

***Register Map (continued)***

| R/W | REGISTER | POR STATE | FUNCTION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W | 05h | 0XX0 0000b | Fan 4 Configuration | Same as Fan 1 Configuration | | | | | | | |
| R/W | 06h | 0XX0 0000b | Fan 5 Configuration | Same as Fan 1 Configuration | | | | | | | |
| R/W | 07h | 0XX0 0000b | Fan 6 Configuration | Same as Fan 1 Configuration | | | | | | | |
| R/W | 08h | 0100 1100b | Fan 1 Dynamics | Speed Range (TACH Periods Counted)<br>000b = 1<br>001b = 2<br>010b = 4 (default)<br>011b = 8<br>100b = 16<br>101b = 32<br>110b = 32<br>111b = 32 | | | PWM Rate-of-Change:<br>000b = 0ms per LSB (PWM)<br>000b = 0.9765ms per LSB (RPM)<br>001b = 1.953125ms per LSB<br>010b = 3.90625ms per LSB<br>011b = 7.8125ms per LSB (default)<br>100b = 15.625ms per LSB<br>101b = 31.25ms per LSB<br>110b = 62.5ms per LSB<br>111b = 125ms per LSB | | | Asymmetric Rate of Change<br>1 = Enabled | RESERVED |
| R/W | 09h | 0100 1100b | Fan 2 Dynamics | Same as Fan 1 Dynamics | | | | | | | |
| R/W | 0Ah | 0100 1100b | Fan 3 Dynamics | Same as Fan 1 Dynamics | | | | | | | |
| R/W | 0Bh | 0100 1100b | Fan 4 Dynamics | Same as Fan 1 Dynamics | | | | | | | |
| R/W | 0Ch | 0100 1100b | Fan 5 Dynamics | Same as Fan 1 Dynamics | | | | | | | |
| R/W | 0Dh | 0100 1100b | Fan 6 Dynamics | Same as Fan 1 Dynamics | | | | | | | |
| R/W | 0Eh | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 0Fh | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 10h | 0000 0000b | Fan Fault Status 2 | RESERVED | RESERVED | Fan 12 Fault<br>1 = Fault | Fan 11 Fault<br>1 = Fault | Fan 10 Fault<br>1 = Fault | Fan 9 Fault<br>1 = Fault | Fan 8 Fault<br>1 = Fault | Fan 7 Fault<br>1 = Fault |
| R/W | 11h | 0000 0000b | Fan Fault Status 1 | RESERVED | RESERVED | Fan 6 Fault<br>1 = Fault | Fan 5 Fault<br>1 = Fault | Fan 4 Fault<br>1 = Fault | Fan 3 Fault<br>1 = Fault | Fan 2 Fault<br>1 = Fault | Fan 1 Fault<br>1 = Fault |
| R/W | 12h | 0011 1111b | Fan Fault Mask 2 | RESERVED | RESERVED | Fan 12 Mask<br>1 = Masked | Fan 11 Mask<br>1 = Masked | Fan 10 Mask<br>1 = Masked | Fan 9 Mask<br>1 = Masked | Fan 8 Mask<br>1 = Masked | Fan 7 Mask<br>1 = Masked |
| R/W | 13h | 0011 1111b | Fan Fault Mask 1 | RESERVED | RESERVED | Fan 6 Mask<br>1 = Masked | Fan 5 Mask<br>1 = Masked | Fan 4 Mask<br>1 = Masked | Fan 3 Mask<br>1 = Masked | Fan 2 Mask<br>1 = Masked | Fan 1 Mask<br>1 = Masked |

***Register Map (continued)***

| R/W | REGISTER | POR STATE | FUNCTION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W | 14h | 0100 0101b | Failed Fan Options/ Sequential Start | Sequential Start Delay<br>000b = 0s<br>001b = 250ms<br>010b = 500ms<br>011b = 1s<br>100b = 2s<br>101b, 110b, 111b = 4s | | | RESERVED | Failed Fan Options<br>00b = duty cycle = 0% on fail<br>01b = Continue PWM or RPM mode operation on fail.<br>10b = duty cycle = 100% on fail<br>11b = All fans to 100% on any unmasked fan failure. | | Fan Faut Queue<br>00b = 1 fault<br>01b = 2 faults<br>10b = 4 faults<br>11b = 6 faults | |
| R/W | 15h | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 16h | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 17h | 0000 0000b | User Byte | — | | | | | | | |
| R | 18h | 1111 1111b | TACH 1 Count MSB | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ |
| R | 19h | 1110 0000b | TACH 1 Count LSB | $2^2$ | $2^1$ | $2^0$ | 0 | 0 | 0 | 0 | 0 |
| R | 1Ah | 1111 1111b | TACH 2 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 1Bh | 1110 0000b | TACH 2 Count LSB | | | | | | | | |
| R | 1Ch | 1111 1111b | TACH 3 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 1Dh | 1110 0000b | TACH 3 Count LSB | | | | | | | | |
| R | 1Eh | 1111 1111b | TACH 4 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 1Fh | 1110 0000b | TACH 4 Count LSB | | | | | | | | |
| R | 20h | 1111 1111b | TACH 5 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 21h | 1110 0000b | TACH 5 Count LSB | | | | | | | | |
| R | 22h | 1111 1111b | TACH 6 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 23h | 1110 0000b | TACH 6 Count LSB | | | | | | | | |
| R | 24h | 1111 1111b | TACH 7 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 25h | 1110 0000b | TACH 7 Count LSB | | | | | | | | |

***Register Map (continued)***

| R/W | REGISTER | POR STATE | FUNCTION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 26h | 1111 1111b | TACH 8 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 27h | 1110 0000b | TACH 8 Count LSB | | | | | | | | |
| R | 28h | 1111 1111b | TACH 9 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 29h | 1110 0000b | TACH 9 Count LSB | | | | | | | | |
| R | 2Ah | 1111 1111b | TACH 10 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 2Bh | 1110 0000b | TACH 10 Count LSB | | | | | | | | |
| R | 2Ch | 1111 1111b | TACH 11 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 2Dh | 1110 0000b | TACH 11 Count LSB | | | | | | | | |
| R | 2Eh | 1111 1111b | TACH 12 Count MSB | Same as TACH 1 Count | | | | | | | |
| R | 2Fh | 1110 0000b | TACH 12 Count LSB | | | | | | | | |
| R | 30h | 0000 0000b | PWMOUT 1 Duty Cycle MSB | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ |
| R | 31h | 0000 0000b | PWMOUT 1 Duty Cycle LSB | $2^0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 32h | 0000 0000b | PWMOUT 2 Duty Cycle MSB | Same as PWMOUT 1 Duty Cycle | | | | | | | |
| R | 33h | 0000 0000b | PWMOUT 2 Duty Cycle LSB | | | | | | | | |
| R | 34h | 0000 0000b | PWMOUT 3 Duty Cycle MSB | Same as PWMOUT 1 Duty Cycle | | | | | | | |
| R | 35h | 0000 0000b | PWMOUT 3 Duty Cycle LSB | | | | | | | | |

## Register Map (continued)

| R/W | REGISTER | POR STATE | FUNCTION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 36h | 0000 0000b | PWMOUT 4 Duty Cycle MSB | Same as PWMOUT 1 Duty Cycle | | | | | | | |
| R | 37h | 0000 0000b | PWMOUT 4 Duty Cycle LSB | Same as PWMOUT 1 Duty Cycle | | | | | | | |
| R | 38h | 0000 0000b | PWMOUT 5 Duty Cycle MSB | Same as PWMOUT 1 Duty Cycle | | | | | | | |
| R | 39h | 0000 0000b | PWMOUT 5 Duty Cycle LSB | Same as PWMOUT 1 Duty Cycle | | | | | | | |
| R | 3Ah | 0000 0000b | PWMOUT 6 Duty Cycle MSB | Same as PWMOUT 1 Duty Cycle | | | | | | | |
| R | 3Bh | 0000 0000b | PWMOUT 6 Duty Cycle LSB | Same as PWMOUT 1 Duty Cycle | | | | | | | |
| R | 3Ch | 0000 0000b | RESERVED | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 3Dh | 0000 0000b | RESERVED | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 3Eh | 0000 0000b | RESERVED | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | 3Fh | 0000 0000b | RESERVED | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | 40h | PWM_START | PWMOUT1 Target Duty Cycle MSB | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ |
| R/W | 41h | PWM_START | PWMOUT1 Target Duty Cycle LSB | $2^0$ | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| R/W | 42h | PWM_START | PWMOUT2 Target Duty Cycle MSB | Same as PWMOUT 1 Target Duty Cycle | | | | | | | |
| R/W | 43h | PWM_START | PWMOUT2 Target Duty Cycle LSB | Same as PWMOUT 1 Target Duty Cycle | | | | | | | |
| R/W | 44h | PWM_START | PWMOUT3 Target Duty Cycle MSB | Same as PWMOUT 1 Target Duty Cycle | | | | | | | |
| R/W | 45h | PWM_START | PWMOUT3 Target Duty Cycle LSB | Same as PWMOUT 1 Target Duty Cycle | | | | | | | |

### Register Map (continued)

| R/W | REGISTER | POR STATE | FUNCTION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W | 46h | PWM_START | PWMOUT4 Target Duty Cycle MSB | Same as PWMOUT 1 Target Duty Cycle | | | | | | | |
| R/W | 47h | PWM_START | PWMOUT4 Target Duty Cycle LSB | | | | | | | | |
| R/W | 48h | PWM_START | PWMOUT5 Target Duty Cycle MSB | Same as PWMOUT 1 Target Duty Cycle | | | | | | | |
| R/W | 49h | PWM_START | PWMOUT5 Target Duty Cycle LSB | | | | | | | | |
| R/W | 4Ah | PWM_START | PWMOUT6 Target Duty Cycle MSB | Same as PWMOUT 1 Target Duty Cycle | | | | | | | |
| R/W | 4Bh | PWM_START | PWMOUT6 Target Duty Cycle LSB | | | | | | | | |
| R/W | 4Ch | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 4Dh | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 4Eh | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 4Fh | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 50h | 0011 1100b | TACH 1 Target Count MSB | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ |
| R/W | 51h | 0000 0000b | TACH 1 Target Count LSB | $2^2$ | $2^1$ | $2^0$ | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| R/W | 52h | 0011 1100b | TACH 2 Target Count MSB | Same as TACH 1 Target Count | | | | | | | |
| R/W | 53h | 0000 0000b | TACH 2 Target Count LSB | | | | | | | | |
| R/W | 54h | 0011 1100b | TACH 3 Target Count MSB | Same as TACH 1 Target Count | | | | | | | |
| R/W | 55h | 0000 0000b | TACH 3 Target Count LSB | | | | | | | | |

***Register Map (continued)***

| R/W | REGISTER | POR STATE | FUNCTION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W | 56h | 0011 1100b | TACH 4 Target Count MSB | Same as TACH 1 Target Count | | | | | | | |
| R/W | 57h | 0000 0000b | TACH 4 Target Count LSB | | | | | | | | |
| R/W | 58h | 0011 1100b | TACH 5 Target Count MSB | Same as TACH 1 Target Count | | | | | | | |
| R/W | 59h | 0000 0000b | TACH 5 Target Count LSB | | | | | | | | |
| R/W | 5Ah | 0011 1100b | TACH 6 Target Count MSB | Same as TACH 1 Target Count | | | | | | | |
| R/W | 5Bh | 0000 0000b | TACH 6 Target Count LSB | | | | | | | | |
| R/W | 5Ch | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 5Dh | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 5Eh | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 5Fh | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 60h | 0000 0000b | Window 1 | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| R/W | 61h | 0000 0000b | Window 2 | Same as Window 1 | | | | | | | |
| R/W | 62h | 0000 0000b | Window 3 | Same as Window 1 | | | | | | | |
| R/W | 63h | 0000 0000b | Window 4 | Same as Window 1 | | | | | | | |
| R/W | 64h | 0000 0000b | Window 5 | Same as Window 1 | | | | | | | |
| R/W | 65h | 0000 0000b | Window 6 | Same as Window 1 | | | | | | | |
| R/W | 66h | 0000 0000b | User Byte | — | | | | | | | |
| R/W | 67h | 0000 0000b | User Byte | — | | | | | | | |

*X = Input state at POR.*

X = Input state at POR.

### Global Configuration Register (00h)

| | |
|---|---|
| Power-On Value | 0010 0XX0b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 00h | $\overline{\text{Run}}$/ Standby | Reset | Bus Timeout | RESERVED | OSC | I²C Watchdog | I²C Watchdog Status |
| | BIT 7 | | | | | | BIT 0 |

| | |
|---|---|
| BIT 7 | **$\overline{\text{Run}}$/Standby:** Places the device in standby mode.<br>0 = Run<br>1 = Standby<br>Entering standby mode sets all PWM duty cycles to 0 and stops fan failure detection. However, driving the $\overline{\text{FULL\_SPEED}}$ input low forces all enabled PWMOUT outputs high (100% duty cycle) regardless of the state of the $\overline{\text{Run}}$ bit. |
| BIT 6 | **Reset:**<br>0 = Normal operation<br>1 = Reset all registers to POR value<br>This bit automatically resets itself and always returns a 0 when read. |
| BIT 5 | **$\overline{\text{Bus Timeout}}$:** I²C bus timeout.<br>0 = Enabled<br>1 = Disabled<br>The I²C interface resets if SDA is low for more than 35ms. |
| BIT 4 | **RESERVED** |
| BIT 3 | **Oscillator Selection:**<br>0 = Internal oscillator (default at power-on)<br>1 = External 32.768kHz crystal<br>Selects on-chip oscillator or external 32.768kHz crystal/ceramic resonator for TACH count and source for CLKOUT pin. Use crystal or ceramic resonator if higher accuracy is required. When switching from the internal oscillator to an external crystal, the device operates from the internal oscillator until the crystal oscillator has started up. If the crystal is damaged or the oscillator fails to start, the device continues to operate from the internal oscillator. |

<table>
<tr><td rowspan="6">BITS 2:1</td><td colspan="3">I²C Watchdog: When active, the watchdog monitors SDA and SCL for valid I²C transactions. If there are no valid transactions between the master and the device within the watchdog period, all fan PWM outputs go to 100%. If the watchdog times out and valid I²C transactions begin to occur again, operation resumes with the previous PWM value. The master can then program the PWM outputs, target TACH counts, or other functions in the normal manner. When the watchdog function is active, ensure that the master communicates to the device periodically, for example, reading a status register. The POR state is set by the state of the WD_START pin at power-up.</td></tr>
<tr><td>BITS 2:1</td><td>I²C WATCHDOG PERIOD (s)</td><td>POR CONDITION</td></tr>
<tr><td>00b</td><td>Inactive (no watchdog)</td><td>WD_START = GND</td></tr>
<tr><td>01b</td><td>5</td><td>—</td></tr>
<tr><td>10b</td><td>10</td><td>—</td></tr>
<tr><td>11b</td><td>30</td><td>WD_START = VCC</td></tr>
<tr><td>BIT 0</td><td colspan="3">I²C Watchdog Status:<br>0 = I²C transactions occurred within watchdog period<br>1 = Time between I²C transaction exceeds watchdog period<br>Clear this bit by writing a 0 to it.</td></tr>
</table>

### PWM Frequency Register (01h)

| | |
|---|---|
| Power-On Value | XXXX XXXXb |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| 01h | PWM4-PWM6 Frequency | PWM1-PWM3 Frequency |
|---|---|---|
| | BIT 7 | BIT 0 |

<table>
<tr><td rowspan="15">BITS 7:4</td><td colspan="3">PWM4-PWM6 Frequency: These bits select the PWM OUT frequency for PWMOUT4, PWMOUT5, and PWMOUT6 according to the following:</td></tr>
<tr><td>BITS 7:4</td><td>PWM OUPUT FREQUENCY</td><td>POR CONDITION</td></tr>
<tr><td>0000b</td><td>25Hz</td><td>—</td></tr>
<tr><td>0001b</td><td>30Hz</td><td>FREQ_START = GND</td></tr>
<tr><td>0010b</td><td>35Hz</td><td>—</td></tr>
<tr><td>0011b</td><td>100Hz</td><td>—</td></tr>
<tr><td>0100b</td><td>125Hz</td><td>—</td></tr>
<tr><td>0101b</td><td>149.7Hz</td><td>—</td></tr>
<tr><td>0110b</td><td>1.25kHz</td><td>—</td></tr>
<tr><td>0111b</td><td>1.47kHz</td><td>FREQ_START = Unconnected</td></tr>
<tr><td>1000b</td><td>3.57kHz</td><td>—</td></tr>
<tr><td>1001b</td><td>5kHz</td><td>—</td></tr>
<tr><td>1010b</td><td>12.5kHz</td><td>—</td></tr>
<tr><td>1011b</td><td>25kHz</td><td>FREQ_START = VCC</td></tr>
<tr><td colspan="3">The POR state is set by the state of the FREQ_START pin at power-up as shown.</td></tr>
<tr><td rowspan="15">BITS 3:0</td><td colspan="3">PWM1-PWM3 Frequency: These bits select the PWM OUT frequency for PWMOUT1, PWMOUT2, and PWMOUT3 according to the following:</td></tr>
<tr><td>BITS 7:4</td><td>PWM OUPUT FREQUENCY</td><td>POR CONDITION</td></tr>
<tr><td>0000b</td><td>25Hz</td><td>—</td></tr>
<tr><td>0001b</td><td>30Hz</td><td>FREQ_START = GND</td></tr>
<tr><td>0010b</td><td>35Hz</td><td>—</td></tr>
<tr><td>0011b</td><td>100Hz</td><td>—</td></tr>
<tr><td>0100b</td><td>125Hz</td><td>—</td></tr>
<tr><td>0101b</td><td>149.7Hz</td><td>—</td></tr>
<tr><td>0110b</td><td>1.25kHz</td><td>—</td></tr>
<tr><td>0111b</td><td>1.47kHz</td><td>FREQ_START = Unconnected</td></tr>
<tr><td>1000b</td><td>3.57kHz</td><td>—</td></tr>
<tr><td>1001b</td><td>5kHz</td><td>—</td></tr>
<tr><td>1010b</td><td>12.5kHz</td><td>—</td></tr>
<tr><td>1011b</td><td>25kHz</td><td>FREQ_START = VCC</td></tr>
<tr><td colspan="3">The POR state is set by the state of the FREQ_START pin at power-up as shown.</td></tr>
</table>

### Fan 1 Configuration Register (02h)
### Fan 2 Configuration Register (03h)
### Fan 3 Configuration Register (04h)
### Fan 4 Configuration Register (05h)
### Fan 5 Configuration Register (06h)
### Fan 6 Configuration Register (07h)

| | |
|---|---|
| Power-On Value | 0XX0 0000b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| 02h, 03h, 04h, 05h, 06h, 07h | Mode | Spin-Up | $\overline{\text{Control}}$/ Monitor | TACH Input Enable | $\overline{\text{TACH}}$/ Locked Rotor | Locked Rotor Polarity | $\overline{\text{PWM}}$/ TACH |
|---|---|---|---|---|---|---|---|
| | BIT 7 | | | | | | BIT 0 |

| | |
|---|---|
| BIT 7 | **Mode:** RPM/PWM mode select.<br>0 = PWM mode. PWM duty cycle is set by the value in the associated PWMOUT Target Duty Cycle register.<br>1 = RPM mode. The PWM duty cycle is adjusted to produce the TACH count value in the associated TACH Target Count register.<br>When changing from PWM to RPM mode, if the current RPM value is different from the value selected in the TACH Target Count register, the PWM duty cycle starts from the current value and increment/decrements toward the desired value at the selected duty cycle rate-of-change. |
| BITS 6:5 | **Spin-Up:** When spin-up is selected and the fan is started with a target PWM duty cycle less than 100%, the device produces 100% duty cycle until two tachometer pulses have been detected. A maximum spin-up time is also selectable to ensure that the spin-up time is not excessive. After two tachometer pulses have been detected, or the spin-up has timed out, the duty cycle goes to the value in the PWMOUT Target Duty Cycle register. The POR state is set by the state of the SPIN_START pin at power-up. |

| BITS 6:5 | SPIN-UP BEHAVIOR | POR CONDITION |
|---|---|---|
| 00b | No spin-up | SPIN_START = GND |
| 01b | Spin-up until two tachometer pulses or 0.5s (max) | SPIN_START = Unconnected |
| 10b | Spin-up until two tachometer pulses or 1s (max) | SPIN_START = VCC |
| 11b | Spin-up until two tachometer pulses or 2s (max) | — |

| | |
|---|---|
| BIT 4 | **$\overline{\text{Control}}$/Monitor:**<br>0 = Control fan speed.<br>1 = Monitor only. Associated duty cycle = 0% regardless of other settings; monitor associated TACH or locked rotor if enabled by bit 3. |

| | |
|---|---|
| BIT 3 | **TACH Input Enable:** Enables associated TACH input function and fan fault detection (automatically enabled in RPM mode).<br>0 = Disabled. When disabled and TACH input is not used, bits 1 and 2 are ignored.<br>1 = Enabled |
| BIT 2 | **$\overline{\text{TACH}}$/Locked Rotor:** Selects TACH input function as TACH count or locked rotor. In locked rotor mode, assertion of the associated TACH input indicates that the fan has stopped.<br>0 = TACH count<br>1 = Locked rotor |
| BIT 1 | **Locked Rotor Polarity:**<br>0 = Low locked rotor. Associated TACH input low in locked rotor mode indicates fan is stopped.<br>1 = High locked rotor. Associated TACH input high in locked rotor mode indicates fan is stopped. |
| BIT 0 | **$\overline{\text{PWM}}$/TACH:** When set to 0, the associated PWMOUT produces a PWM waveform for control of fan speed. When set to 1, PWMOUT becomes a TACH input whose channel number is equal to the number of the PWMOUT channel plus six. |

### Fan 1 Dynamics Register (08h)
### Fan 2 Dynamics Register (09h)
### Fan 3 Dynamics Register (0Ah)
### Fan 4 Dynamics Register (0Bh)
### Fan 5 Dynamics Register (0Ch)
### Fan 6 Dynamics Register (0Dh)

| | |
|---|---|
| Power-On Value | 0100 1100b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh | Speed Range | PWM Rate-of-Change | Asymmetric Rate of Change | Reserved |
|---|---|---|---|---|
| | BIT 7 | | | BIT 0 |

BITS 7:5

**Speed Range:** The device determines fan speed by counting the number of internal 8192Hz ($f_{TOSC}/4$) clock cycles (using an 11-bit counter) during one or more fan tachometer periods. Three bits set the nominal RPM range for the fan, as shown in the table below. For example, a setting of 010b causes the device to count the number of 8192Hz ($f_{TOSC}/4$) clock cycles that occur during four complete tachometer periods. If the fan has a nominal speed of 2000 RPM and two tachometer pulses per revolution, one tachometer period is nominally 15ms, and four tachometer periods are 60ms. With an 8192Hz ($f_{TOSC}/4$) clock, the TACH count is therefore equal to 491. With a fan speed of 1/3 the nominal value, the count is 1474. If the fan's nominal speed is 1000 RPM, the full-speed TACH count is 983. At 1/3 the nominal speed, there are 2948 clock cycles in four tachometer periods. This is greater than the maximum 11-bit count of 2047, so four tachometer periods is too many for this fan; a setting of 001 (two clock cycles) is recommended instead.

The table below shows the full-speed tachometer counts for several combinations of nominal fan speeds and bits 7:5 settings. The shaded combinations provide the best results. Nonshaded combinations should generally be avoided. When setting bits 7:5, the goal is to obtain the highest tachometer count without exceeding the maximum count of 2047 when the fan is at the minimum speed of interest. For example, if the minimum speed of interest is 1/3 of full speed, the maximum tachometer count is three times the value shown in the table.

| BITS 7:5 | NUMBER OF TACH PERIODS COUNTED | RPM | | | | | |
|---|---|---|---|---|---|---|---|
| | | 500 | 1000 | 2000 | 4000 | 8000 | 16000 |
| 000b | 1 | 491 (60ms) | 245 (30ms) | 122 (15ms) | 61 (7.5ms) | 30 (3.75ms) | 15 (1.875ms) |
| 001b | 2 | 983 (120ms) | 491 (60ms) | 245 (30ms) | 122 (15ms) | 61 (7.5ms) | 30 (3.75ms) |
| 010b (default) | 4 | 1966 (240ms) | 983 (120ms) | 491 (60ms) | 245 (30ms) | 122 (15ms) | 61 (7.5ms) |
| 011b | 8 | 2047 (480ms) | 1966 (240ms) | 983 (120ms) | 491 (60ms) | 245 (30ms) | 122 (15ms) |
| 100b | 16 | 2047 (960ms) | 2047 (480ms) | 1966 (240ms) | 983 (120ms) | 491 (60ms) | 245 (30ms) |
| 101b, 110b, 111b | 32 | 2047 (1920ms) | 2047 (960ms) | 2047 (480ms) | 1966 (240ms) | 983 (120ms) | 491 (60ms) |

| | |
|---|---|
| BITS 4:2 | **PWM Rate-of-Change:** PWM duty cycle rate of change. The PWM duty cycle at the associated PWMOUT outputs varies from 0 to full scale in 512 increments. The rate-of-change bits determine the time interval between duty cycle output increments/decrements. Regardless of the settings, there are a few cases for which the rate-of-change is always 0:<br>In RPM mode, when a TACH target count of 2047 (7FFh) is selected, the duty cycle immediately goes to 0%. A full-scale target count is assumed to mean that the intent is to shut down the fan, and going directly to 0% avoids the possibility of loss of control-loop feedback at high TACH counts. If a slow-speed decrease toward 0% is desired, select a TACH target count at the slowest practical value for the fan. Once that count has been reached, selecting a count of 2047 (7FF) then takes the drive immediately to 0%.<br>In PWM mode, when a target duty cycle of 0% is selected, the duty cycle goes to 0%. Again, it is assumed that the intent is to shut down the fan. If a slow-speed decrease toward 0% is desired, a target duty cycle of the slowest practical value for the fan in question should be chosen. Once that duty cycle has been reached, selecting a target value of 0% then takes the drive immediately to 0%.<br>When the current duty cycle is 0% in PWM mode, selecting a new target duty cycle immediately takes the duty cycle to that value. The fan spins up first if spin-up is enabled. When the current duty cycle is 0% in RPM mode, selecting a new TACH target count that is less than 2047 (7FFh) immediately takes the duty cycle to the value in the PWMOUT Target Duty Cycle register. From this value, the duty cycle increments as needed to achieve the desired TACH target count. The fan spins up first if spin-up is enabled. |

| **BITS 4:2** | **TIME BETWEEN DUTY CYCLE INCREMENTS (ms) RPM** | | **TIME FROM 33% TO 100% (s)** | |
|---|---|---|---|---|
| | **PWM** | **RPM** | **PWM** | **RPM** |
| 000b | 0 | 0.9765 | 0 | 0.33 |
| 001b | 1.953125 | | 0.67 | |
| 010b | 3.90625 | | 1.34 | |
| 011b (default) | 7.8125 | | 2.7 | |
| 100b | 15.625 | | 5.3 | |
| 101b | 31.25 | | 10.7 | |
| 110b | 62.5 | | 21.4 | |
| 111b | 125 | | 42.8 | |

| | |
|---|---|
| BIT 1 | **Asymmetric Rate of Change:**<br>0 = Same rate of change whether duty cycle is increasing or decreasing.<br>1 = Rate of change when duty cycle is decreasing is half the rate when increasing. |
| BIT 0 | **RESERVED** |

### User Byte Register (0Eh–0Fh)
### User Byte Register (15h–17h)
### User Byte Register (4Ch–4Fh)
### User Byte Register (5Ch–5Fh)
### User Byte Register (66h–67h)

| | |
|---|---|
| Power-On Value | 0000 0000b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | BIT 7 | | | | | | | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0Eh, 0Fh, 15h, 16h, 17h, 4Ch, 4Dh, 4Eh, 4Fh, 5Ch, 5Dh, 5Eh, 5Fh, 66h, 67h | — | — | — | — | — | — | — | — |

General-purpose volatile bits. These bits have no affect on the device operation.

### Fan Fault Status 2 Register (10h)

| | |
|---|---|
| Power-On Value | 0000 0000b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | BIT 7 | | | | | | | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 10h | RESERVED | RESERVED | Fan 12 Fault | Fan 11 Fault | Fan 10 Fault | Fan 9 Fault | Fan 8 Fault | Fan 7 Fault |

| | |
|---|---|
| BITS 7:6 | **RESERVED** |
| BITS 5:0 | **Fan [12:7] Fault:** This register applies only to PWMOUTs that are being used as TACH inputs. The associated fan experienced faults as defined in the *Fan Failure* section. When a fan fault is detected, the associated fault bit is set to 1. The fault bits latch until they are cleared by writing a PWM target duty cycle or TACH target count to the associate fan's control register, thus allowing short-term faults to be identified. |

### Fan Fault Status 1 Register (11h)

| | |
|---|---|
| Power-On Value | 0000 0000b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 11h | RESERVED | RESERVED | Fan 6 Fault | Fan 5 Fault | Fan 4 Fault | Fan 3 Fault | Fan 2 Fault | Fan 1 Fault |
| | BIT 7 | | | | | | | BIT 0 |

| | |
|---|---|
| BITS 7:6 | **RESERVED** |
| BITS 5:0 | **Fan [6:1] Fault:** The associated fan experienced faults as defined in the *Fan Failure* section. When a fan fault is detected, the associated fault bit is set to 1. The fault bits latch until they are cleared by writing a PWM target duty cycle or TACH target count to the fan's control register, thus allowing short-term faults to be identified. |

### Fan Fault Mask 2 Register (12h)

| | |
|---|---|
| Power-On Value | 0011 1111 b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 12h | RESERVED | RESERVED | Fan 12 Mask | Fan 11 Mask | Fan 10 Mask | Fan 9 Mask | Fan 8 Mask | Fan 7 Mask |
| | BIT 7 | | | | | | | BIT0 |

| | |
|---|---|
| BITS 7:6 | **RESERVED** |
| BITS 5:0 | **Fan [12:7] Mask:** This register applies only to PWMOUTs that are being used as TACH inputs. These bits mask faults on selected fans from asserting the $\overline{\text{FAN\_FAIL}}$ output. Faults are still indicated by the fault status bits:<br>0 = Not masked<br>1 = Masked<br>When a fan fails, the PWM behavior is controlled by the Failed Fan Options register. |

### Fan Fault Mask 1 Register (13h)

| | |
|---|---|
| Power-On Value | 0011 1111b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 13h | RESERVED | RESERVED | Fan 6 Mask | Fan 5 Mask | Fan 4 Mask | Fan 3 Mask | Fan 2 Mask | Fan 1 Mask |
| | BIT 7 | | | | | | | BIT0 |

| | |
|---|---|
| BITS 7:6 | **RESERVED** |
| BITS 5:0 | **Fan [6:1] Mask:** These bits mask faults on selected fans from asserting the $\overline{\text{FAN\_FAIL}}$ output. Faults are still indicated by the fault status bits:<br>0 = Not masked<br>1 = Masked<br>When a fan fails, the PWM behavior is controlled by the Failed Fan Options register. |

### Failed Fan Options/Sequential Start Register (14h)

| | |
|---|---|
| Power-On Value | 0100 0101b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | | | | |
|---|---|---|---|---|
| 14h | Sequential Start Delay | RESERVED | Failed Fan Options | Fan Fault Queue |
| | BIT 7 | | | BIT 0 |

| | | |
|---|---|---|
| BITS 7:5 | **Sequential Start Delay:** Note that faults are not monitored until the channel is activated after its associated start delay. These bits select the time delay between fan activations according to the following: | |
| | **BITS 7:5** | **TIME BETWEEN SEQUENTIAL FAN STARTUP** |
| | 000b | 0s |
| | 001b | 250ms |
| | 010b (default) | 500ms |
| | 011b | 1s |
| | 100b | 2s |
| | 101b<br>110b<br>111b | 4s |
| BIT 4 | **RESERVED** | |
| BITS 3:2 | **Failed Fan Options:** These bits select the behavior following a fan failure according to the following: | |
| | **BITS 3:2** | **SET DUTY CYCLE ON FAILURE** |
| | 00b | 0% |
| | 01b | Continue current PWM or RPM mode operation |
| | 10b | 100% on failed fan |
| | 11b | All fans to 100% on any unmasked fan failure |
| BITS 1:0 | **Fan Fault Queue:** These bits select the number of consecutive fault detections that are required to decide that the fan has failed according to the following: | |
| | **BITS 1:0** | **NUMBER OF QUALIFIED FAULTS** |
| | 00b | 1 |
| | 01b | 2 |
| | 10b | 4 |
| | 11b | 6 |
| | When the selected number of fault detections has occurred, the $\overline{\text{FAN\_FAIL}}$ output asserts (if fault detection is not masked for the fan). **Note:** Fan fault queue has no effect on the locked rotor fan-failure detection. | |

**TACH 1 Count Registers (18h–19h)**
**TACH 2 Count Registers (1Ah–1Bh)**
**TACH 3 Count Registers (1Ch–1Dh)**
**TACH 4 Count Registers (1Eh–1Fh)**
**TACH 5 Count Registers (20h–21h)**
**TACH 6 Count Registers (22h–23h)**
**TACH 7 Count Registers (24h–25h)**
**TACH 8 Count Registers (26h–27h)**
**TACH 9 Count Registers (28h–29h)**
**TACH 10 Count Registers (2Ah–2Bh)**
**TACH 11 Count Registers (2Ch–2Dh)**
**TACH 12 Count Registers (2Eh–2Fh)**

| | |
|---|---|
| Power-On Value | 1111 1111b (MSB)<br>1110 0000b (LSB) |
| Read Access | All |
| Write Access | N/A |
| Memory Type | Volatile |

| | BIT 7 | | | | | | | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 18h, 1Ah, 1Ch, 1Eh, 20h, 22h, 24h, 26h, 28h, 2Ah, 2Ch, 2Eh | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ |
| 19h, 1Bh, 1Dh, 1Fh, 21h, 23h, 25h, 27h, 29h, 2Bh, 2Dh, 2Fh | $2^2$ | $2^1$ | $2^0$ | 0 | 0 | 0 | 0 | 0 |

Indicates the associated number of 8192Hz ($f_{TOSC}$/4) clock pulses counted during the counting period. The TACH Count register consists of 11 bits, left-justified, contained in 2 bytes. The lower 5 bits always return zeros. To minimize noise from spurious tachometer transitions, pulses less that $t_{TACHMIN}$ are ignored. The TACH 7 Count to TACH 12 Count registers apply only to PWMOUTs that are being used as TACH inputs.

**PWMOUT 1 Duty Cycle (30h–31h)**
**PWMOUT 2 Duty Cycle (32h–33h)**
**PWMOUT 3 Duty Cycle (34h–35h)**
**PWMOUT 4 Duty Cycle (36h–37h)**
**PWMOUT 5 Duty Cycle (38h–39h)**
**PWMOUT 6 Duty Cycle (3Ah–3Bh)**

| | |
|---|---|
| Power-On Value | 0000 0000b (MSB)<br>0000 0000b (LSB) |
| Read Access | All |
| Write Access | N/A |
| Memory Type | Volatile |

| | BIT 7 | | | | | | | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 30h, 32h, 34h, 36h, 38h, 3Ah | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ |
| 31h, 33h, 35h, 37h, 39h, 3Bh | $2^0$ | 0 | 0 | 0 | 0 | 0 | 0 | FS |

This is a 9-bit left-justified value that ranges from 0 to 511 and is contained in 2 bytes. This register shows the actual PWM duty cycle for the associate PWM output. When the value is 511 (decimal), the duty cycle is 100%. The 6:1 bits always return zeros. Register does not apply when associated PWMOUTs are being used as TACH inputs. The register value is converted to the duty cycle at the fan as follows:

| **BITS 15:7** | | **PWM DUTY CYCLE (%)** |
|---|---|---|
| **DECIMAL** | **HEX** | |
| 0 | 000h | 0 |
| 200 | 0C8h | 39 |
| 300 | 12Ch | 59 |
| 400 | 190h | 78 |
| 480 | 1E0h | 94 |
| 511 | 1FFh | 100 |

When duty cycle reaches 100%, bit 0 is set to a 1.

**PWMOUT 1 Target Duty Cycle (40h–41h)**
**PWMOUT 2 Target Duty Cycle (42h–43h)**
**PWMOUT 3 Target Duty Cycle (44h–45h)**
**PWMOUT 4 Target Duty Cycle (46h–47h)**
**PWMOUT 5 Target Duty Cycle (48h–49h)**
**PWMOUT 6 Target Duty Cycle (4Ah–4Bh)**

| | |
|---|---|
| Power-On Value | XXXX XXXXb (MSB)<br>X000 0000b (LSB) |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | BIT 7 | | | | | | | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 40h, 42h, 44h, 46h, 48h, 4Ah | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ |
| 41h, 43h, 45h, 47h, 49h, 4Bh | $2^0$ | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |

This is a 9-bit left-justified value that ranges from 0 to 511 and is contained in 2 bytes.
In PWM mode, write the desired PWM duty cycle to these two registers. The device then increments the duty cycle to this value at a rate determined by the PWM duty cycle rate-of-change bits.
In RPM mode, the value contained in this register is the duty cycle at PWMOUT immediately after spin-up or after changing the TACH target count from 2047 (7FF) to any value lower than 2047 (7FF). For example, if the fan is currently stopped with spin-up disabled, and a new TACH target count corresponding to 60% of the full-scale fan speed is to be selected, the duty cycle can be programmed to immediately go to 60% when the new TACH target count is selected, and then close the RPM control loop starting from that duty cycle. The register value is converted to the duty cycle at the fan as follows:

| **BITS 15:7** | | **PWM DUTY CYCLE (%)** |
|---|---|---|
| **DECIMAL** | **HEX** | |
| 0 | 000h | 0 |
| 200 | 0C8h | 39 |
| 300 | 12Ch | 59 |
| 400 | 190h | 78 |
| 480 | 1E0h | 94 |
| 511 | 1FFh | 100 |

The value of the PWMOUT target duty cycle at POR depends on the state of the PWM_START0 and PWM_START1 inputs as follows:

| **POR CONDITION** | | |
|---|---|---|
| **PWM_START0** | **PWM_START1** | **PWM DUTY CYCLE (%)** |
| GND | GND | 0 |
| GND | Unconnected | 30 |
| GND | $V_{CC}$ | 40 |
| Unconnected | GND | 50 |
| Unconnected | $V_{CC}$ | 60 |
| $V_{CC}$ | GND | 75 |
| $V_{CC}$ | $V_{CC}$ | 100 |

### TACH 1 Target Count (50h–51h)
### TACH 2 Target Count (52h–53h)
### TACH 3 Target Count (54h–55h)
### TACH 4 Target Count (56h–57h)
### TACH 5 Target Count (58h–59h)
### TACH 6 Target Count (5Ah–5Bh)

| | |
|---|---|
| Power-On Value | 0011 1100b (MSB)<br>0000 0000b (LSB) |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | BIT 7 | | | | | | | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 50h, 52h, 54h, 56h, 58h, 5Ah | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ |
| 51h, 53h, 55h, 57h, 59h, 5Bh | $2^2$ | $2^1$ | $2^0$ | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |

This is an 11-bit left-justified value that is contained in 2 bytes. It indicates the desired number of 8192Hz ($f_{TOSC}/4$) clock pulses counted during the counting period.

In RPM mode, write the desired tachometer count to this register. The device then adjusts the associated PWM duty cycle to achieve this tachometer count.

In PWM mode, this register is not used as part of the fan control algorithm. In both PWM and RPM modes, this register is used to determine fan faults. See the Fan Faults register description for details.

When changing from PWM mode to RPM mode, best results are obtained by loading this register with the current TACH count before changing to RPM mode. The TACH target count for a given RPM is obtained by the following equation:

$$\text{TACH Count} = \frac{60}{NP \times RPM} \times SR \times 8192$$

where:

NP = number of TACH pulse per revolution

SR = 1, 2, 4, 8, 16, 32 (see the Speed Range bit information in the associated Fan Dynamics register)

### Window 1 Register (60h)
### Window 2 Register (61h)
### Window 3 Register (62h)
### Window 4 Register (63h)
### Window 5 Register (64h)
### Window 6 Register (65h)

| | |
|---|---|
| Power-On Value | 0000 0000b |
| Read Access | All |
| Write Access | All |
| Memory Type | Volatile |

| | BIT 7 | | | | | | | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 60h, 61h, 62h, 63h, 64h, 65h | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |

When the fan's speed is near the target speed in RPM mode—that is, when the TACH count is near the corresponding TACH target count—the control loop dynamics can often be improved by slowing the rate of change of the PWM duty cycle. This operates as follows: First, set a value for the count "window" and store it in the appropriate window register. In RPM mode, calculate the difference between the current TACH count and the target TACH count. If the absolute value of this difference is less than the value in the window register, then the update rate of the PWM duty cycle is slowed to 1 LSB per second. When the current TACH count falls outside of the window, the duty cycle rate of change reverts to the selected value. **Note:** When operating in PWM mode, the window value is typically set to 0.

## I²C Serial Interface Description

### I²C Definitions

The following terminology is commonly used to describe I²C data transfers. See the timing diagram (Figure 1) and the *I²C AC Electrical Characteristics* table for additional information.

**Master Device:** The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

**Slave Devices:** Slave devices send and receive data at the master's request.

**Bus Idle or Not Busy:** Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

**START Condition:** A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

**STOP Condition:** A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

**Repeated START condition:** The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

**Bit Write:** Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

**Bit Read:** At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

**Acknowledgement (ACK and NACK):** An acknowledgement (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one (done by releasing SDA) during the 9th bit. The timing (Figure 1) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

**Byte Write:** A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

**Byte Read:** A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

**Slave Address Byte:** Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. See the *Slave Address Byte and Address Pins* section for details on the MAX31790's slave address.

If an incorrect (nonmatching) slave address is written, the MAX31790 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

**Memory Address:** During an I²C write operation to the MAX31790, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

### I²C Communication

See Figure 8 for I²C communication examples.

**Writing a Single Byte to a Slave:** The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. The master must read the slave's acknowledgement during all byte write operations.

**Reading a Single Byte from a Slave:** Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ =1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

**Manipulating the Address Counter for Reads:** A dummy write cycle can be used to force the address counter to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. Recall that the master must NACK the last byte to inform the slave that no additional bytes are to be read.

**Reading Multiple Bytes from a Slave:** The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and generates a STOP condition.

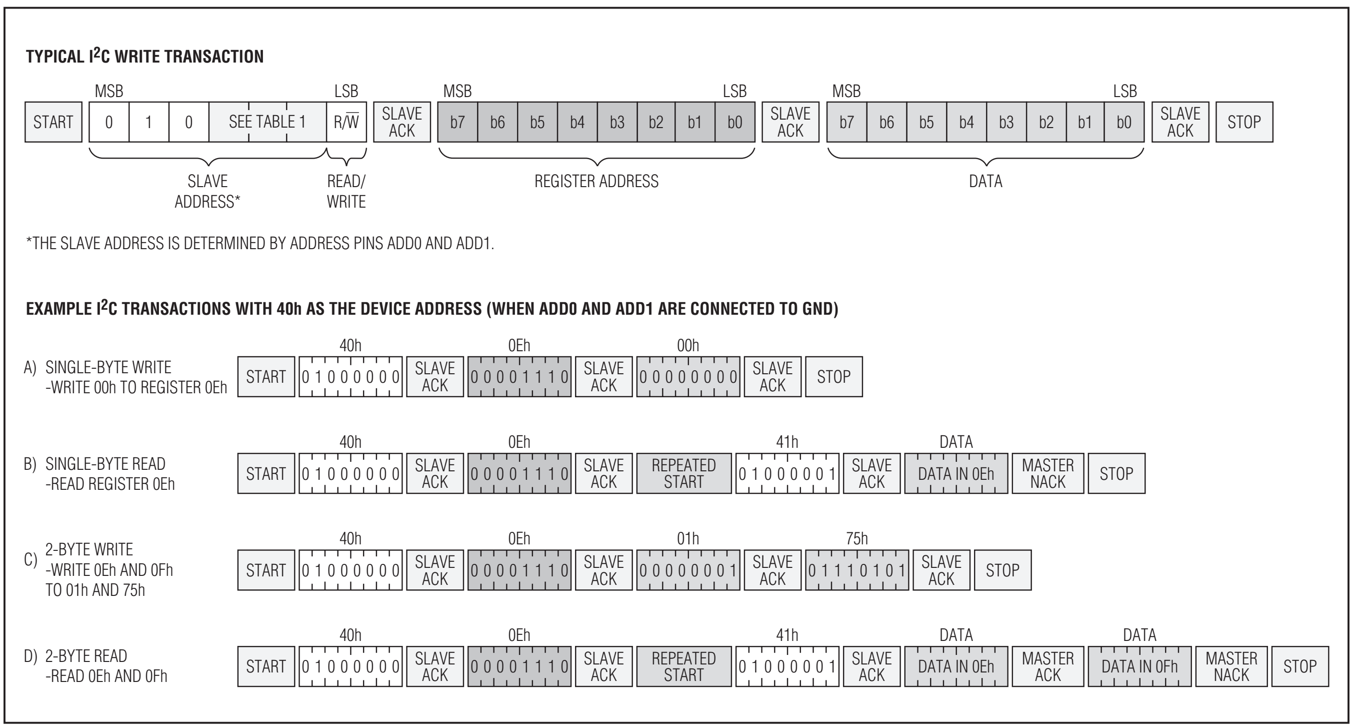



*Figure 8. I²C Communication Examples*

## Applications Information

### Controlling 4-Wire Fans (PWM Mode)

**Initial Settings:**

- Begin with the POR settings.
- Write the desired number of tachometer periods to be counted in the Speed Range bits (7:5 of the corresponding Fan Dynamics register).
- Write the maximum allowable tachometer count to the corresponding TACH Target Count register. Tachometer counts greater than this value results in a fan fault detection. Choose a value that is not encountered during normal operation, accounting for normal fan speed tolerances.
- Set the TACH Input Enable bit in the corresponding Fan Configuration register to 1. **Note:** This bit can be set after the fan has been started, if desired. If the bit is set before writing a PWMOUT target duty cycle, the duty cycle should be set immediately after enabling the TACH input to avoid failure detection before the fan has started spinning.

**Starting the Fan:**

- Write the desired duty cycle value to the corresponding PWMOUT Target Duty Cycle register.

**Changing Speeds:**

- Write the new desired duty-cycle value to the corresponding PWMOUT Target Duty Cycle register.

**Stopping the Fan:**

- Write a duty cycle value of 0% to the PWMOUT Target Duty Cycle register.
- If a gradual decrease in fan speed is desired, write the lowest duty cycle at which the fan can reliably operate. When the duty cycle reaches that value, write 0% to the PWMOUT Target Duty Cycle register.

### Controlling 4-Wire Fans (RPM Mode)

Begin as in PWM mode and start the fan.

**Changing from PWM Mode to RPM Mode:**

- Write the desired tachometer count to the corresponding TACH Target Count registers.
- Set bit 7 of the corresponding Fan Configuration register to 1. This selects RPM mode. The fan goes to the selected TACH target count.

**Changing Speeds:**

- Write the desired tachometer count to the corresponding TACH Target Count register.

**Stopping the Fan:**

- Set the TACH target count value to full scale. The PWM duty cycle immediately goes to 0%.

**Or:**

- Write the current duty cycle into the corresponding PWMOUT Target Duty Cycle register.
- Write a value greater than the current tachometer count into the TACH Target Count register.
- Write a 0 to bit 7 of the corresponding Fan Configuration register. This selects PWM mode.
- Write a duty cycle value of 0% to the PWMOUT Target Duty Cycle register.
- If a gradual decrease in fan speed is desired, write the lowest duty cycle at which the fan can reliably operate. When the duty cycle reaches that value, write 0 to the PWMOUT Target Duty Cycle register.

### Controlling 2-Wire and 3-Wire Fans

Although the device is optimized for use with fans that have speed-control inputs (generally referred to as 4-wire fans), it can also be used with fans that have no speed-control inputs. When a fan has no speed-control input, its speed can be controlled by modulating the fan's power-supply voltage. One approach is shown in Figure 9, where the PWM output of the fan is lowpass filtered and converted to a variable DC voltage that powers the fan. The highest available PWM frequency should be used. This approach works well with a wide variety of fans. Because the fan's supply current must pass through the MOSFET, this approach is best with lower power fans that use on the order of 200mA or less supply current.

For higher power fans, more efficient DC drive can be generated using a low-cost DC-DC converter. A DC-DC converter can be used to efficiently transform the device's PWMOUT signal into a variable power supply for the fan, as shown in Figure 10.

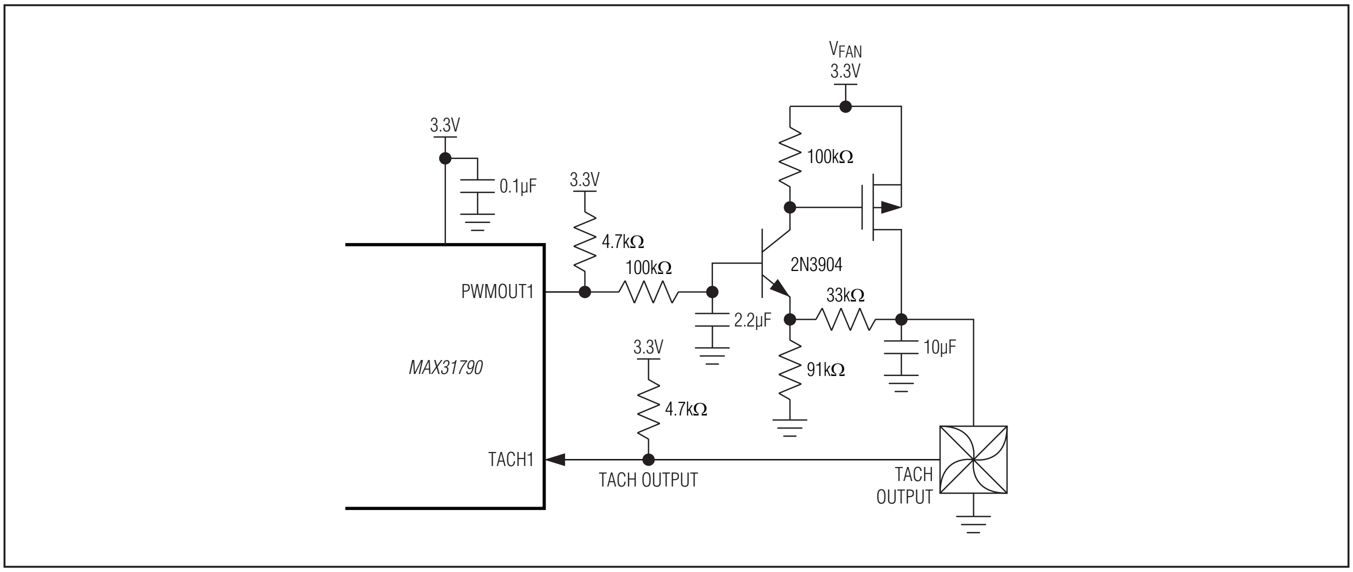



*Figure 9. High-Side Linear Drive Circuit for 2-Wire or 3-Wire Fans*

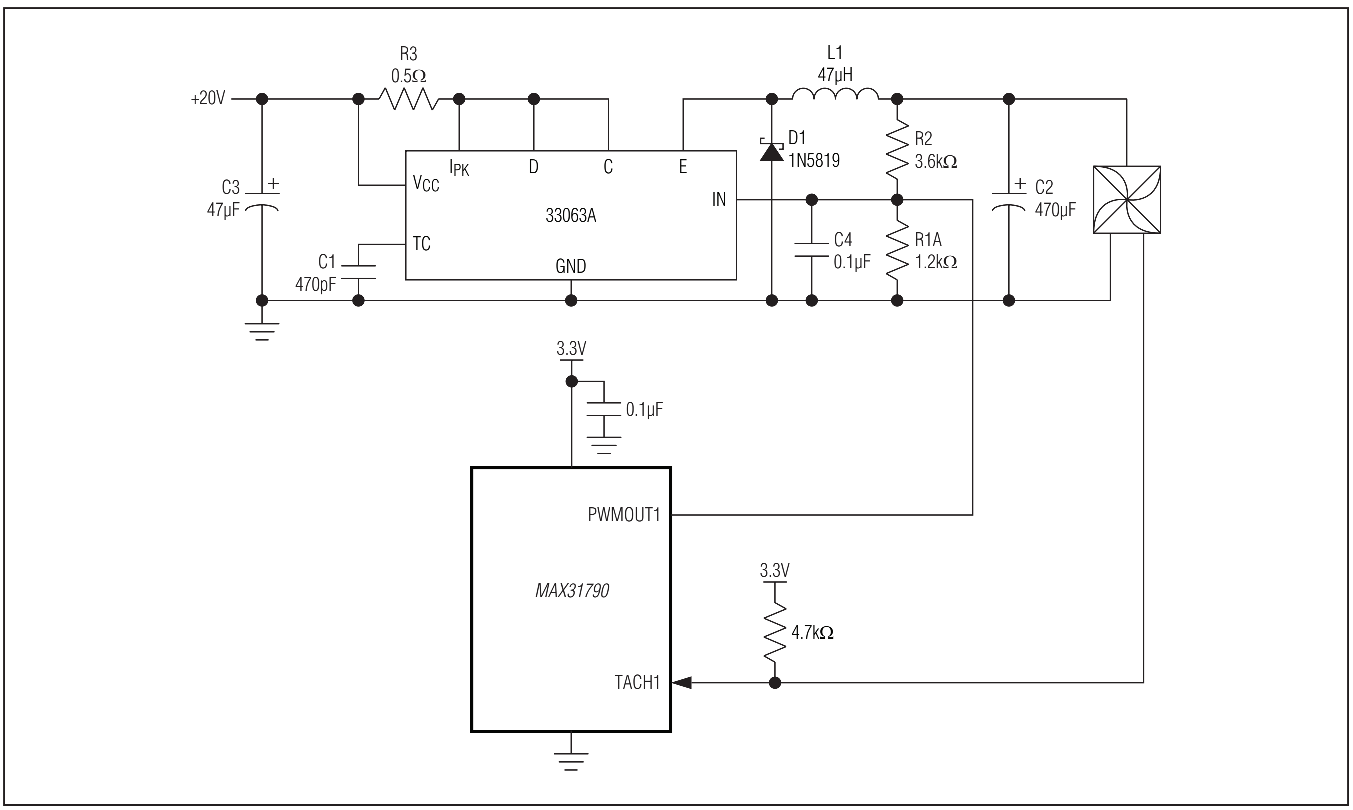



*Figure 10. Using a Low-Cost DC-DC Converter to Efficiently Transform PWMOUT Signal Into Variable Power Supply for the Fan*

A simpler approach to driving a 2-wire or 3-wire fan, although with important limitations, is to modulate the fan's power supply with the PWM signal. In this case, a low PWM frequency (typically in the 30Hz range) is used to drive the gate of an n-channel MOSFET, which provides the connection between the fan and the power supply ground, as shown in Figure 11. There are three important disadvantages to this approach. First, the rapid application and removal of the supply voltage when modulated at a 30Hz rate causes an audible increase in fan noise. Second, some fan vendors recommend against modulating the power supply with a PWM output because of reliability concerns. Check with your fan vendor to confirm that this approach is compatible with the fan you plan to use. Third, when using a 3-wire fan, the TACH signal is modulated by the PWM signal, making the TACH signal difficult to use for closed-loop speed control.

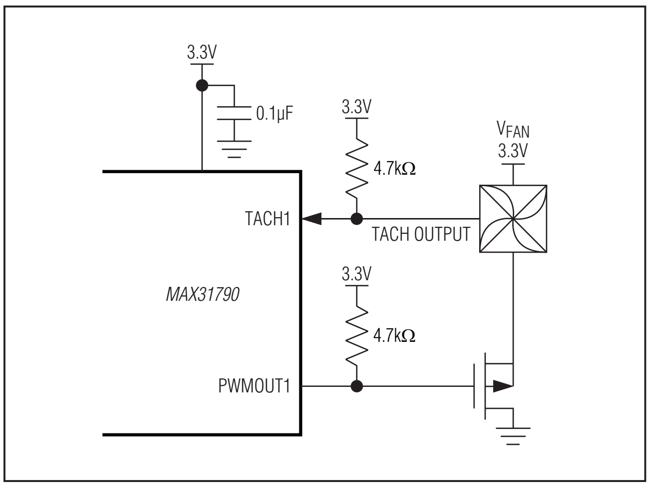



*Figure 11. Controlling the Speed of a 2-/3-Wire Fan by Pulse-Width Modulating the Fan's Power-Supply Voltage*

### *Power-Supply Decoupling*

To achieve the best results when using the MAX31790, decouple the power supply with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high frequency response for decoupling applications.

### *Layout Considerations*

The crystal should be placed very close to the device to minimize excessive loading due to parasitic capacitances. Care should also be taken to minimize loading on pins that could be left unconnected as a programming option (SPIN_START, PWM_START0, PWM_START1, FREQ_START). Coupling on inputs due to clocks should be minimized.

## *Ordering Information*

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX31790ATI+ | -40°C to +125°C | 28 TQFN-EP* |
| MAX31790ATI+T | -40°C to +125°C | 28 TQFN-EP* |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*
*T = Tape and reel.*
**EP = Exposed pad.*

## *Packaging Information*

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 28 TQFN-EP | T2844+1 | **21-0139** | **90-0035** |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 12/12 | Initial release | — |

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