700MHz – 1050MHz High Linearity Direct Quadrature Modulator

FEATURES

- **Frequency Range: 700MHz to 1050MHz**
- **High OIP3: +22.9dBm at 850MHz**
- **Low Output Noise Floor at 5MHz Offset:**
  No RF: –160.3dBm/Hz
  P_{OUT} = 4dBm: –154dBm/Hz
- **3-Ch CDMA2000 ACPR: –71.4dBc at 850MHz**
- **Integrated LO Buffer and LO Quadrature Phase Generator**
- **50Ω AC-Coupled Single-Ended LO and RF Ports**
- **50Ω DC Interface to Baseband Inputs**
- **Low Carrier Leakage: –43dBm at 850MHz**
- **High Image Rejection: –46dBc at 850MHz**
- 16-Lead 4mm × 4mm QFN Package

APPLICATIONS

- Infrastructure Tx for Cellular Bands
- Image Reject Up-Converters for Cellular Bands
- Low-Noise Variable Phase-Shifter for 700MHz to 1050MHz Local Oscillator Signals
- RFID Reader

DESCRIPTION

The LT®5568 is a direct I/Q modulator designed for high performance wireless applications, including wireless infrastructure. It allows direct modulation of an RF signal using differential baseband I and Q signals. It supports PHS, GSM, EDGE, TD-SCDMA, CDMA, CDMA2000, W-CDMA, and other systems. It may also be configured as an image reject upconverting mixer, by applying 90° phase-shifted signals to the I and Q inputs. The I/Q baseband inputs consist of voltage-to-current converters that in turn drive double-balanced mixers. The outputs of these mixers are summed and applied to an on-chip RF transformer, which converts the differential mixer signals to a 50Ω single-ended output. The four balanced I and Q baseband input ports are intended for DC coupling from a source with a common mode voltage level of about 0.5V. The LO path consists of an LO buffer with single-ended input, and precision quadrature generators that produce the LO drive for the mixers. The supply voltage range is 4.5V to 5.25V.

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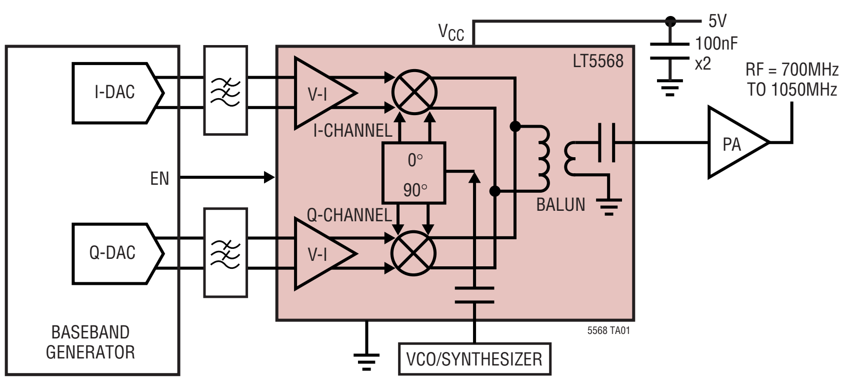
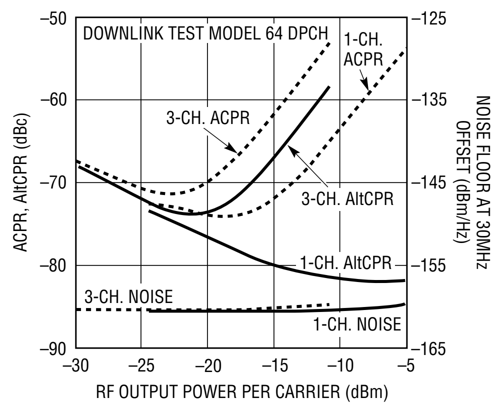
TYPICAL APPLICATION

700MHz to 1050MHz Direct Conversion Transmitter Application



CDMA2000 ACPR, AltCPR and Noise vs RF Output Power at 850MHz for 1 and 3 Carriers



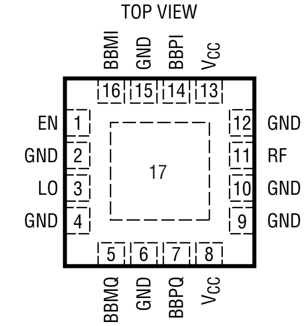
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 5.5V
Common Mode Level of BBPI, BBMI and
BBPQ, BBMQ 2.5V
Operating Ambient Temperature
(Note 2) .... –40°C to 85°C
Storage Temperature Range................... –65°C to 125°C
Voltage on any Pin
Not to Exceed...................... –500mV to V_{CC} + 500mV

PACKAGE/ORDER INFORMATION

TOP VIEW



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 17) IS GROUND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	UF PART MARKING
LT5568EUF	5568

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 850MHz, f_{RF} = 852MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency = 2MHz, I&Q 90° shifted (upper side-band selection). $P_{RF, OUT}$ = –10dBm, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Output (RF)						
f_{RF}	RF Frequency Range RF Frequency Range	–3dB Bandwidth –1dB Bandwidth		0.6 to 1.2 0.7 to 1.05		GHz GHz
$S_{22, ON}$	RF Output Return Loss	EN = High (Note 6)		–14		dB
$S_{22, OFF}$	RF Output Return Loss	EN = Low (Note 6)		–12		dB
NFloor	RF Output Noise Floor	No Input Signal (Note 8) P_{OUT} = 4dBm (Note 9) P_{OUT} = 4dBm (Note 10)		–160.3 –154 –154		dBm/Hz dBm/Hz dBm/Hz
G_P	Conversion Power Gain	$P_{OUT}/P_{IN, I\&Q}$	–9	–6.8	–3	dB
G_V	Conversion Voltage Gain	20 • Log ($V_{OUT, 50\Omega}/V_{IN, DIFF, I or Q}$)		–6.8		dB
P_{OUT}	Absolute Output Power	1$V_{P-P DIFF}$ CW Signal, I and Q		–2.8		dBm
$G_{3LO vs LO}$	3 • LO Conversion Gain Difference	(Note 17)		–23		dB
OP1dB	Output 1dB Compression	(Note 7)		8.3		dBm
OIP2	Output 2nd Order Intercept	(Notes 13, 14)		63		dBm
OIP3	Output 3rd Order Intercept	(Notes 13, 15)		22.9		dBm
IR	Image Rejection	(Note 16)		–46		dBc
LOFT	Carrier Leakage (LO Feedthrough)	EN = High, P_{LO} = 0dBm (Note 16) EN = Low, P_{LO} = 0dBm (Note 16)		–43 –65		dBm dBm

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 850MHz, f_{RF} = 852MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency = 2MHz, I&Q 90° shifted (upper side-band selection). $P_{RF, OUT}$ = –10dBm, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LO Input (LO)						
f_{LO}	LO Frequency Range			0.6 to 1.2		GHz
P_{LO}	LO Input Power		–10	0	5	dBm
$S_{11, ON}$	LO Input Return Loss	EN = High (Note 6)		–11.4		dB
$S_{11, OFF}$	LO Input Return Loss	EN = Low (Note 6)		–2.7		dB
NF_{LO}	LO Input Referred Noise Figure	(Note 5) at 850MHz		12.7		dB
G_{LO}	LO to RF Small Signal Gain	(Note 5) at 850MHz		23.8		dB
$IIP3_{LO}$	LO Input 3rd Order Intercept	(Note 5) at 850MHz		–11.5		dBm
Baseband Inputs (BBPI, BBMI, BBPQ, BBMQ)						
BW_{BB}	Baseband Bandwidth	–3dB Bandwidth		380		MHz
V_{CMBB}	DC Common Mode Voltage	(Note 4)		0.54		V
$R_{IN, SE}$	Single-Ended Input Resistance	(Note 4)		48		Ω
P_{LO2BB}	Carrier Feedthrough on BB	P_{OUT} = 0 (Note 4)		–38		dBm
IP1dB	Input 1dB Compression Point	Differential Peak-to-Peak (Notes 7, 18)		4.3		$V_{P-P, DIFF}$
$\Delta G_{I/Q}$	I/Q Absolute Gain Imbalance			0.07		dB
$\Delta\varphi_{I/Q}$	I/Q Absolute Phase Imbalance			0.45		Deg
Power Supply (V_{CC})						
V_{CC}	Supply Voltage		4.5	5	5.25	V
$I_{CC, ON}$	Supply Current	EN = High	80	117	165	mA
$I_{CC, OFF}$	Supply Current, Sleep Mode	EN = 0V			50	µA
t_{ON}	Turn-On Time	EN = Low to High (Note 11)		0.3		µs
t_{OFF}	Turn-Off Time	EN = High to Low (Note 12)		1.4		µs
Enable (EN), Low = Off, High = On						
Enable	Input High Voltage Input High Current	EN = High EN = 5V	1.0	 230		V µA
Sleep	Input Low Voltage Input Low Current	EN = Low EN = 0V		 0	0.5	V µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Tests are performed as shown in the configuration of Figure 7.

Note 4: On each of the four baseband inputs BBPI, BBMI, BBPQ and BBMQ.

Note 5: V(BBPI) – V(BBMI) = 1V_{DC}, V(BBPQ) – V(BBMQ) = 1V_{DC}.

Note 6: Maximum value within –1dB bandwidth.

Note 7: An external coupling capacitor is used in the RF output line.

Note 8: At 20MHz offset from the LO signal frequency.

Note 9: At 20MHz offset from the CW signal frequency.

Note 10: At 5MHz offset from the CW signal frequency.

Note 11: RF power is within 10% of final value.

Note 12: RF power is at least 30dB lower than in the ON state.

Note 13: Baseband is driven by 2MHz and 2.1MHz tones. Drive level is set in such a way that the two resulting RF tones are –10dBm each.

Note 14: IM2 measured at LO frequency + 4.1MHz.

Note 15: IM3 measured at LO frequency + 1.9MHz and LO frequency + 2.2MHz.

Note 16: Amplitude average of the characterization data set without image or LO feedthrough nulling (unadjusted).

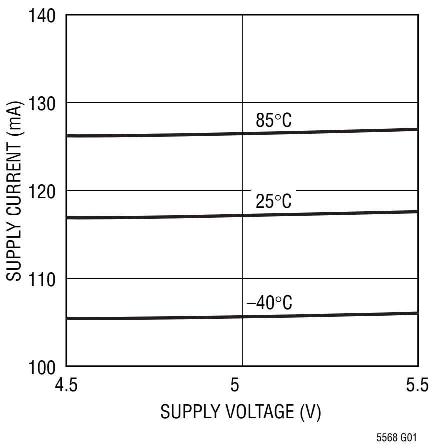
Note 17: The difference in conversion gain between the spurious signal at f = 3 • LO – BB versus the conversion gain at the desired signal at f = LO + BB for BB = 2MHz and LO = 850MHz.

Note 18: The input voltage corresponding to the output P1dB.

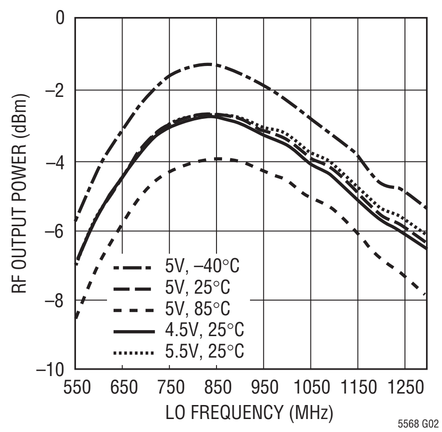
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 850MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency f_{BB} = 2MHz, I&Q 90° shifted. f_{RF} = f_{BB} + f_{LO} (upper sideband selection). $P_{RF, OUT}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

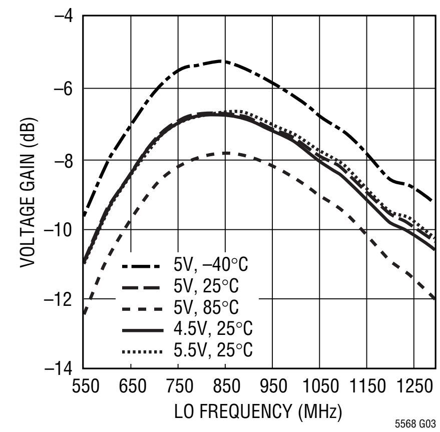
Supply Current vs Supply Voltage



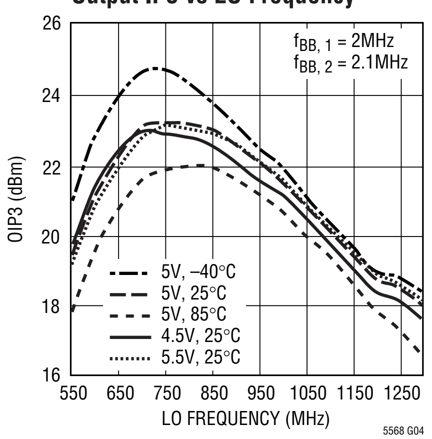
RF Output Power vs LO Frequency at 1V_{P-P} Differential Baseband Drive



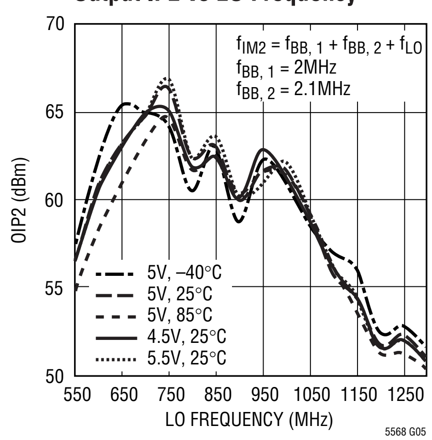
Voltage Gain vs LO Frequency



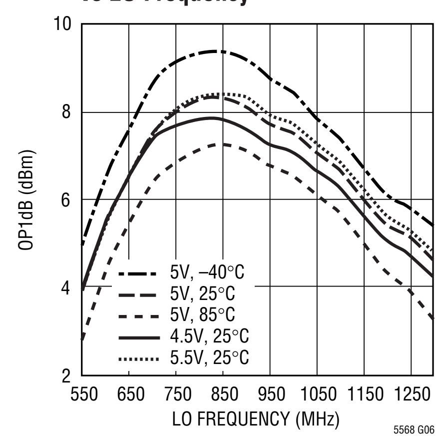
Output IP3 vs LO Frequency



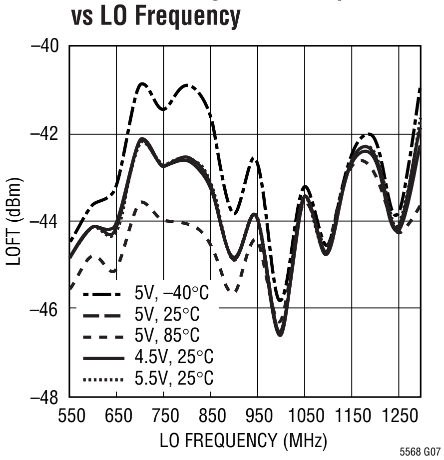
Output IP2 vs LO Frequency



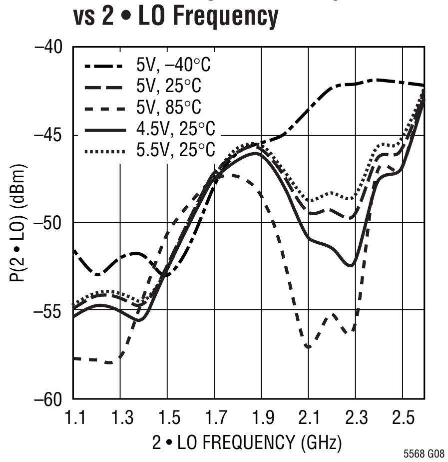
Output 1dB Compression vs LO Frequency



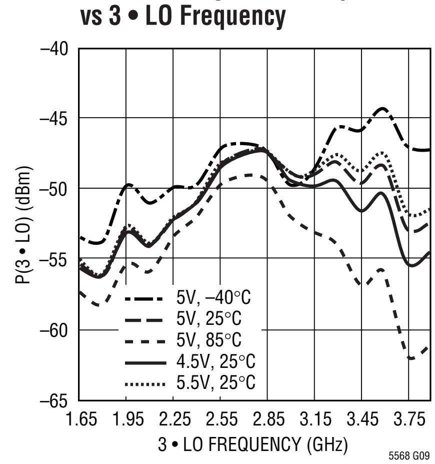
LO Feedthrough to RF Output vs LO Frequency



2 • LO Leakage to RF Output vs 2 • LO Frequency



3 • LO Leakage to RF Output vs 3 • LO Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 850MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency f_{BB} = 2MHz, I&Q 90° shifted. f_{RF} = f_{BB} + f_{LO} (upper sideband selection). $P_{RF, OUT}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

Noise Floor vs RF Frequency

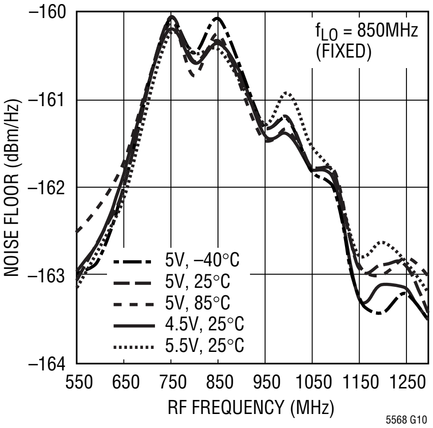
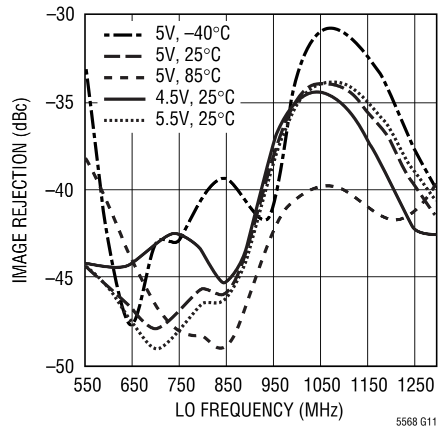
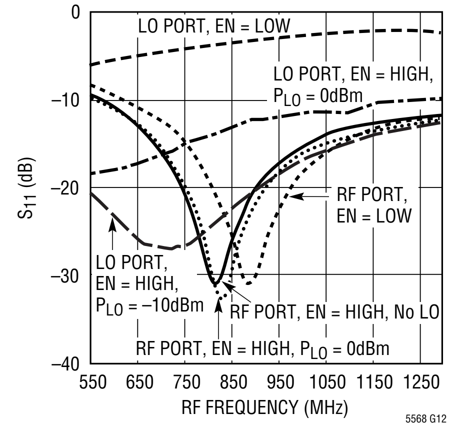


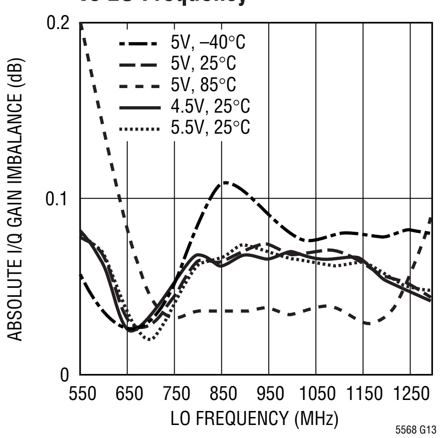
Image Rejection vs LO Frequency



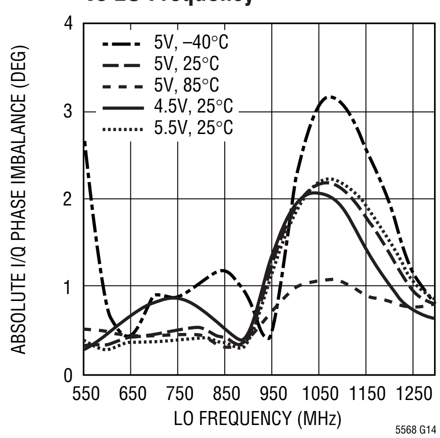
LO and RF Port Return Loss vs RF Frequency



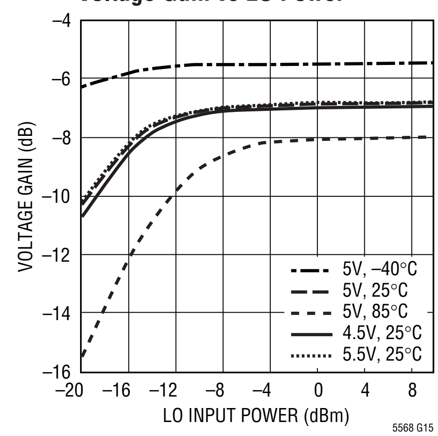
Absolute I/Q Gain Imbalance vs LO Frequency



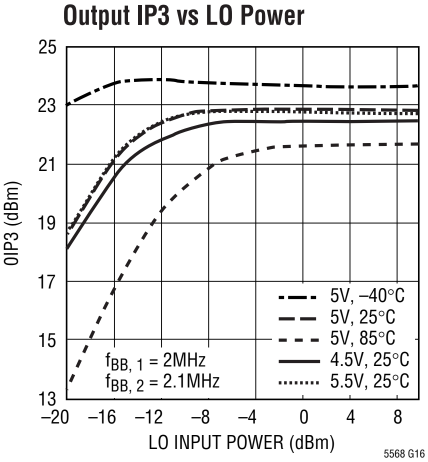
Absolute I/Q Phase Imbalance vs LO Frequency



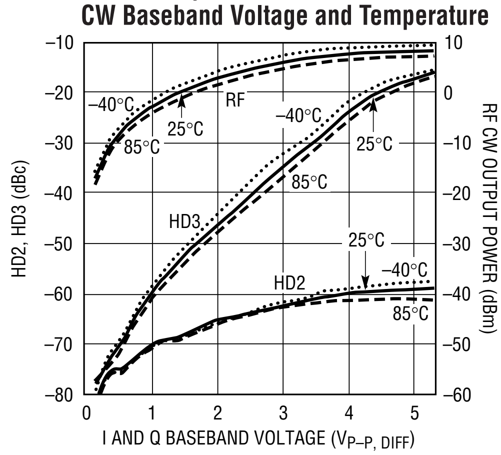
Voltage Gain vs LO Power



Output IP3 vs LO Power



RF CW Output Power, HD2 and HD3 vs CW Baseband Voltage and Temperature



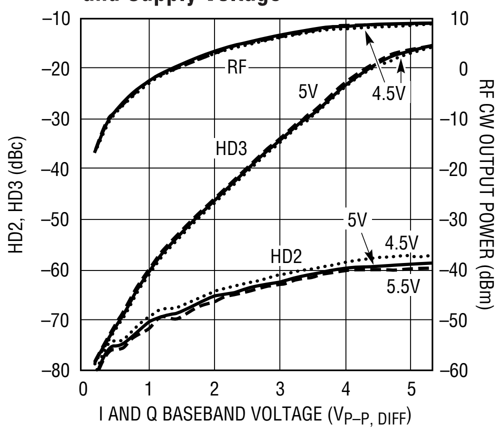
HD2 = MAX POWER AT f_{LO} + 2 • f_{BB} OR f_{LO} – 2 • f_{BB}
HD3 = MAX POWER AT f_{LO} + 3 • f_{BB} OR f_{LO} – 3 • f_{BB}

5568 G17

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 850MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency f_{BB} = 2MHz, I&Q 90° shifted. f_{RF} = f_{BB} + f_{LO} (upper sideband selection). $P_{RF,\ OUT}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

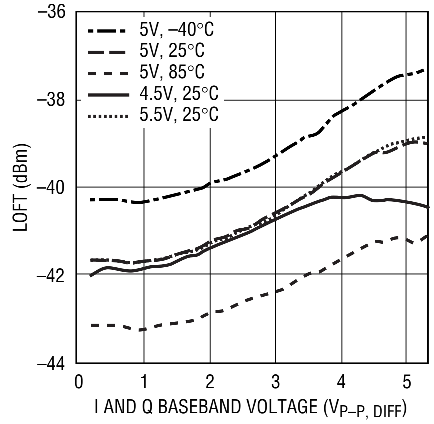
RF CW Output Power, HD2 and HD3 vs CW Baseband Voltage and Supply Voltage



HD2 = MAX POWER AT f_{LO} + 2 • f_{BB} OR f_{LO} – 2 • f_{BB}
HD3 = MAX POWER AT f_{LO} + 3 • f_{BB} OR f_{LO} – 3 • f_{BB}

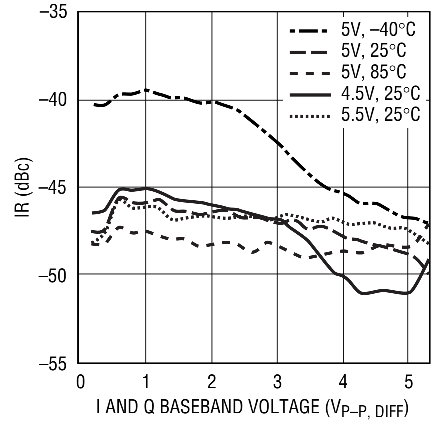
5568 G18

LO Feedthrough to RF Output vs CW Baseband Voltage



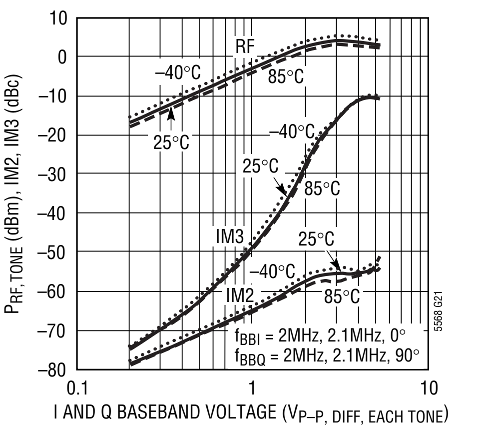
5568 G19

Image Rejection vs CW Baseband Voltage



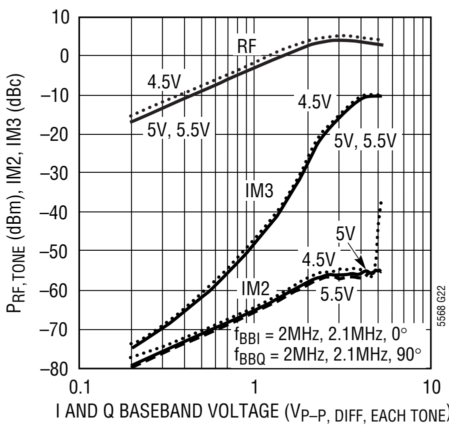
5568 G20

RF Two-Tone Power (Each Tone), IM2 and IM3 vs Baseband Voltage and Temperature



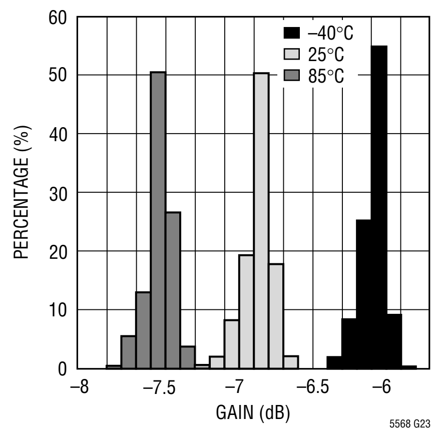
IM2 = POWER AT f_{LO} + 4.1MHz
IM3 = MAX POWER AT f_{LO} + 1.9MHz OR f_{LO} + 2.2MHz

RF Two-Tone Power (Each Tone), IM2 and IM3 vs Baseband Voltage and Supply Voltage



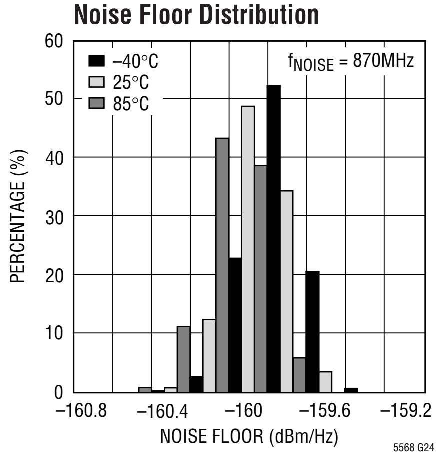
IM2 = POWER AT f_{LO} + 4.1MHz
IM3 = MAX POWER AT f_{LO} + 1.9MHz OR f_{LO} + 2.2MHz

Gain Distribution



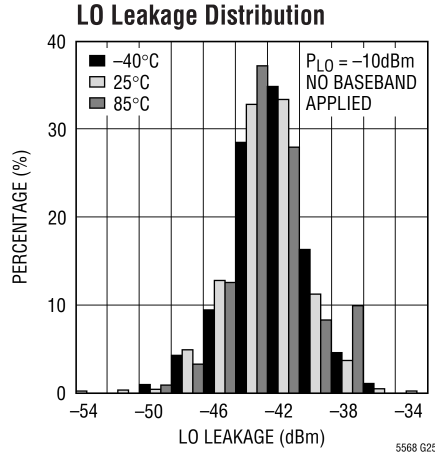
5568 G23

Noise Floor Distribution



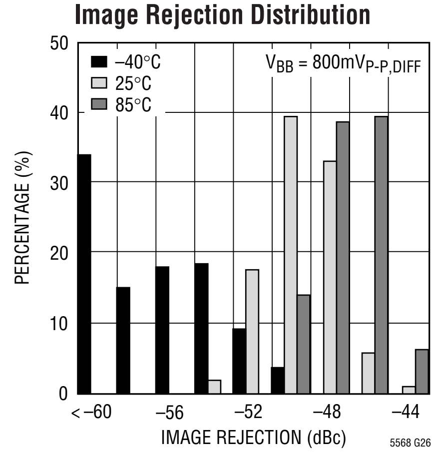
5568 G24

LO Leakage Distribution



5568 G25

Image Rejection Distribution



5568 G26

5568f

PIN FUNCTIONS

EN (Pin 1): Enable Input. When the enable pin voltage is higher than 1V, the IC is turned on. When the input voltage is less than 0.5V, the IC is turned off.

GND (Pins 2, 4, 6, 9, 10, 12, 15): Ground. Pins 6, 9, 15 and 17 (exposed pad) are connected to each other internally. Pins 2 and 4 are connected to each other internally and function as the ground return for the LO signal. Pins 10 and 12 are connected to each other internally and function as the ground return for the on-chip RF balun. For best RF performance, pins 2, 4, 6, 9, 10, 12, 15 and the Exposed Pad 17 should be connected to the printed circuit board ground plane.

LO (Pin 3): LO Input. The LO input is an AC-coupled single-ended input with approximately 50Ω input impedance at RF frequencies. Externally applied DC voltage should be within the range –0.5V to V_{CC} + 0.5V in order to avoid turning on ESD protection diodes.

BBPQ, BBMQ (Pins 7, 5): Baseband Inputs for the Q-channel, each 50Ω input impedance. Internally biased at about 0.54V. Applied voltage must stay below 2.5V.

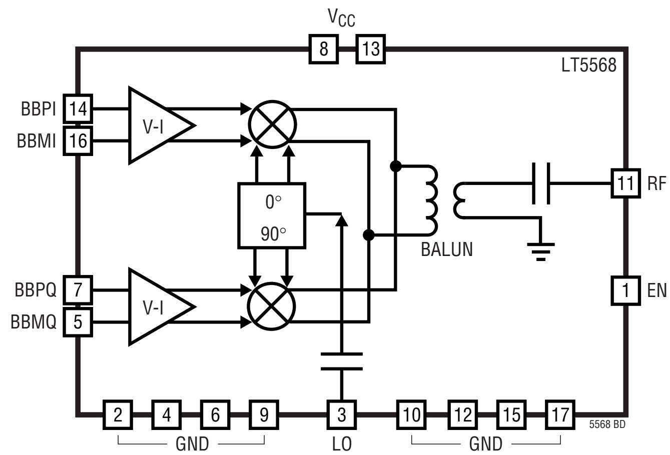
V_{CC} (Pins 8, 13): Power Supply. Pins 8 and 13 are connected to each other internally. It is recommended to use 0.1µF capacitors for decoupling to ground on each of these pins.

RF (Pin 11): RF Output. The RF output is an AC-coupled single-ended output with approximately 50Ω output impedance at RF frequencies. Externally applied DC voltage should be within the range –0.5V to V_{CC} + 0.5V in order to avoid turning on ESD protection diodes.

BBPI, BBMI (Pins 14, 16): Baseband Inputs for the I-channel, each with 50Ω input impedance. Internally biased at about 0.54V. Applied voltage must stay below 2.5V.

Exposed Pad (Pin 17): Ground. This pin must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT5568 consists of I and Q input differential voltage-to-current converters, I and Q up-conversion mixers, an RF output balun, an LO quadrature phase generator and LO buffers.

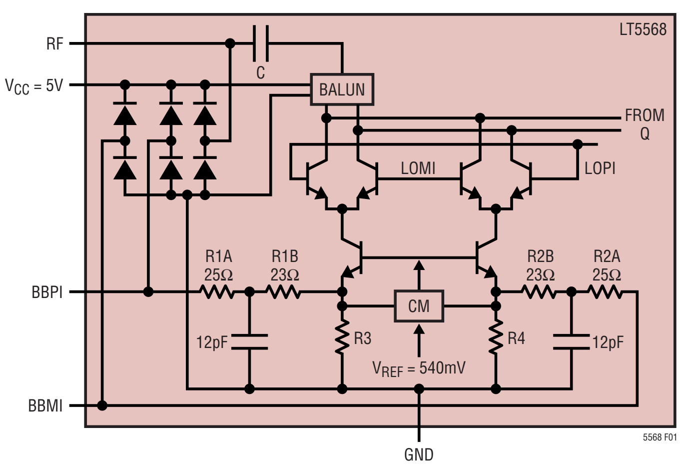


Figure 1. Simplified Circuit Schematic of the LT5568 (Only I-Half is Drawn)

External I and Q baseband signals are applied to the differential baseband input pins, BBPI, BBMI, and BBPQ, BBMQ. These voltage signals are converted to currents and translated to RF frequency by means of double-balanced up-converting mixers. The mixer outputs are combined in an RF output balun, which also transforms the output impedance to 50Ω. The center frequency of the resulting RF signal is equal to the LO signal frequency. The LO input drives a phase shifter which splits the LO signal into in-phase and quadrature LO signals. These LO signals are then applied to on-chip buffers which drive the up-conversion mixers. Both the LO input and RF output are single-ended, 50Ω-matched and AC coupled.

Baseband Interface

The baseband inputs (BBPI, BBMI), (BBPQ, BBMQ) present a differential input impedance of about 100Ω. At each of the four baseband inputs, a first-order lowpass filter using 25Ω

APPLICATIONS INFORMATION

and 12pF to ground is incorporated (see Figure 1), which limits the baseband bandwidth to approximately 330MHz (–1dB point). The common mode voltage is about 0.54V and is approximately constant over temperature.

It is important that the applied common mode voltage level of the I and Q inputs is about 0.54V in order to properly bias the LT5568. Some I/Q test generators allow setting the common mode voltage independently. In this case, the common mode voltage of those generators must be set to 0.27V to match the LT5568 internal bias, because for DC signals, there is no –6dB source-load voltage division (see Figure 2).

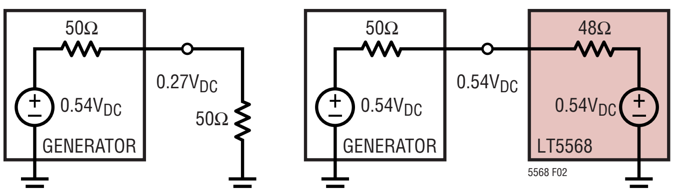


Figure 2. DC Voltage Levels for a Generator Programmed at $0.27V_{DC}$ for a 50Ω Load and the LT5568 as a Load

The baseband inputs should be driven differentially; otherwise, the even-order distortion products will degrade the overall linearity severely. Typically, a DAC will be the signal source for the LT5568. Reconstruction filters should be placed between the DAC output and the LT5568's baseband inputs. In Figure 3, an example interface schematic shows a commonly used DAC output interface followed by a passive 5th order ladder filter. The DAC in this example sources a current from 0mA to 20mA. The interface may be DC coupled. This allows adjustment of the DAC's differential output current to minimize the LO feedthrough. Optionally, transformer T1 can be inserted to improve the current balance in the BBPI and BBMI pins. This will improve the 2nd order distortion performance (OIP2).

The maximum single sideband CW RF output power at 850MHz using both I and Q channels with the configuration shown in Figure 3 is about –3dBm. The maximum CW output power can be increased by connecting load resistors R5 and R6 to –5V instead of GND, and changing their values to 550Ω. In that case, the maximum single sideband CW RF output power at 850MHz will be about +2dBm. In addition, the ladder filter component values require adjustment for a higher source impedance.

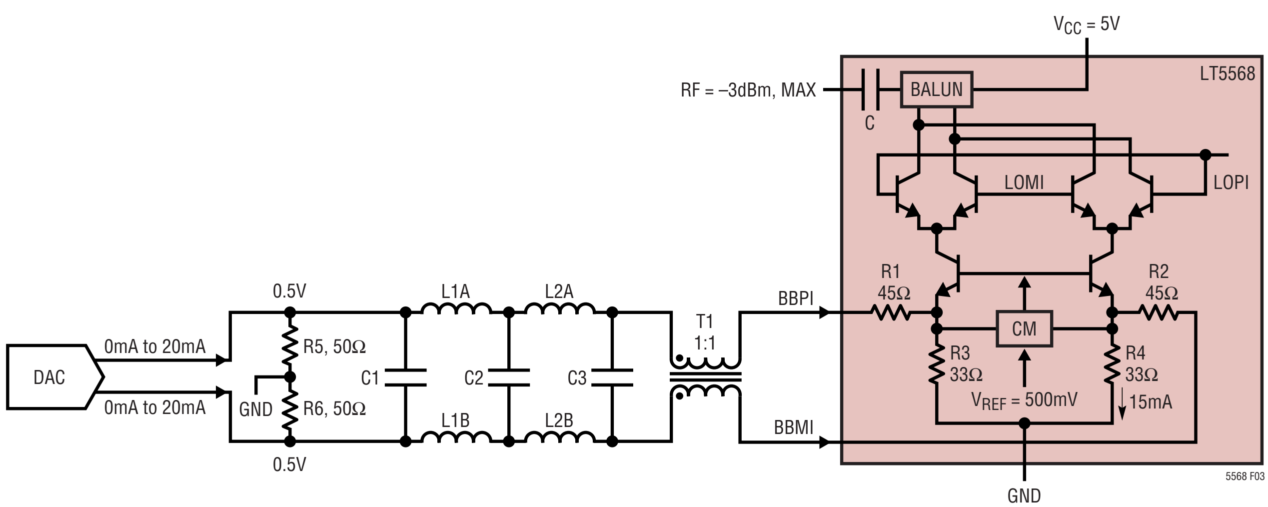


Figure 3. LT5568 5th Order Filtered Baseband Interface with Common DAC (Only I-Channel is Shown)

APPLICATIONS INFORMATION

LO Section

The internal LO input amplifier performs single-ended to differential conversion of the LO input signal. Figure 4 shows the equivalent circuit schematic of the LO input.

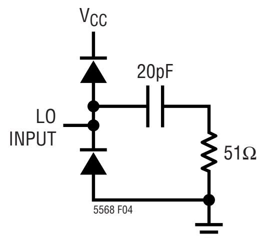


Figure 4. Equivalent Circuit Schematic of the LO Input

The internal, differential LO signal is then split into in-phase and quadrature (90° phase shifted) signals that drive LO buffer sections. These buffers drive the double balanced I and Q mixers. The phase relationship between the LO input and the internal in-phase LO and quadrature LO signals is fixed, and is independent of start-up conditions. The internal phase shifters are designed to deliver accurate quadrature signals. For LO frequencies significantly below 600MHz or above 1GHz, however, the quadrature accuracy will diminish, causing the image rejection to degrade. The LO pin input impedance is about 50Ω, and the recommended LO input power is 0dBm. For lower LO input power, the gain, OIP2, OIP3 and noise floor at P_{RF} = 4dBm will degrade, especially below –5dBm and at T_A = 85°C. For high LO input power (e.g., +5dBm), the LO feedthrough will increase with no improvement in linearity or gain. For lower LO input power, e.g., P_{LO} = –5dBm, the image rejection improves (especially around 950MHz) at the cost of 1.5dB degradation of the noise floor at P_{RF} = 4dBm. Harmonics present on the LO signal can degrade the image rejection because they can introduce a small excess phase shift in the internal phase splitter. For the second (at 1.7GHz) and third harmonics (at 2.55GHz) at –20dBc, the resulting signal at the image frequency is about –56dBc or lower, corresponding to an excess phase shift of much less than 1 degree. For the second and third LO harmonics at –10dBc, the introduced signal at the image frequency is about –47dBc. Higher harmonics than the third will have less impact. The LO return loss typically will be better than 11dB over the 700MHz to 1.05GHz range. Table 1 shows the LO port input impedance vs frequency.

Table 1. LO Port Input Impedance vs Frequency for EN = High and P_{LO} = 0dBm

Frequency MHz	Input Impedance Ω	S_{11} Mag	S_{11} Angle
500	47.5 + j12.1	0.126	95.0
600	59.4 + j8.4	0.115	37.8
700	66.2 – j1.14	0.140	–3.41
800	67.2 – j13.4	0.185	–31.7
900	61.1 – j23.9	0.232	–53.2
1000	53.3 – j26.8	0.252	–68.7
1100	48.2 – j26.1	0.258	–79.4
1200	42.0 – j27.4	0.297	–90.0

If the part is in shutdown mode, the input impedance of the LO port will be different. The LO input impedance for EN = Low is given in Table 2.

Table 2. LO Port Input Impedance vs Frequency for EN = Low and P_{LO} = 0dBm

Frequency MHz	Input Impedance Ω	S_{11} Mag	S_{11} Angle
500	33.6 + j41.3	0.477	85.4
600	59.8 + j69.1	0.539	49.8
700	140 + j89.8	0.606	19.6
800	225 – j62.6	0.659	–6.8
900	92.9 – j128	0.704	–29.6
1000	39.8 – j95.9	0.735	–45.5
1100	22.8 – j72.7	0.755	–65.6
1200	16.0 – j57.3	0.763	–79.7

RF Section

After up-conversion, the RF outputs of the I and Q mixers are combined. An on-chip balun performs internal differential to single-ended output conversion, while transforming the output signal impedance to 50Ω. Table 3 shows the RF port output impedance vs frequency.

Table 3. RF Port Output Impedance vs Frequency for EN = High and P_{LO} = 0dBm

Frequency MHz	Input Impedance Ω	S_{22} Mag	S_{22} Angle
500	22.0 + j5.7	0.395	164.2
600	28.2 + j12.5	0.317	141.3
700	38.8 + j14.8	0.206	117.5
800	49.4 + j7.2	0.072	90.6
900	49.3 – j5.1	0.051	–94.7
1000	42.5 – j11.1	0.143	–117.0
1100	36.7 – j11.7	0.202	–130.7
1200	33.0 – j10.3	0.238	–141.6

APPLICATIONS INFORMATION

The RF output S_{22} with no LO power applied is given in Table 4.

Table 4. RF Port Output Impedance vs Frequency for EN = High and No LO Power Applied

Frequency MHz	Input Impedance Ω	S_{22} Mag	S_{22} Angle
500	22.7 + j5.6	0.381	164.0
600	29.7 + j11.6	0.290	142.0
700	40.5 + j11.6	0.164	121.9
800	47.3 + j2.2	0.037	139.6
900	44.1 – j6.7	0.094	–126.9
1000	38.2 – j9.8	0.171	–133.9
1100	34.0 – j9.4	0.218	–143.1
1200	31.5 – j7.8	0.245	–151.6

For EN = Low the S_{22} is given in Table 5.

Table 5. RF Port Output Impedance vs Frequency for EN = Low

Frequency MHz	Input Impedance Ω	S_{22} Mag	S_{22} Angle
500	21.2 + j5.4	0.409	164.9
600	26.6 + j12.5	0.340	142.5
700	36.6 + j16.6	0.241	118.1
800	49.2 + j11.6	0.116	87.4
900	52.9 – j2.0	0.034	–33.1
1000	46.4 – j11.2	0.121	–101.1
1100	39.3 – j13.2	0.188	–120.6
1200	34.4 – j12.1	0.231	–133.8

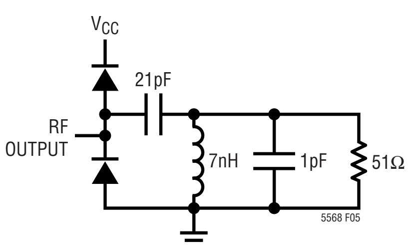


Figure 5. Equivalent Circuit Schematic of the RF Output

Note that an ESD diode is connected internally from the RF output to ground. For strong output RF signal levels (higher than 3dBm), this ESD diode can degrade the linearity performance if the 50Ω termination impedance is connected directly to ground. To prevent this, a coupling capacitor can be inserted in the RF output line. This is strongly recommended during a 1dB compression measurement.

Enable Interface

Figure 6 shows a simplified schematic of the EN pin interface. The voltage necessary to turn on the LT5568 is 1V. To disable (shut down) the chip, the enable voltage must be below 0.5V. If the EN pin is not connected, the chip is disabled. This EN = Low condition is assured by the 75k on-chip pull-down resistor. It is important that the voltage at the EN pin does not exceed V_{CC} by more than 0.5V. If this should occur, the supply current could be sourced through the EN pin ESD protection diodes, which are not designed to carry the full supply current, and damage may result.

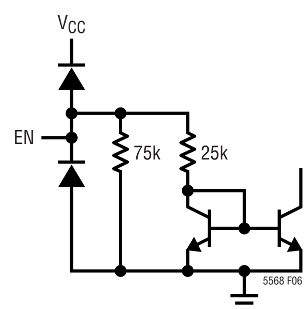


Figure 6. EN Pin Interface

APPLICATIONS INFORMATION

Evaluation Board

Figure 7 shows the evaluation board schematic. A good ground connection is required for the exposed pad. If this is not done properly, the RF performance will degrade. Additionally, the exposed pad provides heat sinking for the part and minimizes the possibility of the chip overheating.

R1 (optional) limits the EN pin current in the event that the EN pin is pulled high while the V_{CC} inputs are low. In Figures 8 and 9 the silk screens and the PCB board layout are shown.

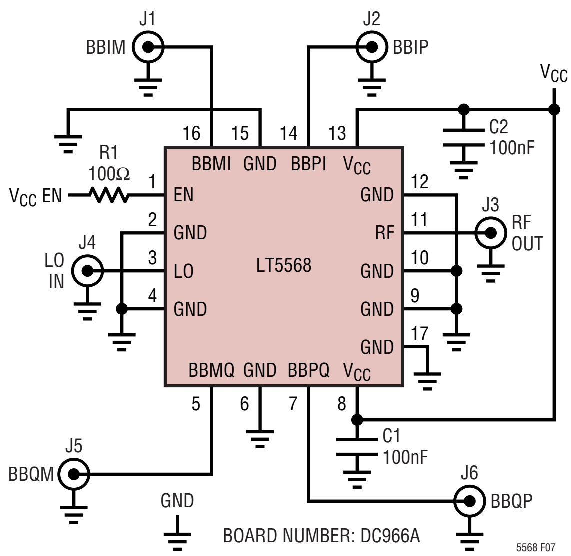


Figure 7. Evaluation Circuit Schematic

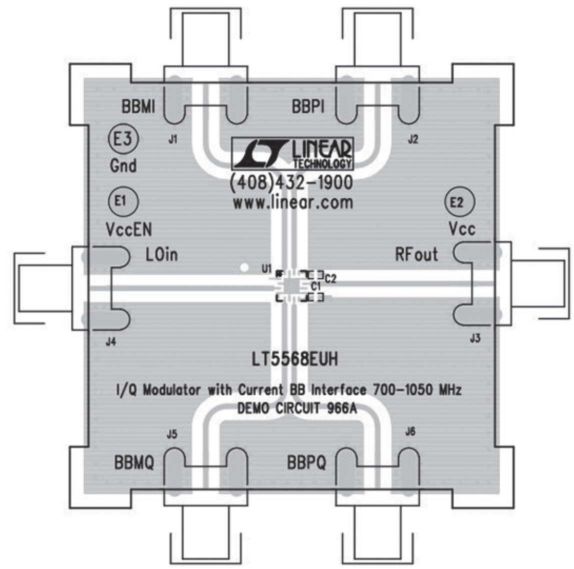


Figure 8. Component Side of Evaluation Board

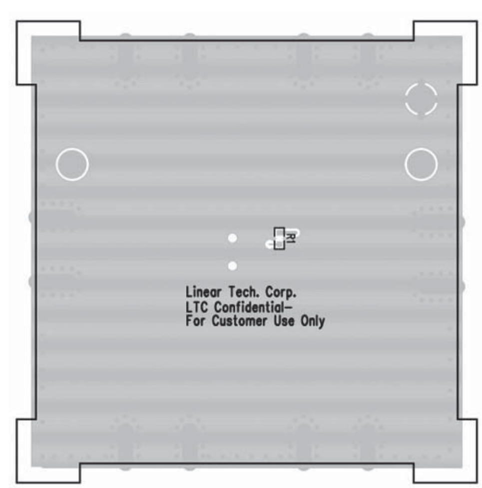


Figure 9. Bottom Side of Evaluation Board

APPLICATIONS INFORMATION

Application Measurements

The LT5568 is recommended for base-station applications using various modulation formats. Figure 10 shows a typical application. Figure 11 shows the ACPR performance for CDMA2000 using 1- and 3-carrier modulation. Figures 12 and 13 illustrate the 1- and 3-carrier CDMA2000 RF spectrum. To calculate ACPR, a correction is made for the spectrum analyzer noise floor. If the output power is high, the ACPR will be limited by the linearity performance of the part. If the output power is low, the ACPR will be limited by the noise performance of the part. In the middle, an optimum ACPR is observed.

Because of the LT5568's very high dynamic range, the test equipment can limit the accuracy of the ACPR measurement. See Application Note 99. Consult the factory for advice on the ACPR measurement, if needed.

The ACPR performance is sensitive to the amplitude match of the BBIP and BBIM (or BBQP and BBQM) inputs. This is because a difference in AC current amplitude will give rise to a difference in amplitude between the even-order harmonic products generated in the internal V-I converter. As a result, they will not cancel out entirely. Therefore, it is important to keep the currents in those pins exactly the same (but of opposite sign). The current will enter the LT5568's common-base stage, and will flow to the mixer upper switches. This can be seen in Figure 1 where the internal circuit of the LT5568 is drawn. For best results, a high ohmic source is recommended; for example, the

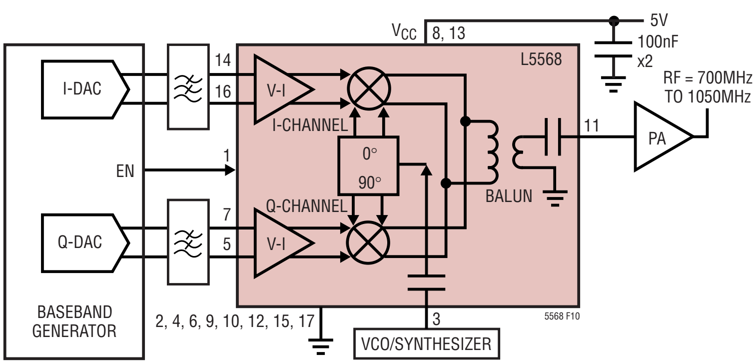


Figure 10. 700MHz to 1050MHz Direct Conversion Transmitter Application

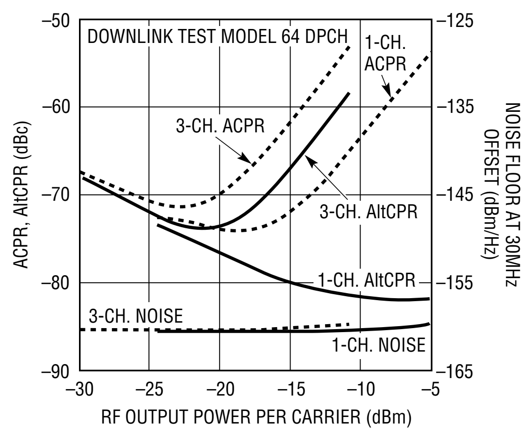


Figure 11. APCR, AltCPR and Noise CDMA2000 Modulation

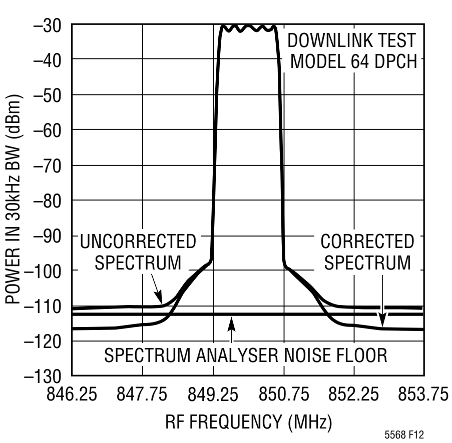


Figure 12. 1-Carrier CDMA2000 Spectrum

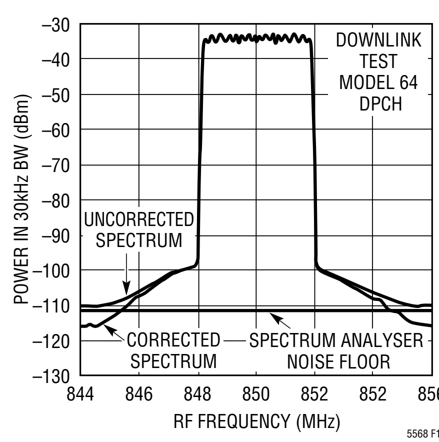


Figure 13. 3-Carrier CDMA2000 Spectrum

APPLICATIONS INFORMATION

interface circuit drawn in Figure 3, modified by pulling resistors R5 and R6 to a –5V supply and adjusting their values to 550Ω, with T1 omitted.

Another method to reduce current mismatch between the currents flowing in the BBIP and BBIM pins (or the BBQP and BBQM pins) is to use a 1:1 transformer with the two windings in the DC path (T1 in Figure 3). For DC, the transformer forms a short, and for AC, the transformer will reduce the common mode current component, which forces the two currents to be better matched. Alternatively, a transformer with 1:2 impedance ratio can be used, which gives a convenient DC separation between primary and secondary in combination with the required impedance match. The secondary center tap should not be connected, which allows some voltage swing if there is a single-ended input impedance difference at the baseband pins. As a result, both currents will be equal. The disadvantage is that there is no DC coupling, so the LO feedthrough calibration cannot be performed via the BB connections. After calibration when the temperature changes, the LO feedthrough and the image rejection performance will change. This is illustrated in Figure 14. The LO feedthrough and image rejection can also change as a function of the baseband drive level, as is depicted in Figure 15. In Figures 16 and 17 the LO feedthrough and image rejection vs LO power are shown.

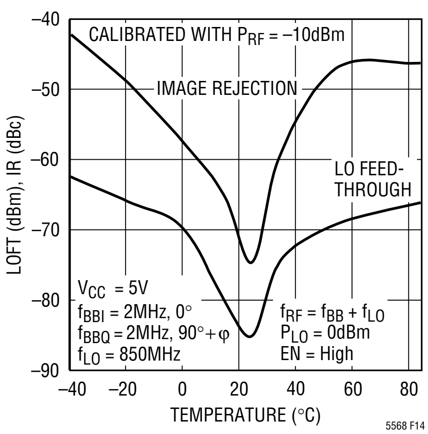


Figure 14. LO Feedthrough and Image Rejection vs Temperature after Calibration at 25°C

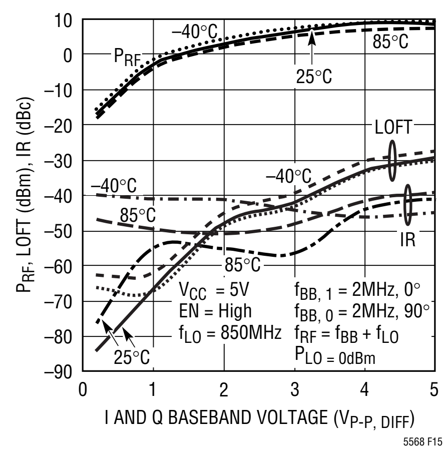


Figure 15. LO Feedthrough and Image Rejection vs Baseband Drive Voltage after Calibration at 25°C

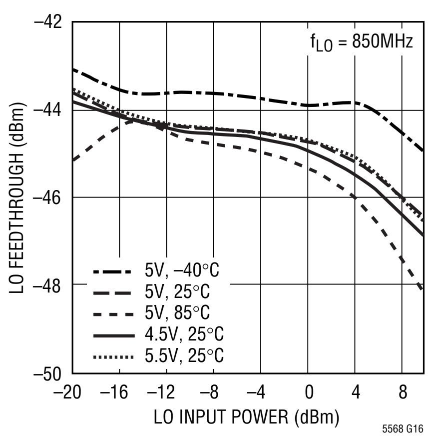


Figure 16. LO Feedthrough vs LO Power

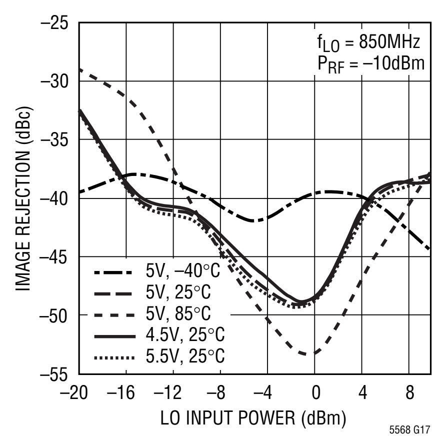
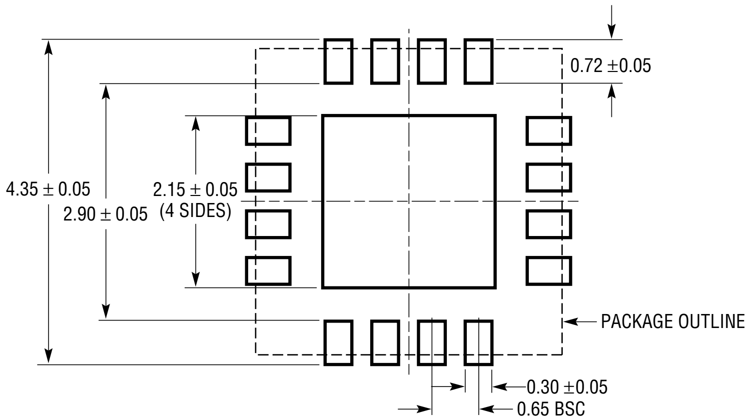


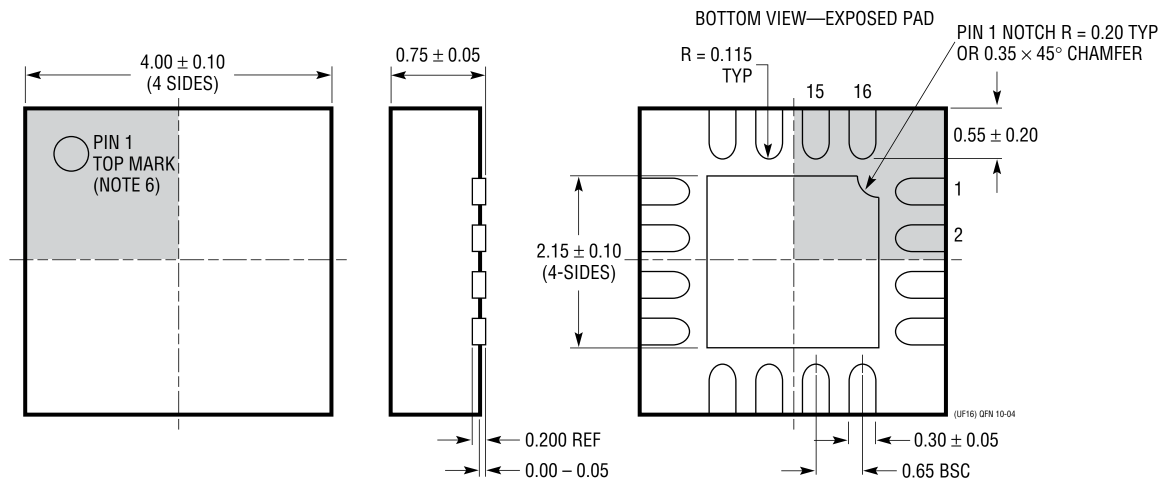
Figure 17. Image Rejection vs LO Power

PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
ON THE TOP AND BOTTOM OF PACKAGE

LINEAR TECHNOLOGY
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RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT5511	High Linearity Upconverting Mixer	RF Output to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5512	DC to 3GHz High Signal Level Downconverting Mixer	DC to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5514	Ultralow Distortion, IF Amplifier/ADC Driver with Digitally Controlled Gain	850MHz Bandwidth, 47dBm OIP3 at 100MHz, 10.5dB to 33dB Gain Control Range
LT5515	1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator	20dBm IIP3, Integrated LO Quadrature Generator
LT5516	0.8GHz to 1.5GHz Direct Conversion Quadrature Demodulator	21.5dBm IIP3, Integrated LO Quadrature Generator
LT5517	40MHz to 900MHz Quadrature Demodulator	21dBm IIP3, Integrated LO Quadrature Generator
LT5518	1.5GHz to 2.4GHz High Linearity Direct Quadrature Modulator	22.8dBm OIP3 at 2GHz, –158.2dBm/Hz Noise Floor, 50Ω Single-Ended LO and RF Ports, 4-Ch W-CDMA ACPR = –64dBc at 2.14GHz
LT5519	0.7GHz to 1.4GHz High Linearity Upconverting Mixer	17.1dBm IIP3 at 1GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5520	1.3GHz to 2.3GHz High Linearity Upconverting Mixer	15.9dBm IIP3 at 1.9GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5521	10MHz to 3700MHz High Linearity Upconverting Mixer	24.2dBm IIP3 at 1.95GHz, NF = 12.5dB, 3.15V to 5.25V Supply, Single-Ended LO Port Operation
LT5522	600MHz to 2.7GHz High Signal Level Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5524	Low Power, Low Distortion ADC Driver with Digitally Programmable Gain	450MHz Bandwidth, 40dBm OIP3, 4.5dB to 27dB Gain Control
LT5526	High Linearity, Low Power Downconverting Mixer	3V to 5.3V Supply, 16.5dBm IIP3, 100kHz to 2GHz RF, NF = 11dB, I_{CC} = 28mA, –65dBm LO-RF Leakage
LT5527	400MHz to 3.7GHz High Signal Level Downconverting Mixer	IIP3 = 23.5dBm and NF = 12.5dB at 1900MHz, 4.5V to 5.25V Supply, I_{CC} = 78mA
LT5528	1.5GHz to 2.4GHz High Linearity Direct Quadrature Modulator	21.8dBm OIP3 at 2GHz, –159.3dBm/Hz Noise Floor, 50Ω, 0.5V_{DC} Baseband Interface, 4-Ch W-CDMA ACPR = –66dBc at 2.14GHz
RF Power Detectors		
LTC®5505	RF Power Detectors with >40dB Dynamic Range	300MHz to 3GHz, Temperature Compensated, 2.7V to 6V Supply
LTC5507	100kHz to 1000MHz RF Power Detector	100kHz to 1GHz, Temperature Compensated, 2.7V to 6V Supply
LTC5508	300MHz to 7GHz RF Power Detector	44dB Dynamic Range, Temperature Compensated, SC70 Package
LTC5509	300MHz to 3GHz RF Power Detector	36dB Dynamic Range, Low Power Consumption, SC70 Package
LTC5532	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Adjustable Gain and Offset
LT5534	50MHz to 3GHz Loq RF Power Detector with 60dB Dynamic Range	±1dB Output Variation over Temperature, 38ns Response Time
LTC5536	Precision 600MHz to 7GHz RF Detector with Fast Comparater	25ns Response Time, Comparator Reference Input, Latch Enable Input, –26dBm to +12dBm Input Range
LT5537	Wide Dynamic Range Loq RF/IF Detector	Low Frequency to 800MHz, 83dB Dynamic Range, 2.7V to 5.25V Supply
High Speed ADCs		
LTC2220-1	12-Bit, 185Msps ADC	Single 3.3V Supply, 910mW Consumption, 67.5dB SNR, 80dB SFDR, 775MHz Full Power BW
LTC2249	14-Bit, 80Msps ADC	Single 3V Supply, 222mW Consumption, 73dB SNR, 90dB SFDR
LTC2255	14-Bit, 125Msps ADC	Single 3V Supply, 395mW Consumption, 72.4dB SNR, 88dB SFDR, 640MHz Full Power BW

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