

4-Mbit (256K words × 16 bit) Static RAM

Features

- High speed
 - $t_{AA} = 10 \text{ ns} / 15 \text{ ns}$
- Low active and standby currents
 - Active current: $I_{CC} = 38\text{-mA}$ typical
 - Standby current: $I_{SB2} = 6\text{-mA}$ typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 44-pin SOJ, 44-pin TSOP II, and 48-ball VFBGA packages

Functional Description

CY7C1041GN is high-performance CMOS fast static RAM Organized as 256K words by 16-bits.

Data writes are performed by asserting the Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW, while providing the data on I/O₀ through I/O₁₅ and address on A₀ through A₁₇ pins. The Byte High Enable (\overline{BHE}) and Byte Low Enable (\overline{BLE}) inputs control write operations to the upper and lower bytes of the specified memory location. \overline{BHE} controls I/O₈ through I/O₁₅ and \overline{BLE} controls I/O₀ through I/O₇.

Data reads are performed by asserting the Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O₀ through I/O₁₅). Byte accesses can be performed by asserting the required byte enable signal (\overline{BHE} or \overline{BLE}) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O₀ through I/O₁₅) are placed in a high-impedance state during the following events:

- The device is deselected (\overline{CE} HIGH)
- The control signals (\overline{OE} , \overline{BLE} , \overline{BHE}) are de-asserted

The logic block diagram is on page 2.

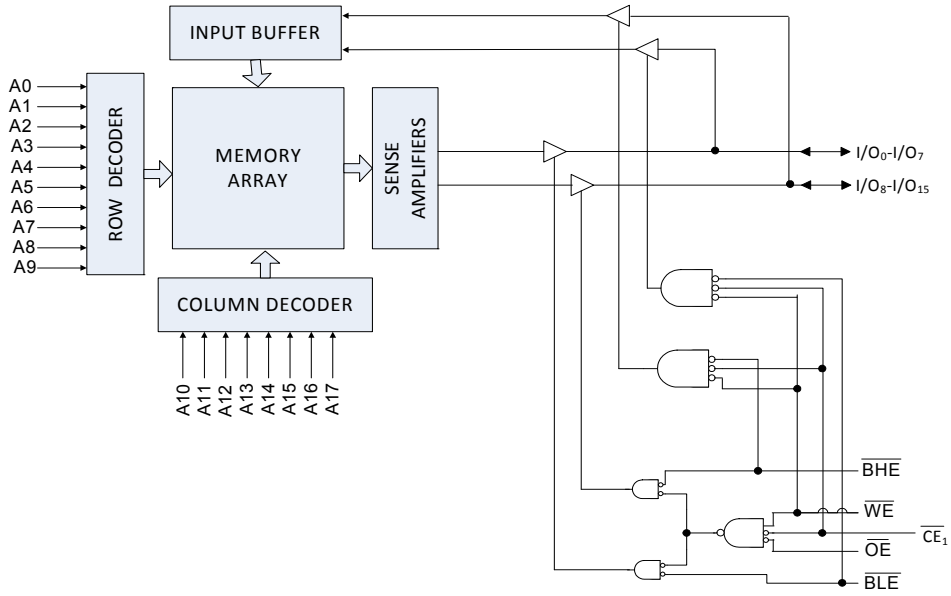
Product Portfolio

| Product | Range | V _{CC} Range (V) | Speed (ns) 10/15 | Power Dissipation | | | |
|--------------|------------|---------------------------|---------------------|--------------------------------|-----|--------------------------------|-----|
| | | | | Operating I _{CC} (mA) | | Standby, I _{SB2} (mA) | |
| | | | | f = f _{max} | | | |
| | | | | Typ ^[1] | Max | Typ ^[1] | Max |
| CY7C1041GN18 | Industrial | 1.65 V–2.2 V | 15 | – | 40 | 6 | 8 |
| CY7C1041GN30 | | 2.2 V–3.6 V | 10 | 38 | 45 | | |
| CY7C1041GN | | 4.5 V–5.5 V | 10 | 38 | 45 | | |

Notes

1. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY7C1041GN



Contents

| | | | |
|---|-----------|--|-----------|
| Pin Configurations | 4 | Package Diagrams | 14 |
| Maximum Ratings | 5 | Acronyms | 16 |
| Operating Range | 5 | Document Conventions | 16 |
| DC Electrical Characteristics | 5 | Units of Measure | 16 |
| Capacitance | 6 | Document History Page | 17 |
| Thermal Resistance | 6 | Sales, Solutions, and Legal Information | 18 |
| AC Test Loads and Waveforms | 6 | Worldwide Sales and Design Support | 18 |
| Data Retention Characteristics | 7 | Products | 18 |
| Data Retention Waveform | 7 | PSoC® Solutions | 18 |
| AC Switching Characteristics | 8 | Cypress Developer Community | 18 |
| Switching Waveforms | 9 | Technical Support | 18 |
| Truth Table | 12 | | |
| Ordering Information | 13 | | |
| Ordering Code Definitions | 13 | | |

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Package/Grade ID: BVXI [2, 3]

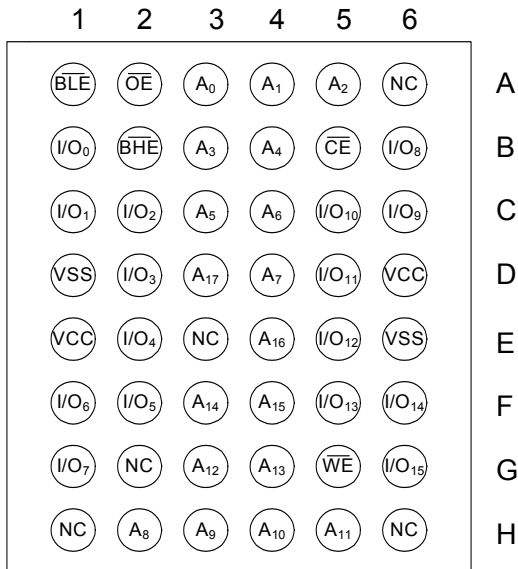


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Package/Grade ID: BVJXI [2]

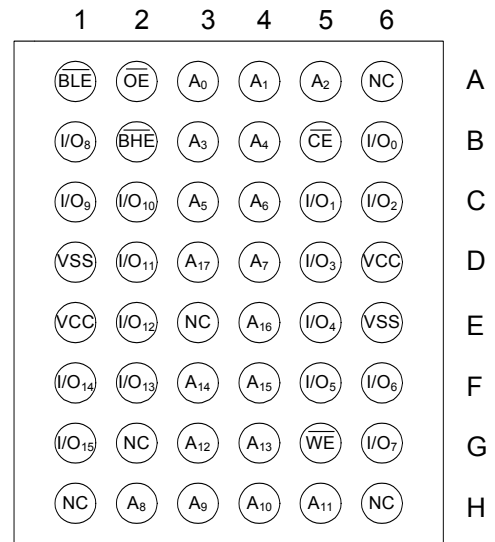
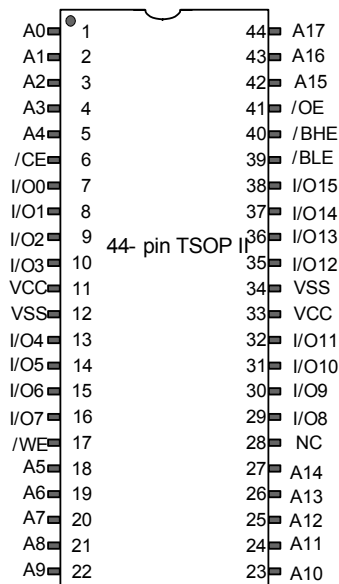


Figure 3. 44-pin TSOP II / 44-pin SOJ pinout [2]



Notes

- 2. NC pins are not connected internally to the die.
- 3. Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O_[7:0] and I/O_[15:8] balls are swapped.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature
with power applied -55 °C to +125 °C

Supply voltage
on V_{CC} relative to GND ^[4] -0.5 V to $V_{CC} + 0.5$ V

DC voltage applied to outputs
in HI-Z State ^[4] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[4] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (in LOW state) 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 140 mA

Operating Range

| Grade | Ambient Temperature | V_{CC} |
|------------|---------------------|---|
| Industrial | -40 °C to +85 °C | 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V |

DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

| Parameter | Description | Test Conditions | 10 ns / 15 ns | | | Unit | |
|-----------|---|---|---|-------------------------------|-----|-------------------------------|----|
| | | | Min | Typ ^[5] | Max | | |
| V_{OH} | Output HIGH voltage | 1.65 V to 2.2 V | $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$ | 1.4 | - | - | V |
| | | 2.2 V to 2.7 V | $V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$ | 2 | - | - | |
| | | 2.7 V to 3.6 V | $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$ | 2.2 | - | - | |
| | | 4.5 V to 5.5 V | $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | - | - | |
| | | 4.5 V to 5.5 V | $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$ | $V_{CC} - 0.5$ ^[6] | - | - | |
| V_{OL} | Output LOW voltage | 1.65 V to 2.2 V | $V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$ | - | - | 0.2 | V |
| | | 2.2 V to 2.7 V | $V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$ | - | - | 0.4 | |
| | | 2.7 V to 3.6 V | $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$ | - | - | 0.4 | |
| | | 4.5 V to 5.5 V | $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$ | - | - | 0.4 | |
| V_{IH} | Input HIGH voltage | 1.65 V to 2.2 V | - | 1.4 | - | $V_{CC} + 0.2$ ^[4] | V |
| | | 2.2 V to 2.7 V | - | 2 | - | $V_{CC} + 0.3$ ^[4] | |
| | | 2.7 V to 3.6 V | - | 2 | - | $V_{CC} + 0.3$ ^[4] | |
| | | 4.5 V to 5.5 V | - | 2.2 | - | $V_{CC} + 0.5$ ^[4] | |
| V_{IL} | Input LOW voltage | 1.65 V to 2.2 V | - | -0.2 ^[4] | - | 0.4 | V |
| | | 2.2 V to 2.7 V | - | -0.3 ^[4] | - | 0.6 | |
| | | 2.7 V to 3.6 V | - | -0.3 ^[4] | - | 0.8 | |
| | | 4.5 V to 5.5 V | - | -0.5 ^[4] | - | 0.8 | |
| I_{IX} | Input leakage current | $GND \leq V_{IN} \leq V_{CC}$ | -1 | - | +1 | μA | |
| I_{OZ} | Output leakage current | $GND \leq V_{OUT} \leq V_{CC}$, Output disabled | -1 | - | +1 | μA | |
| I_{CC} | Operating supply current | Max V_{CC} , $I_{OUT} = 0 \text{ mA}$, CMOS levels | f = 100 MHz | - | 38 | 45 | mA |
| | | | f = 66.7 MHz | - | - | 40 | |
| I_{SB1} | Automatic CE power-down current – TTL inputs | Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX} | - | - | 15 | mA | |
| I_{SB2} | Automatic CE power-down current – CMOS inputs | Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, f = 0 | - | 6 | 8 | mA | |

Notes

4. $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 2 ns.

5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8 \text{ V}$ (for V_{CC} range of 1.65 V–2.2 V), $V_{CC} = 3 \text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), and $V_{CC} = 5 \text{ V}$ (for V_{CC} range of 4.5 V–5.5 V), $T_A = 25 \text{ }^\circ\text{C}$.

6. This parameter is guaranteed by design and not tested.

Capacitance

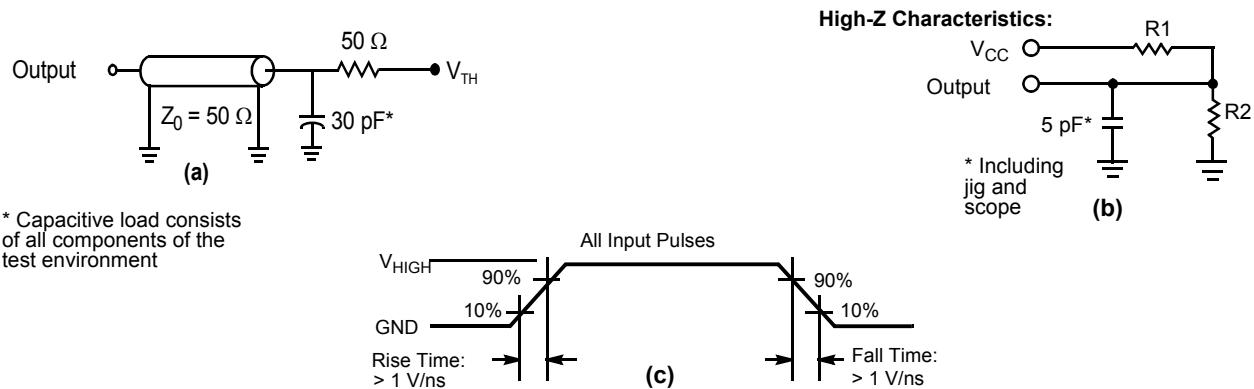
| Parameter [7] | Description | Test Conditions | 48-ball VFBGA | 44-pin SOJ | 44-pin TSOP II | Unit |
|---------------|-------------------|--|---------------|------------|----------------|------|
| C_{IN} | Input capacitance | $T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC}(\text{typ})$ | 10 | 10 | 10 | pF |
| C_{OUT} | I/O capacitance | | 10 | 10 | 10 | pF |

Thermal Resistance

| Parameter [7] | Description | Test Conditions | 48-ball VFBGA | 44-pin SOJ | 44-pin TSOP II | Unit |
|---------------|--|--|---------------|------------|----------------|--------------------|
| Θ_{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3×4.5 inch, four-layer printed circuit board | 31.35 | 55.37 | 68.85 | $^\circ\text{C/W}$ |
| Θ_{JC} | Thermal resistance (junction to case) | | 14.74 | 30.41 | 15.97 | $^\circ\text{C/W}$ |

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms [8]



* Capacitive load consists of all components of the test environment

| Parameters | 1.8 V | 3.0 V | 5.0 V | Unit |
|------------|-------|-------|-------|----------|
| R1 | 1667 | 317 | 317 | Ω |
| R2 | 1538 | 351 | 351 | Ω |
| V_{TH} | 0.9 | 1.5 | 1.5 | V |
| V_{HIGH} | 1.8 | 3 | 3 | V |

Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full-device AC operation assumes a $100\text{-}\mu\text{s}$ ramp time from 0 to $V_{CC}(\text{min})$ and a $100\text{-}\mu\text{s}$ wait time after V_{CC} stabilization.

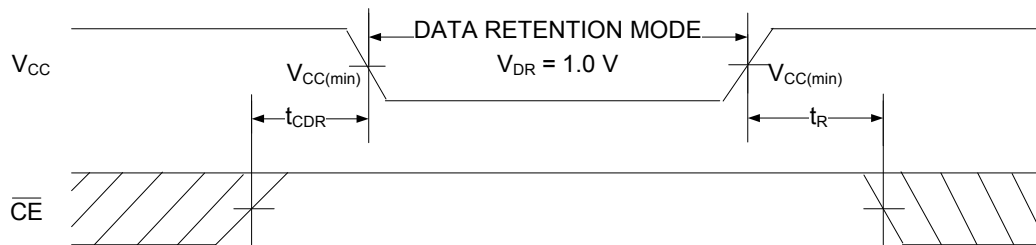
Data Retention Characteristics

Over the operating range of -40 °C to 85 °C

| Parameter | Description | Conditions | Min | Max | Unit |
|---------------------------|--------------------------------------|--|-----|-----|------|
| V_{DR} | V_{CC} for data retention | | 1 | - | V |
| I_{CCDR} | Data retention current | $V_{CC} = 1.2\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ ^[9] , $V_{IN} \geq V_{CC} - 0.2\text{ V}$, or $V_{IN} \leq 0.2\text{ V}$ | - | 8 | mA |
| t_{CDR} ^[10] | Chip deselect to data retention time | | 0 | - | ns |
| t_R ^[9, 10] | Operation recovery time | $V_{CC} \geq 2.2\text{ V}$ | 10 | - | ns |
| | | $V_{CC} < 2.2\text{ V}$ | 15 | - | ns |

Data Retention Waveform

Figure 5. Data Retention Waveform ^[9]



Notes

- 9. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 100\ \mu\text{s}$ or stable at $V_{CC(min)}$ $\geq 100\ \mu\text{s}$.
- 10. These parameters are guaranteed by design.

AC Switching Characteristics

Over the operating range of $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

| Parameter ^[11] | Description | 10 ns | | 15 ns | | Unit |
|--|--|-------|-----|-------|-----|------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t_{RC} | Read cycle time | 10 | – | 15 | – | ns |
| t_{AA} | Address to data | – | 10 | – | 15 | ns |
| t_{OHA} | Data hold from address change | 3 | – | 3 | – | ns |
| t_{ACE} | \overline{CE} LOW to data ^[12] | – | 10 | – | 15 | ns |
| t_{DOE} | \overline{OE} LOW to data | – | 4.5 | – | 8 | ns |
| t_{LZOE} | \overline{OE} LOW to low impedance ^[13, 14] | 0 | – | 0 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to HI-Z ^[13, 14] | – | 5 | – | 8 | ns |
| t_{LZCE} | \overline{CE} LOW to low impedance ^[12, 13, 14] | 3 | – | 3 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to HI-Z ^[12, 13, 14] | – | 5 | – | 8 | ns |
| t_{PU} | \overline{CE} LOW to power-up ^[12, 14, 15] | 0 | – | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to power-down ^[12, 14, 15] | – | 10 | – | 15 | ns |
| t_{DBE} | Byte enable to data valid | – | 4.5 | – | 8 | ns |
| t_{LZBE} | Byte enable to low impedance ^[14] | 0 | – | 0 | – | ns |
| t_{HZBE} | Byte disable to HI-Z ^[14] | – | 6 | – | 8 | ns |
| Write Cycle ^[15, 16] | | | | | | |
| t_{WC} | Write cycle time | 10 | – | 15 | – | ns |
| t_{SCE} | \overline{CE} LOW to write end ^[12] | 7 | – | 12 | – | ns |
| t_{AW} | Address setup to write end | 7 | – | 12 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 7 | – | 12 | – | ns |
| t_{SD} | Data setup to write end | 5 | – | 8 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | 0 | – | ns |
| t_{LZWE} | \overline{WE} HIGH to low impedance ^[13, 14] | 3 | – | 3 | – | ns |
| t_{HZWE} | \overline{WE} LOW to HI-Z ^[13, 14] | – | 5 | – | 8 | ns |
| t_{BW} | Byte Enable to write end | 7 | – | 12 | – | ns |

Notes

- Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3\text{ V}$) and $V_{CC}/2$ (for $V_{CC} < 3\text{ V}$), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3\text{ V}$) and 0 to V_{CC} (for $V_{CC} < 3\text{ V}$). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 4 on page 6, unless specified otherwise.
- For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} , t_{LZOE} , t_{LZCE} , t_{LZWE} , and t_{LZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 4 on page 6. Transition is measured $\pm 200\text{ mV}$ from steady state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and \overline{BHE} or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle pulse width in Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled) [17, 18]

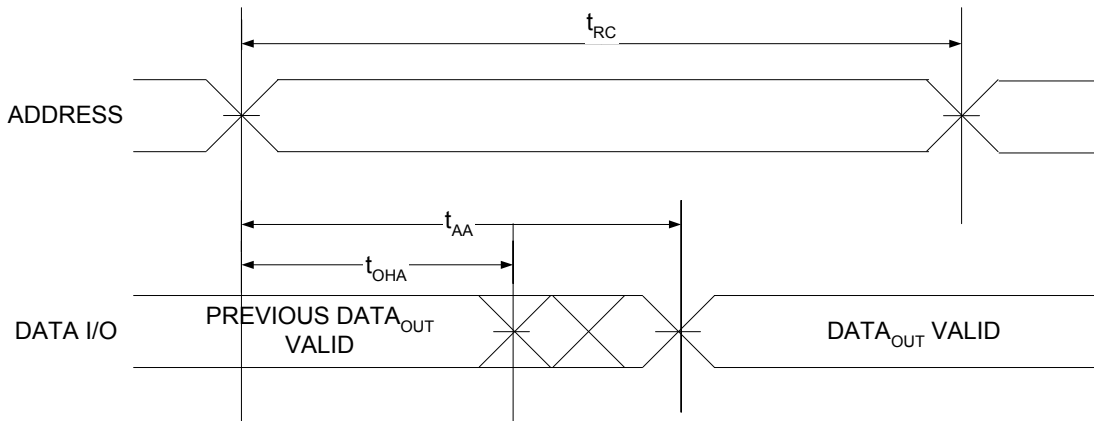
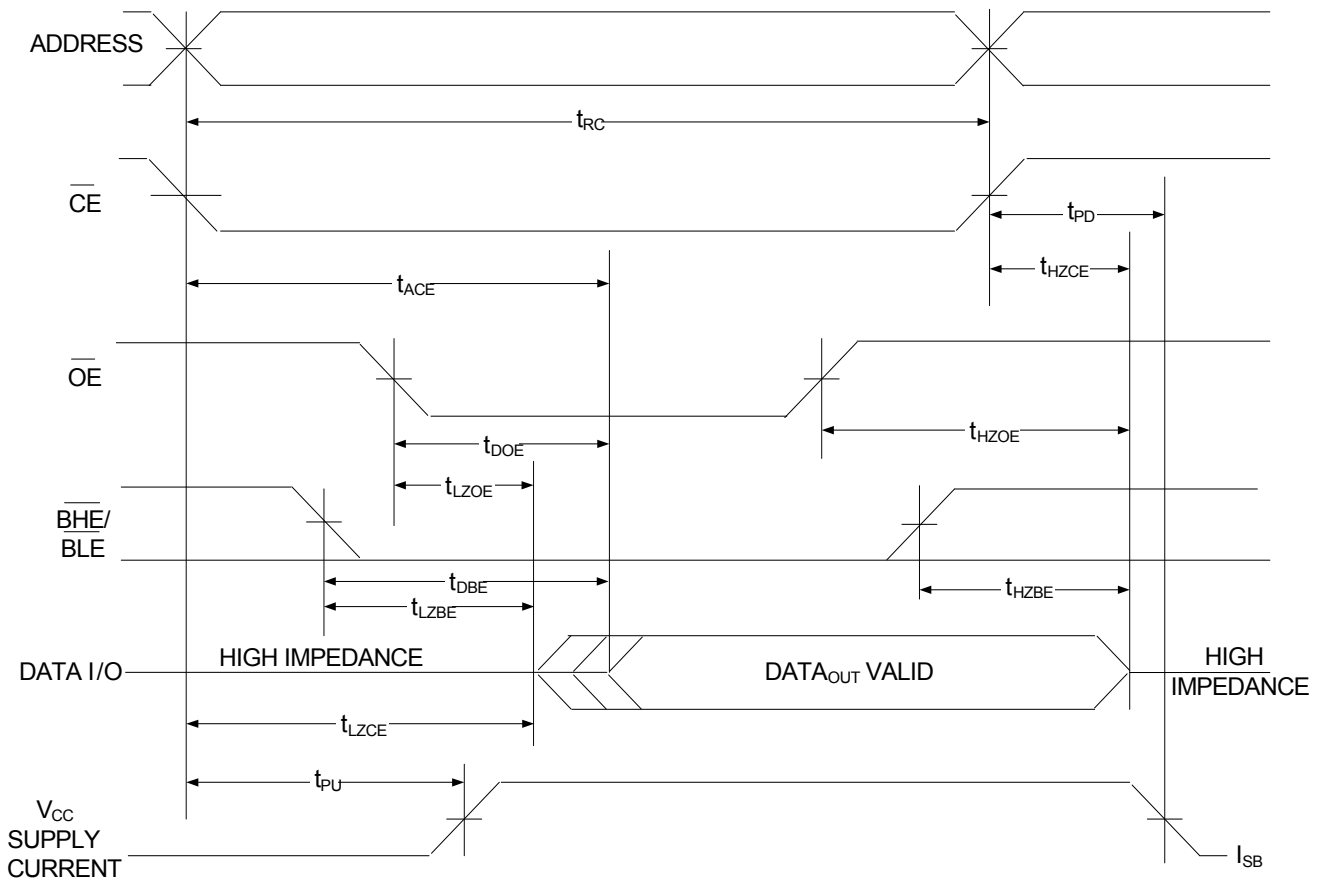


Figure 7. Read Cycle No. 2 (\overline{OE} Controlled) [18, 19]



Notes

- 17. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} .
- 18. \overline{WE} is HIGH for the read cycle.
- 19. Address valid prior to or coincident with \overline{CE} LOW transition.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [20, 21]

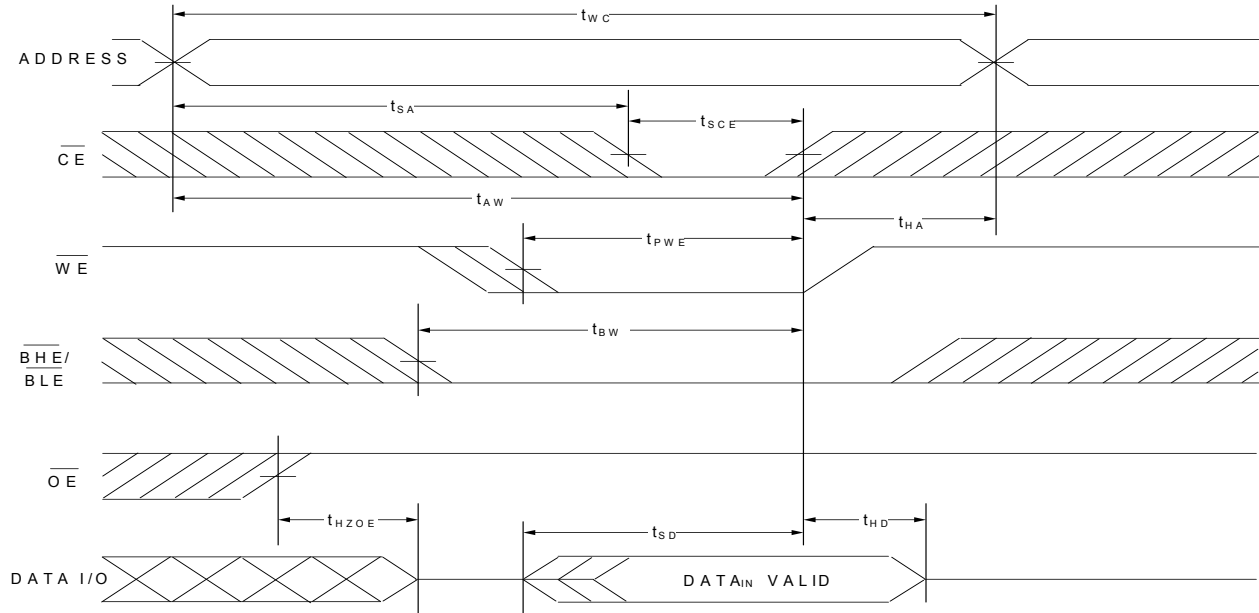
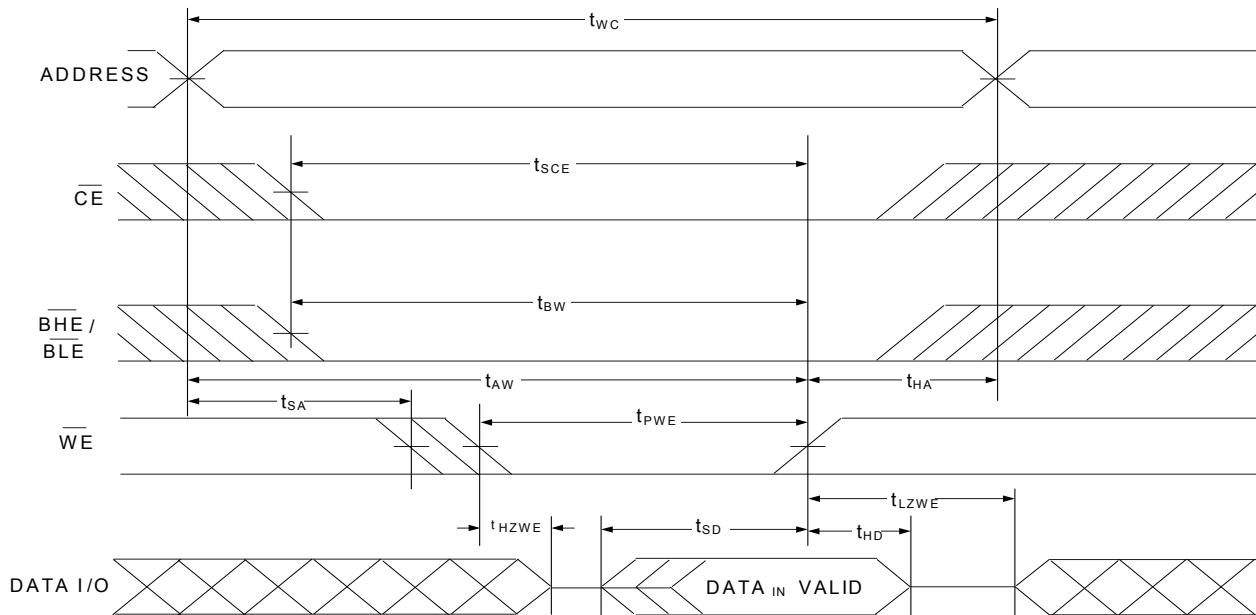


Figure 9. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [20, 21, 22]



Notes

- 20. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 21. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$, or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
- 22. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE} .

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled) [23, 24]

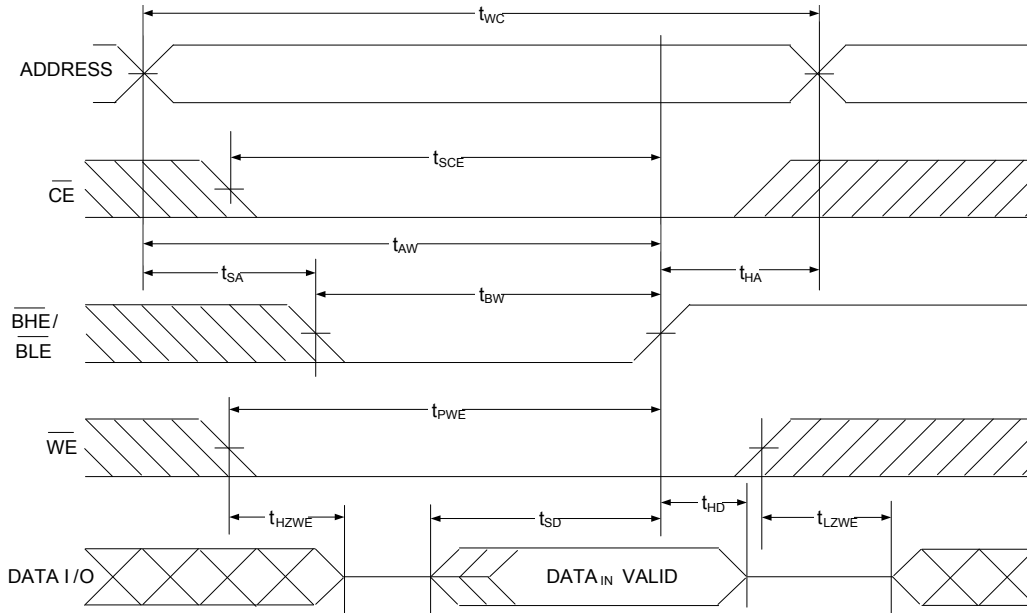
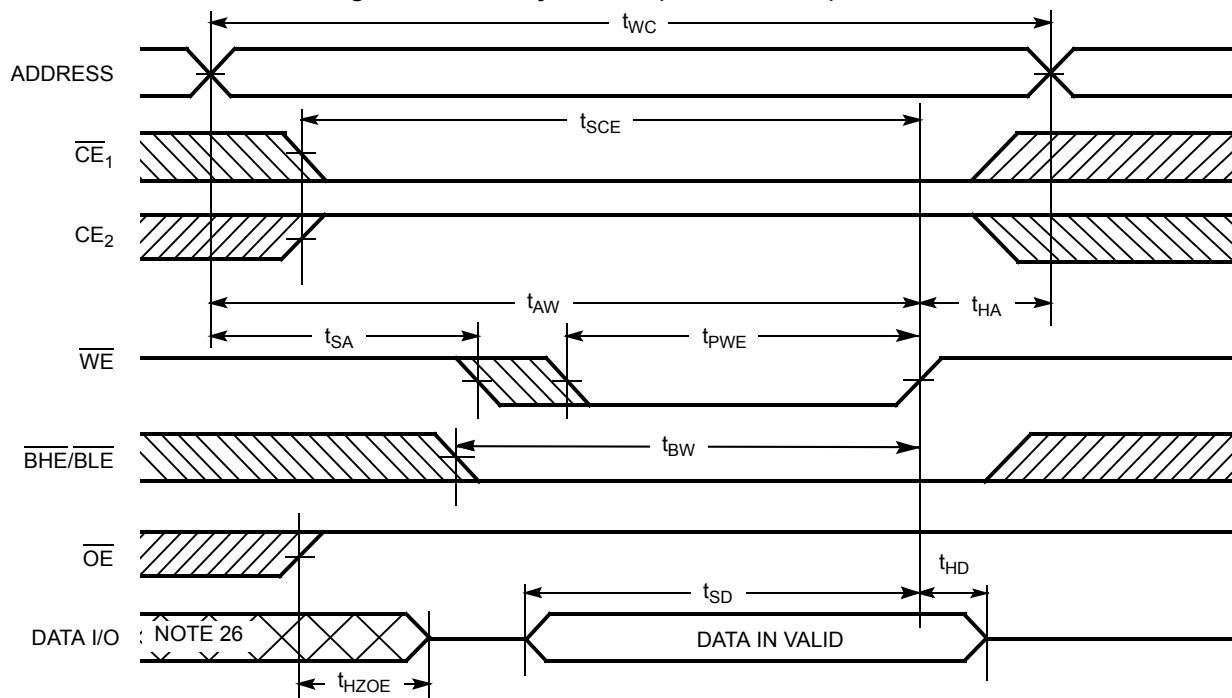


Figure 11. Write Cycle No. 4 ($\overline{\text{WE}}$ Controlled) [23, 24, 25]



Notes

23. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

24. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{\text{IH}}$, $\overline{\text{OE}} = V_{\text{IH}}$, or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.

25. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.

26. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

| \overline{CE} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O ₀ –I/O ₇ | I/O ₈ –I/O ₁₅ | Mode | Power |
|-----------------|-------------------|-------------------|-------------------|-------------------|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H | X ^[27] | X ^[27] | X ^[27] | X ^[27] | HI-Z | HI-Z | Power down | Standby (I _{SB}) |
| L | L | H | L | L | Data out | Data out | Read all bits | Active (I _{CC}) |
| L | L | H | L | H | Data out | HI-Z | Read lower bits only | Active (I _{CC}) |
| L | L | H | H | L | HI-Z | Data out | Read upper bits only | Active (I _{CC}) |
| L | X | L | L | L | Data in | Data in | Write all bits | Active (I _{CC}) |
| L | X | L | L | H | Data in | HI-Z | Write lower bits only | Active (I _{CC}) |
| L | X | L | H | L | HI-Z | Data in | Write upper bits only | Active (I _{CC}) |
| L | H | H | X | X | HI-Z | HI-Z | Selected, outputs disabled | Active (I _{CC}) |

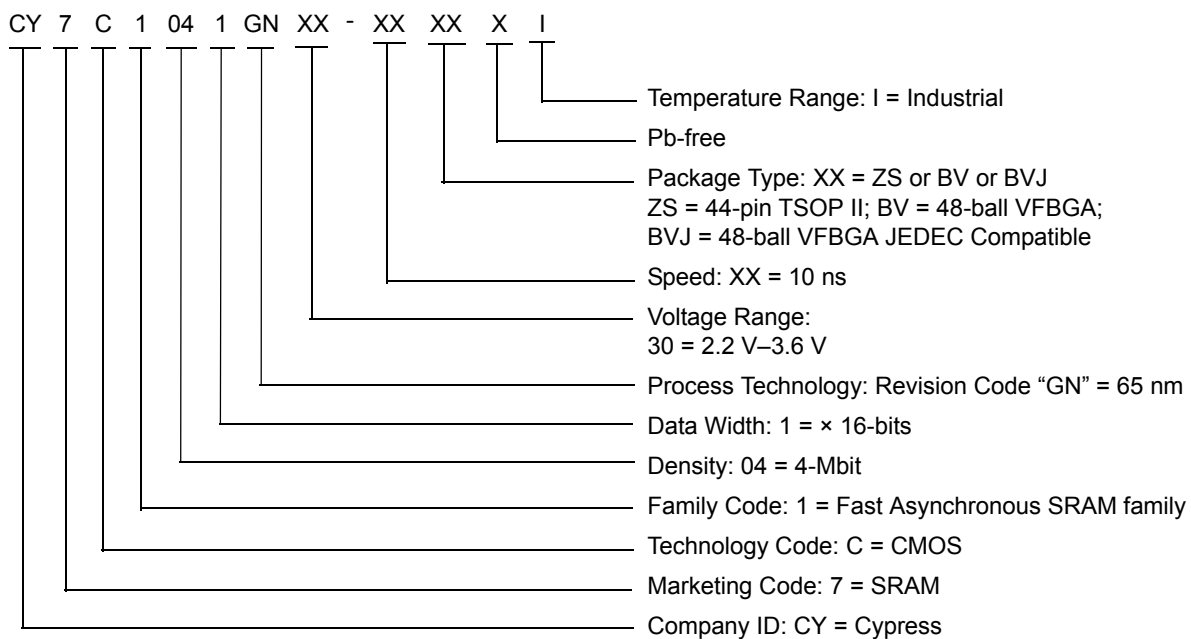
Notes

27. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

| Speed (ns) | Voltage Range | Ordering Code | Package Diagram | Package Type (all Pb-free) | Operating Range |
|------------|---------------|----------------------|-----------------|--|-----------------|
| 10 | 2.2 V–3.6 V | CY7C1041GN30-10ZSXI | 51-85087 | 44-pin TSOP II | Industrial |
| | | CY7C1041GN30-10BVXI | 51-85150 | 48-ball VFBGA (6 × 8 × 1.0 mm) | |
| | | CY7C1041GN30-10BVJXI | 51-85150 | 48-ball VFBGA (6 × 8 × 1.0 mm), JEDEC Compatible | |
| | 4.5 V–5.5 V | CY7C1041GN-10ZSXI | | 44-pin TSOP II | |

Ordering Code Definitions



Package Diagrams

Figure 12. 44-pin TSOP II (Z44) Package Outline, 51-85087

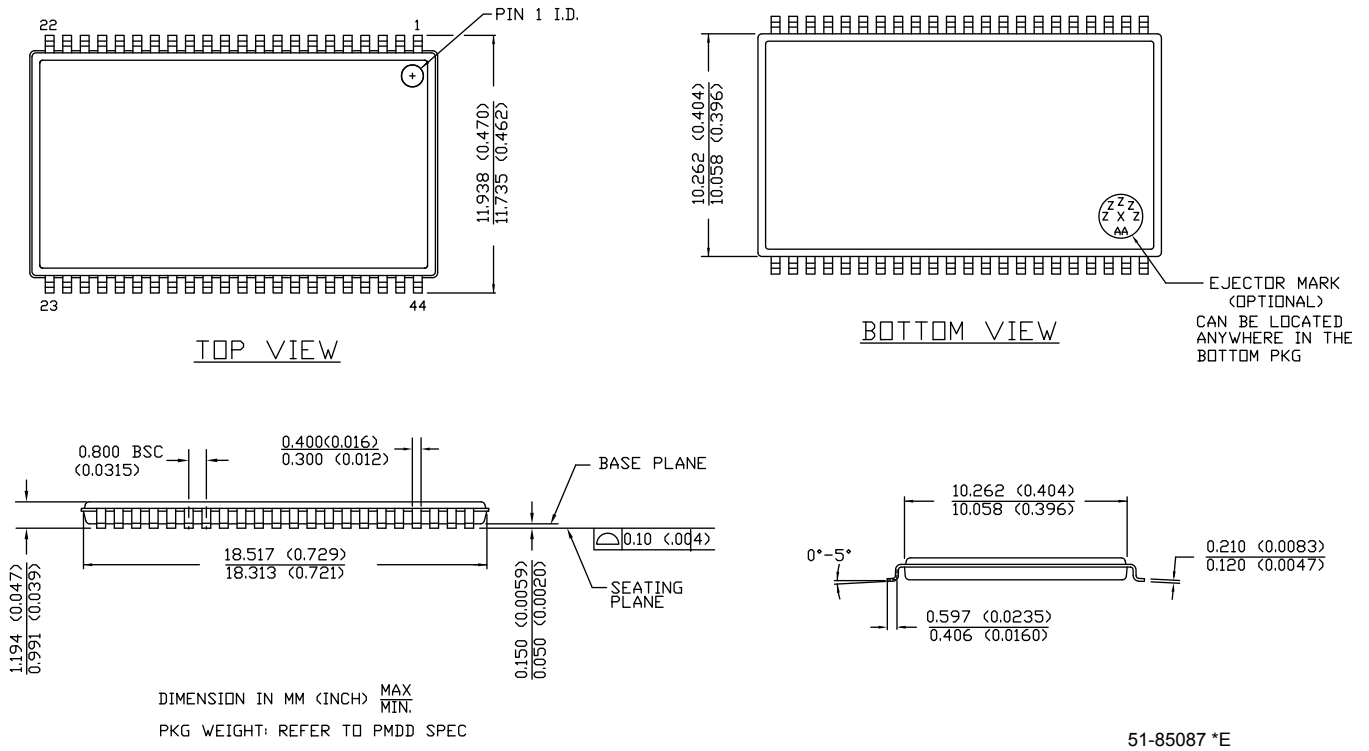
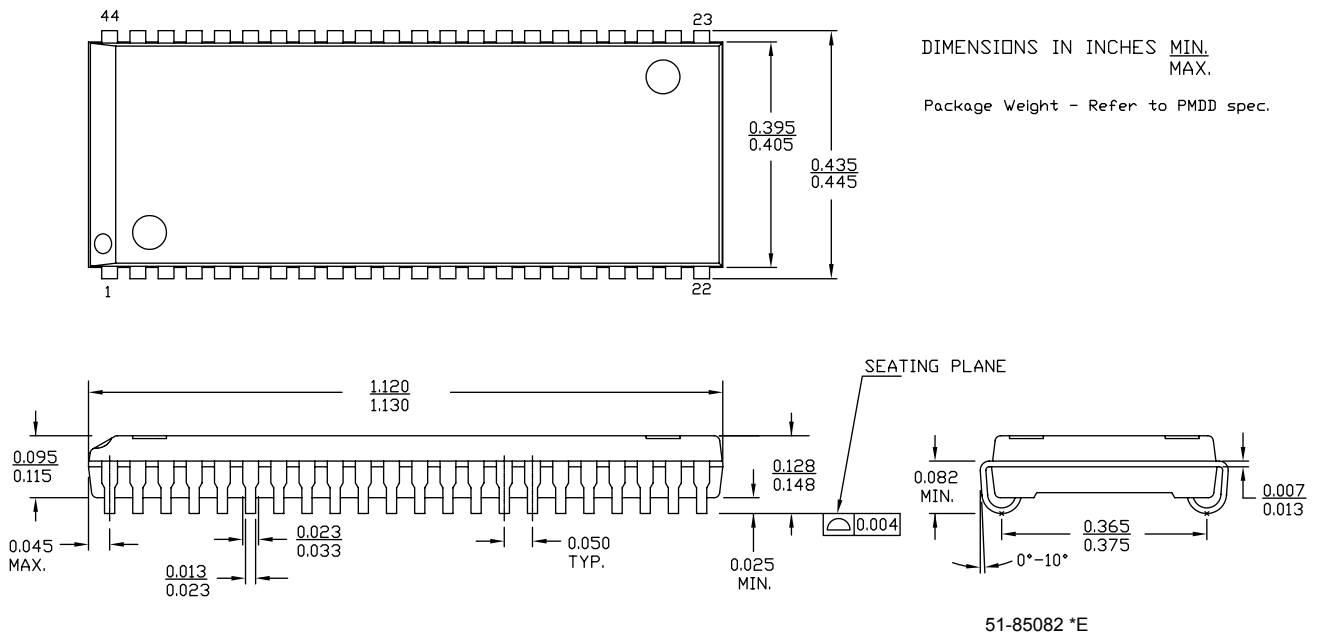
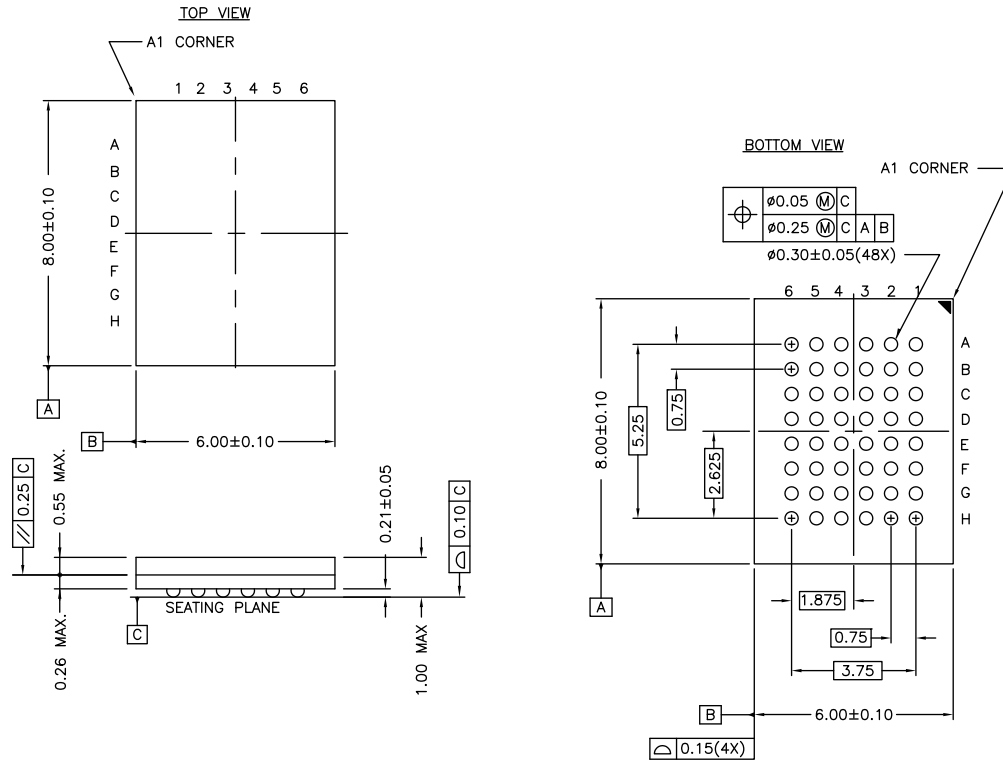


Figure 13. 44-pin SOJ (400 Mils) Package Outline, 51-85082



Package Diagrams (continued)

Figure 14. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

| Acronym | Description |
|-------------------------|---|
| $\overline{\text{BHE}}$ | byte high enable |
| $\overline{\text{BLE}}$ | byte low enable |
| $\overline{\text{CE}}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| $\overline{\text{OE}}$ | output enable |
| SRAM | static random-access memory |
| TSOP | thin small outline package |
| TTL | transistor-transistor logic |
| VFBGA | very fine-pitch ball grid array |
| $\overline{\text{WE}}$ | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | Degrees Celsius |
| MHz | megahertz |
| μA | microamperes |
| μs | microseconds |
| mA | milliamperes |
| mm | millimeters |
| ns | nanoseconds |
| Ω | ohms |
| % | percent |
| pF | picofarads |
| V | volts |
| W | watts |

Document History Page

| Document Title: CY7C1041GN, 4-Mbit (256K words × 16 bit) Static RAM Document Number: 001-95413 | | | | |
|---|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | 5074414 | NILE | 01/06/2016 | New data sheet. |
| *A | 5082573 | NILE | 01/12/2016 | Updated Logic Block Diagram – CY7C1041GN . Updated Ordering Information : Updated part numbers. |
| *B | 5120171 | VINI | 02/01/2016 | Updated Logic Block Diagram – CY7C1041GN . |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|--|---|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc |
| Memory | cypress.com/go/memory |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC[®] Solutions

[psoc.cypress.com/solutions](#)
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2016. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.



Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331