# MC74HC4316A

# Quad Analog Switch/ Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies

## High−Performance Silicon−Gate CMOS

The MC74HC4316A utilizes silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF−channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full analog power−supply range (from $V_{CC}$ to $V_{EE}$).

The HC4316A is similar in function to the metal−gate CMOS MC14016 and MC14066, and to the High−Speed CMOS HC4066A. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances ($R_{ON}$) are much more linear over input voltage than $R_{ON}$ of metal−gate CMOS analog switches. Logic−level translators are provided so that the On/Off Control and Enable logic−level voltages need only be $V_{CC}$ and GND, while the switch is passing signals ranging between $V_{CC}$ and $V_{EE}$. When the Enable pin (active−low) is high, all four analog switches are turned off.

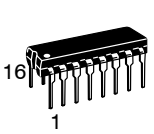
### Features

- Logic−Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power−Supply Voltage Range ($V_{CC} - V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power−Supply Voltage Range ($V_{CC}$ − GND) = 2.0 V to 6.0 V, Independent of $V_{EE}$
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

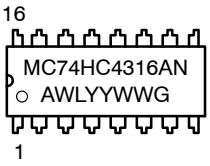
**ON Semiconductor®**

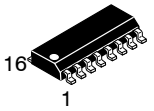
**http://onsemi.com**

**MARKING DIAGRAMS**

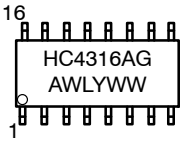


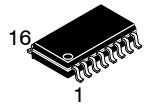

**PDIP−16**
**N SUFFIX**
**CASE 648**



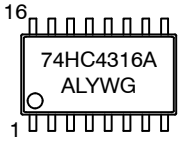




**SOIC−16**
**D SUFFIX**
**CASE 751B**




**SOEIAJ−16**
**F SUFFIX**
**CASE 966**




| | |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G | = Pb−Free Package |

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC74HC4316ANG | PDIP−16 (Pb−Free) | 500 Units / Box |
| MC74HC4316ADR2G | SOIC−16 (Pb−Free) | 2500/Tape&Reel |
| MC74HC4316AFELG | SOEIAJ−16 (Pb−Free) | 50/Tape&Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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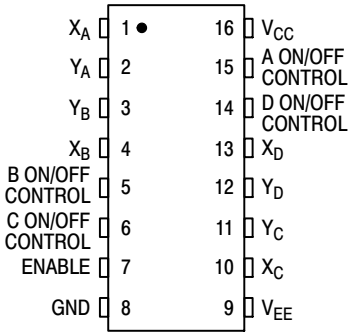



**Figure 1. Pin Assignment**

**FUNCTION TABLE**

| Inputs | | State of Analog Switch |
|---|---|---|
| Enable | On/Off Control | |
| L | H | On |
| L | L | Off |
| H | X | Off |

X = Don't Care.

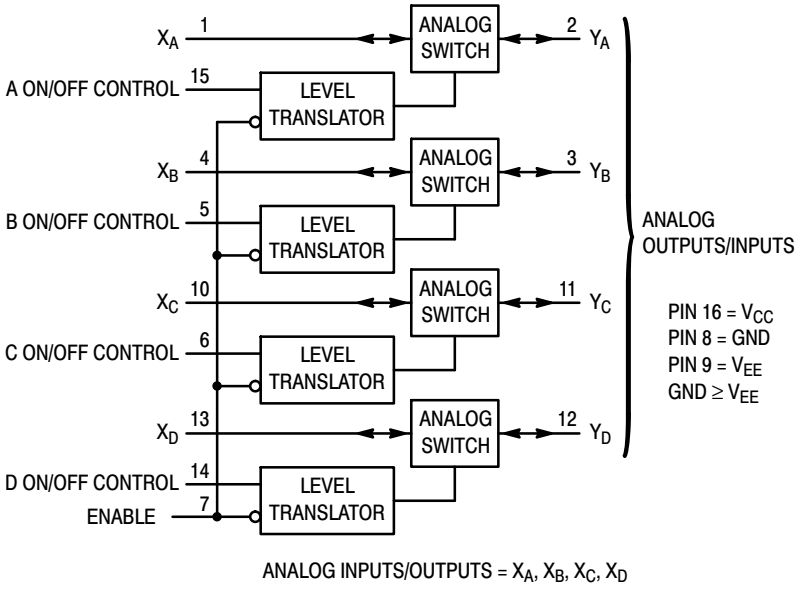



**Figure 2. Logic Diagram**

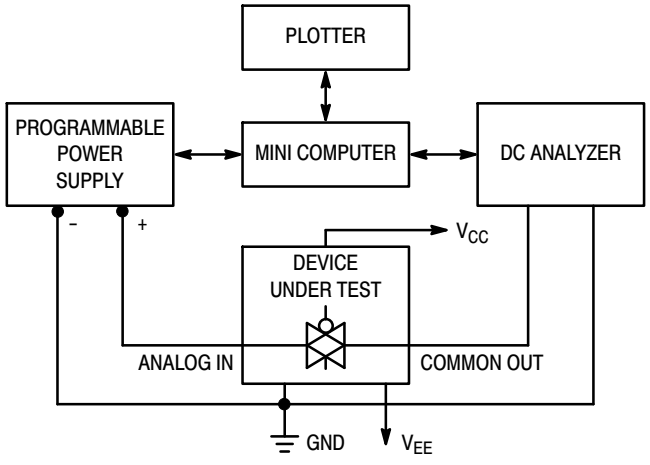



**Figure 3. On Resistance Test Set−Up**

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | (Ref. to GND)<br>(Ref. to $V_{EE}$) | − 0.5 to + 7.0<br>− 0.5 to + 14.0 | V |
| $V_{EE}$ | Negative DC Supply Voltage (Ref. to GND) | | − 7.0 to + 0.5 | V |
| $V_{IS}$ | Analog Input Voltage | | $V_{EE}$ − 0.5 to $V_{CC}$ + 0.5 | V |
| $V_{in}$ | DC Input Voltage (Ref. to GND) | | − 0.5 to $V_{CC}$ + 0.5 | V |
| I | DC Current Into or Out of Any Pin | | ± 25 | mA |
| $P_D$ | Power Dissipation in Still Air | Plastic DIP*<br>EIAJ/SOIC Package*<br>TSSOP Package* | 750<br>500<br>450 | mW |
| $T_{stg}$ | Storage Temperature | | − 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, SOIC or TSSOP Package) | | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*Derating − Plastic DIP: − 10 mW/°C from 65° to 125°C
EIAJ/SOIC Package: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage (Ref. to GND) | | 2.0 | 6.0 | V |
| $V_{EE}$ | Negative DC Supply Voltage (Ref. to GND) | | − 6.0 | GND | V |
| $V_{IS}$ | Analog Input Voltage | | $V_{EE}$ | $V_{CC}$ | V |
| $V_{in}$ | Digital Input Voltage (Ref. to GND) | | GND | $V_{CC}$ | V |
| $V_{IO}$* | Static or Dynamic Voltage Across Switch | | − | 1.2 | V |
| $T_A$ | Operating Temperature, All Package Types | | − 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time<br>(Control or Enable Inputs)<br>(Figure 10) | $V_{CC}$ = 2.0 V<br>$V_{CC}$ = 3.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | 0<br>0<br>0<br>0 | 1000<br>600<br>500<br>400 | ns |

*For voltage drops across the switch greater than 1.2 V (switch on), excessive $V_{CC}$ current may be drawn; i.e., the current out of the switch may contain both $V_{CC}$ and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

**DC ELECTRICAL CHARACTERISTICS** Digital Section (Voltages Referenced to GND) $V_{EE}$ = GND Except Where Noted

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High–Level Voltage, Control or Enable Inputs | $R_{on}$ = Per Spec | 2.0<br>3.0<br>4.5<br>6.0 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | V |
| $V_{IL}$ | Maximum Low–Level Voltage, Control or Enable Inputs | $R_{on}$ = Per Spec | 2.0<br>3.0<br>4.5<br>6.0 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | V |
| $I_{in}$ | Maximum Input Leakage Current, Control or Enable Inputs | $V_{in}$ = $V_{CC}$ or GND<br>$V_{EE}$ = – 6.0 V | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$V_{IO}$ = 0 V $V_{EE}$ = GND<br>$V_{EE}$ = – 6.0 | <br>6.0<br>6.0 | <br>2<br>4 | <br>20<br>40 | <br>40<br>160 | μA |

**DC ELECTRICAL CHARACTERISTICS** Analog Section (Voltages Referenced to $V_{EE}$)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $V_{EE}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $R_{on}$ | Maximum “ON” Resistance | $V_{in}$ = $V_{IH}$<br>$V_{IS}$ = $V_{CC}$ to $V_{EE}$<br>$I_S$ ≤ 2.0 mA (Figure 3) | 2.0*<br>4 5<br>4.5<br>6.0 | 0.0<br>0.0<br>– 4.5<br>– 6.0 | –<br>160<br>90<br>90 | –<br>200<br>110<br>110 | –<br>240<br>130<br>130 | Ω |
| | | $V_{in}$ = $V_{IH}$<br>$V_{IS}$ = $V_{CC}$ or $V_{EE}$ (Endpoints)<br>$I_S$ ≤ 2.0 mA (Figure 3) | 2.0<br>4.5<br>4.5<br>6.0 | 0.0<br>0.0<br>– 4.5<br>– 6.0 | –<br>90<br>70<br>70 | –<br>115<br>90<br>90 | –<br>140<br>105<br>105 | |
| $\Delta R_{on}$ | Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package | $V_{in}$ = $V_{IH}$<br>$V_{IS}$ = 1/2 ($V_{CC}$ – $V_{EE}$)<br>$I_S$ ≤ 2.0 mA | 2.0<br>4.5<br>4.5<br>6.0 | 0.0<br>0.0<br>– 4.5<br>– 6.0 | –<br>20<br>15<br>15 | –<br>25<br>20<br>20 | –<br>30<br>25<br>25 | Ω |
| $I_{off}$ | Maximum Off–Channel Leakage Current, Any One Channel | $V_{in}$ = $V_{IL}$<br>$V_{IO}$ = $V_{CC}$ or $V_{EE}$<br>Switch Off (Figure 4) | 6.0 | – 6.0 | 0.1 | 0.5 | 1.0 | μA |
| $I_{on}$ | Maximum On–Channel Leakage Current, Any One Channel | $V_{in}$ = $V_{IH}$<br>$V_{IS}$ = $V_{CC}$ or $V_{EE}$<br>(Figure 5) | 6.0 | – 6.0 | 0.1 | 0.5 | 1.0 | μA |

*At supply voltage ($V_{CC}$ – $V_{EE}$) approaching 2.0 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Control or Enable $t_r = t_f$ = 6 ns, $V_{EE}$ = GND)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Analog Input to Analog Output (Figures 9 and 10) | 2.0<br>4.5<br>6.0 | 40<br>6<br>5 | 50<br>8<br>7 | 60<br>9<br>8 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Control or Enable to Analog Output (Figures 11 and 12) | 2.0<br>4.5<br>6.0 | 130<br>40<br>30 | 160<br>50<br>40 | 200<br>60<br>50 | ns |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay, Control or Enable to Analog Output (Figures 11 and 12) | 2.0<br>4.5<br>6.0 | 140<br>40<br>30 | 175<br>50<br>40 | 250<br>60<br>50 | ns |
| C | Maximum Capacitance — ON/OFF Control and Enable Inputs | – | 10 | 10 | 10 | pF |
| | Control Input = GND<br>Analog I/O<br>Feedthrough | <br>–<br>– | <br>35<br>1.0 | <br>35<br>1.0 | <br>35<br>1.0 | |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Switch) (Figure 14)* | 15 | pF |

*Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

**ADDITIONAL APPLICATION CHARACTERISTICS** (GND = 0 V)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $V_{EE}$ V | Limit* 25°C | Unit |
|---|---|---|---|---|---|---|
| BW | Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6) | $f_{in}$ = 1 MHz Sine Wave<br>Adjust $f_{in}$ Voltage to Obtain 0 dBm at $V_{OS}$<br>Increase $f_{in}$ Frequency Until dB Meter Reads – 3 dB<br>$R_L$ = 50 Ω, $C_L$ = 10 pF | 2.25<br>4.50<br>6.00 | – 2.25<br>– 4.50<br>– 6.00 | 150<br>160<br>160 | MHz |
| – | Off–Channel Feedthrough Isolation (Figure 7) | $f_{in}$ ≡ Sine Wave<br>Adjust $f_{in}$ Voltage to Obtain 0 dBm at $V_{IS}$<br>$f_{in}$ = 10 kHz, $R_L$ = 600 Ω, $C_L$ = 50 pF | 2.25<br>4.50<br>6.00 | – 2.25<br>– 4.50<br>– 6.00 | – 50<br>– 50<br>– 50 | dB |
| | | $f_{in}$ = 1.0 MHz, $R_L$ = 50 Ω, $C_L$ = 10 pF | 2.25<br>4.50<br>6.00 | – 2.25<br>– 4.50<br>– 6.00 | – 40<br>– 40<br>– 40 | |
| – | Feedthrough Noise, Control to Switch (Figure 8) | $V_{in}$ ≤ 1 MHz Square Wave ($t_r = t_f$ = 6 ns)<br>Adjust $R_L$ at Setup so that $I_S$ = 0 A<br>$R_L$ = 600 Ω, $C_L$ = 50 pF | 2.25<br>4.50<br>6.00 | – 2.25<br>– 4.50<br>– 6.00 | 30<br>65<br>100 | $mV_{PP}$ |
| | | $R_L$ = 10 kΩ, $C_L$ = 10 pF | 2.25<br>4.50<br>6.00 | – 2.25<br>– 4.50<br>– 6.00 | 60<br>130<br>200 | |
| – | Crosstalk Between Any Two Switches (Figure 13) | $f_{in}$ ≡ Sine Wave<br>Adjust $f_{in}$ Voltage to Obtain 0 dBm at $V_{IS}$<br>$f_{in}$ = 10 kHz, $R_L$ = 600 Ω, $C_L$ = 50 pF | 2.25<br>4.50<br>6.00 | – 2.25<br>– 4.50<br>– 6.00 | – 70<br>– 70<br>– 70 | dB |
| | | $f_{in}$ = 1.0 MHz, $R_L$ = 50 Ω, $C_L$ = 10 pF | 2.25<br>4.50<br>6.00 | – 2.25<br>– 4.50<br>– 6.00 | – 80<br>– 80<br>– 80 | |
| THD | Total Harmonic Distortion (Figure 15) | $f_{in}$ = 1 kHz, $R_L$ = 10 kΩ, $C_L$ = 50 pF<br>$THD = THD_{Measured} - THD_{Source}$<br>$V_{IS}$ = 4.0 $V_{PP}$ sine wave<br>$V_{IS}$ = 8.0 $V_{PP}$ sine wave<br>$V_{IS}$ = 11.0 $V_{PP}$ sine wave | <br><br>2.25<br>4.50<br>6.00 | <br><br>– 2.25<br>– 4.50<br>– 6.00 | <br><br>0.10<br>0.06<br>0.04 | % |

*Limits not tested. Determined by design and verified by qualification.

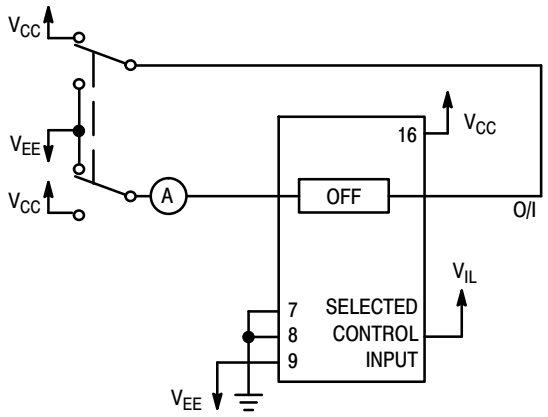



**Figure 4. Maximum Off Channel Leakage Current, Any One Channel, Test Set−Up**

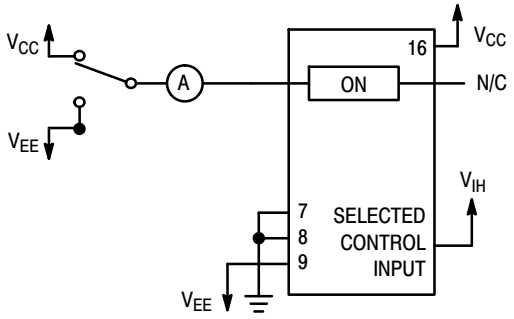
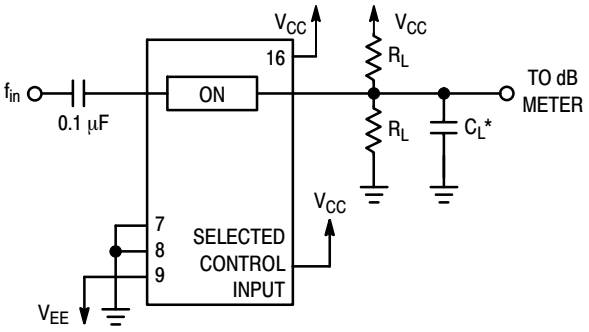
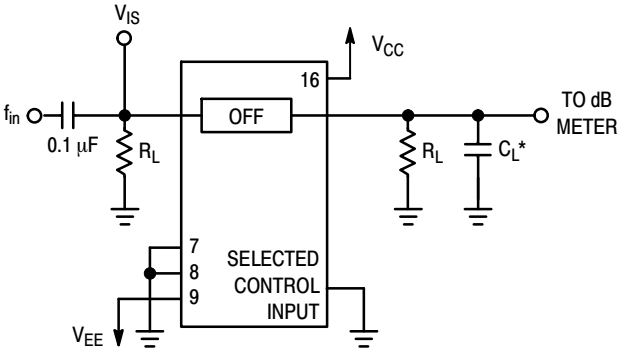



**Figure 5. Maximum On Channel Leakage Current, Test Set−Up**



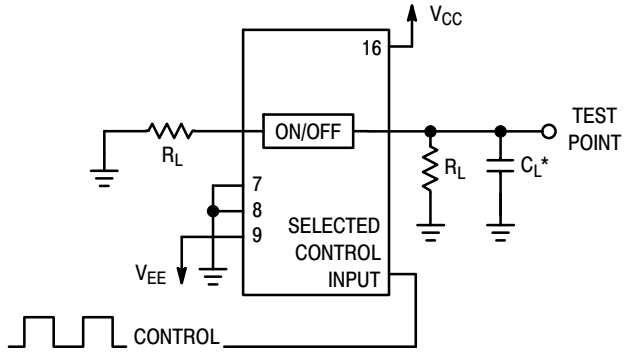

*Includes all probe and jig capacitance.

**Figure 6. Maximum On−Channel Bandwidth Test Set−Up**




*Includes all probe and jig capacitance.

**Figure 7. Off−Channel Feedthrough Isolation, Test Set−Up**




*Includes all probe and jig capacitance.

**Figure 8. Feedthrough Noise, Control to Analog Out, Test Set−Up**

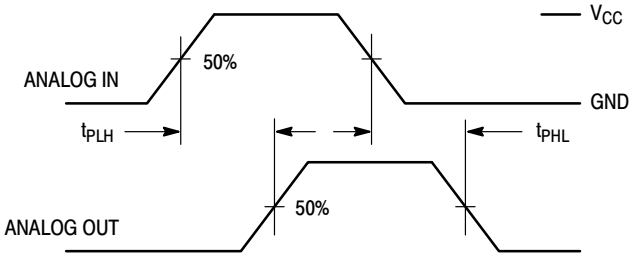
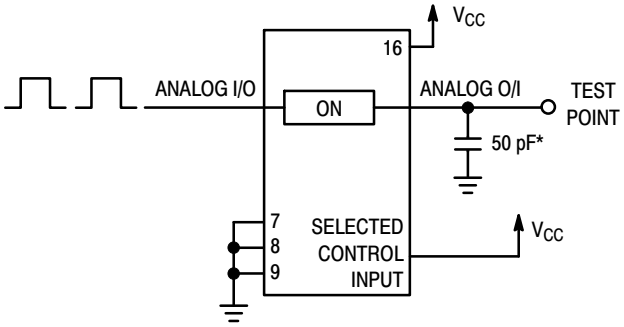



**Figure 9. Propagation Delays, Analog In to Analog Out**




*Includes all probe and jig capacitance.

**Figure 10. Propagation Delay Test Set−Up**

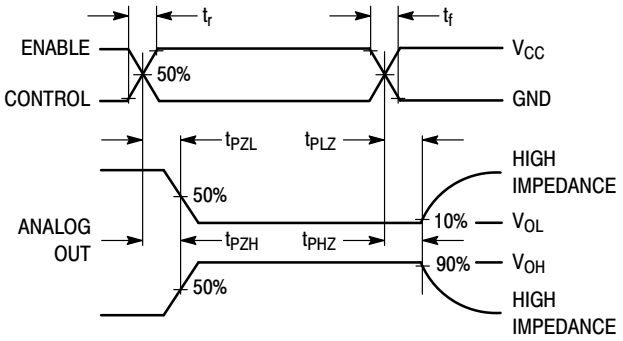
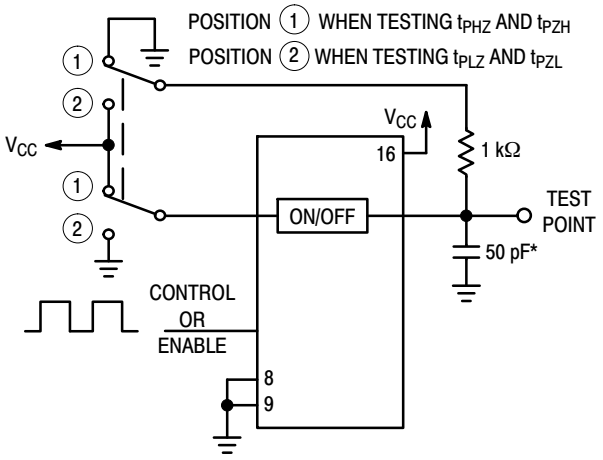
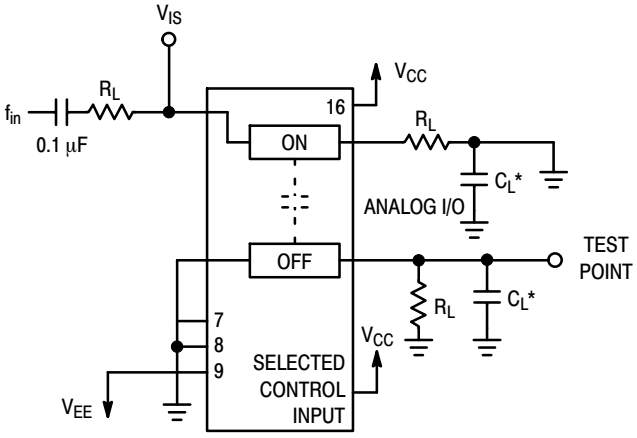



**Figure 11. Propagation Delay, ON/OFF Control to Analog Out**




*Includes all probe and jig capacitance.

**Figure 12. Propagation Delay Test Set−Up**




*Includes all probe and jig capacitance.

**Figure 13. Crosstalk Between Any Two Switches, Test Set−Up (Adjacent Channels Used)**

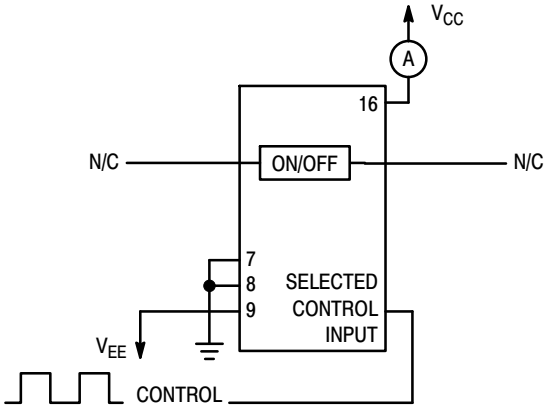
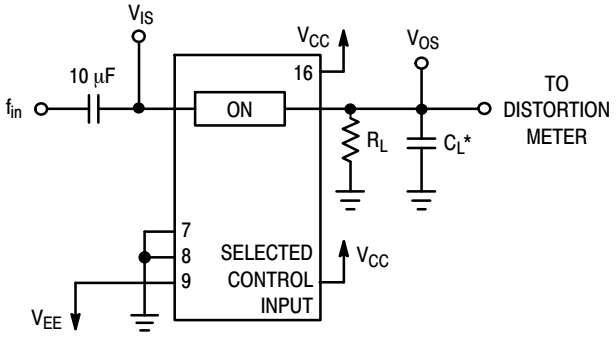



**Figure 14. Power Dissipation Capacitance Test Set−Up**




*Includes all probe and jig capacitance.

**Figure 15. Total Harmonic Distortion, Test Set−Up**

## APPLICATIONS INFORMATION

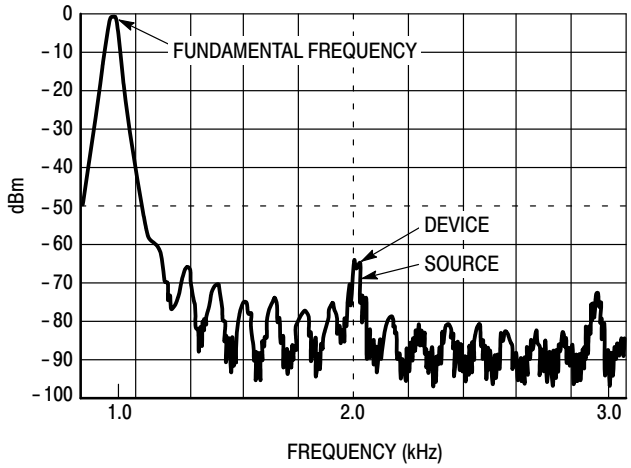



**Figure 16. Plot, Harmonic Distortion**

The Enable and Control pins should be at $V_{CC}$ or GND logic levels, $V_{CC}$ being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to $V_{CC}$ or $V_{EE}$ through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages $V_{CC}$ and $V_{EE}$. The positive peak analog voltage should not exceed $V_{CC}$. Similarly, the negative peak analog voltage should not go below $V_{EE}$. In the example below, the difference between $V_{CC}$ and $V_{EE}$ is 12 V. Therefore, using the configuration in Figure 17, a maximum analog signal of twelve volts peak−to−peak can be controlled.

When voltage transients above $V_{CC}$ and/or below $V_{EE}$ are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 18. These diodes should be small signal, fast turn−on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MOSORBs (MOSORB™ is an acronym for high current surge protectors). MOSORBs are fast turn−on devices ideally suited for precise dc protection with no inherent wear out mechanism.

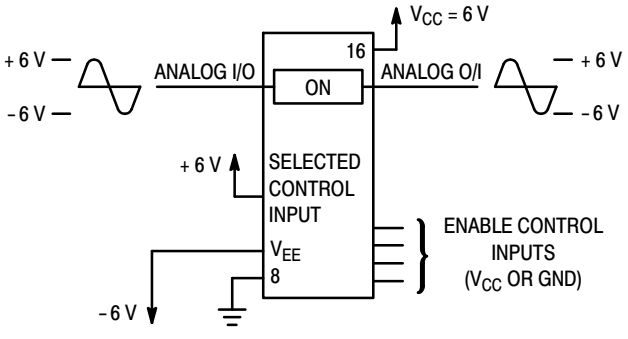



**Figure 17.**

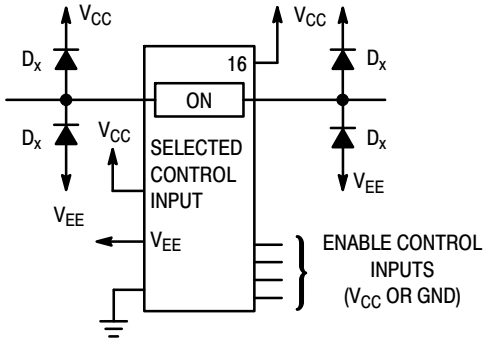
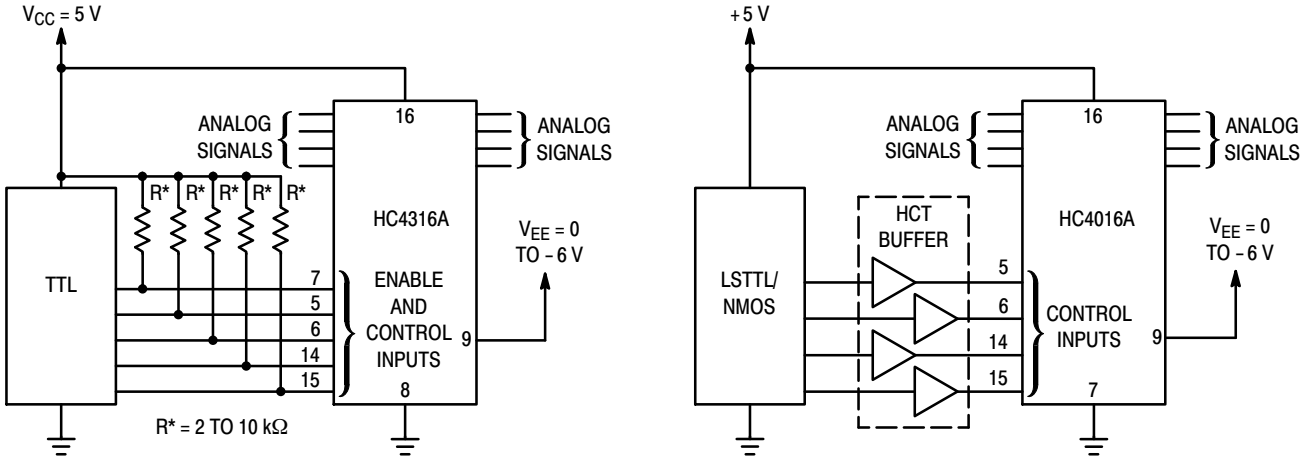



**Figure 18. Transient Suppressor Application**




**a. Using Pull−Up Resistors** **b. Using HCT Buffer**

**Figure 19. LSTTL/NMOS to HCMOS Interface**

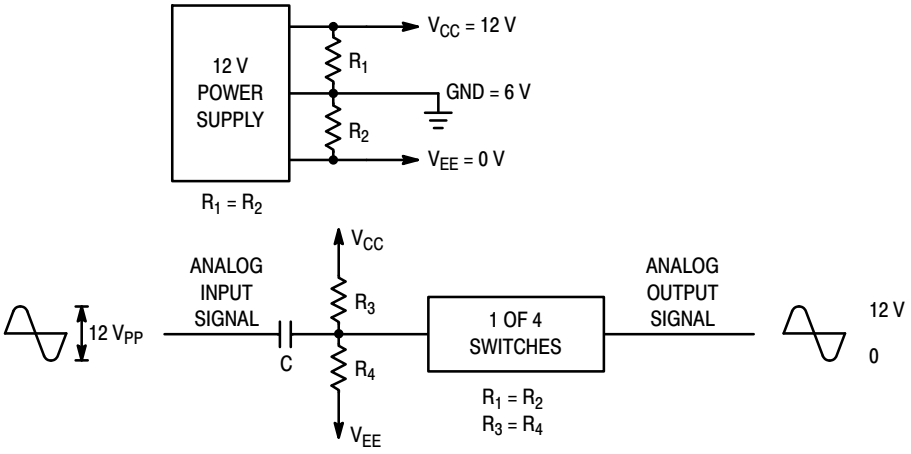



**Figure 20. Switching a 0−to−12 V Signal Using a Single Power Supply (GND ≠ 0 V)**

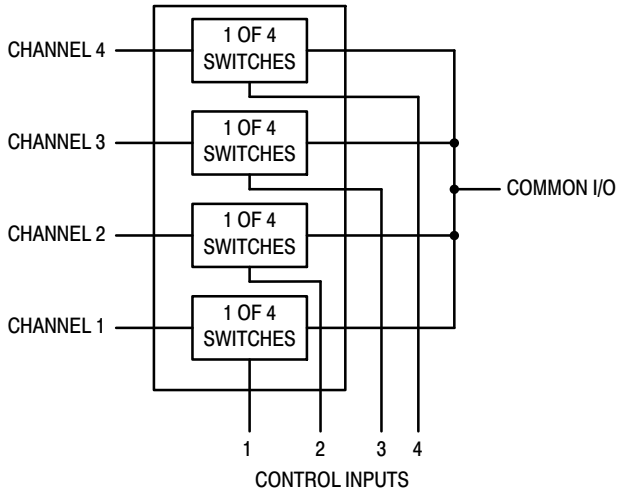



**Figure 21. 4−Input Multiplexer**

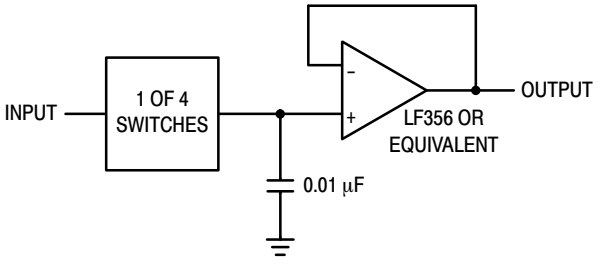
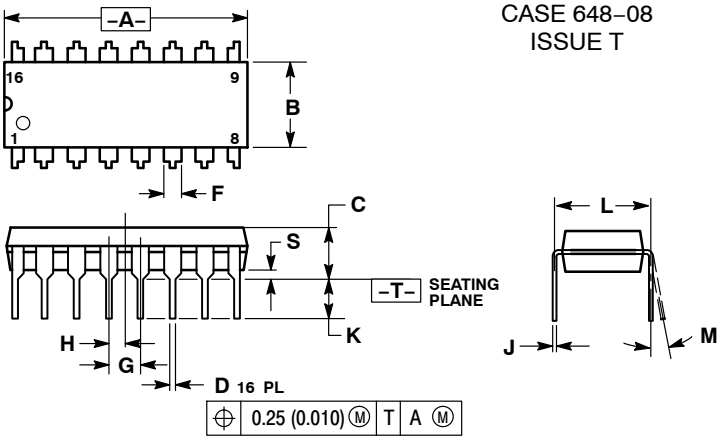



**Figure 22. Sample/Hold Amplifier**

## PACKAGE DIMENSIONS

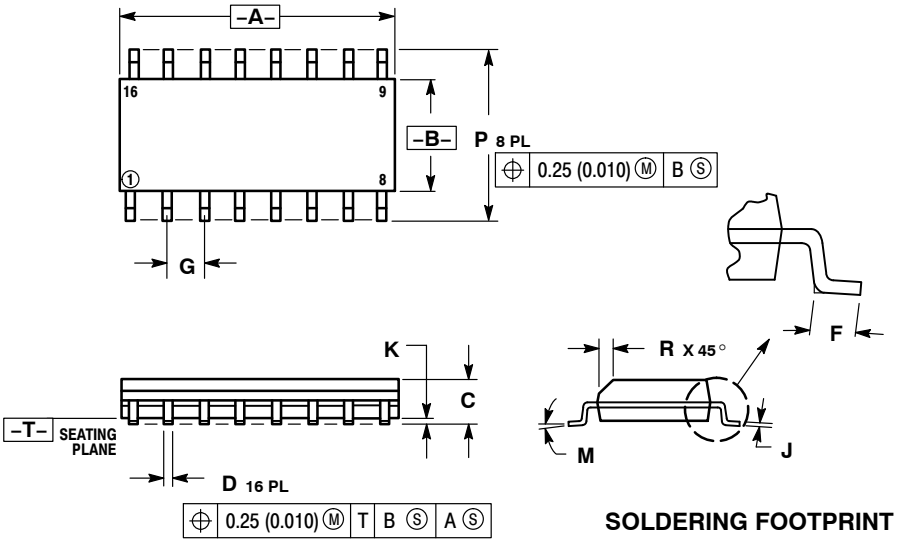
**PDIP−16**
**N SUFFIX**
CASE 648−08
ISSUE T




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

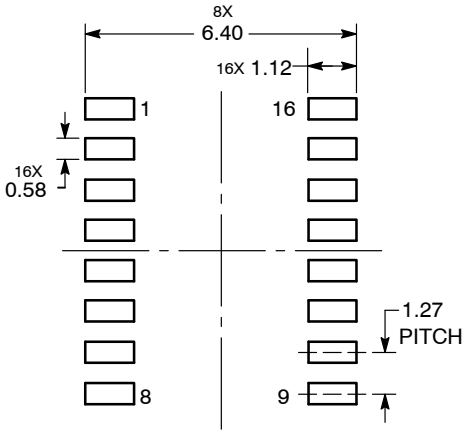
**SOIC−16**
**D SUFFIX**
CASE 751B−05
ISSUE K




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

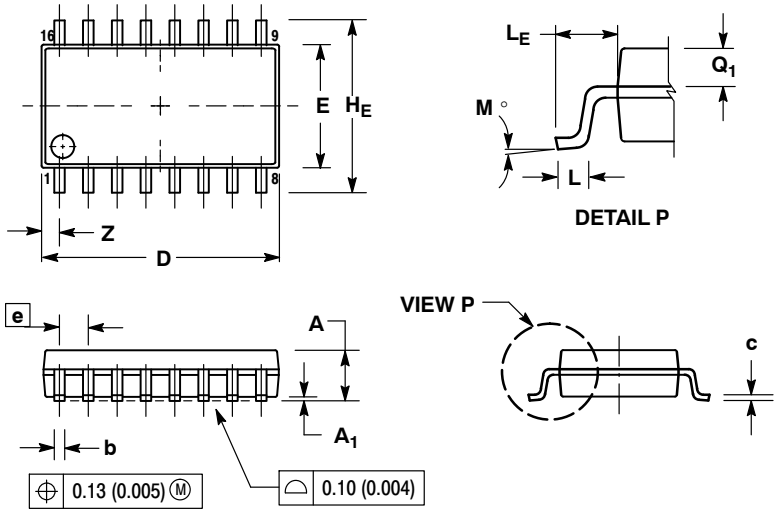
**SOLDERING FOOTPRINT**




DIMENSIONS: MILLIMETERS

## PACKAGE DIMENSIONS

**SOEIAJ−16**
**F SUFFIX**
CASE 966−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

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