STK5Q4U362J-E

Advance Information

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Inverter IPM for 3-phase Motor Drive

Overview

This "Inverter Power IPM" is highly integrated device containing all High Voltage (HV) control from HV-IC to 3-phase outputs in a single small DIP module. Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP). Internal bootstrap circuit is provided for high side gate drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control inputs and status outputs are at low voltage levels directly compatible with microcontrollers
- Built-in cross conduction prevention
- Having open emitter output for low side IGBTs ; individual shunt resistor per phase for OCP
- Externally accessible embedded thermistor for substrate temperature measurement
- Shutdown function 'ITRIP' to disable all operations of the 3 phase output stage by external input

Specifications

Absolute Maximum Ratings at Tc= 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}	P to U-(V-,W-), surge<500V *1	450	V
Collector-emitter voltage	V_{CE}	P to U(V,W) or U(V,W) to U-(V-,W-)	600	V
Output current	Io	P,U-,V-,W-,U,V,W terminal current	±10	A
		P,U-,V-,W-,U,V,W terminal current, Tc=100°C	±5	A
Output peak current	Iop	P,U-,V-,W-,U,V,W terminal current, P.W.=1ms	±20	A
Pre-driver voltage	VD1, 2, 3, 4	VB1 to U, VB2 to V, VB3 to W, V_{DD} to V_{SS} *2	–0.3 to +20.0	V
Input signal voltage	VIN	HIN1, 2, 3, LIN1, 2, 3	–0.3 to V_{DD}	V
FAULT terminal voltage	VFAULT	FAULT terminal	–0.3 to V_{DD}	V
RCIN terminal voltage	VRCIN	RCIN terminal	–0.3 to V_{DD}	V
ITRIP terminal voltage	VITRIP	ITRIP terminal	–0.3 to +10.0	V
ENABLE terminal voltage	VENABLE	ENABLE terminal	–0.3 to V_{DD}	V
Maximum power dissipation	Pd	IGBT per 1 channel	31	W
Junction temperature	Tj	IGBT, Diode, Pre-Driver IC	150	°C
Storage temperature	Tstg		–40 to +125	°C
Operating case temperature	Tc	IPM case temperature	–20 to +100	°C
Tightening torque		Case mounting screw	0.6	Nm
Withstand voltage	Vis	50Hz sine wave AC 1 minute *3	2000	VRMS

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

*1 : Surge voltage developed by the switching operation due to the wiring inductance between P and U-(V-, W-) terminal.
*2 : VD1=VB1 to U, VD2=VB2 to V, VD3=VB3 to W, VD4=V_{DD} to V_{SS} terminal voltage.
*3 : Test conditions : AC2500V, 1 second

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

Electrical Characteristics at Tc=25°C, VD1, VD2, VD3, VD4=15V

Parameter	Symbol	Conditions	Test circuit	Ratings			Unit
				min	typ	max	
Power output section							
Collector-emitter cut-off current	I_{CE}	V_{CE}=600V	Fig.1	-	-	100	μA
Collector to emitter saturation voltage	V_{CE}(SAT)	Ic=10A, Tj=25°C	Fig.2	-	1.9	2.7	V
		Ic=5A, Tj=100°C		-	1.6	-	V
Diode forward voltage	VF	IF=10A, Tj=25°C	Fig.3	-	1.5	2.2	V
		IF=5A, Tj=100°C		-	1.2	-	V
Bootstrap ON Resistance	RB	IB=1mA	Fig.4	-	110	-	Ω
Junction to case thermal resistance	θj-c(T)	IGBT	-	-	-	4	°C/W
	θj-c(T)	FWD				5.5	°C/W
Control (Pre-driver) section							
Pre-driver power dissipation	ID	VD1, 2, 3=15V	Fig.5	-	0.07	0.4	mA
		VD4=15V		-	0.95	3	
High level Input voltage	Vin H	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 to V_{SS}		2.5	-	-	V
Low level Input voltage	Vin L			-	-	0.8	V
Logic 1 input leakage current	I_{IN+}	VIN=+3.3V		-	660	900	μA
Logic 0 input leakage current	I_{IN-}	VIN=0V		-	-	3	μA
FAULT terminal sink current	IoSD	FAULT : ON / VFAULT=0.1V		-	2	-	mA
FAULT clearance delay time	FLTCLR	From time fault condition clear R=2MΩ, C=1nF		1.1	1.65	2.2	ms
ENABLE Threshold	VEN +	VEN rising		-	-	2.5	V
	VEN –	VEN falling		0.8	-	-	V
ITRIP threshold voltage	VITRIP	ITRIP(10) to V_{SS}(1)		0.44	0.49	0.54	V
ITRIP to shutdown propagation delay	t_{ITRIP}			-	1.1	-	μs
ITRIP blanking time	$t_{ITRIPBL}$			250	350	-	ns
V_{CC} and V_{BS} supply undervoltage positive going input threshold	V_{CCUV+} V_{BSUV+}			10.2	11.1	11.8	V
V_{CC} and V_{BS} supply undervoltage negative going input threshold	V_{CCUV-} V_{BSUV-}			10.0	10.9	11.6	V
V_{CC} and V_{BS} supply undervoltage $I_{lockout}$ hysteresis	V_{CCUVH} V_{BSUVH}			-	0.2	-	V

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

Electrical Characteristics at Tc=25°C, VD1, VD2, VD3, VD4=15V, V_{CC}=300V, L=3.9mH

Parameter	Symbol	Conditions	Test circuit	min	typ	max	Unit
Switching Character							
Switching time	t ON	Ic = 10A	Fig.6	-	0.6	1.3	μs
	t OFF			-	1.0	1.6	
Turn-on switching loss	Eon	Ic=10A	Fig.6	-	300	-	μJ
Turn-off switching loss	Eoff			-	90	-	μJ
Total switching loss	Etot			-	390	-	μJ
Turn-on switching loss	Eon	Ic=10A,Tc=100°C	Fig.6	-	360	-	μJ
Turn-off switching loss	Eoff			-	110	-	μJ
Total switching loss	Etot			-	470	-	μJ
Diode reverse recovery energy	Erec	I_F=10A,Tc=100°C		-	60	-	μJ
Diode reverse recovery time	trr			-	160	-	ns
Reverse bias safe operating area	RBSOA	Ic=20A, V_{CE}=450V		Full Square			-
Short circuit safe operating area	SCSOA	V_{CE}=400V		4	-	-	μs
Allowable offset voltage slew rate	dv/dt	Between U(V,W) to U-(V-,W-)		–50	-	50	V/ns

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. When pre-driver protection circuit protects the device, the fault output that is open drain terminal is turn on. The protection operation will not be latched. After the protection operation ends, the IPM operation resumes after typ.1.65ms (R=2MΩ, C=1nF). Therefore, please turn all the input signals OFF (LOW) as soon as the protection operation is detected. The pre-drive power supply low voltage protection has approximately 200mV of hysteresis and operates as follows.

   Upper side : The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'.

   Lower side : The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

2. When assembling the IPM on the heat sink with M3 type screw, tightening torque range is 0.4Nm to 0.6Nm.

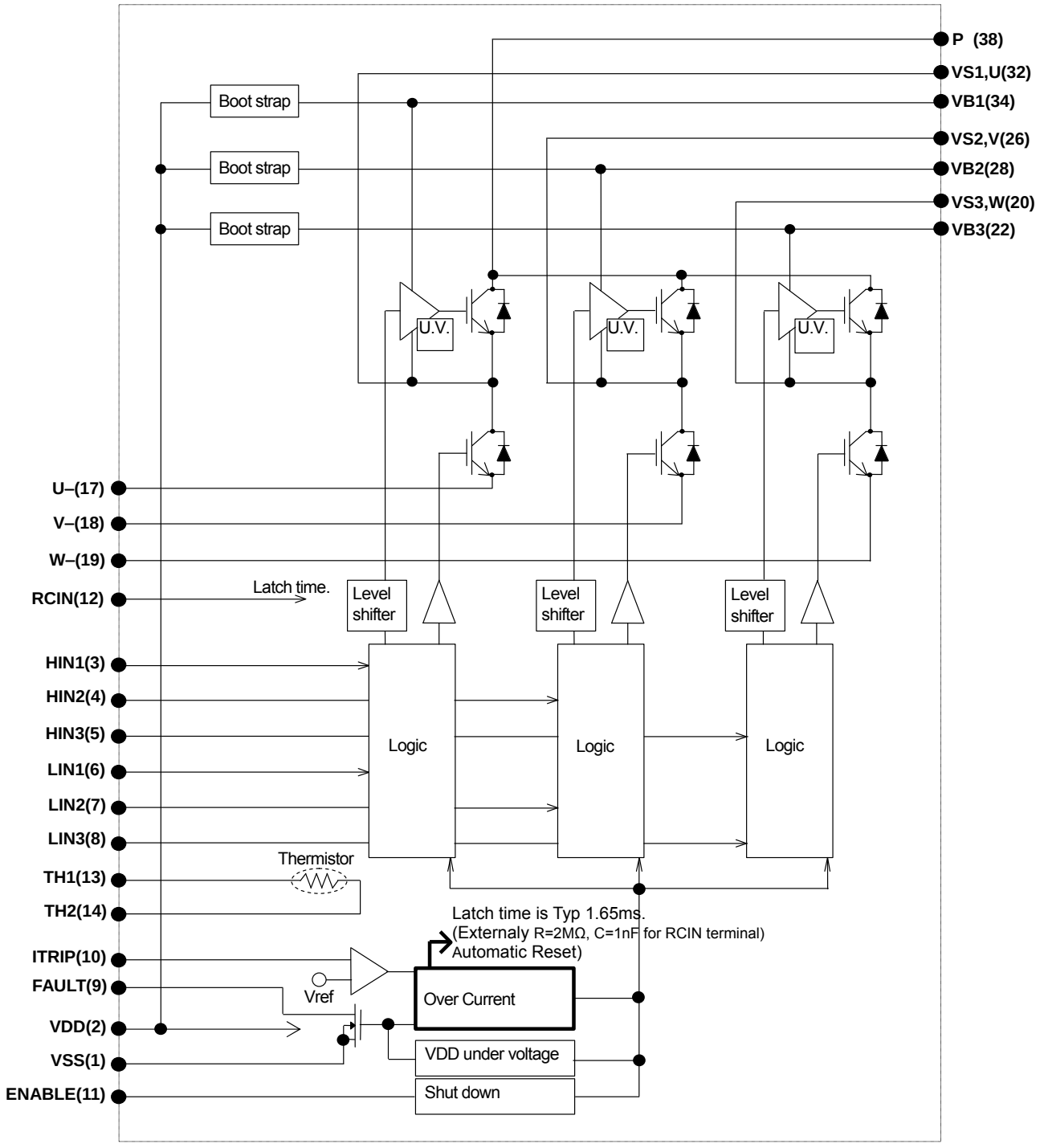
3. The pre-drive low voltage protection is the function to protect devices when the pre-drive supply voltage falls due to an operating malfunction.

4. When using the over-current protection with external resistor, please set resistance value so that current protection value becomes equal to or less than the double (2 times) of the rating output electric current (Io).

Pin Assignment

Pin	Name	Description
1	V_{SS}	Negative Main Supply
2	V_{DD}	+15V Main Supply
3	HIN1	Logic Input High Side Gate Driver - Phase U
4	HIN2	Logic Input High Side Gate Driver - Phase V
5	HIN3	Logic Input High Side Gate Driver - Phase W
6	LIN1	Logic Input Low Side Gate Driver - Phase U
7	LIN2	Logic Input Low Side Gate Driver - Phase V
8	LIN3	Logic Input Low Side Gate Driver - Phase W
9	FAULT	Fault output
10	ITRIP	Current protection pin
11	ENABLE	Enable input
12	RCIN	R,C connection terminal for setting FAULT clear time
13	TH1	Thermistor output1
14	TH2	Thermistor output2
15	(N.C)	Without pin
16	(N.C)	Without pin
17	U-	Low Side Emitter Connection - Phase U
18	V-	Low Side Emitter Connection - Phase V
19	W-	Low Side Emitter Connection - Phase W
20	W, VS3	Output 3 - High Side Floating Supply Offset Voltage
21	(N.C)	Without pin
22	VB3	High Side Floating Supply Voltage 3
23	(N.C)	Without pin
24	(N.C)	Without pin
25	(N.C)	Without pin
26	V,VS2	Output 2 - High Side Floating Supply Offset Voltage
27	(N.C)	Without pin
28	VB2	High Side Floating Supply voltage 2
29	(N.C)	Without pin
30	(N.C)	Without pin
31	(N.C)	Without pin
32	U,VS1	Output 1 - High Side Floating Supply Offset Voltage
33	(N.C)	Without pin
34	VB1	High Side Floating Supply voltage 1
35	(N.C)	Without pin
36	(N.C)	Without pin
37	(N.C)	Without pin
38	P	Positive Bus Input Voltage

Block Diagram



Test Circuit

(The tested phase : U+ shows the upper side of the U phase and U- shows the lower side of the U phase.)

■ ICE

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19

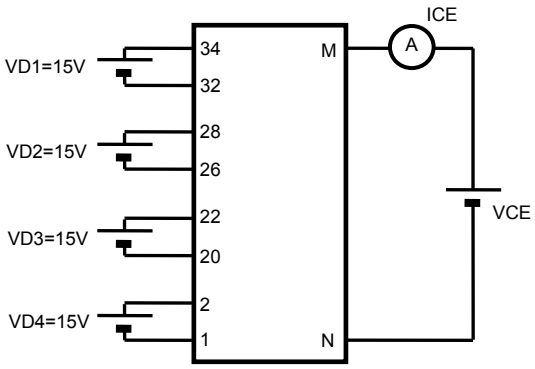


Fig.1

■ VCE(sat) (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19
m	3	4	5	6	7	8

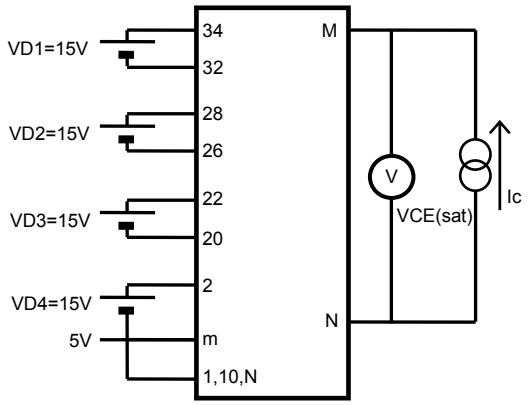


Fig.2

■ VF (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19

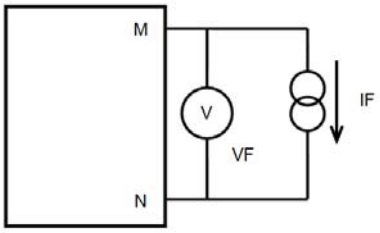


Fig.3

■ RB (Test by pulse)

	U+	V+	W+
M	2	2	2
N	34	28	22

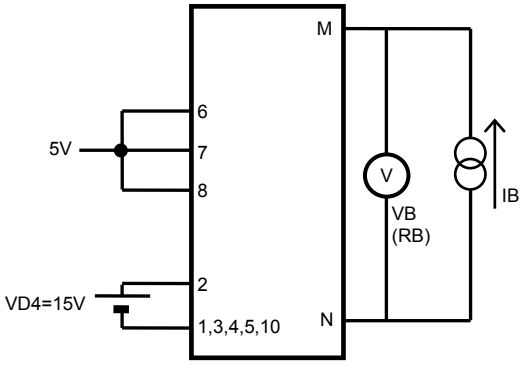


Fig.4

■ ID

	VD1	VD2	VD3	VD4
M	34	28	22	2
N	32	26	20	1

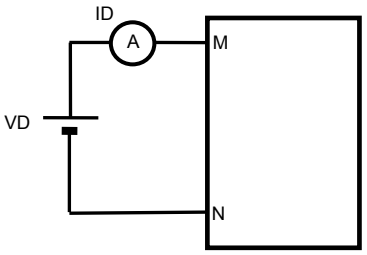
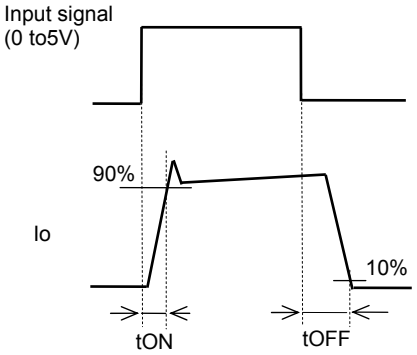


Fig. 5

■ Switching time (The circuit is a representative example of the lower side U phase.)



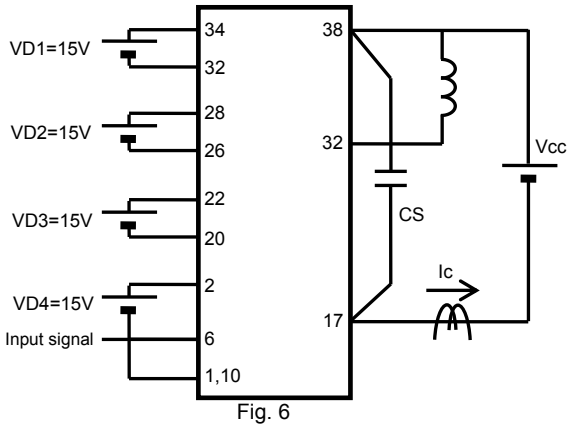
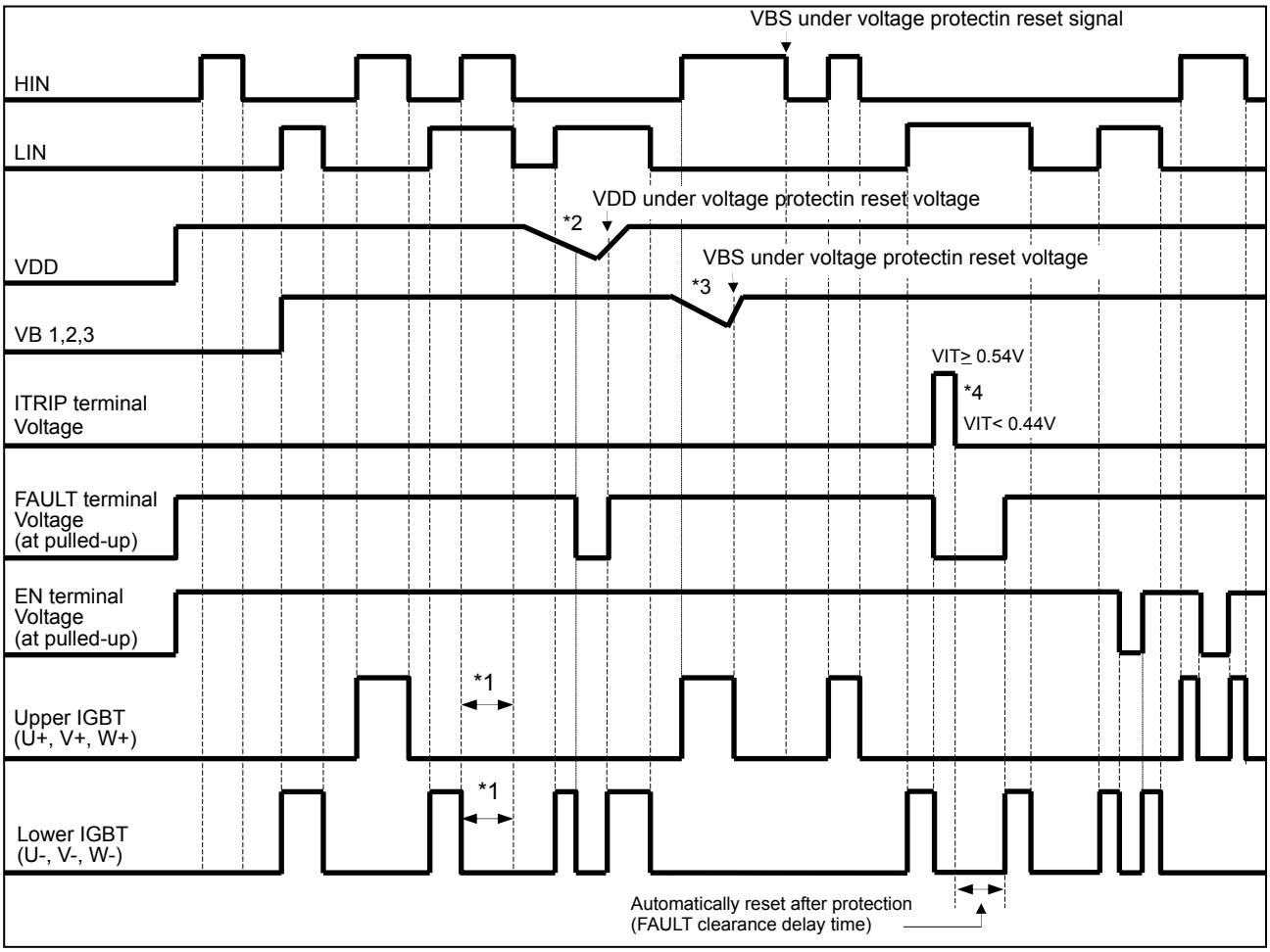


Fig. 6

Input / Output Timing Chart



After the V_{DD} turned on, the HIN voltage do not pass the IC until LIN voltage come.

Fig.7

Notes

1. *1 shows the prevention of shoot-thru via control logic, however, more dead time must be added to account for switching delay externally.
2. *2 when V_{DD} decreases all gate output signals will go low and cut off all 6 IGBT outputs. When V_{DD} rises the operation will resume immediately.
3. *3 when the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal 4. operation immediately after the upper side gate voltage rises.
4. *4 when VITRIP exceeds threshold all IGBT's are turned off and normal operation resumes typ 1.65ms (R=2MΩ, C=1nF) later after over current condition is removed.

Logic level table

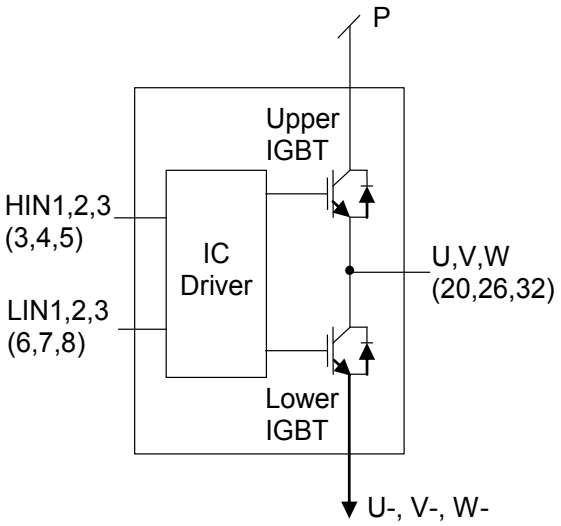


Fig.8

INPUT				OUTPUT			
HIN	LIN	Itrip	Enable	Upper IGBT	Lower IGBT	U,V,W	FLTEN
H	L	L	H	ON	OFF	P	OFF
L	H	L	H	OFF	ON	U-,V-,W-	OFF
L	L	L	H	OFF	OFF	High Impedance	OFF
H	H	L	H	OFF	OFF	High Impedance	OFF
X	X	H	H	OFF	OFF	High Impedance	ON
X	X	X	L	OFF	OFF	High Impedance	OFF

Sample Application Circuit

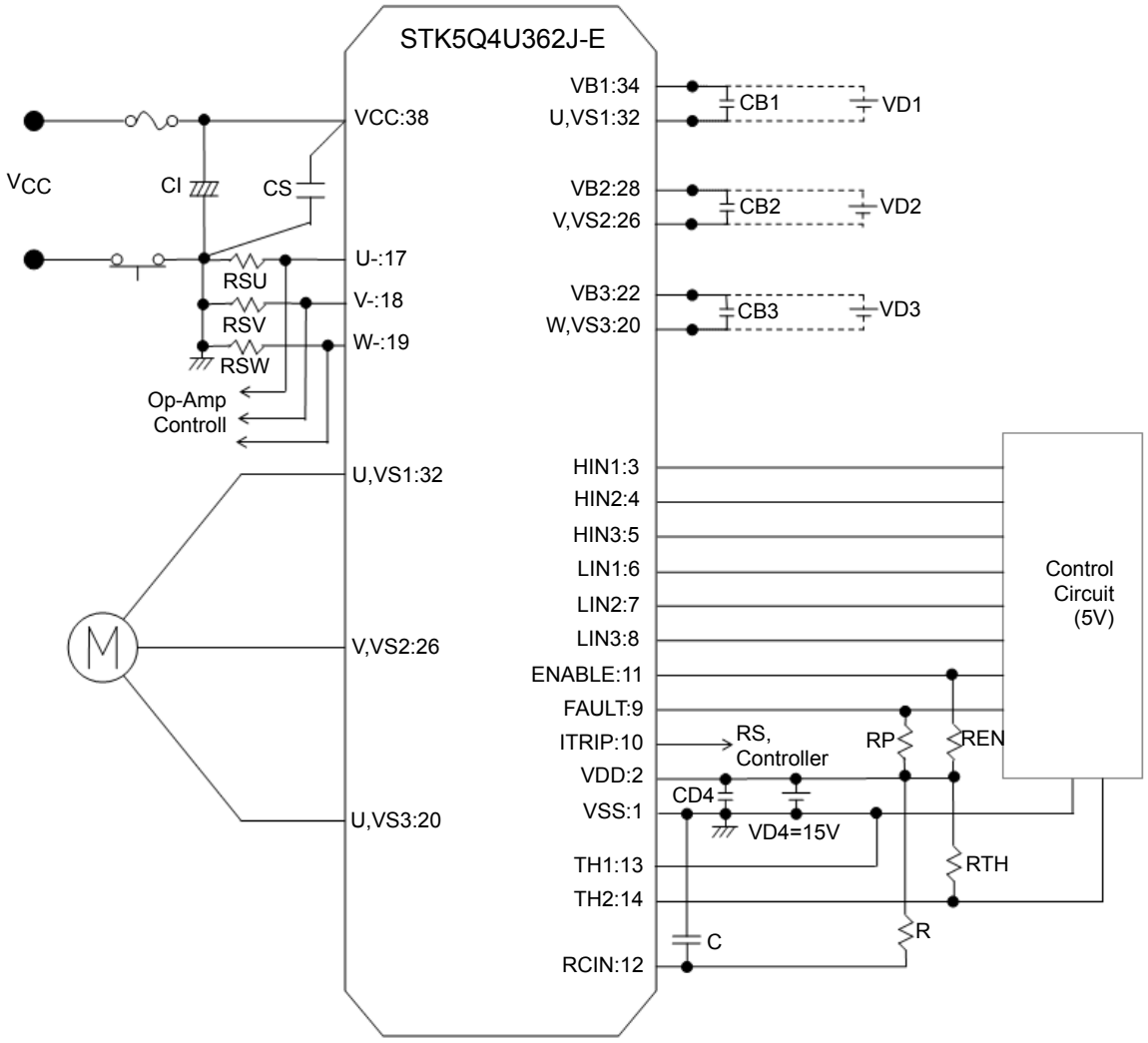


Fig. 9

Recommended Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}	V_{CC} to U- (V-, W-)	0	280	400	V
Pre-driver supply voltage	VD1,2,3	VB1 to U, VB2 to V, VB3 to W	12.5	15	17.5	V
	VD4	V_{DD} to V_{SS} *1	13.5	15	16.5	
ON-state input voltage	VIN(ON)	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3	3.0	-	5.0	V
OFF-state input voltage	VIN(OFF)		0	-	0.3	
PWM frequency	fPWM		1	-	20	kHz
Dead time	DT	Turn-off to turn-on (external)	1	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque		'M3' type screw	0.4	-	0.6	Nm

*1 : Pre-drive power supply (VD4=15±1.5V) must have the capacity of Io=20mA (DC), 0.5A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Usage Precaution

1. This IPM includes internal bootstrap circuit. By adding a bootstrap capacitor "CB", a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47μF, however, this value needs to be verified prior to production. When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.

2. The built-in Boot-Strap circuit is comprised of MOSFET. Because this MOSFET turn ON sync with turn ON of lower side IGBT, let lower side IGBT turn ON when charge to Boot-Strap capacitor.

3. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of "CS" is in the range of 0.1 to 10μF.

4. The "FAULT" terminal (Pin 9) is open Drain (It operates as "FAULT" when becoming Low). When the pull up voltage (VP) is 5V, connect pull up resistor (RP) with resistance of 6.8kΩ or above, and in case of VP=15V, connect RP with resistance of 20kΩ or above.

5. The "ENABLE" terminal (Pin 11) serves as the shut down input of the built-in pre-driver. (Normal operation when the terminal voltage is above 2.5V. Shut down when it is equal to or less than 0.8V.) Please make pulling up outside so that "ENABLE" terminal voltages become more than 3V. When the pull up voltage (VP) is 5V, connect pull up resistor (REN) with resistance of 6.8kΩ or above, and in case of VP=15V, connect RP with resistance of 20kΩ or above.

6. Inside the IPM, a thermistor used as the temperature monitor for internal subatrate is connected between TH1 terminal and TH2 terminal, therefore, an external pull up resistor connected between the TH1(or TH2) terminal and an external power supply should be used. Please check the temperature moniter opplication at Fig9, and Fig10.

7. The over-current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.

8. Disconnection of terminals U, V, or W during normal motor operation will cause damage to IPM, use caution with this connection.

9. The "ITRIP" terminal (Pin 10) is the input terminal of the built-in comparator. It can stop operation by inputting the voltage more than Vref (0.44V to 0.54V). (Apply voltage less than Vref to this pin when normal operation.).
   Please use it as various protections such as the over current protection (feedback from external shunt resistor).
   In addition, the protection operation will not be latched.
   After the protection operation ends, the IPM operation resumes after typ.1.65ms(R=2MΩ, C=1nF). Therefore, please turn all the input signals OFF (LOW) as soon as the protection operation is detected.

10. When input pulse width is less than 1μs, an output may not react to the pulse. (Both ON signal and OFF signal)

■ This data shows the example of the application circuit, and does not guarantee a design as the mass production set.

The characteristic of thermistor

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc=25℃	99	100	101	kΩ
	R_{100}	Tc=100℃	5.18	5.38	5.60	kΩ
B-Constant (25 to 50℃)	B		4208	4250	4293	K
Temperature Range			−40		+125	℃

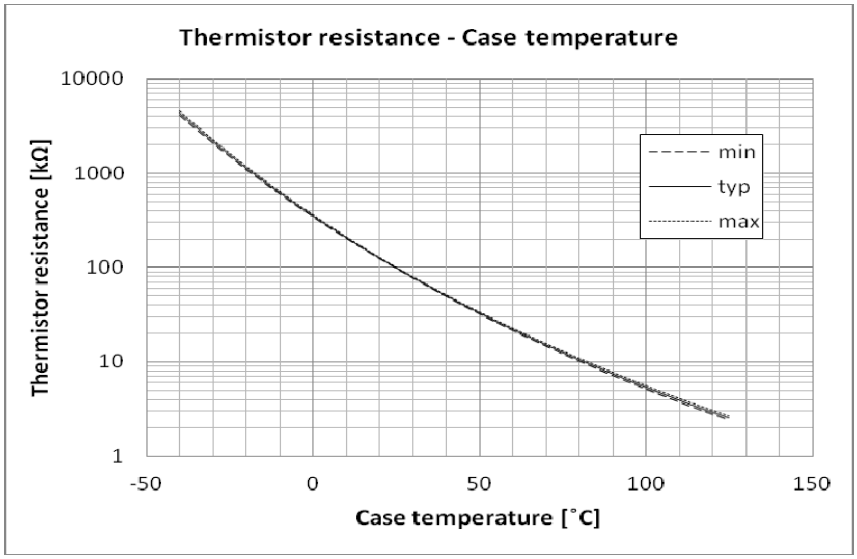
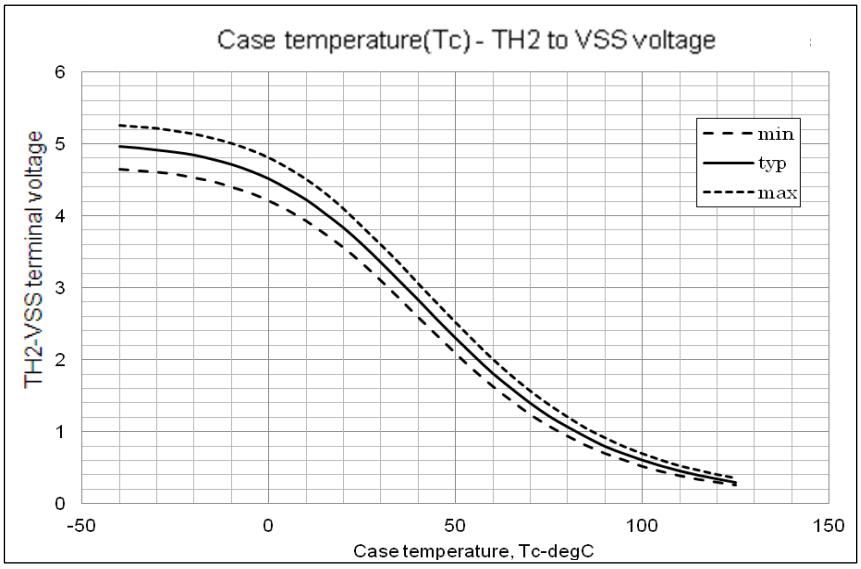


Fig. 10



*Condition : Pull-up resistor (RTH) = 39kΩ +/−1%, Pull-up voltage of VTH= 5V +/−0.3V
Refer to application circuit.

Fig. 11

The characteristic of PWM switching frequency

Maximum sinusoidal phase current as function of switching frequency at Tc=100°C, V_{CC}=300V

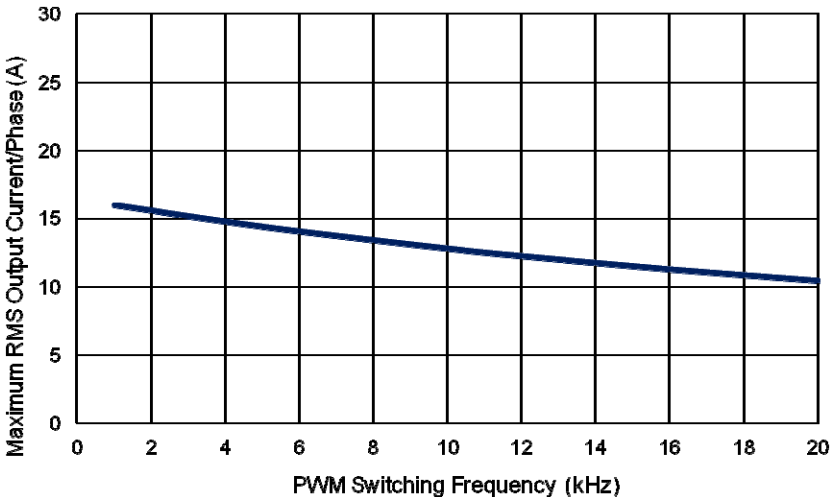


Fig.12

Switching waveform

IGBT Turn-on. Typical turn-on waveform at Tc=100°C, V_{CC}=400V

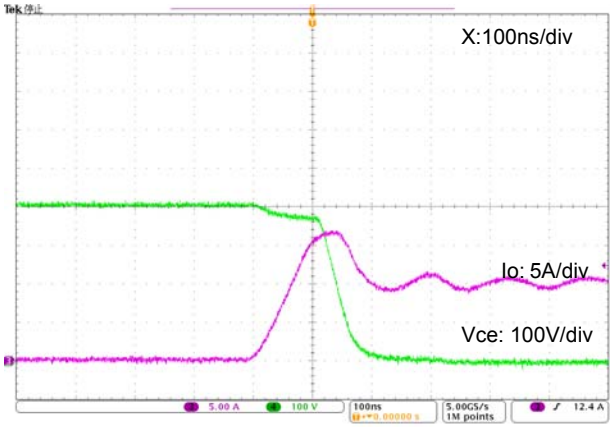


Fig. 13

IGBT Turn-off. Typical turn-off waveform at Tc=100°C, V_{CC}=400V

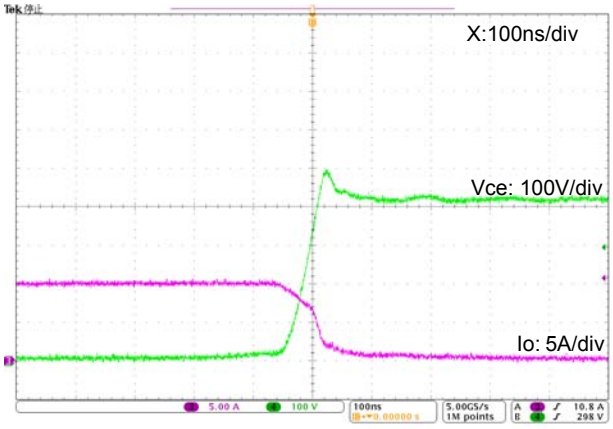


Fig. 14

CB capacitor value calculation for bootstrap circuit

Calculate condition

Item	Symbol	Value	Unit
Upper side power supply.	VBS	15	V
Total gate charge of output power IGBT at 15V.	Qg	45	nC
Upper side power supply low voltage protection.	UVLO	12	V
Upper side power dissipation.	IDMAX	400	μA
ON time required for CB voltage to fall from 15V to UVLO	TONMAX	-	s

Capacitance calculation formula

Tonmax is upper arm maximum on time equal the time when the CB voltage falls from 15V to the upper limit of Low voltage protection level.
“ton-maximum" of upper side is the time that CB decreases 15V to the maximum low voltage protection of the upper side (12V).
Thus, CB is calculated by the following formula.

VBS * CB – Qg – IDMAX * TONMAX = UVLO * CB
CB = (Qg + IDMAX * TONMAX) / (VBS – UVLO)

The relationship between tonmax and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of Cb is in the range of 1 to 47μF, however, the value needs to be verified prior to production.

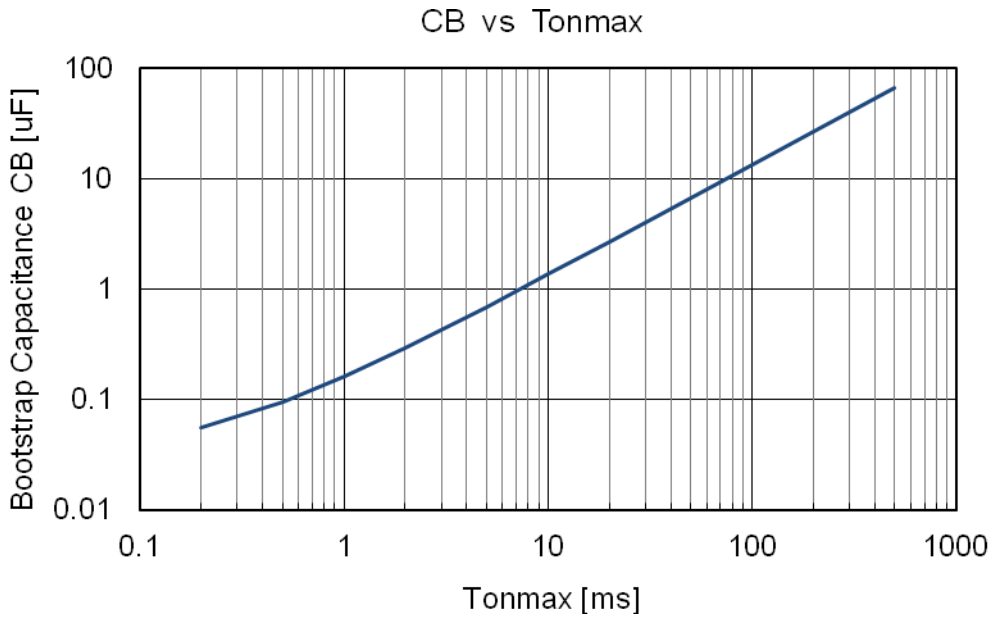
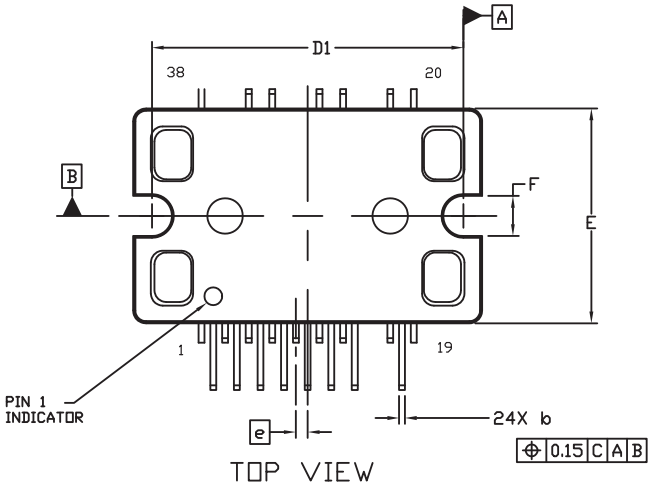


Fig.15 TONMAX vs CB characteristic

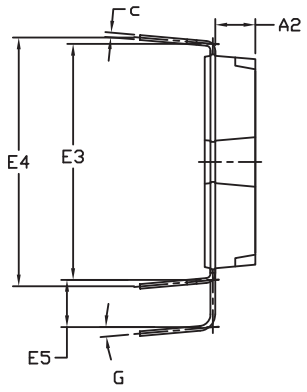
Package Dimensions

unit : mm

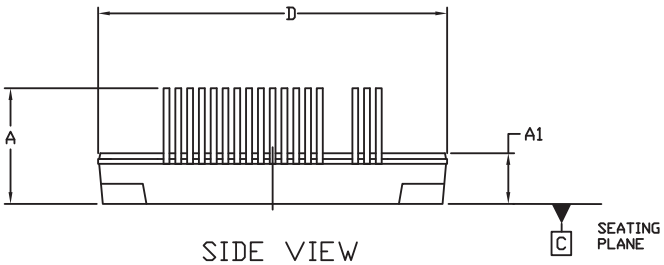
MODULE SPCM24 29.6x18.2 DIP S3
CASE MODBL
ISSUE O



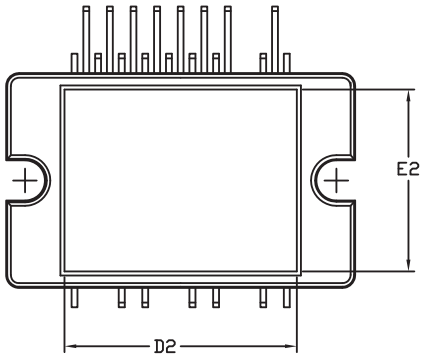
TOP VIEW



END VIEW



SIDE VIEW



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED LEAD AND IS MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. PACKAGE IS MISSING PINS: 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, AND 37.

	MILLIMETERS	
DIM	MIN.	MAX.
A	9.30	10.30
A1	3.80	4.80
A2	2.90	3.90
b	0.45	0.70
c	0.35	0.60
D	29.10	30.10
D1	26.30	26.50
D2	19.20	20.20
E	17.70	18.70
E2	14.90	15.90
E3	19.50	20.50
E4	21.10 REF	
e	1.00 BSC	
F	2.90	3.90
G	4°	6°

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK5Q4U362J-E	MODULE SPCM24 29.6x18.2 DIP S3 (Pb-Free)	50 / Tube

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