

MOSFETs Silicon N-Channel MOS (DTMOS V)

TK290P65Y

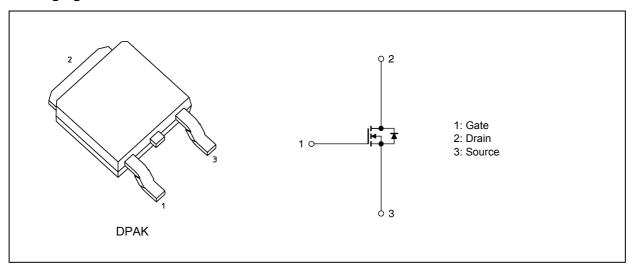
1. Applications

· Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 0.23 \Omega$ (typ.) by using Super Junction Structure: DTMOS
- (2) Easy to control Gate switching
- (3) Enhancement mode: $V_{th} = 3$ to 4 V ($V_{DS} = 10$ V, $I_D = 0.45$ mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (T_a = 25 °C unless otherwise specified)

Characteris	stics		Symbol	Rating	Unit
Drain-source voltage			V _{DSS}	650	V
Gate-source voltage			V _{GSS}	±30	
Drain current (DC)	(T _c = 25 °C)	(Note 1)	I _D	11.5	Α
Drain current (DC)	(T _c = 100 °C)	(Note 1)	I _D	7.3	Α
Drain current (pulsed)	(T _c = 25 °C)	(Note 1)	I _{DP}	46	Α
Power dissipation	(T _c = 25 °C)		P _D	100	W
Single-pulse avalanche energy		(Note 2)	E _{AS}	106	mJ
Single-pulse avalanche current			I _{AS}	3	Α
Reverse drain current (DC)		(Note 1)	I _{DR}	11.5]
Reverse drain current (pulsed)		(Note 1)	I _{DRP}	46	Α
Channel temperature			T _{ch}	150	°C
Storage temperature			T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production



5. Thermal Characteristics

Characteristics		Max	Unit
Channel-to-case thermal resistance	R _{th(ch-c)}	1.25	°C/W
Channel-to-ambient thermal resistance		125	

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: V_{DD} = 90 V, T_{ch} = 25 °C (initial), L = 20.9 mH, R_G = 25 Ω , I_{AS} = 3 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μΑ
Drain cut-off current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V	_	_	10	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 10 mA, V _{GS} = 0 V	650	_	_	V
Gate threshold voltage	V _{th}	V _{DS} = 10 V, I _D = 0.45 mA	3	_	4	
Drain-source on-resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 5.8 A	_	0.23	0.29	Ω

6.2. Dynamic Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	$V_{DS} = 300 \text{ V}, V_{GS} = 0 \text{ V}, f = 100 \text{ kHz}$	_	730	_	pF
Reverse transfer capacitance	C _{rss}		_	2.5	_	
Output capacitance	C _{oss}		_	26	_	
Effective output capacitance	C _{o(er)}	V _{DS} = 0 to 400 V, V _{GS} = 0 V	_	48	_	
Gate resistance	r _g	V _{DS} = OPEN , f = 1 MHz	_	32	_	Ω
Switching time (rise time)	t _r	See Figure 6.2.1	_	25	_	ns
Switching time (turn-on time)	t _{on}		_	65	_	
Switching time (fall time)	t _f		_	8.5	_	
Switching time (turn-off time)	t _{off}		_	170	_	
MOSFET dv/dt ruggedness	dv/dt	$V_{DS} \le V_{(BR)DSS}$, $I_D \le 5.8 A$	50	_		V/ns

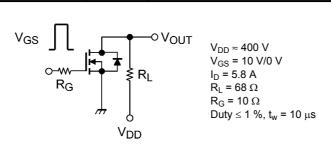


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 11.5 \text{ A}$		25		nC
Gate-source charge 1	Q _{gs1}			4	_	
Gate-drain charge	Q_{gd}			13		

6.4. Source-Drain Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Diode forward voltage	V _{DSF}	I _{DR} = 11.5 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	V _{DD} ≈ 400 V	_	240	_	ns
Reverse recovery charge	Q _{rr}	I _{DR} = 5.8 A, V _{GS} = 0 V -dI _{DR} /dt = 100 A/μs	_	2.3	_	μС
Peak reverse recovery current	I _{rr}	-αιρκαι – 100 Α/μο	_	20	_	Α
Diode dv/dt ruggedness	dv/dt	$V_{DS} \le 400 \text{ V}, I_{DR} \le 5.8 \text{ A}, V_{GS} = 0 \text{ V}$	15	_	_	V/ns



7. Marking

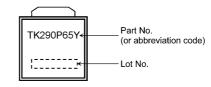


Fig. 7.1 Marking

8. Characteristics Curves (Note)

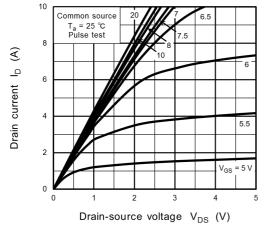
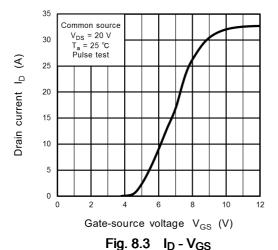


Fig. 8.1 I_D - V_{DS}



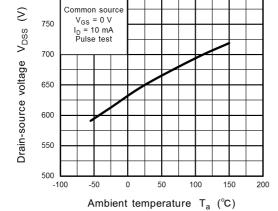


Fig. 8.5 V_{DSS} - T_a

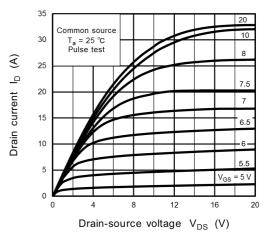


Fig. 8.2 I_D - V_{DS}

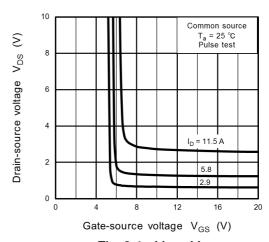


Fig. 8.4 V_{DS} - V_{GS}

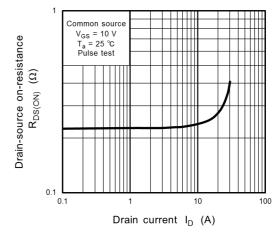


Fig. 8.6 R_{DS(ON)} - I_D

800

750

 \leq

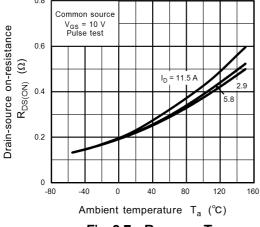


Fig. 8.7 R_{DS(ON)} - T_a

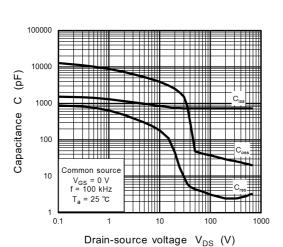


Fig. 8.9 C - V_{DS}

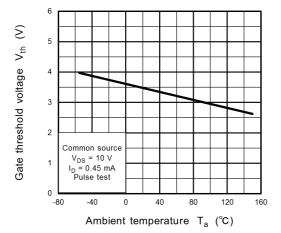


Fig. 8.11 V_{th} - T_a

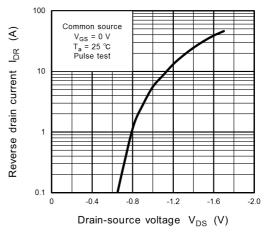


Fig. 8.8 IDR - VDS

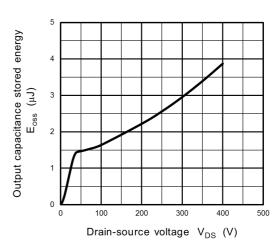


Fig. 8.10 Eoss - VDS

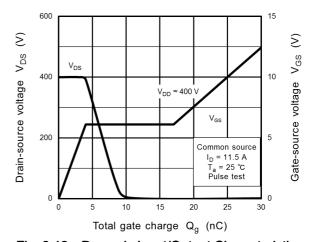


Fig. 8.12 Dynamic Input/Output Characteristics

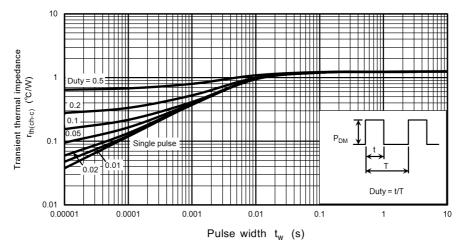


Fig. 8.13 r_{th} - t_w (Guaranteed Maximum)

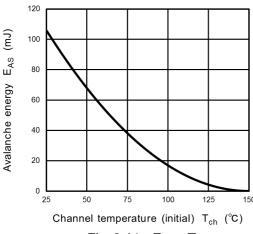


Fig. 8.14 E_{AS} - T_{ch} (Guaranteed Maximum)

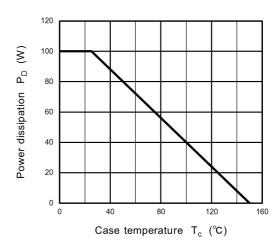
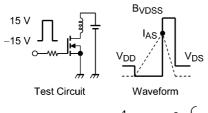


Fig. 8.15 P_D - T_c (Guaranteed Maximum)



$$R_G = 25 \Omega$$
, $V_{DD} = 90 V$ $E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}}\right)$

Fig. 8.16 Test Circuit/Waveform

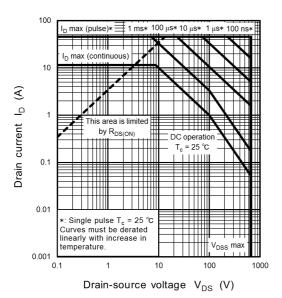


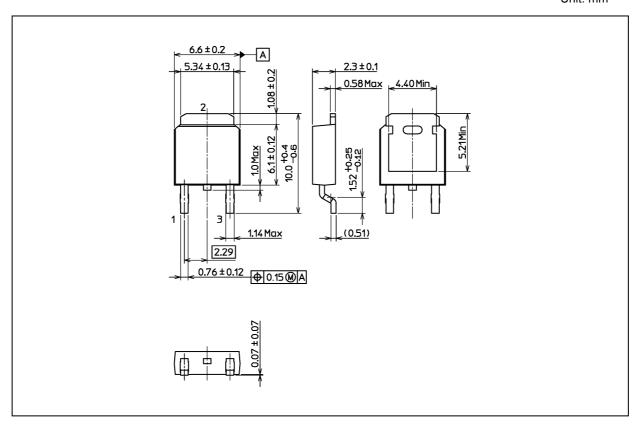
Fig. 8.17 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 0.36 g (typ.)

	Package Name(s)
TOSHIBA: 2-7K1S	
Nickname: DPAK	



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