CS42L73

Ultra Low Power Mobile Audio and Telephony CODEC

Product Overview

For the full datasheet, visit
www.cirrus.com/codec-datasheets/CS42L73

- Stereo ADC
- Dual Analog or Digital MIC Support
- Dual MIC Bias Generators
- Four DACs Coupled to Five Outputs
  - Ground-Centered Stereo Headphone Amp.
  - Ground-Centered Stereo Line Output
  - Mono Ear Speaker Amplifier
  - Mono 1 W Speakerphone Amplifier
  - Mono Speakerphone Line Output for Stereo Speakerphone Expansion
- Three Serial Ports with Asynchronous Sample Rate Converters
- Digital Audio Mixing and Routing

Ultra Low Power Consumption

- 3.5 mW Quiescent Headphone Playback

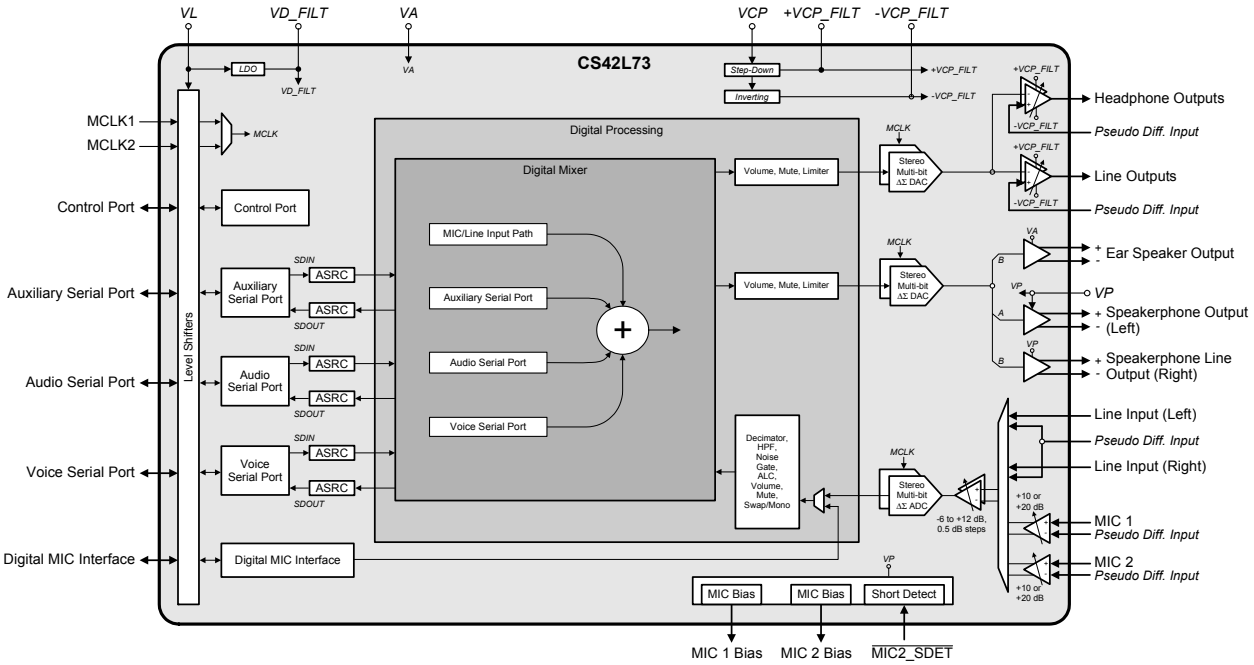
Applications

- Smart Phones, UMPCs, and MIDs

System Features

- Native (no PLL required) Support for 6/12/24 MHz, 13/26 MHz, and 19.2/38.4 MHz Master Clock Rates in Add. to Typ. Audio Clock Rates
- Integrated High-efficiency Power Management Reduces Power Consumption
  - Internal LDO Regulator to Reduce Internal Digital Operating Voltage to VL/2
  - Step-down Charge Pump Provides Low Headphone/Line Out Supply Voltage
  - Inverting Charge Pump Accommodates Low System Voltage by Providing Negative Rail for HP and Line Amp
- Flexible Speakerphone Amplifier Powering
  - 3.00 V to 5.25 V Range
  - Independent Cycling
- Power Down Management
  - Individual Controls for ADCs, Dig. MIC Interface, MIC Bias Generators, Serial Ports, and Output Amplifiers & Associated DACs
- Programmable Thermal Overload Notification
- High-speed I²C™ Control Port (400 kHz)

(**Features** continued on page 2)



Advance Product Information

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Stereo Analog to Digital Features

- 91 dB Dynamic Range (A-wtd)
- -85 dB THD+N
- Independent ADC Channel Control
- 2:1 Stereo Analog Input MUX
- Stereo Line Input
  - Shared Pseudo-differential Reference Input
- Dual Analog MIC Inputs
  - Pseudo-diff. or Single-ended
  - Two, Independent, Programmable, Low-noise, MIC Bias Outputs
  - MIC Short Detect to Support Headset Button
- Analog Programmable Gain Amplifier (PGA) (+12 to -6 dB in 0.5 dB steps)
- +10 dB or +20 dB Analog MIC Boost in Addition to PGA Gain Settings
- Programmable Automatic Level Control (ALC)
  - Noise Gate for Noise Suppression
  - Progr. Threshold & Attack/Release Rates

Dual Digital Microphone Interface

- Programable Clock Rate
  - Integer Divide by 2 or 4 of Internal MCLK

Stereo DAC to Headphone Amplifier

- 94 dB Dynamic Range (A-wtd)
- -81 dB THD+N into 32 Ω
- Integrated Step-down/Inverting Charge Pump
- Class H Amplifier - Automatic Supply Adj.
  - High Efficiency
  - Low EMI
- Pseudo-differential Ground-centered Outputs
- High HP Power Output at -70/-81 dB THD+N
  - 2 x 17/8.5 mW into 16/32 Ω @ 1.8 V
- Pop and Click Suppression
- Analog Vol. Ctl. (+12 to -50 dB in 1 dB steps; to -76 dB in 2 dB steps) with Zero-cross Trans.
- Digital Vol. Ctl. (+12 to -102 dB in 0.5 dB steps) with Soft-ramp Transitions
- Programmable Peak-detect and Limiter

Stereo DAC to Line Outputs

- 97 dB Dynamic Range (A-wtd)
- -86 dB THD+N
- Class-H Amplifier
- Pseudo-differential Ground-centered Outputs
- 1 V_{RMS} Line Output @ 1.8 V
- Pop and Click Suppression
- Analog Vol. Ctl. (+12 to -50 dB in 1 dB steps; to -76 dB in 2 dB steps) with Zero-cross Trans.
- Digital Vol. Ctl. (+12 to -102 dB in 0.5 dB steps) with Soft-ramp Transitions
- Programmable Peak-detect and Limiter

Mono DAC to Ear Speaker Amplifier

- High Power Output at -70 dB (0.032%) THD+N
  - 45 mW into 16 Ω @ 1.8 V
- Pop and Click Suppression
- Digital Vol. Ctl. (+12 to -102 dB in 0.5 dB steps) with Soft-ramp Transitions
- Programmable Peak-detect and Limiter

Mono DAC to Speakerphone Amplifier

- High Output Power at ≤ 1% THD+N
  - 1.18/0.84/0.66 W into 8 Ω @ 5.0/4.2/3.7 V
- Direct Battery-powered Operation
- Pop and Click Suppression
- Digital Vol. Ctl. (+12 to -102 dB in 0.5 dB steps) with Soft-ramp Transitions
- Programmable Peak-detect and Limiter

Mono DAC to Speakerph. Line Output

- 84 dB Dynamic Range (A-wtd)
- -75 dB THD+N
- High Voltage (1.53 V_{RMS} @ VA = 1.8 V, VP = 3.7 V) Line Output to Ensure Maximum Output from a Wide Variety of External Amplifiers
- Pop and Click Suppression
- Digital Vol. Ctl. (+12 to -102 dB in 0.5 dB steps) with Soft-ramp Transitions
- Programmable Peak-detect and Limiter

Serial Ports

- Three Independent Serial Ports: Auxiliary, Audio, and Voice
- 8.00, 11.025, 12.00, 16.00, 22.05, 24.00, 32.00, 44.10, and 48.00 kHz Sample Rates
- All Ports Support Master or Slave Operation with I²S Interface
- Auxiliary and Voice Ports Support Slave Operation with PCM Interface
- Auxiliary and Audio Ports are Stereo-Input/Stereo-Output to/from Digital Mixer
- Voice Port is Mono-Input/Stereo-Output to/from Digital Mixer
- Integrated Asynch. Sample Rate Converters

General Description

The CS42L73 is a highly integrated, low-power, audio and telephony CODEC for portable applications such as smartphones and ultra mobile personal computers.

The CS42L73 features a **flexible clocking architecture**, allowing the device to utilize reference clock frequencies of 6, 12, 24, 13, 26, 19.2, or 38.4 MHz, or any standard audio master clock. Up to two reference/master clock sources may be connected; either one can be selected to drive the internal clocks and processing rate of the CS42L73. Thus, multiple master clock sources within a system can be dynamically activated and de-activated to minimize system-level power consumption.

Three asynchronous bidirectional serial ports (Auxiliary, Audio, and Voice Serial Ports) support multiple clock domains of various digital audio sources or destinations. Three low-latency, fast-locking, integrated **high-performance asynchronous sample rate converters** synchronize and convert the audio samples to the internal processing rate of the CS42L73.

A stereo line input or two mono (one stereo) microphone (MIC) inputs are routed to a **stereo ADC**. The MIC inputs may be selectively pre-amplified by +10 or +20 dB. Two independent, low-noise MIC bias voltage supplies are also provided. A programmable gain amplifier (PGA) is applied to the inputs before they reach the ADC.

The **stereo input path** that follows the stereo ADC begins with a multiplexer to selectively choose data from a **digital MIC interface**. Following the multiplexer, the data is decimated, selectively DC high-pass filtered, channel-swapped or mono-to-stereo routed (fanned-out), and volume adjusted or muted. The volume levels can be automatically adjusted via a programmable Automatic Level Control (ALC) and noise gate.

A **digital mixer** is utilized to mix and route the CS42L73's inputs (analog inputs to ADC, digital MIC, or serial ports) to outputs (DAC-fed amplifiers or serial ports). There is independent attenuation on each mixer input for each output.

The processing along the **output paths** from the digital mixer to the **two stereo DACs** includes volume adjustment and mute control. A peak-detector can be used to automatically adjust the volume levels via a programmable limiter.

The first stereo DAC feeds the **stereo headphone and line output amplifiers**, which are powered from a dedicated positive supply. An integrated **charge pump** provides a negative supply. This allows a ground-centered analog output with a wide signal swing, and eliminates external DC-blocking capacitors while reducing pops and clicks. Tri-level Class-H amplification is utilized to reduce power consumption under low-signal-level conditions. Analog volume controls are provided on the stereo headphone and line outputs.

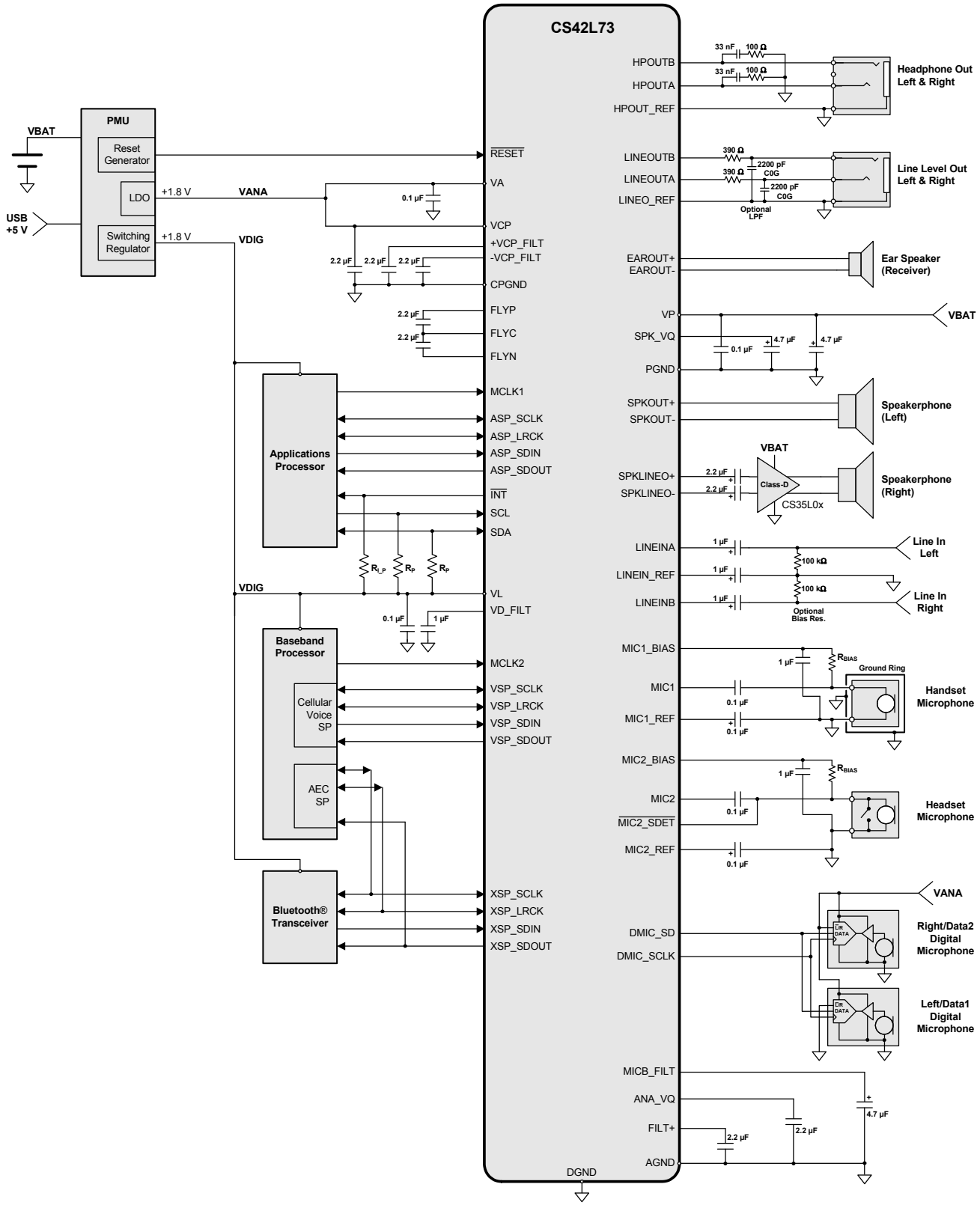
The second stereo DAC feeds several mono outputs. The left channel of the DAC sources a **mono, differential-drive, speakerphone amplifier** for driving the handset speakerphone. The right channel sources a **mono, differential-drive, earphone amplifier** for driving the handset earphone. The right channel is also routed to a **mono, differential-drive, speakerphone line output**, which may be connected to an external amplifier to implement a stereo speakerphone configuration when it is used in conjunction with the integrated speakerphone amplifier.

The CS42L73 implements **robust power management** to achieve ultra-low power consumption. High granularity in power-down controls allows individual functional blocks to be powered down when unused. The internal low drop-out regulator (LDO) saves power by running the internal digital circuits at half the logic interface supply voltage (VL/2). In a system with an existing high-efficiency supply at VL/2, the internal LDO may be disabled and the digital circuits powered directly by the external VL/2 supply.

A high-speed **I²C control port** interface capable of up to 400 kHz operation facilitates register programming.

The CS42L73 is available in space-saving 64-ball WLCSP and 65-ball FBGA packages for the commercial (-40° to +85° C) grade.

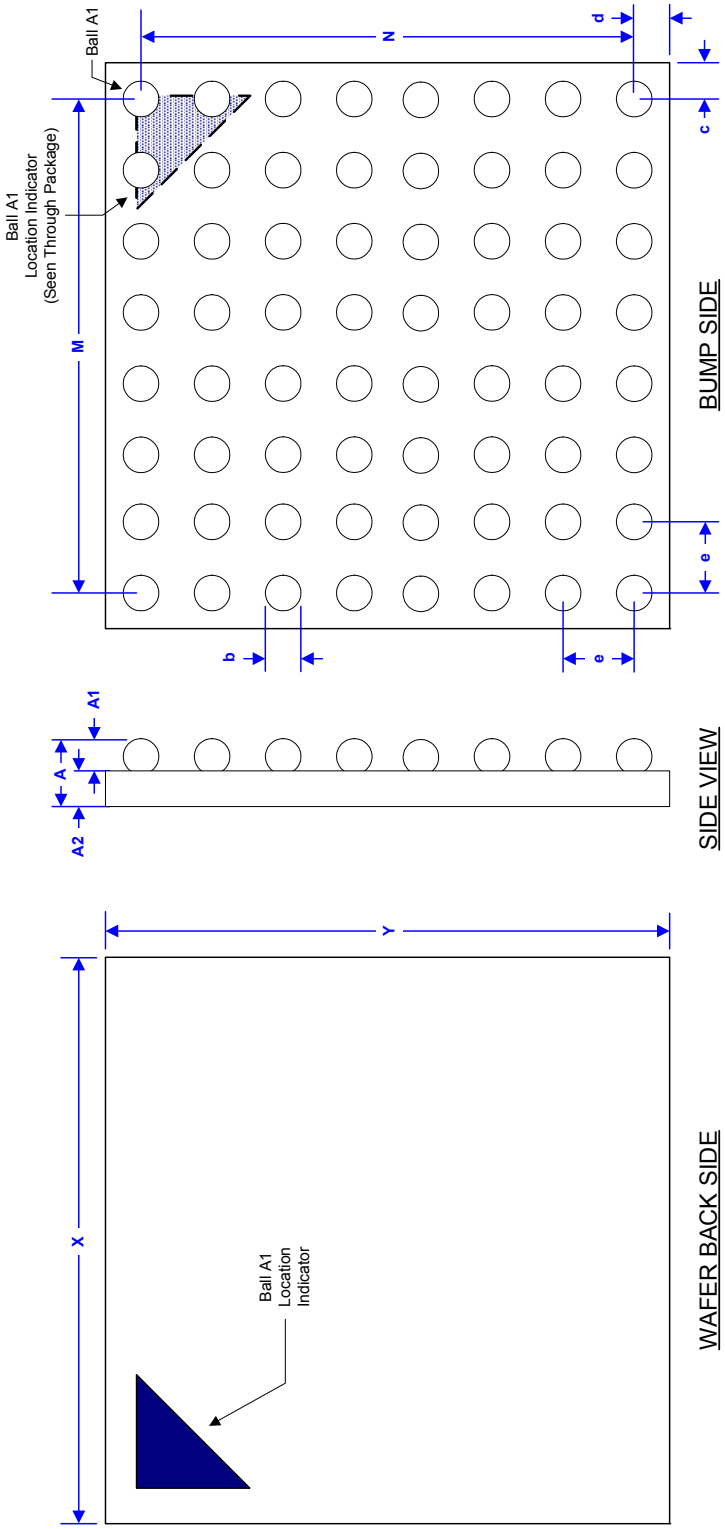
1. TYPICAL CONNECTION DIAGRAM



2. PACKAGE DIMENSIONS

2.1 WLCSP Package

64 Ball WLCSP (3.44 x 3.44 mm Body) Package Drawing



Notes:

1. Controlling dimensions are in millimeters.
2. Dimensioning and tolerances per ASME Y 14.5M-1994.
3. Dimension "b" applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane.
4. Unless otherwise specified, tolerances are: Linear ±0.05 mm, Angular ±1°.

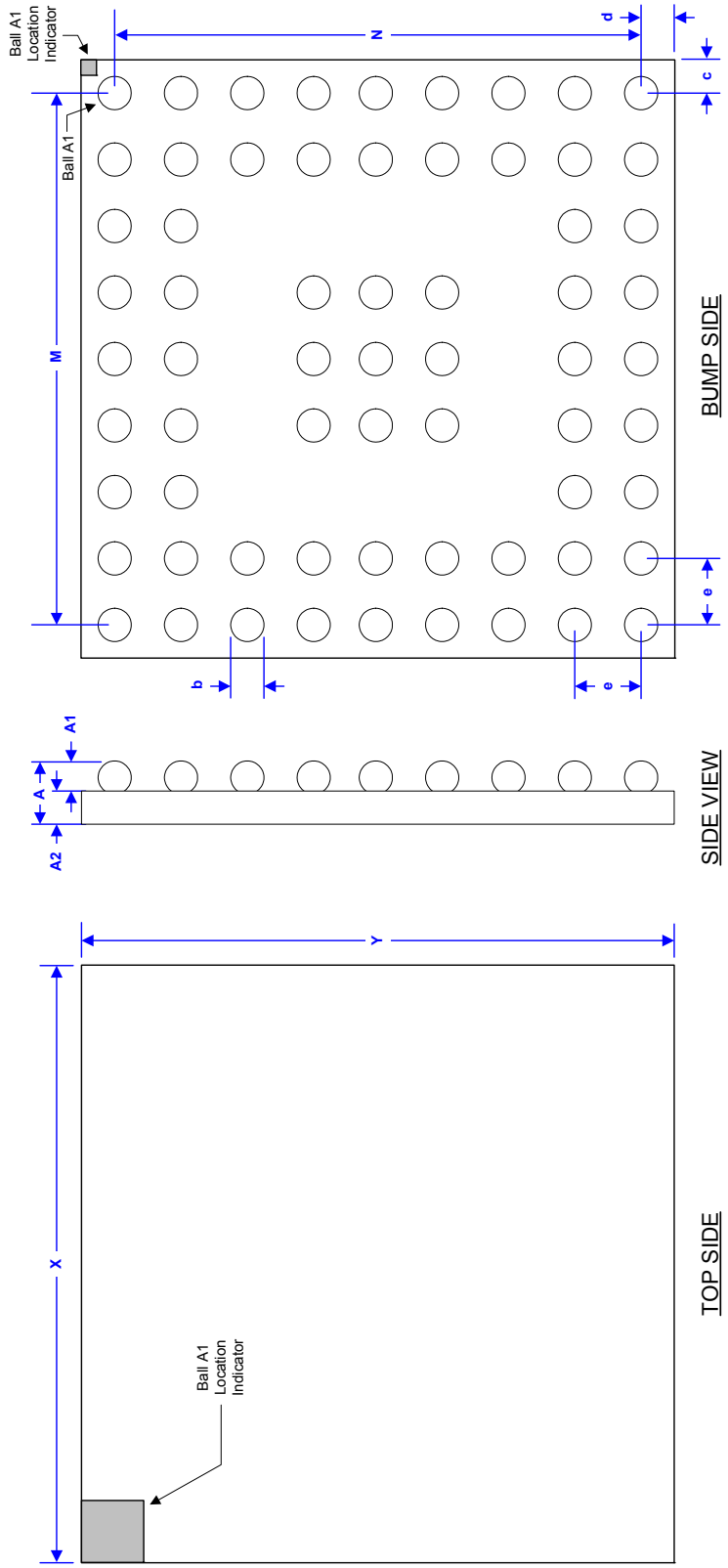
Dim	MILLIMETERS		
	MIN	NOM	MAX
A	0.450	0.505	0.560
A1	0.170	0.200	0.230
A2	0.280	0.305	0.330
M	-	2.800	-
N	-	2.800	-
b	0.230	0.260	0.290
c	-	0.320	-
d	-	0.320	-
e	-	0.400	-
X	3.415	3.440	3.465
Y	3.415	3.440	3.465

Controlling Dimension is Millimeters.

Table 1. WLCSP Package Dimensions

2.2 FBGA Package

65 Ball FBGA (5 x 5 mm Body) Package Drawing



Notes:

1. Controlling dimensions are in millimeters.
2. Dimensioning and tolerances per ASME Y 14.5M-1994.
3. Dimension "b" applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane.
4. Unless otherwise specified, tolerances are: Linear ±0.05 mm, Angular ±1°.

Dim	MILLIMETERS		
	MIN	NOM	MAX
A	0.74	0.87	1.00
A1	0.16	0.21	0.26
A2	0.58	0.66	0.74
M	-	4.00	-
N	-	4.00	-
b	0.27	0.30	0.37
c	-	0.50	-
d	-	0.50	-
e	-	0.50	-
X	4.90	5.00	5.10
Y	4.90	5.00	5.10

Controlling Dimension is Millimeters.

Table 2. FBGA Package Dimensions

3. THERMAL CHARACTERISTICS

Parameter (Notes 1 and 2)	Symbol	Min	Typ	Max	Units
WLCSP Package					
Junction to Ambient Thermal Impedance	θ_{JA}	-	43	-	°C/Watt
FBGA Package					
Junction to Ambient Thermal Impedance	θ_{JA}	-	58	-	°C/Watt

Notes:

1. Test Printed Circuit Board Assembly (PCBA) constructed in accordance with JEDEC standard JESD51-9. Two signal, two plane (2s2p) PCB utilized.
2. Test conducted with still air in accordance with JEDEC standards JESD51, JESD51-2A, and JESD51-8.

4. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42L73	Ultra Low Power Mobile Audio and Telephony CODEC	64 Ball WLCSP	YES	Commercial	-40 to +85 °C	Tray	CS42L73-CWZ
						Tape & Reel	CS42L73-CWZR
		65 Ball FBGA				Tray	CS42L73-CRZ
						Tape & Reel	CS42L73-CRZR

Contacting Cirrus Logic Support

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