



# BUK9K6R2-40E

Dual N-channel TrenchMOS logic level FET

23 April 2013

Product data sheet

## 1. General description

Dual logic level N-channel MOSFET in a LFP56D package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)} > 0.5 \text{ V @ } 175 \text{ °C}$

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

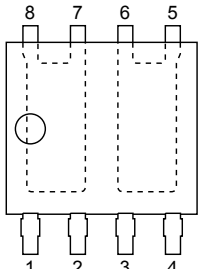
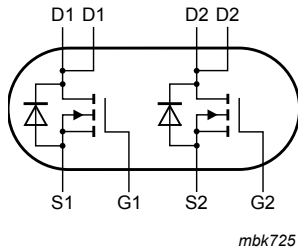
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25 \text{ °C}; T_j \leq 175 \text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C}; \text{Fig. 1}$	-	-	40	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ °C}; \text{Fig. 2}$	-	-	68	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ °C}; \text{Fig. 12}$	-	5.27	6.2	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 10 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	5.8	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFAK56D (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K6R2-40E	LFAK56D	Plastic single ended surface mounted package (LFAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K6R2-40E	96E240

## 8. Limiting values

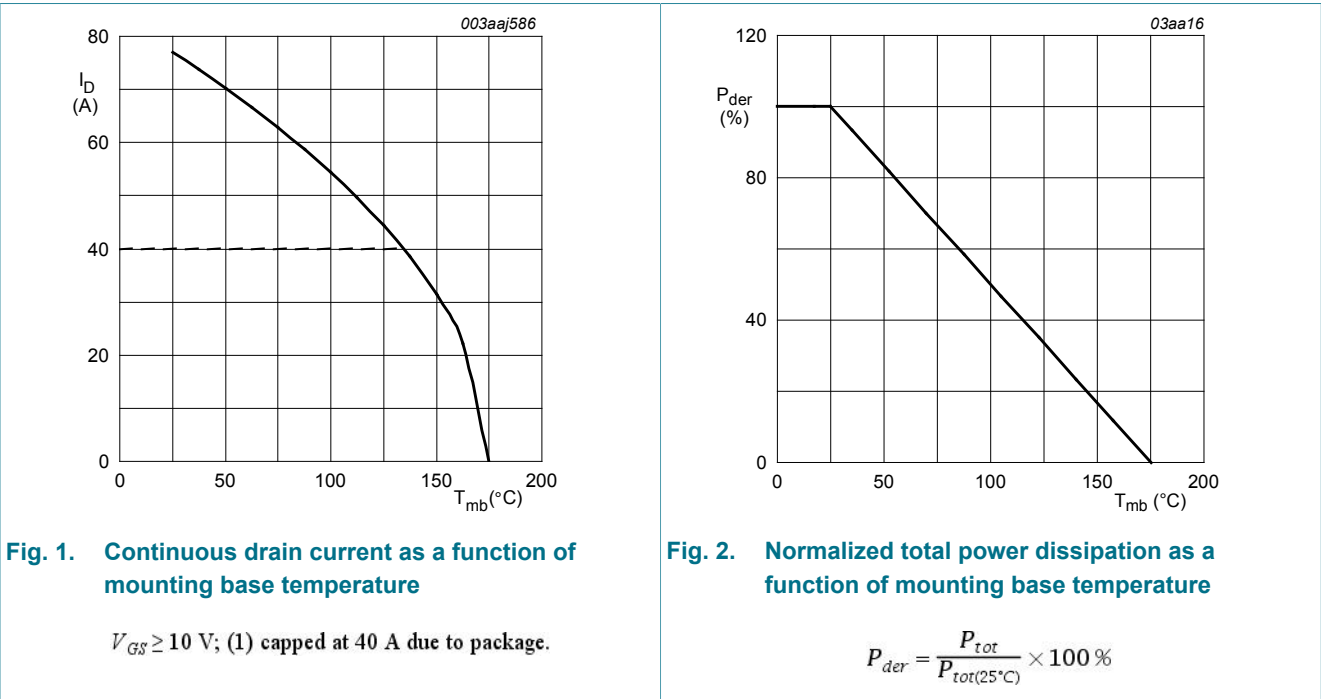
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$ ; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$ ; $T_j \geq 25\text{ }^{\circ}\text{C}$ ; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	40	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ }^{\circ}\text{C}$ ; DC	-10	10	V
		$T_j \leq 175\text{ }^{\circ}\text{C}$ ; Pulsed	[1][2] -15	15	V
$I_D$	drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	40	A
		$T_{mb} = 100\text{ }^{\circ}\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	40	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4	-	295	A

Symbol	Parameter	Conditions		Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	68	W
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drain diode FET1 and FET2						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	40	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	295	A
Avalanche Ruggedness FET1 and FET2						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 40 A; V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; <a href="#">Fig. 3</a>	<a href="#">[3][4]</a>	-	166	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and or V<sub>GS</sub>.
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



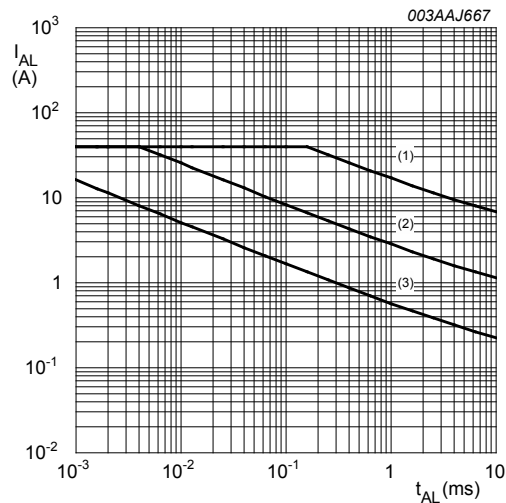


Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

- (1) Single-pulse;  $T_j = 25\text{ }^{\circ}\text{C}$ .
- (2) Single-pulse;  $T_j = 150\text{ }^{\circ}\text{C}$ .
- (3) Repetitive.

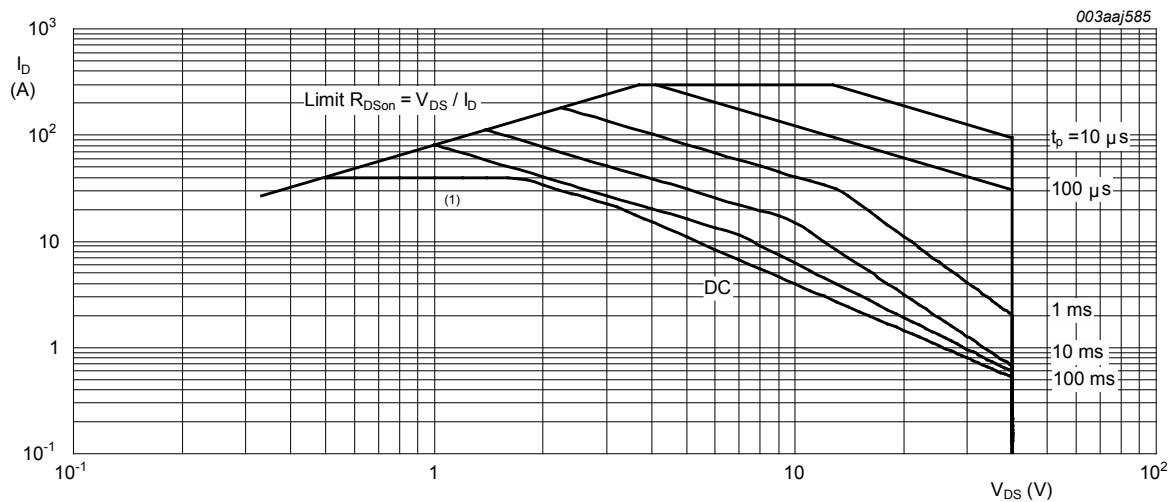


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $I_{DM}$  is a single pulse; (1) Capped at 40 A due to package

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.21	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

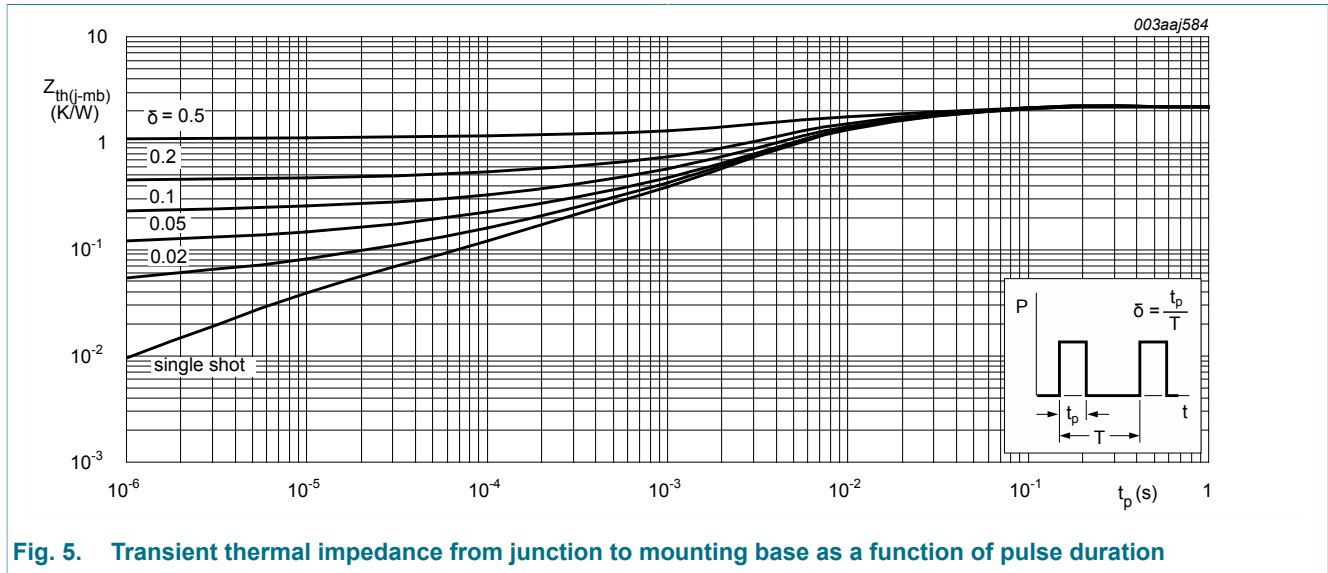


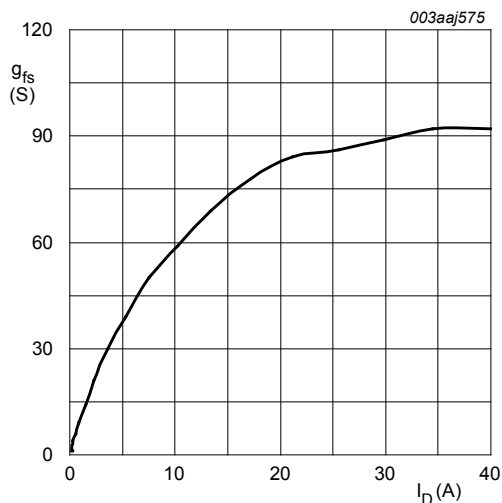
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

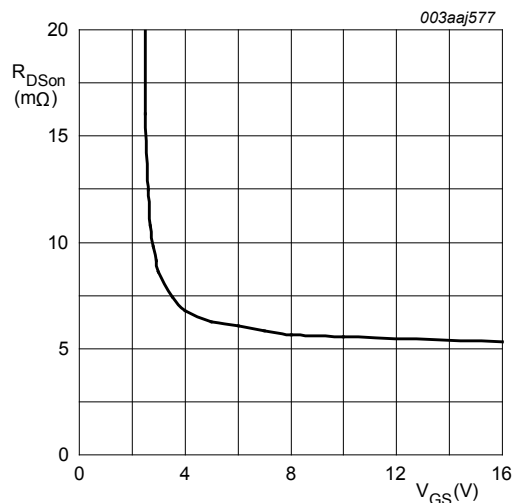
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_J = -55 ^\circ C$	36	-	-	V
		$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_J = 25 ^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_J = 25 ^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	1.4	1.7	2.1	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_J = 175 ^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	0.5	-	-	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_J = -55 ^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 V$ ; $V_{GS} = 0 V$ ; $T_J = 175 ^\circ C$	-	-	500	$\mu A$
		$V_{DS} = 40 V$ ; $V_{GS} = 0 V$ ; $T_J = 25 ^\circ C$	-	0.02	1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -10 V$ ; $V_{DS} = 0 V$ ; $T_J = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = 10 V$ ; $V_{DS} = 0 V$ ; $T_J = 25 ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 V$ ; $I_D = 20 A$ ; $T_J = 25 ^\circ C$ ; <a href="#">Fig. 12</a>	-	5.27	6.2	m $\Omega$
		$V_{GS} = 5 V$ ; $I_D = 20 A$ ; $T_J = 175 ^\circ C$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	10.2	12.5	m $\Omega$

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$V_{GS} = 10\text{ V}$ ; $I_D = 20\text{ A}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 12</a>		-	4.84	6	mΩ
Dynamic characteristics FET1 and FET2							
$Q_{G(\text{tot})}$	total gate charge	$I_D = 10\text{ A}$ ; $V_{DS} = 32\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	35.4	-	nC
$Q_{GS}$	gate-source charge			-	4.4	-	nC
$Q_{GD}$	gate-drain charge			-	5.8	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 16</a>		-	2461	3281	pF
$C_{oss}$	output capacitance			-	345	414	pF
$C_{rss}$	reverse transfer capacitance			-	162	222	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 32\text{ V}$ ; $R_L = 3.3\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $R_{G(\text{ext})} = 5\text{ }\Omega$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; $I_D = 10\text{ A}$		-	6	-	ns
$t_r$	rise time			-	7.1	-	ns
$t_{d(\text{off})}$	turn-off delay time			-	44.4	-	ns
$t_f$	fall time			-	19.8	-	ns
Source-drain diode FET1 and FET2							
$V_{SD}$	source-drain voltage	$I_S = 15\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 17</a>		-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$		-	23.7	-	ns
$Q_r$	recovered charge			-	16.8	-	nC



**Fig. 6. Forward transconductance as a function of drain current; typical values**

$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 15\text{ V}$$



**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$$

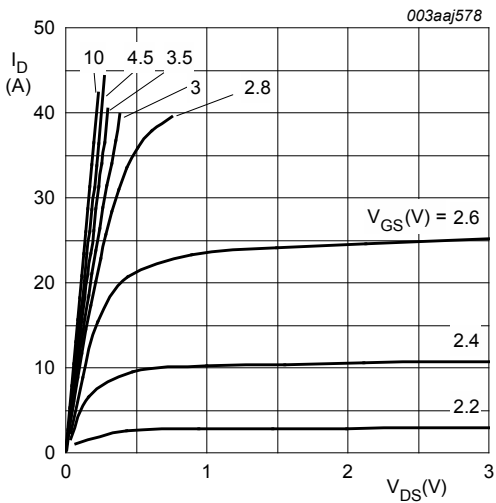


Fig. 8. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}$

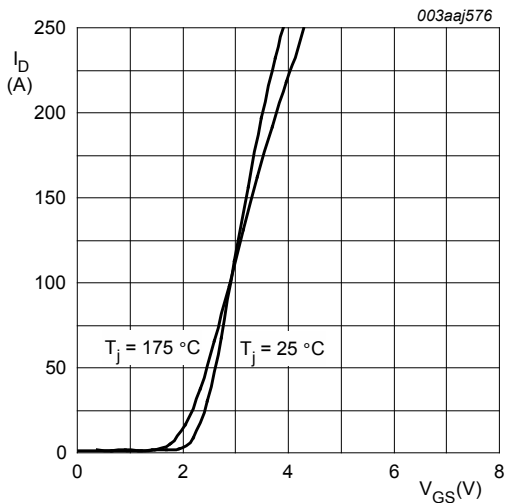


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

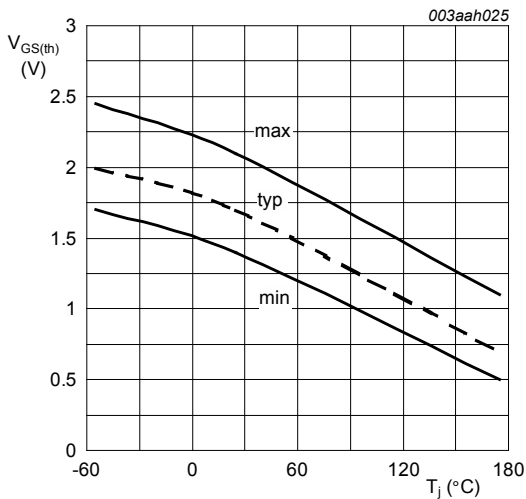


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

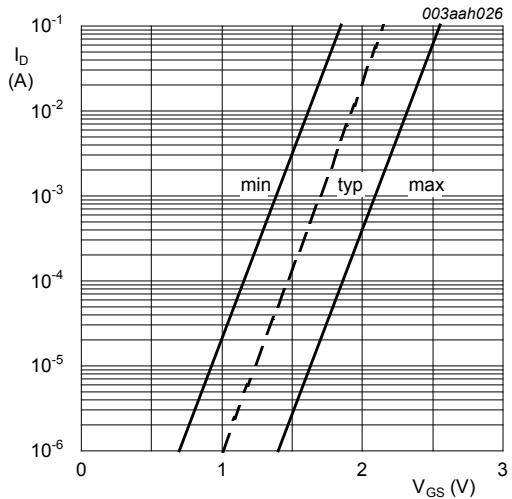


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

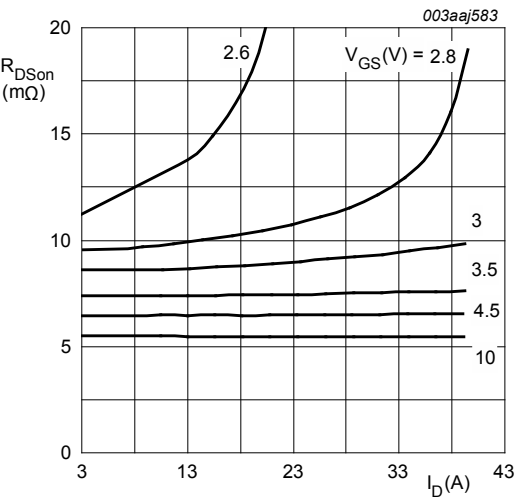


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

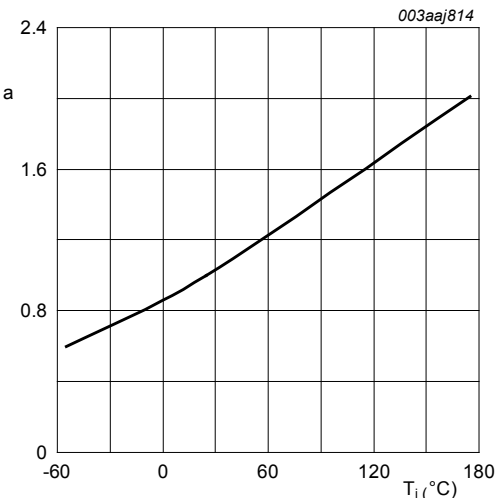


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

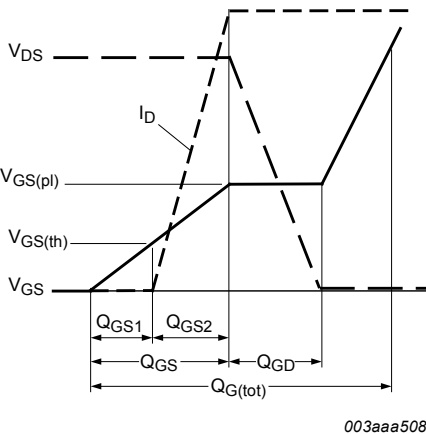


Fig. 14. Gate charge waveform definitions

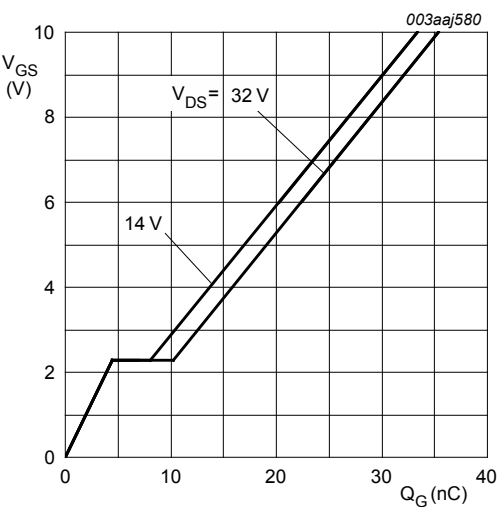


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$



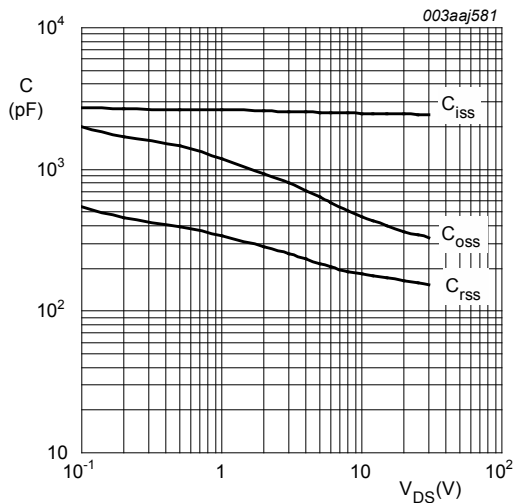


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

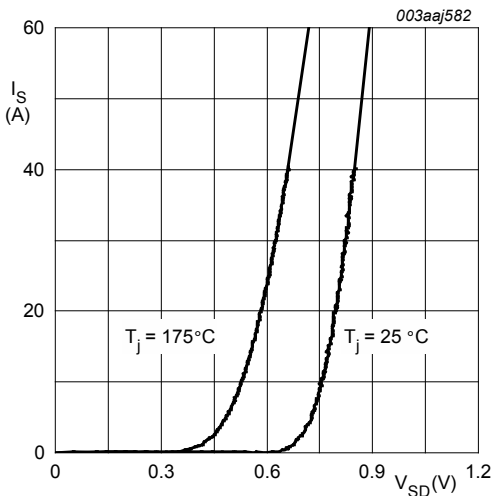


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0\text{ V}$

11. Package outline

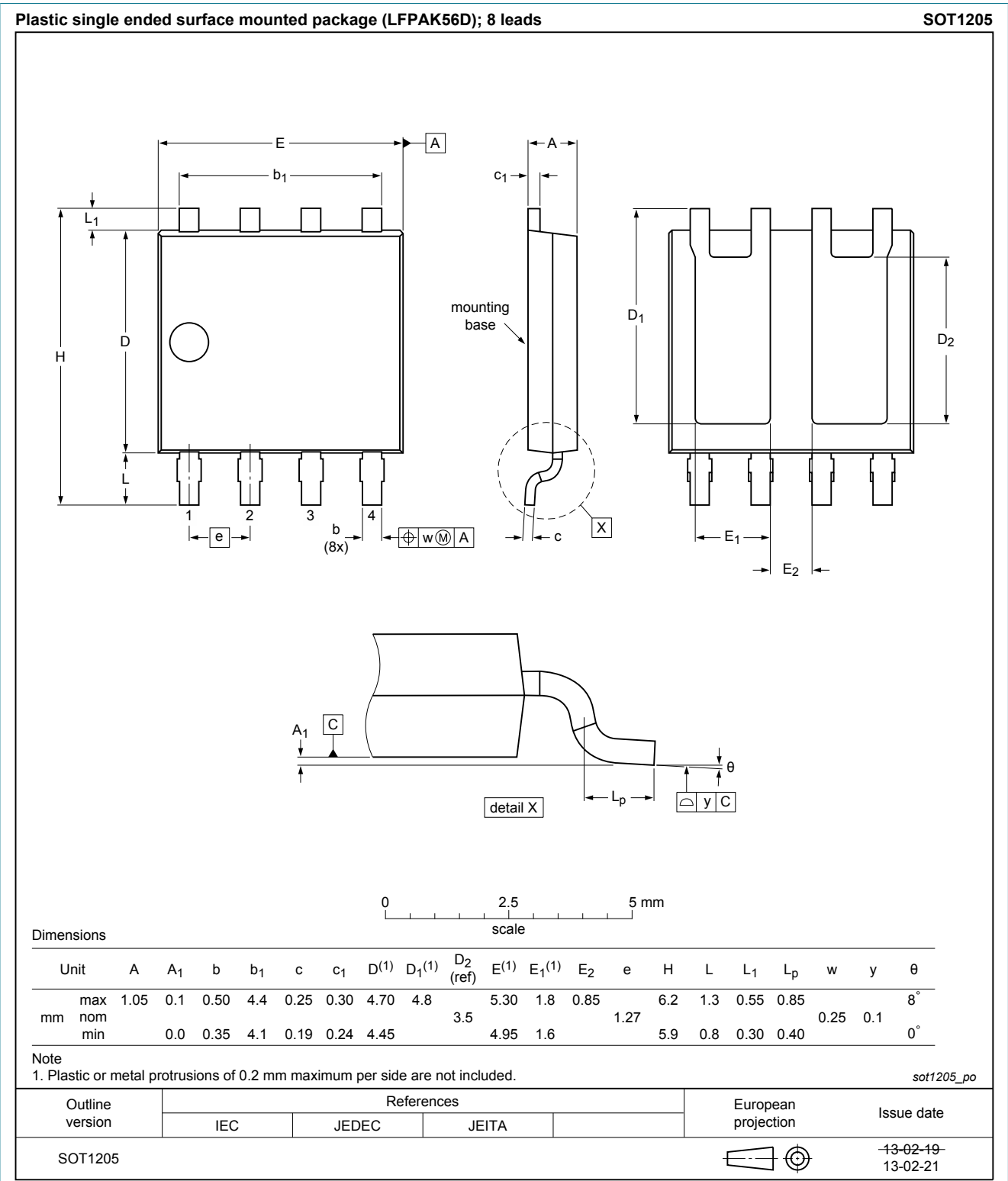


Fig. 18. Package outline LPAK56D (SOT1205)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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