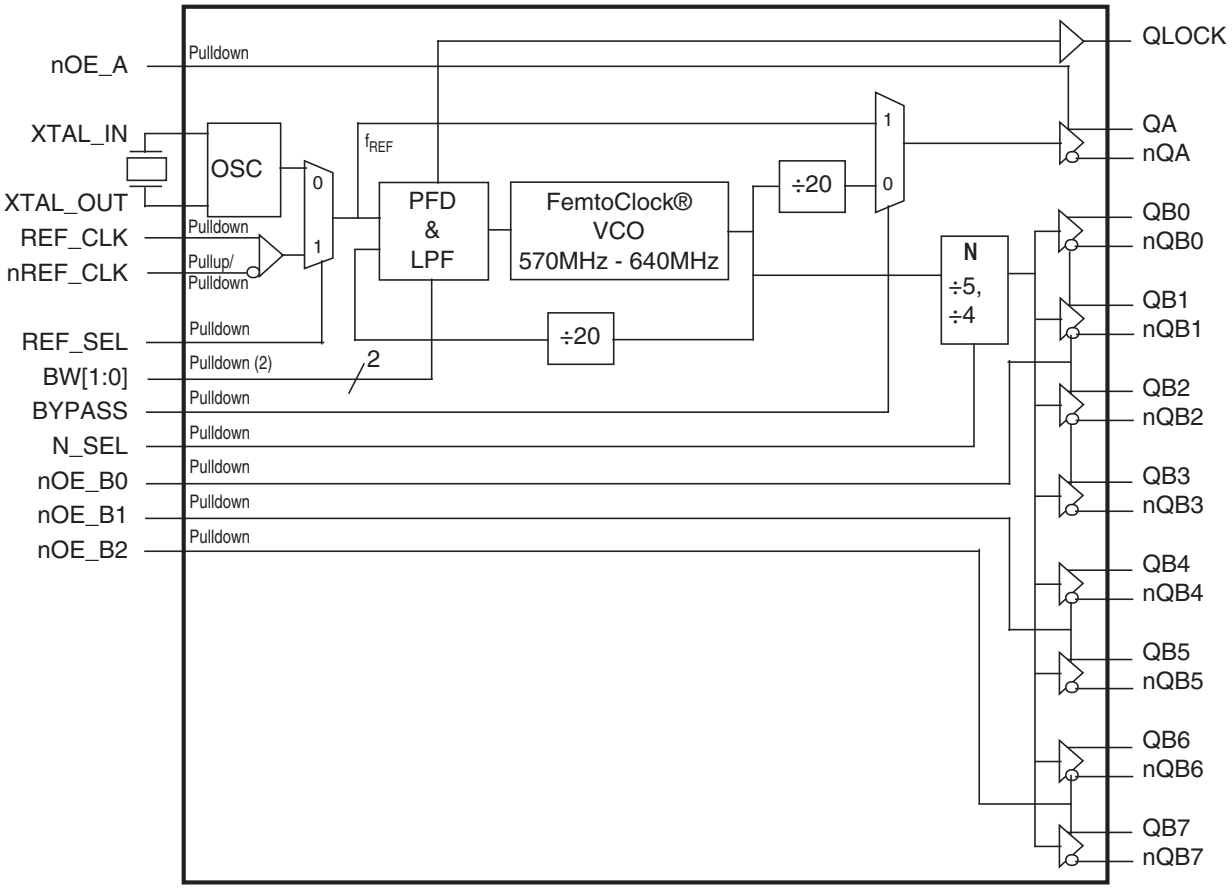
General Description

The 814S208 is an eight LVDS output clock synthesizer designed for wireless infrastructure applications. The device generates eight copies of a selectable 122.88MHz or 153.6MHz clock signal with excellent phase jitter performance. The PLL is optimized for a reference frequency of 30.72MHz. Both a crystal interface and a differential system clock input are supported for the reference frequency. An extra LVDS output duplicates the reference frequency and is provided for clock tree cascading. The device uses IDT's third generation FemtoClock® technology for an optimum of high clock frequency and low phase noise performance, combined with a low power consumption. A PLL lock status output is provided for monitoring and diagnosis purpose. The device supports a 3.3V voltage supply and is packaged in a small, lead-free (RoHS 6) 48-lead VFQFN package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

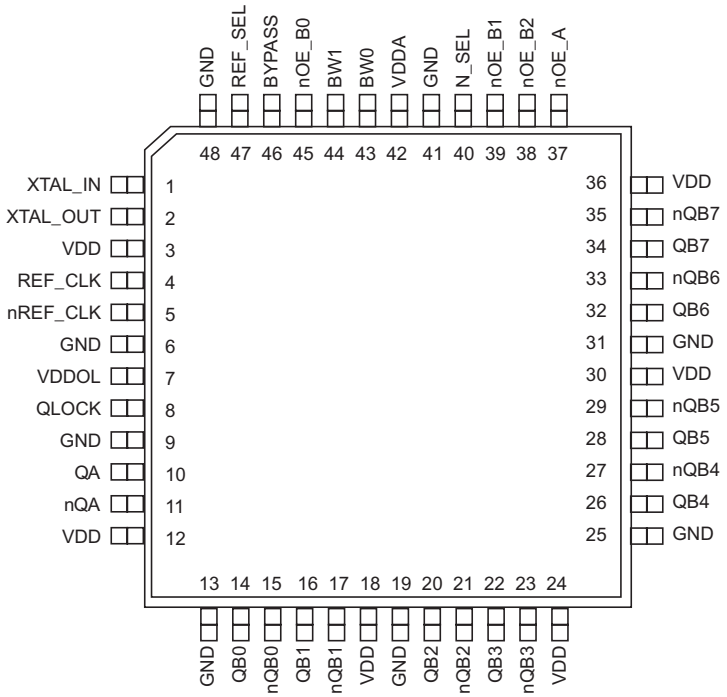
Features

- Third generation FemtoClock® technology
- Selectable 122.88MHz or 153.6MHz output clock synthesized from a 30.72MHz fundamental mode crystal
- Eight differential LVDS clock outputs
- Differential reference clock input pair
- PLL lock indicator output
- Crystal interface designed for a 30.72MHz, parallel resonant crystal
- RMS phase jitter @ 122.88MHz, using a 30.72MHz crystal (12kHz - 20MHz): 0.650ps (typical)
- RMS phase jitter @ 153.6MHz, using a 30.72MHz crystal (12kHz - 20MHz): 0.642ps (typical)
- LVCMOS interface levels for the control input
- Full 3.3V supply voltage
- Available in Lead-free (RoHS 6) 48-lead VFQFN package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



814S208
48-lead VFQFN
7.0mm x 7.0mm x 0.925mm, package body
K Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
3, 12, 18, 24, 30, 36	V_{DD}	Power		Core power supply pins.
4	REF_CLK	Input	Pulldown	Non-inverting differential reference clock input. Differential output can accept the following differential input levels: LVPECL, LVDS, CML.
5	nREF_CLK	Input	Pullup/ Pulldown	Inverting differential reference clock input. Differential output can accept the following differential input levels: LVPECL, LVDS, CML.
6, 9, 13, 19, 25, 31, 41, 48	GND	Power		Power supply ground.
7	V_{DDOL}	Power		Output supply pin for the PLL lock output (QLOCK). Supports 3.3V, 2.5V or 1.8V.
8	QLOCK	Output		PLL lock indication. See Table 3I for function. Supports 3.3V, 2.5V or 1.8V.
10, 11	QA, nQA	Output		Differential clock output pair. LVDS interface levels.
14, 15	QB0, nQB0	Output		Differential clock output pair. LVDS interface levels
16, 17	QB1, nQB1	Output		Differential clock output pair. LVDS interface levels
20, 21	QB2, nQB2	Output		Differential clock output pair. LVDS interface levels
22, 23	QB3, nQB3	Output		Differential clock output pair. LVDS interface levels
26, 27	QB4, nQB4	Output		Differential clock output pair. LVDS interface levels
28, 29	QB5, nQB5	Output		Differential clock output pair. LVDS interface levels
32, 33	QB6, nQB6	Output		Differential clock output pair. LVDS interface levels
34, 35	QB7, nQB7	Output		Differential clock output pair. LVDS interface levels
37	nOE_A	Input	Pulldown	Output enable input. See Table 3E for function. LVCMOS/LVTTL interface levels.
38, 39, 45	nOE_B2, nOE_B1, nOE_B0	Input	Pulldown	Output enable inputs. See Tables 3F-3H for function. LVCMOS/LVTTL interface levels.
40	N_SEL	Input	Pulldown	Frequency select pin. See Table 3A for function. LVCMOS/LVTTL interface levels.
42	V_{DDA}	Power		Analog power supply.
43, 44	BW0, BW1	Input	Pulldown	PLL bandwidth control pins. See Table 3D for function. LVCMOS/LVTTL interface levels.
46	BYPASS	Input	Pulldown	PLL bypass mode select pin. See Table 3B for function. LVCMOS/LVTTL interface levels.
47	REF_SEL	Input	Pulldown	Reference select input. See Table 3C for function. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{PULLUP}	Input Pullup Resistor				51		kΩ
R_{OUT}	Output Impedance	QLOCK	QLOCK = HIGH, V_{DDOL} = 3.3V		26		Ω
			QLOCK = HIGH, V_{DDOL} = 2.5V		32		Ω
			QLOCK = HIGH, V_{DDOL} = 1.8V		44		Ω
			QLOCK = LOW, V_{DDOL} = 3.3V, 2.5V, 1.8V		22		Ω

Function Tables

Table 3A. Output Divider N Function Table

Inputs	Operation	
N_SEL	**N**	**QB[0:7] Frequency with f_{REF} = 30.72MHz**
0 (default)	÷5	122.88MHz, (4 * f_{REF})
1	÷4	153.6MHz, (5 * f_{REF})

NOTE: N_SEL is an asynchronous control.
NOTE: With f_{XTAL}= 30.72MHz and all control inputs in the default state, the ICS814S208I generates 30.72MHz at the QA output and 122.88MHz at the QBx outputs.

Table 3B. PLL BYPASS Function Table

Input	Operation	
BYPASS	**QA**	**QB[0:7]**
0 (default)	f_{OUT}, QA = f_{VCO} ÷ 20	f_{OUT}, QBx = f_{REF} * 20 ÷ N
1	f_{OUT}, QA = f_{REF} (PLL bypass)	

NOTE: BYPASS is an asynchronous control.
NOTE: In PLL bypass mode, the frequency f_{REF} is output at QA without frequency division. AC specifications do not apply in PLL bypass mode.

Table 3C. PLL Reference Clock Select Function Table

Input	
REF_SEL	**Operation**
0 (default)	The crystal interface is selected as reference clock
1	The REF_CLK input is selected as reference clock

NOTE: REF_SEL is an asynchronous control.

Table 3D. PLL Bandwidth Function Table

Inputs		Operation
BW1	**BW0**	**PLL Bandwidth**
0 (default)	0 (default)	240kHz
0 (default)	1	520kHz
1	0 (default)	1MHz
1	1	2MHz

NOTE: BW[1:0] is an asynchronous control.
NOTE: With the lowest PLL bandwidth setting (BW[1:0] = 00, 240kHz), the PLL attenuates input reference jitter with spectral components above 240kHz. With the highest PLL bandwidth setting (BW[1:0] = 11, 2MHz), the PLL is not optimized for input reference jitter attenuation.

Table 3E. nOE_A Output Enable Function Table

Input	
nOEA	**Operation**
0 (default)	QA, nQA outputs are enabled
1	QA, nQA outputs are disabled (high-impedance)

NOTE: nOE_A is an asynchronous control.

Table 3I. QLOCK Output Function Table

Output	
QLOCK	**PLL Status**
0	The PLL is locked to the input reference clock
1	The PLL is not locked to the input reference clock

NOTE: QLOCK supports 3.3V, 2.5V or 1.8V according to the voltage supplied at V_{DDOL}. See Table 4B.

Table 3F. nOE_B0 Output Enable Function Table

Input	
nOE_B0	**Operation**
0 (default)	QB[0:3], nQB[0:3] outputs are enabled
1	QB[0:3]. nQB[0:3] outputs are disabled (high-impedance)

NOTE: nOE_B0 is an asynchronous control.

Table 3G. nOE_B1 Output Enable Function Table

Input	
nOE_B1	**Operation**
0 (default)	QB[4:5], nQB[4:5] outputs are enabled
1	QB[4:5], nQB[4:5] outputs are disabled (high-impedance)

NOTE: nOE_B1 is an asynchronous control.

Table 3H. nOE_B2 Output Enable Function Table

Input	
nOE_B2	**Operation**
0 (default)	QB[6:7], nQB[6:7] outputs are enabled
1	QB[6:7], nQB[6:7] outputs are disabled (high-impedance)

NOTE: nOE_B2 is an asynchronous control.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	30.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDOL} = 1.8V±0.2V, 2.5V±5% or 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3V	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.22	3.3V	V_{DD}	V
V_{DDOL}	QLOCK Output Supply Voltage		1.6	1.8	2.0	V
			2.375	2.5	2.625	V
			3.135	3.3	3.465	V
I_{DDA}	Analog Supply Current				22	mA
I_{DD}	Power Supply Current				355	mA

NOTE: For the Power Supply Voltage Sequence Information Application Note, see page 12.

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5%, V_{DDOL} = 1.8V±0.2V, 2.5V±5% or 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
I_{IH}	Input High Current	BW[1:0], BYPASS, nOE_A, nOE_B[2:0], REF_SEL, N_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	BW[1:0], BYPASS, nOE_A, nOE_B[2:0], REF_SEL, N_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
V_{OH}	Output High Voltage	QLOCK	V_{DDOL} = 3.465V, I_{OH} = -8mA	2.6			V
			V_{DDOL} = 2.625V, I_{OH} = -8mA	1.8			V
			V_{DDOL} = 2V, I_{OH} = -8mA	1.5			V
V_{OL}	Output Low Voltage	QLOCK	V_{DDOL} = 3.465V or 2.625V, I_{OL} = 8mA			0.5	V
			V_{DDOL} = 2V, I_{OL} = 8mA			0.4	V

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	REF_CLK, nREF_CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	REF_CLK	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nREF_CLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			GND + 1.2		V_{DD}	V

NOTE 1: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		28.5	30.72	32	MHz
Equivalent Series Resistance (ESR)				80	Ω
Shunt Capacitance				7	pF
Drive Level; NOTE 1				100	µW

NOTE 1: Using typical crystal parameter for ESR, C_O, and C_L in a 30.72MHz crystal.

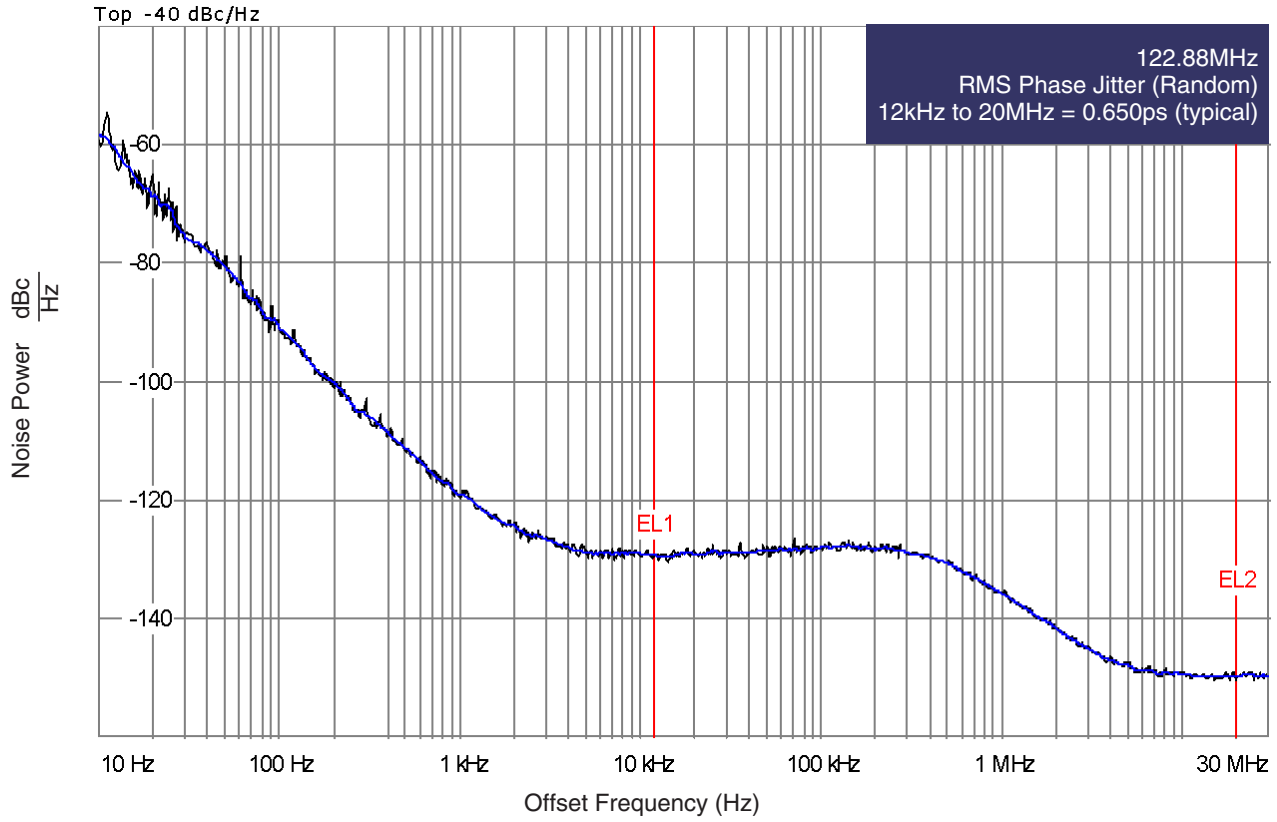
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V±5%, V_{DDOL} = 1.8V±0.2V, 2.5V±5% or 3.3V±5%, T_A = -40°C to 85°C

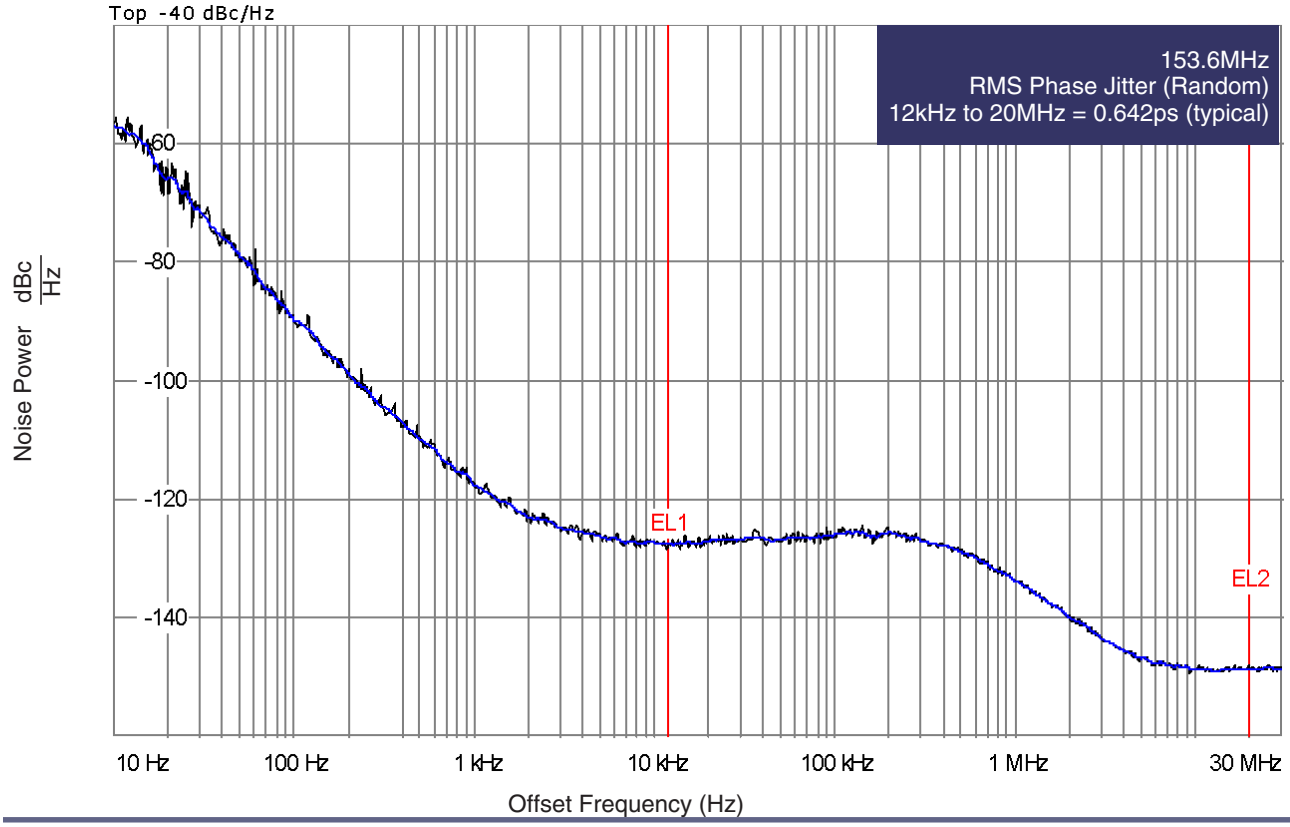
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Frequency		BYPASS = 0	570	614.4	640	MHz
f_{OUT}	Output Frequency	QB[0:7], nQB[0:7]	N_SEL = 0	114	122.88	128	MHz
			N_SEL = 1	142.5	153.6	160	MHz
		QA, nQA	BYPASS = 0	28.5	30.72	32	MHz
f_{REF}	Reference Frequency		BYPASS = 0	28.5	30.72	32	MHz
$t_{jit}(Ø)$	RMS Phase Jitter (Random); NOTE 1		122.88MHz, Integration Range: 1kHz – 40MHz		0.695	0.96	ps
			122.88MHz, Integration Range: 12kHz – 20MHz		0.650	0.89	ps
			153.6MHz, Integration Range: 1kHz – 40MHz		0.714	0.93	ps
			153.6MHz, Integration Range: 12kHz – 20MHz		0.642	0.89	ps
Φ_N	Single-Side Band Noise Power		122.88MHz, Offset: 100Hz		-91		dBc/Hz
			122.88MHz, Offset: 1kHz		-118		dBc/Hz
			122.88MHz, Offset: 10kHz		-130		dBc/Hz
			122.88MHz, Offset: 100kHz		-128		dBc/Hz
t_{jit}(per)	Period Jitter, RMS	QA, nQA			2.1	4.0	ps
		QBx, nQBx			2.3	4.8	ps
		QBx, nQBx	at 122.88MHz		2.3	4.0	ps
TIE	Time Interval Error		Accumulated Period Jitter, 10^6 Samples		±9	±30	ps
t_{PD}	Propagation Delay; NOTE 2		REF_CLK, nREF_CLK to QA, nQA, BYPASS = 1, REF_SEL = 1	550	770	950	ps
tsk(o)	Output Skew; NOTE 3, 4		BYPASS = 0		25	100	ps
tsk(b)	Bank Skew; NOTE 4, 5				25	100	ps
t_R / t_F	Output Rise/Fall Time		10% to 90%	75	200	350	ps
t_{LOCK}	PLL Lock Time				20	100	ms
odc	Output Duty Cycle	QA, nQA	BYPASS = 0	49	50	51	%
		QBx, nQBx	BYPASS = 0	49	50	51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using Rohde & Schwarz SMA100A Signal Generator with f_{REF} = 30.72MHz, unless noted otherwise. V_{DD} and V_{DDA} connected. BW[1:0] = 00.
NOTE 1: Refer to the phase noise plots.
NOTE 2: Measured from the differential input crossing point to the differential output crossing point.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

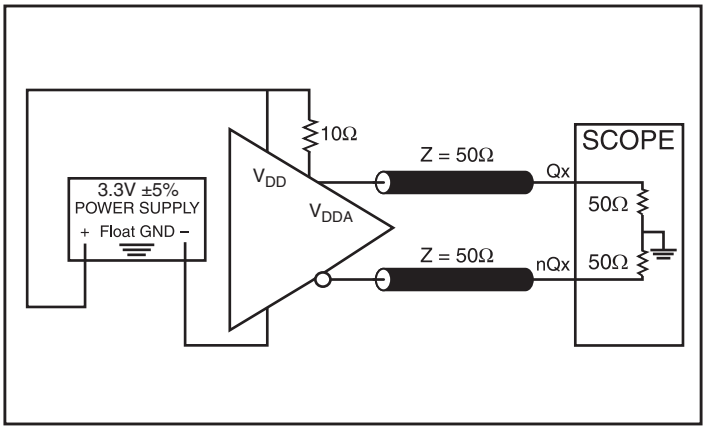
Typical Phase Noise at 122.88MHz



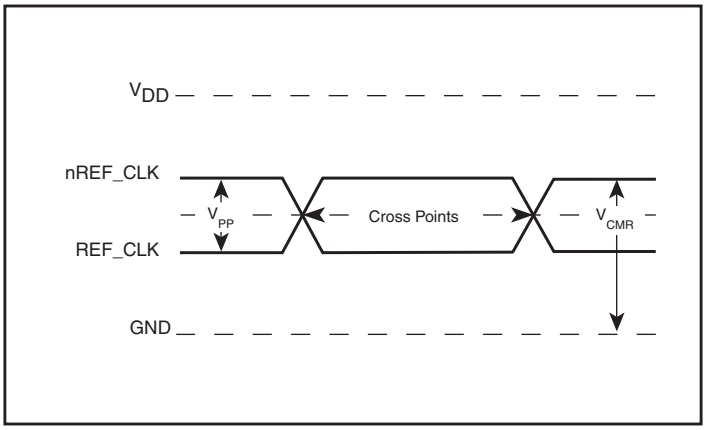
Typical Phase Noise at 153.6MHz



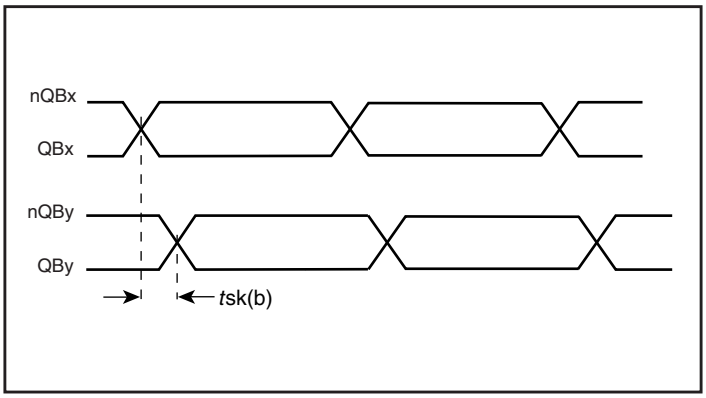
Parameter Measurement Information



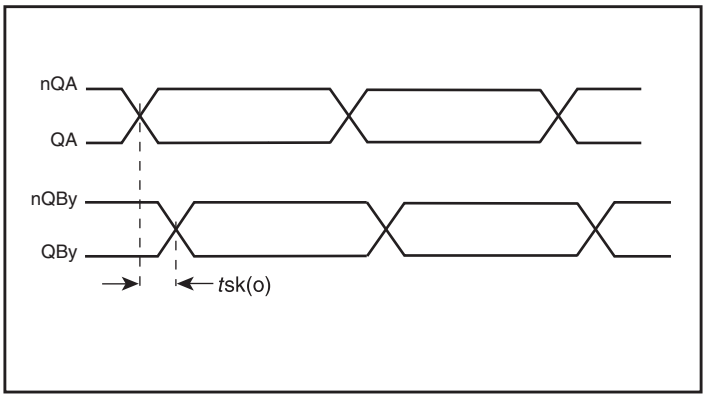
3.3V LVDS Output Load AC Test Circuit



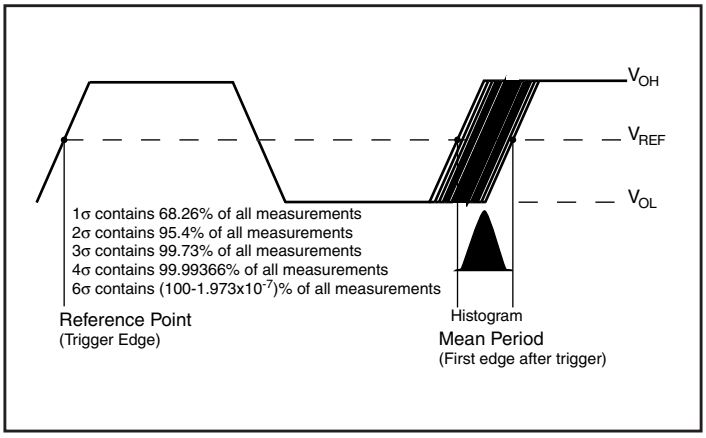
Differential Input Level



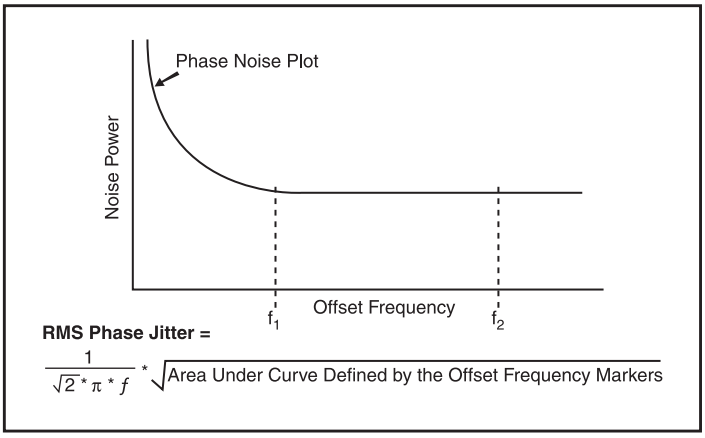
Bank Skew



Output Skew

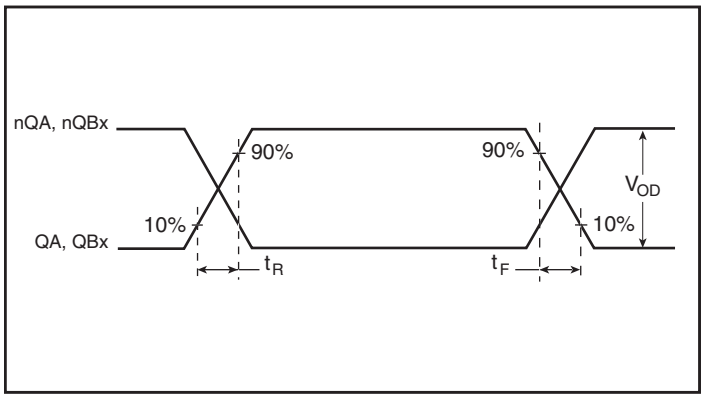


Period Jitter, RMS

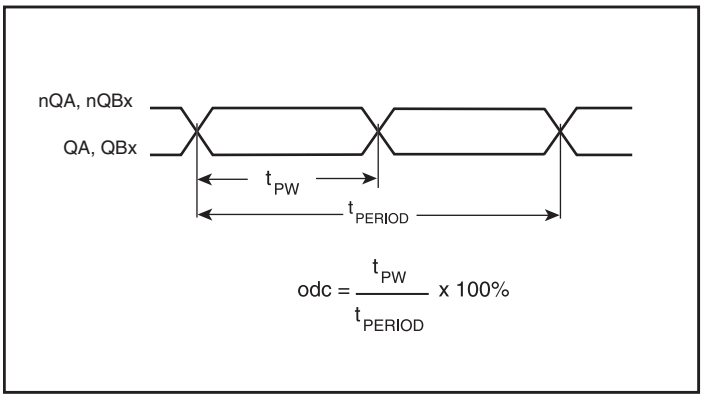


RMS Phase Jitter

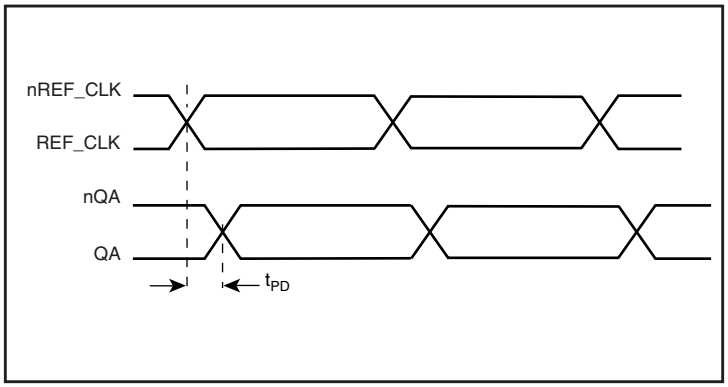
Parameter Measurement Information, continued



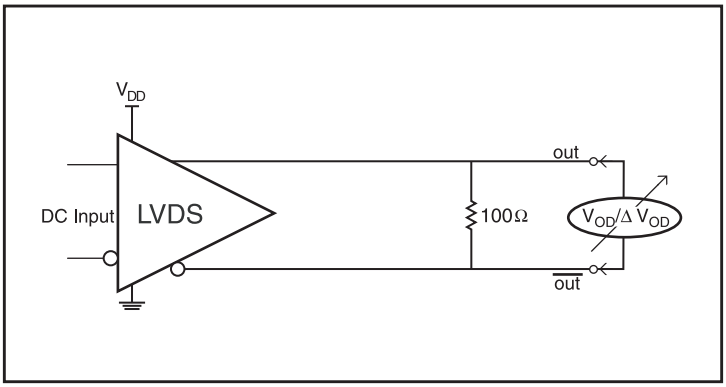
Output Rise and Fall Time



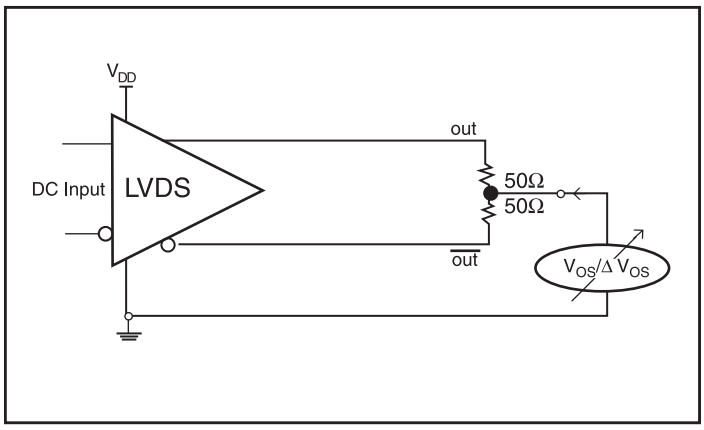
Output Duty Cycle/Pulse Width/Period



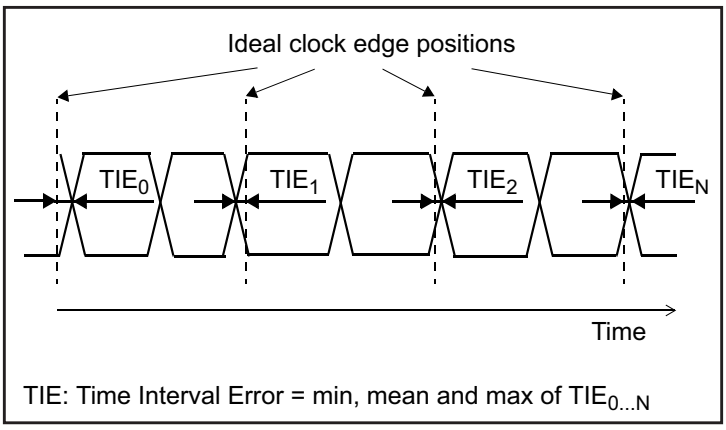
Propagation Delay



Differential Output Voltage Setup Propagation Delay



Offset Voltage Setup



Time Interval Error

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

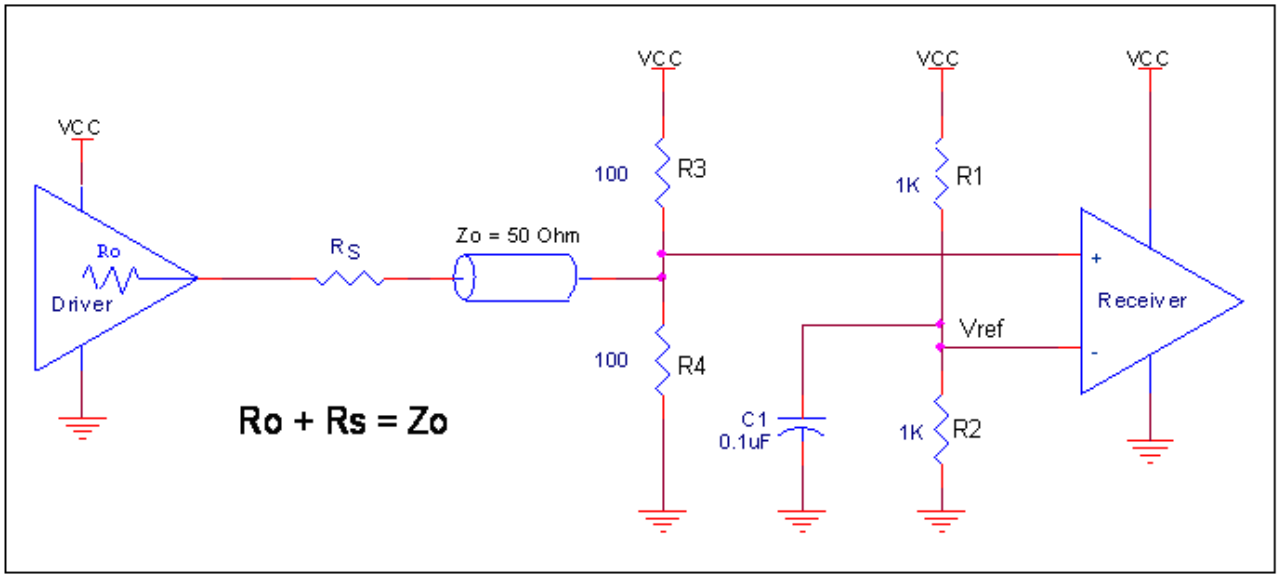


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Power Supply Voltage Sequence Information

No power sequence restrictions apply if V_{DD} and V_{DDA} are supplied by the same power plane and the recommended V_{DDA} filter is used (see Figure 6). V_{DDOL} may be applied at any time before or after V_{DD} and V_{DDA} are applied. If V_{DD} and V_{DDA} are not supplied by the same power plane, V_{DDA} must be powered on before or at the same time V_{DD} is applied. The V_{DDOL} supply voltage may be applied at any time.

3.3V LVPECL Clock Input Interface

The REF_CLK/nREF_CLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the REF_CLK/nREF_CLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

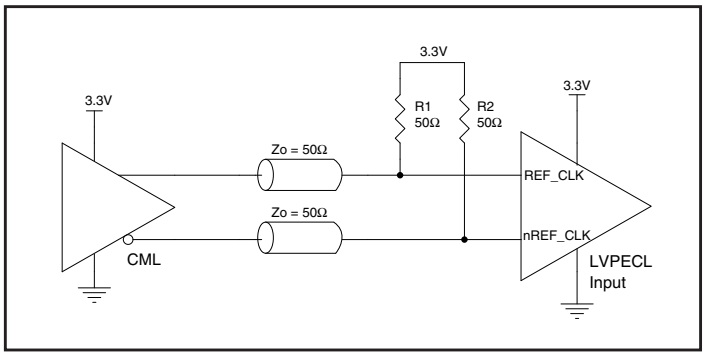


Figure 2A. REF_CLK/nREF_CLK Input Driven by an IDT Open Collector CML Driver

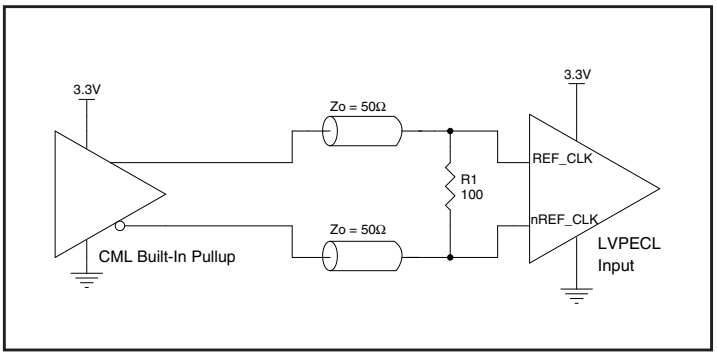


Figure 2B. REF_CLK/nREF_CLK Input Driven by a Built-In Pullup CML Driver

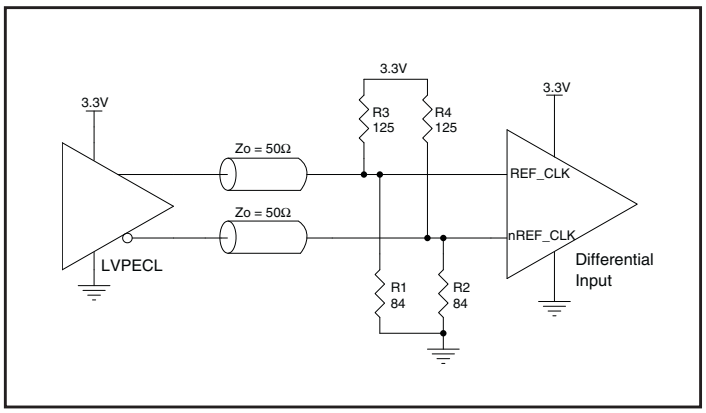


Figure 2C. REF_CLK/nREF_CLK Input Driven by a 3.3V LVPECL Driver

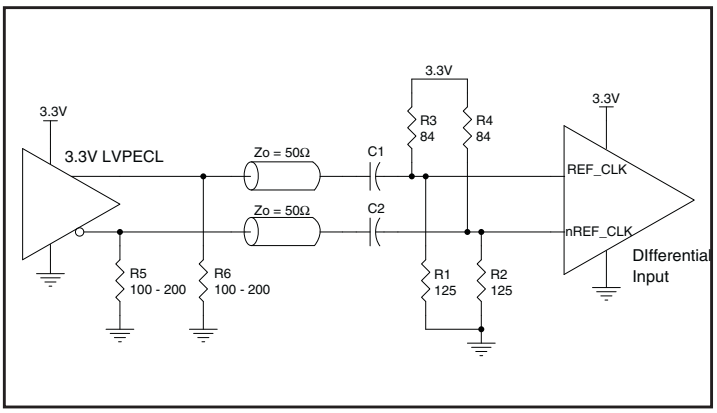


Figure 2D. REF_CLK/nREF_CLK Input Driven by a 3.3V LVPECL Driver with AC Couple

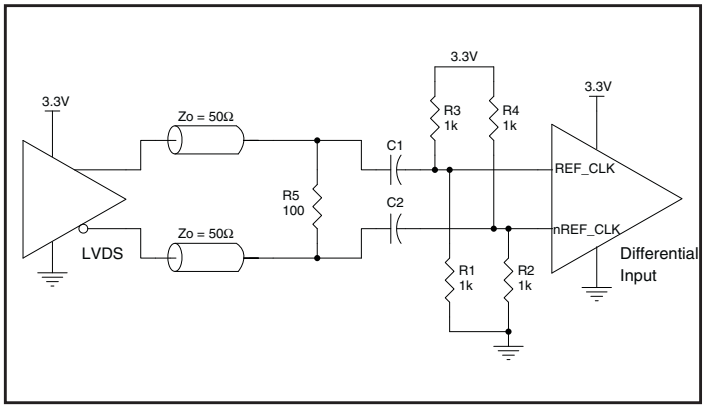


Figure 2E. REF_CLK/nREF_CLK Input Driven by a 3.3V LVDS Driver

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

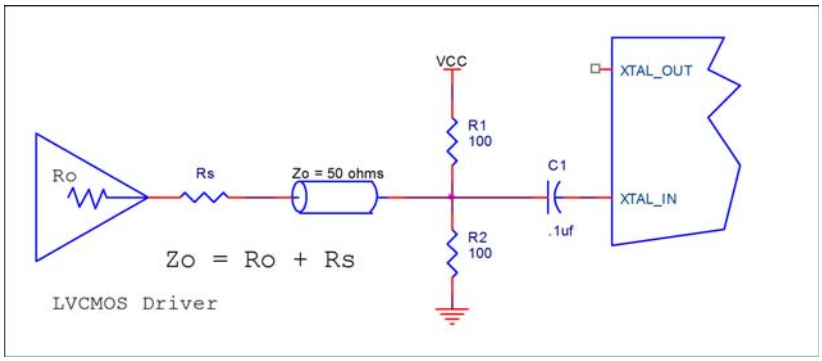


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

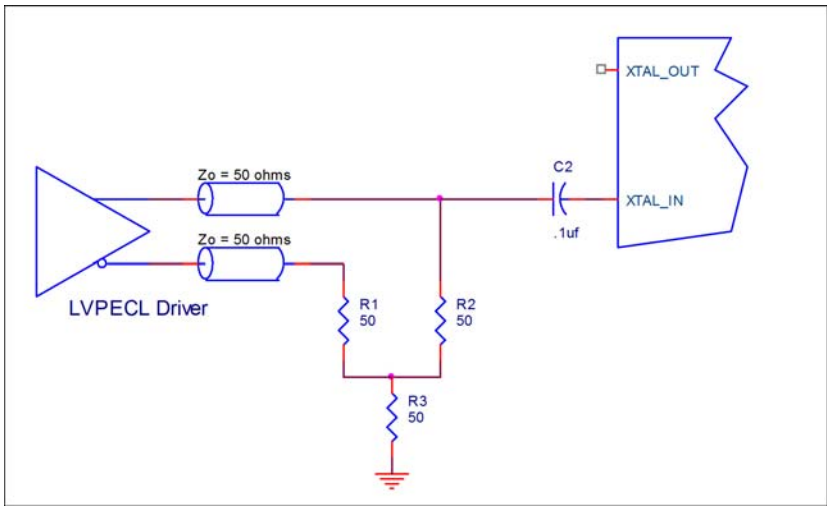


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

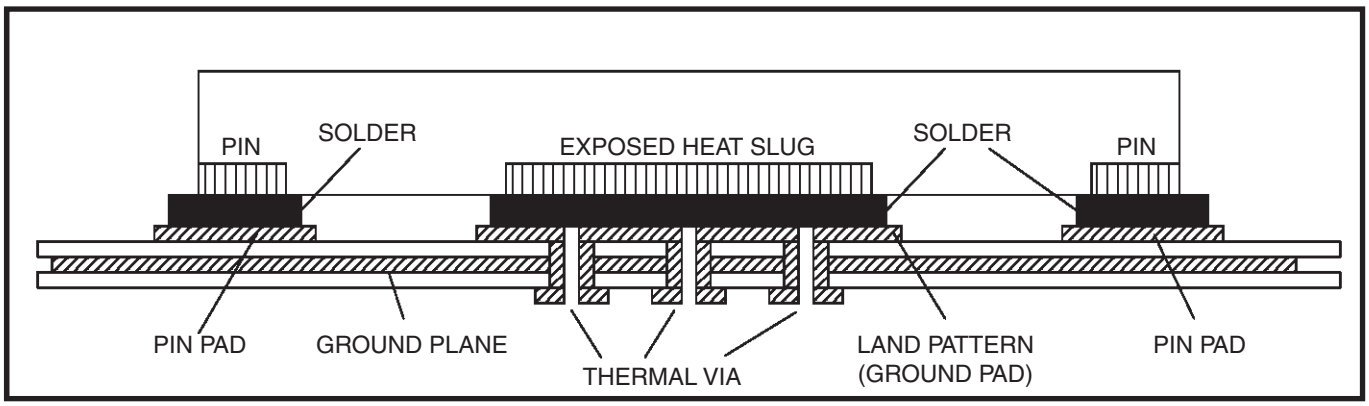


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 5A* can be used with either type of output structure. *Figure 5B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

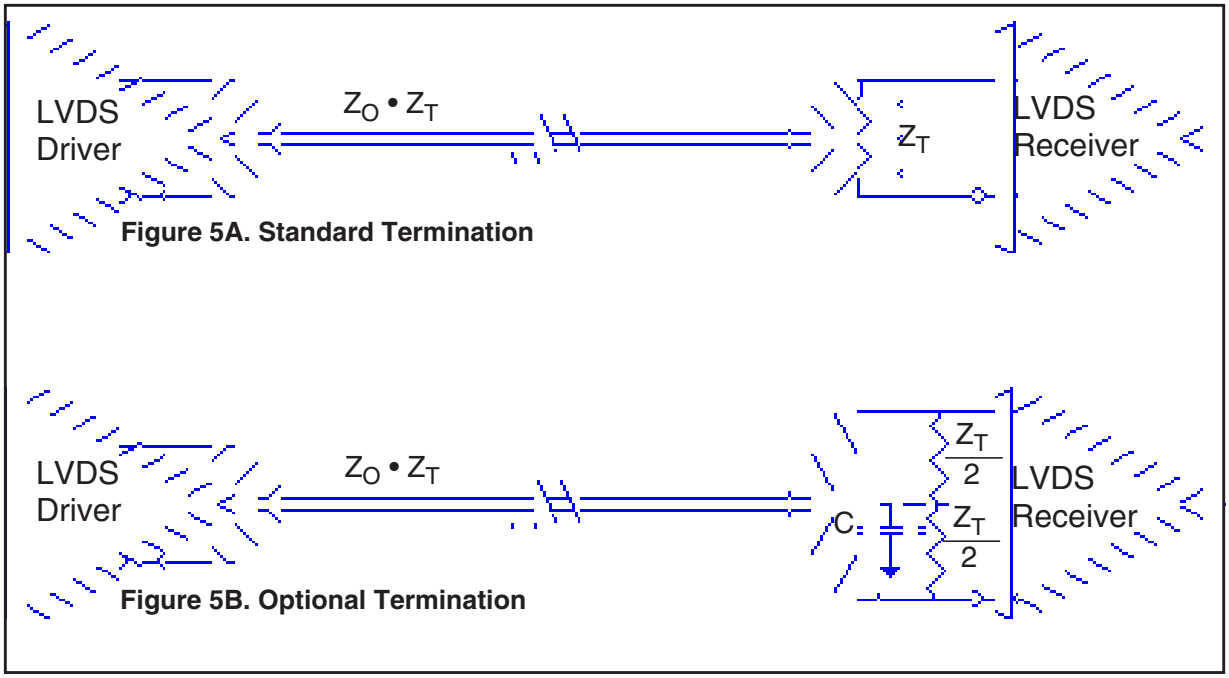


Figure 5A. Standard Termination

Figure 5B. Optional Termination

LVDS Termination

Recommendations for Unused Input and Output Pins

Inputs:

REF_CLK/nREF_CLK Inputs

For applications not requiring the use of the differential input, both REF_CLK and nREF_CLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from REF_CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVCMOS Output

The unused LVCMOS output can be left floating. There should be no trace attached.

Schematic Example

Figure 6 shows an example of an 814S208 application schematic. In this example, the device is operated at a V_{DD} = V_{DDOL} = 3.3V. The 12pF parallel resonant 30.72MHz crystal is used. The load capacitance values C1 = 6.8pF and C2 = 6.8pF are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 814S208 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

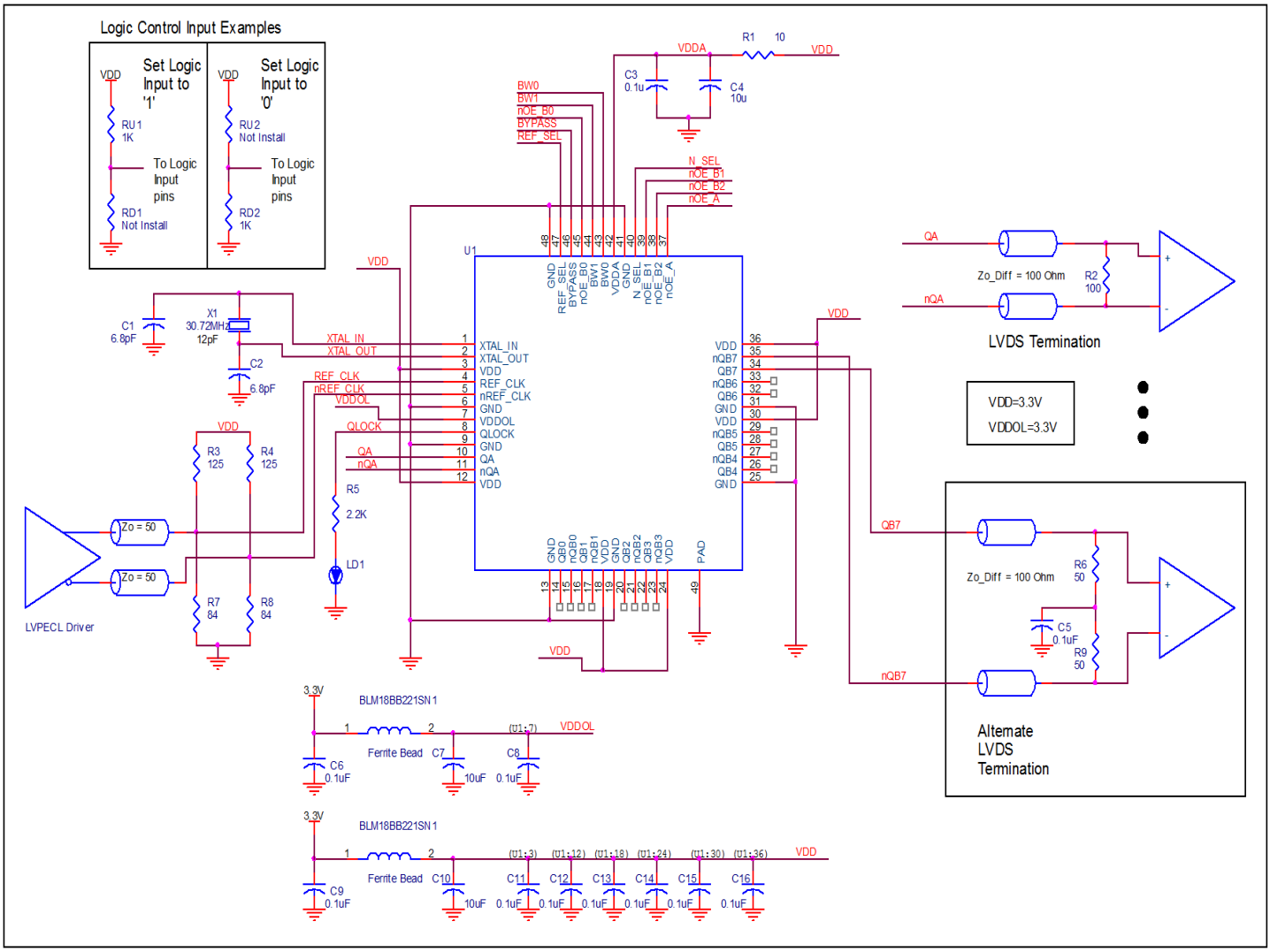


Figure 6. 814S208 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 814S208.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 814S208 is the sum of the core power plus the analog power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The maximum current at 85°C is as follows:
I_{DD_MAX} = 332mA
I_{DDA_MAX} = 20mA

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (332mA + 20mA) =$ **1219.68mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 30.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.220W * 30.5°C/W = 122.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 48 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	30.5°C/W	26.7°C/W	23.9°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 48-lead VFQFN

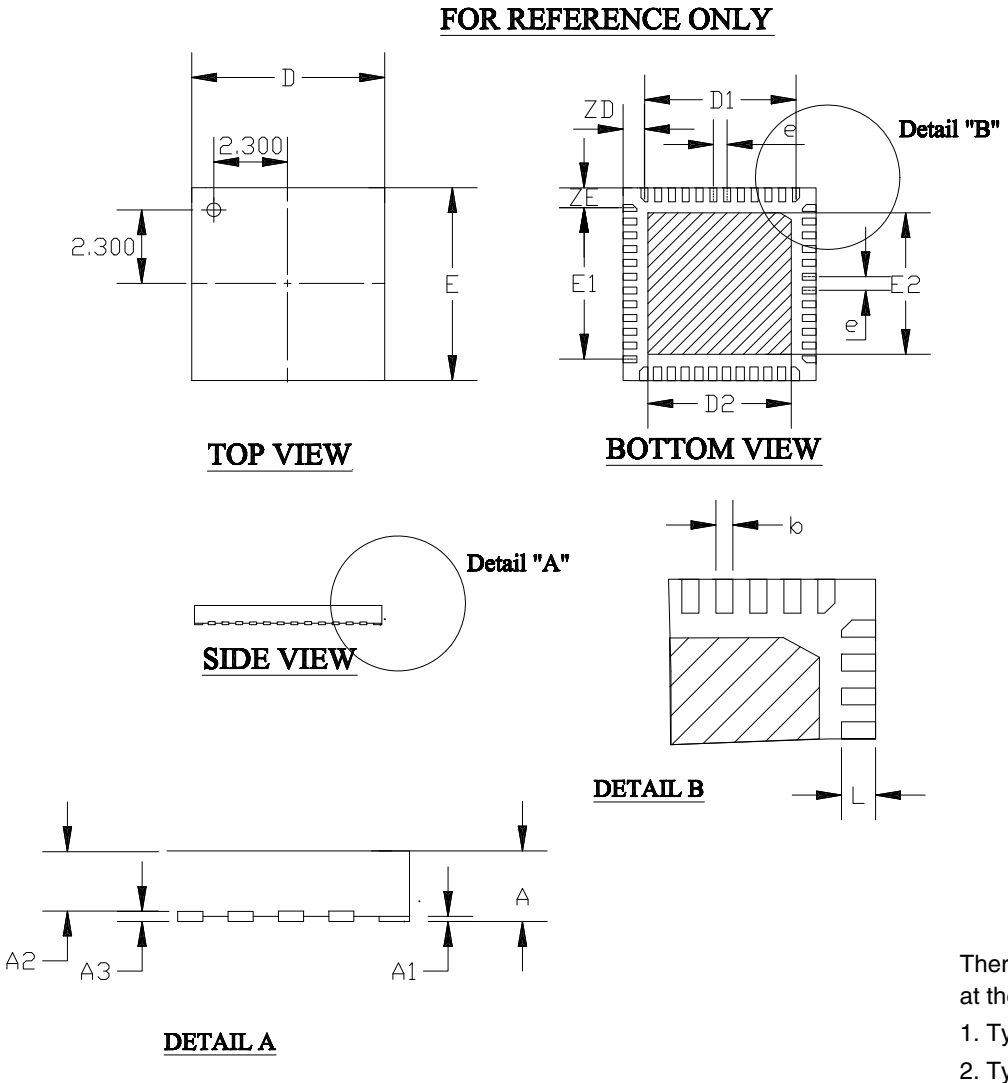
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	30.5°C/W	26.7°C/W	23.9°C/W

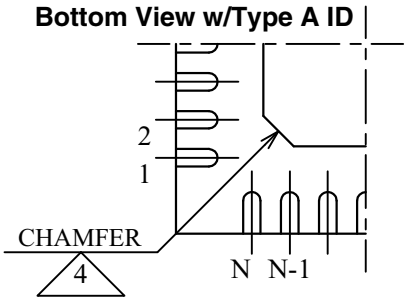
Transistor Count

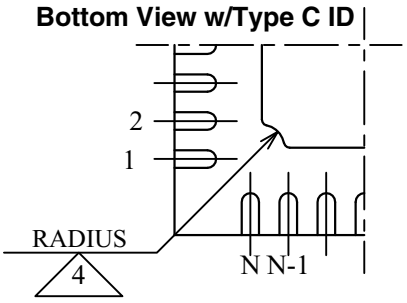
The transistor count for 814S208 is: 9,137

Package Outline and Package Dimensions

Package Outputline -K Suffix for 48 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. PackageDimensions for 48 Lead VFQFN

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A		0.8	0.9
A1	0	0.02	0.05
A3		0.2 Ref.	
b	0.18	0.25	0.30
D & E		7.00 Basic	
D1 & E1		5.50 Basic	
D2 & E2	5.50	5.65	5.80
e		0.50 Basic	
R		0.20~0.25	
ZD & ZE		0.75 Basic	
L	0.35	0.40	0.45

Reference Document: IDT Drawing #PSC-4203

Ordering Information

Table 10. Ordering Information Table

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
814S208BKILF	ICS814S208BIL	Lead-Free, 48-lead VFQFN	Tray	-40°C to 85°C
814S208BKILFT	ICS814S208BIL	Lead-Free, 48-lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T6	8 16	AC Characteristics Table - added Period JItter spec for QBx, nQBx outputs at 122.88MHz. Updated LVDS Termination application note.	10/13/11
C	T10	21	Ordering Information Table - deleted ‘Tape & Reel” count and table note. Deleted “ICS” prefix from part number. Updated datasheet header/footer.	4/7/16

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
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