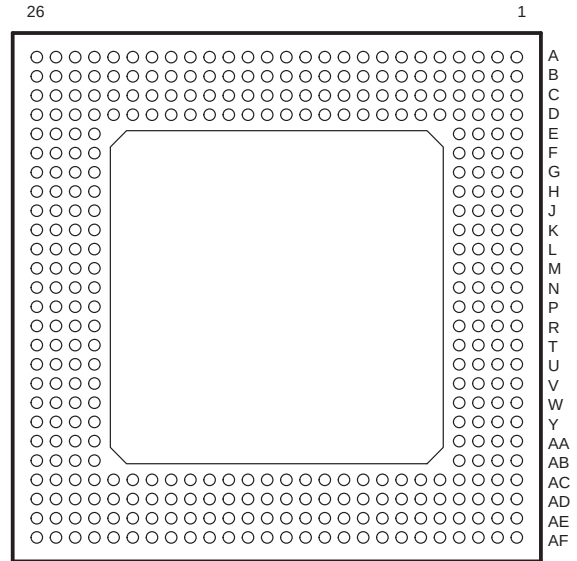


- **Highest Performance Floating-Point Digital Signal Processor (DSP) TMS320C6701**
  - 8.3-, 6.7-, 6-ns Instruction Cycle Time
  - 120-, 150-, 167-MHz Clock Rate
  - Eight 32-Bit Instructions/Cycle
  - 1 GFLOPS
  - TMS320C6201 Fixed-Point DSP Pin-Compatible
- **VelociTI™ Advanced Very Long Instruction Word (VLIW) C67x CPU Core**
  - Eight Highly Independent Functional Units:
    - Four ALUs (Floating- and Fixed-Point)
    - Two ALUs (Fixed-Point)
    - Two Multipliers (Floating- and Fixed-Point)
  - Load-Store Architecture With 32 32-Bit General-Purpose Registers
  - Instruction Packing Reduces Code Size
  - All Instructions Conditional
- **Instruction Set Features**
  - Hardware Support for IEEE Single-Precision Instructions
  - Hardware Support for IEEE Double-Precision Instructions
  - Byte-Addressable (8-, 16-, 32-Bit Data)
  - 8-Bit Overflow Protection
  - Saturation
  - Bit-Field Extract, Set, Clear
  - Bit-Counting
  - Normalization
- **1M-Bit On-Chip SRAM**
  - 512K-Bit Internal Program/Cache (16K 32-Bit Instructions)
  - 512K-Bit Dual-Access Internal Data (64K Bytes)
- **32-Bit External Memory Interface (EMIF)**
  - Glueless Interface to Synchronous Memories: SDRAM and SBSRAM
  - Glueless Interface to Asynchronous Memories: SRAM and EPROM
  - 52M-Byte Addressable External Memory Space
- **Four-Channel Bootloading Direct-Memory-Access (DMA) Controller With an Auxiliary Channel**

**GJC (352-PIN BGA) PACKAGE  
(BOTTOM VIEW)**



- **16-Bit Host-Port Interface (HPI)**
  - Access to Entire Memory Map
- **Two Multichannel Buffered Serial Ports (McBSPs)**
  - Direct Interface to T1/E1, MVIP, SCSA Framers
  - ST-Bus-Switching Compatible
  - Up to 256 Channels Each
  - AC97-Compatible
  - Serial-Peripheral-Interface (SPI) Compatible (Motorola™)
- **Two 32-Bit General-Purpose Timers**
- **Flexible Phase-Locked-Loop (PLL) Clock Generator**
- **IEEE-1149.1 (JTAG†) Boundary-Scan-Compatible**
- **352-Pin Ball Grid Array (BGA) Package (GJC Suffix)**
- **0.18-μm/5-Level Metal Process**
  - CMOS Technology
- **3.3-V I/Os, 1.8-V Internal (120-, 150-MHz)**
- **3.3-V I/Os, 1.9-V Internal (167-MHz Only)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

VelociTI is a trademark of Texas Instruments.

Motorola is a trademark of Motorola, Inc.

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Copyright © 2004, Texas Instruments Incorporated

TMS320C6701  
FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

| Table of Contents                                                                                             |    |
|---------------------------------------------------------------------------------------------------------------|----|
| GJC BGA package (bottom view) . . . . .                                                                       | 1  |
| description . . . . .                                                                                         | 2  |
| device characteristics . . . . .                                                                              | 3  |
| functional block and CPU diagram . . . . .                                                                    | 4  |
| CPU description . . . . .                                                                                     | 5  |
| signal groups description . . . . .                                                                           | 7  |
| signal descriptions . . . . .                                                                                 | 9  |
| development support . . . . .                                                                                 | 20 |
| documentation support . . . . .                                                                               | 23 |
| clock PLL . . . . .                                                                                           | 24 |
| power-down logic mode . . . . .                                                                               | 26 |
| absolute maximum ratings over operating case temperature range . . . . .                                      | 29 |
| recommended operating conditions . . . . .                                                                    | 29 |
| electrical characteristics over recommended ranges of supply voltage and operating case temperature . . . . . | 30 |
| parameter measurement information . . . . .                                                                   | 31 |
| signal-transition levels . . . . .                                                                            | 31 |
| input and output clocks . . . . .                                                                             | 32 |
| asynchronous memory timing . . . . .                                                                          | 35 |
| synchronous-burst memory timing . . . . .                                                                     | 37 |
| synchronous DRAM timing . . . . .                                                                             | 41 |
| HOLD/HOLDA timing . . . . .                                                                                   | 45 |
| reset timing . . . . .                                                                                        | 46 |
| external interrupt timing . . . . .                                                                           | 48 |
| host-port interface timing . . . . .                                                                          | 49 |
| multichannel buffered serial port timing . . . . .                                                            | 52 |
| DMAC, timer, power-down timing . . . . .                                                                      | 63 |
| JTAG test-port timing . . . . .                                                                               | 65 |
| mechanical data . . . . .                                                                                     | 66 |
| revision history . . . . .                                                                                    | 67 |

description

The TMS320C67x DSPs are the floating-point DSP family in the TMS320C6000™ DSP platform. The TMS320C6701 (C6701) device is based on the high-performance, advanced VelociTI very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making this DSP an excellent choice for multichannel and multifunction applications. With performance of up to 1 giga floating-point operations per second (GFLOPS) at a clock rate of 167 MHz, the C6701 offers cost-effective solutions to high-performance DSP programming challenges. The C6701 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. This processor has 32 general-purpose registers of 32-bit word length and eight highly independent functional units. The eight functional units provide four floating-/fixed-point ALUs, two fixed-point ALUs, and two floating-/fixed-point multipliers. The C6701 can produce two multiply-accumulates (MACs) per cycle for a total of 334 million MACs per second (MMACS). The C6701 DSP also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals.

The C6701 includes a large bank of on-chip memory and has a powerful and diverse set of peripherals. Program memory consists of a 64K-byte block that is user-configurable as cache or memory-mapped program space. Data memory consists of two 32K-byte blocks of RAM. The peripheral set includes two multichannel buffered serial ports (McBSPs), two general-purpose timers, a host-port interface (HPI), and a glueless external memory interface (EMIF) capable of interfacing to SDRAM or SBSRAM and asynchronous peripherals.

The C6701 has a complete set of development tools which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.

TMS320C6000 is a trademark of Texas Instruments.  
Windows is a registered trademark of Microsoft Corporation.

## device characteristics

Table 1 provides an overview of the C6701 DSP. The table shows significant features of each device, including the capacity of on-chip RAM, the peripherals, the execution time, and the package type with pin count, etc.

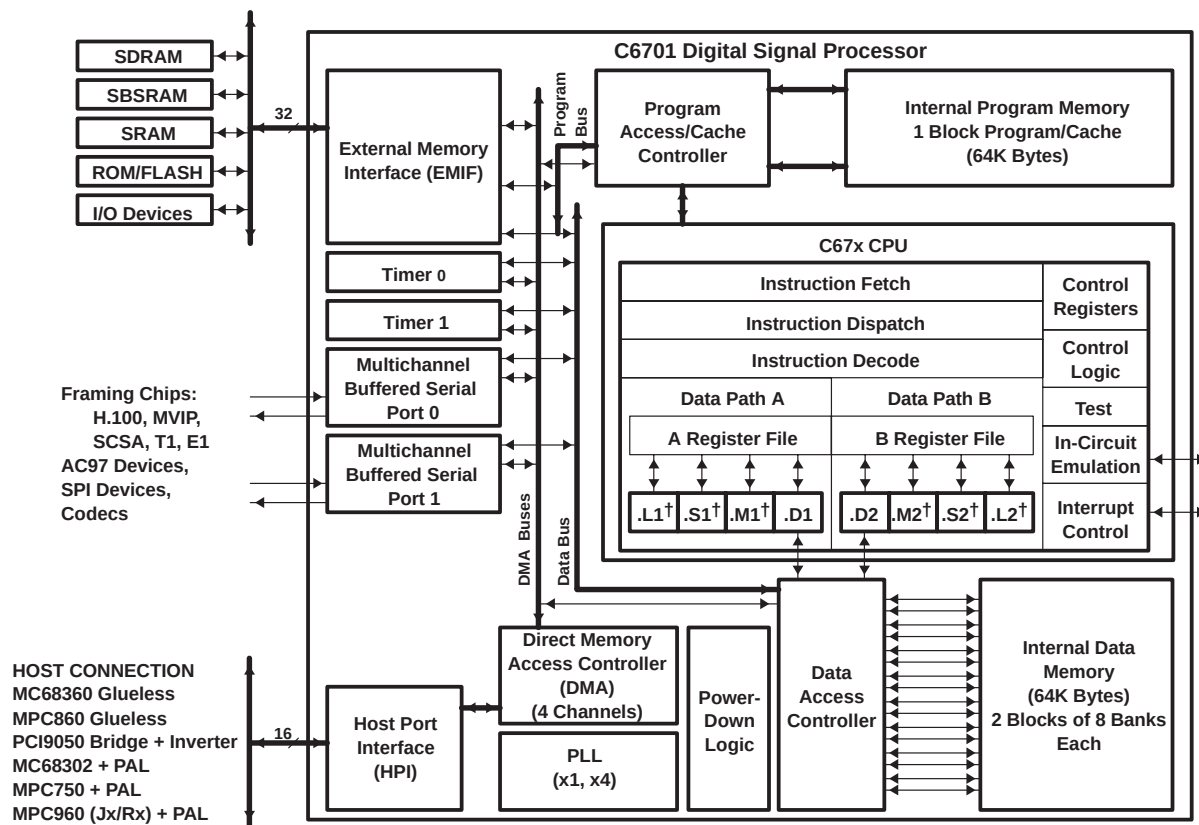
**Table 1. Characteristics of the C6701 Processors**

| HARDWARE FEATURES       |                                                                          | C6701                                                 |
|-------------------------|--------------------------------------------------------------------------|-------------------------------------------------------|
| Peripherals             | EMIF                                                                     | 1                                                     |
|                         | DMA                                                                      | 4-Channel                                             |
|                         | Host-Port Interface (HPI)                                                | 1                                                     |
|                         | McBSPs                                                                   | 2                                                     |
|                         | 32-Bit Timers                                                            | 2                                                     |
| Internal Program Memory | Size (Bytes)                                                             | 64K                                                   |
|                         | Organization                                                             | 64K Bytes Cache/Mapped Program                        |
| Internal Data Memory    | Size (Bytes)                                                             | 64K                                                   |
|                         | Organization                                                             | 2 Blocks: Eight 16-Bit Banks per Block 50/50 Split    |
| Frequency               | MHz                                                                      | 120, 150, 167                                         |
| Cycle Time              | ns                                                                       | 6 ns (6701-167); 6.7 ns (6701-150); 8.3 ns (6701-120) |
| Voltage                 | Core (V)                                                                 | 1.8 (6701-120, -150)                                  |
|                         |                                                                          | 1.9 (6701-167 only)                                   |
|                         | I/O (V)                                                                  | 3.3                                                   |
| PLL Options             | CLKIN frequency multiplier                                               | Bypass (x1), x4                                       |
| BGA Package             | 35 × 35 mm                                                               | 352-pin GJC                                           |
| Process Technology      | μm                                                                       | 0.18 μm                                               |
| Product Status          | Product Preview (PP)<br>Advance Information (AI)<br>Production Data (PD) | PD                                                    |

# TMS320C6701 FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## functional block and CPU diagram



† These functional units execute floating-point instructions.

## CPU description

The CPU fetches VelociTI advanced very-long instruction words (VLIW) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VelociTI VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet. Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C67x CPU from other VLIW architectures.

The CPU features two sets of functional units. Each set contains four units and a register file. One set contains functional units .L1, .S1, .M1, and .D1; the other set contains units .D2, .M2, .S2, and .L2. The two register files contain 16 32-bit registers each for the total of 32 general-purpose registers. The two sets of functional units, along with two register files, compose sides A and B of the CPU (see the Functional and CPU Block diagram and Figure 1). The four functional units on each side of the CPU can freely share the 16 registers belonging to that side. Additionally, each side features a single data bus connected to all registers on the other side, by which the two sets of functional units can access data from the register files on opposite sides. While register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle, register access using the register file across the CPU supports one read and one write per cycle.

The C67x CPU executes all TMS320C62x™ DSP fixed-point instructions. In addition to the C62x DSP fixed-point instructions, the six out of eight functional units (.L1, .M1, .D1, .D2, .M2, and .L2) also execute floating-point instructions. The remaining two functional units (.S1 and .S2) also execute the new LDDW instruction which loads 64 bits per CPU side for a total of 128 bits per cycle.

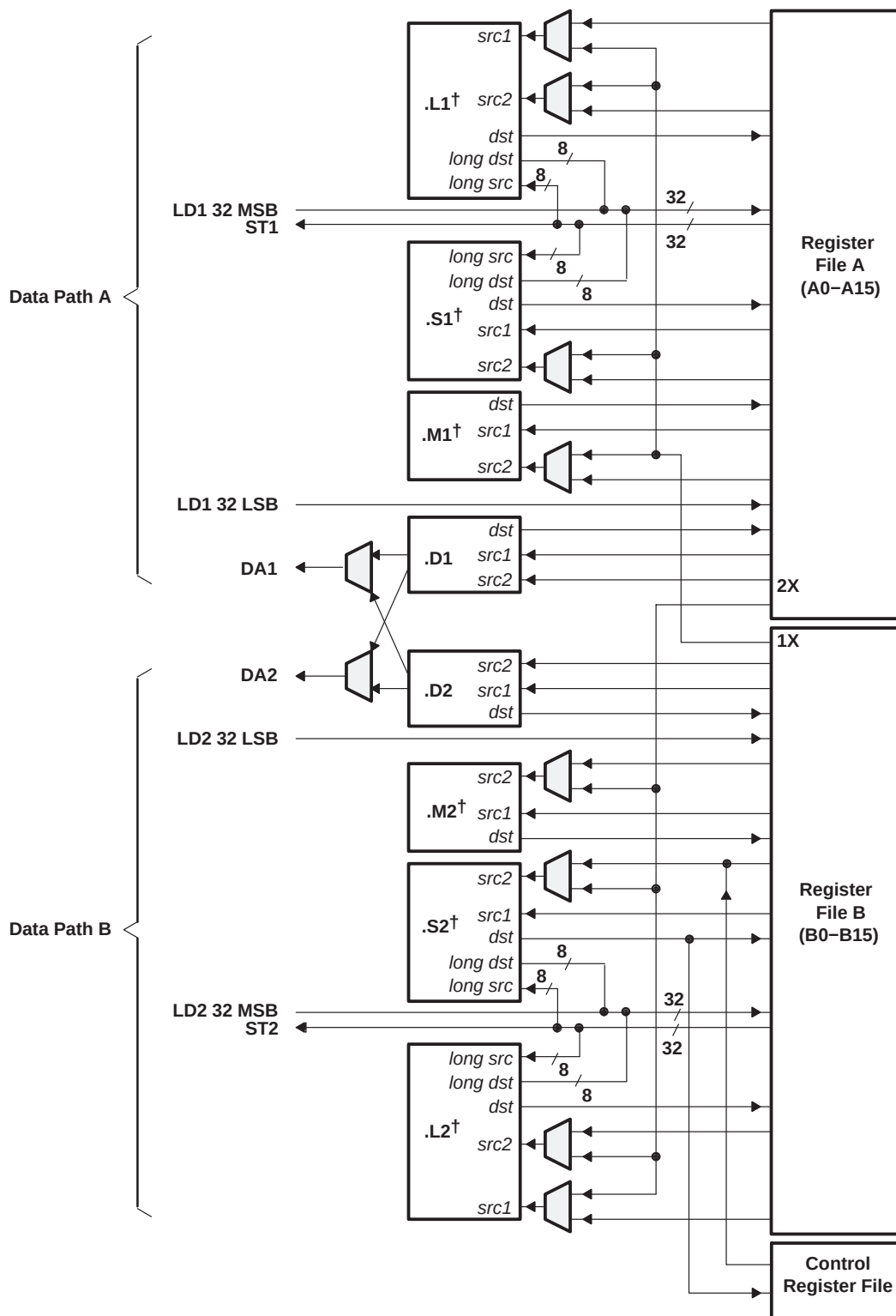
Another key feature of the C67x CPU is the load/store architecture, where all instructions operate on registers (as opposed to data in memory). Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file. The C67x CPU supports a variety of indirect-addressing modes using either linear- or circular-addressing modes with 5- or 15-bit offsets. All instructions are conditional, and most can access any one of the 32 registers. Some registers, however, are singled out to support specific addressing or to hold the condition for conditional instructions (if the condition is not automatically “true”). The two .M functional units are dedicated for multiplies. The two .S and .L functional units perform a general set of arithmetic, logical, and branch functions with results available every clock cycle.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are “linked” together by “1” bits in the least significant bit (LSB) position of the instructions. The instructions that are “chained” together for simultaneous execution (up to eight in total) compose an execute packet. A “0” in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. If an execute packet crosses the fetch-packet boundary (256 bits wide), the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory as bytes or half-words as well. All load and store instructions are byte-, half-word, or word-addressable.

# TMS320C6701 FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## CPU description (continued)



† These functional units execute floating-point instructions.

Figure 1. TMS320C67x CPU Data Paths

## signal groups description

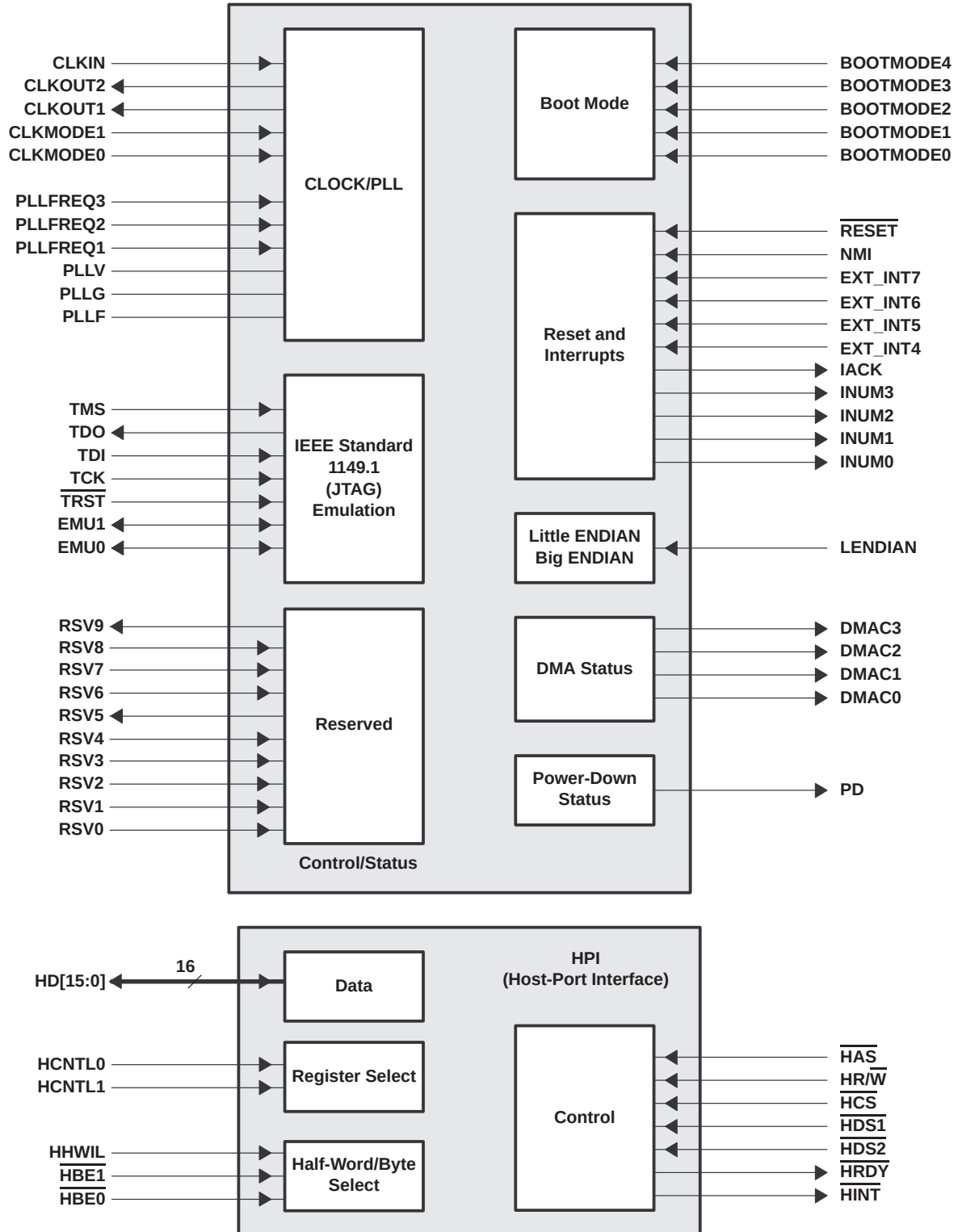


Figure 2. CPU and Peripheral Signals

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### signal groups description (continued)

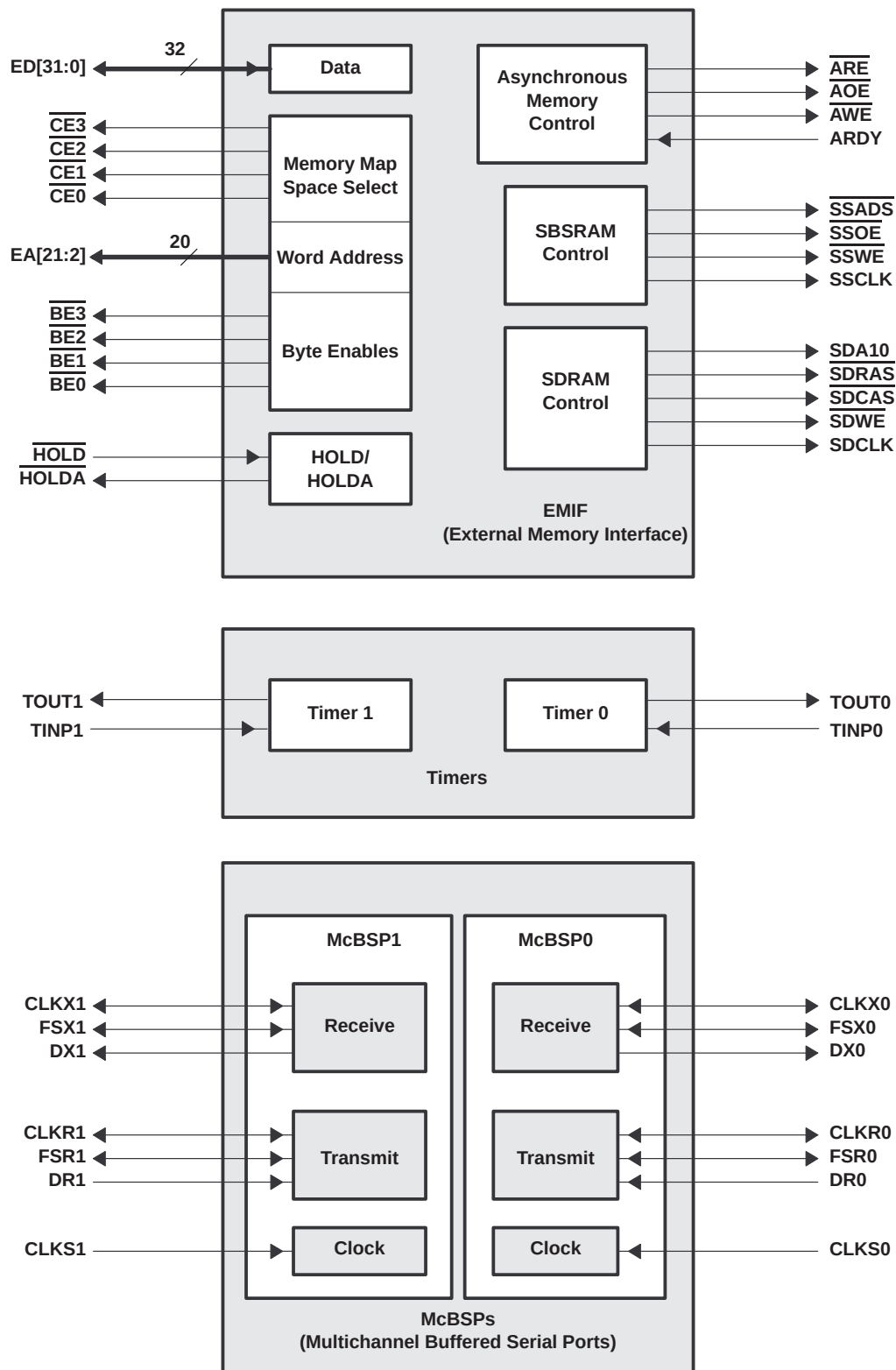


Figure 3. Peripheral Signals



### Signal Descriptions

| SIGNAL<br>NAME        | NO.  | TYPE†          | DESCRIPTION                                                                                                                                                                                                                       |
|-----------------------|------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>CLOCK/PLL</b>      |      |                |                                                                                                                                                                                                                                   |
| CLKIN                 | C10  | I              | Clock Input                                                                                                                                                                                                                       |
| CLKOUT1               | AF22 | O              | Clock output at full device speed                                                                                                                                                                                                 |
| CLKOUT2               | AF20 | O              | Clock output at half of device speed                                                                                                                                                                                              |
| CLKMODE1              | C6   | I              | Clock mode select                                                                                                                                                                                                                 |
| CLKMODE0              | C5   |                | <input type="checkbox"/> Selects whether the output clock frequency = input clock frequency x4 or x1                                                                                                                              |
| PLLREQ3               | A9   | I              | PLL frequency range (3, 2, and 1)<br><input type="checkbox"/> The target range for CLKOUT1 frequency is determined by the 3-bit value of the PLLREQ pins.                                                                         |
| PLLREQ2               | D11  |                |                                                                                                                                                                                                                                   |
| PLLREQ1               | B10  |                |                                                                                                                                                                                                                                   |
| PLL <sup>‡</sup>      | D12  | A <sup>§</sup> | PLL analog V <sub>CC</sub> connection for the low-pass filter                                                                                                                                                                     |
| PLL <sup>‡</sup>      | C12  | A <sup>§</sup> | PLL analog GND connection for the low-pass filter                                                                                                                                                                                 |
| PLLF                  | A11  | A <sup>§</sup> | PLL low-pass filter connection to external components and a bypass capacitor                                                                                                                                                      |
| <b>JTAG EMULATION</b> |      |                |                                                                                                                                                                                                                                   |
| TMS                   | L3   | I              | JTAG test-port mode select (features an internal pullup)                                                                                                                                                                          |
| TDO                   | W2   | O/Z            | JTAG test-port data out                                                                                                                                                                                                           |
| TDI                   | R4   | I              | JTAG test-port data in (features an internal pullup)                                                                                                                                                                              |
| TCK                   | R3   | I              | JTAG test-port clock                                                                                                                                                                                                              |
| TRST                  | T1   | I              | JTAG test-port reset (features an internal pulldown)                                                                                                                                                                              |
| EMU1                  | Y1   | I/O/Z          | Emulation pin 1, pullup with a dedicated 20-kΩ resistor¶                                                                                                                                                                          |
| EMU0                  | W3   | I/O/Z          | Emulation pin 0, pullup with a dedicated 20-kΩ resistor¶                                                                                                                                                                          |
| <b>CONTROL</b>        |      |                |                                                                                                                                                                                                                                   |
| RESET                 | K2   | I              | Device reset                                                                                                                                                                                                                      |
| NMI                   | L2   | I              | Nonmaskable interrupt<br><input type="checkbox"/> Edge-driven (rising edge)                                                                                                                                                       |
| EXT_INT7              | U3   | I              | External interrupts<br><input type="checkbox"/> Edge-driven (rising edge)                                                                                                                                                         |
| EXT_INT6              | V2   |                |                                                                                                                                                                                                                                   |
| EXT_INT5              | W1   |                |                                                                                                                                                                                                                                   |
| EXT_INT4              | U4   |                |                                                                                                                                                                                                                                   |
| IACK                  | Y2   | O              | Interrupt acknowledge for all active interrupts serviced by the CPU                                                                                                                                                               |
| INUM3                 | AA1  | O              | Active interrupt identification number<br><input type="checkbox"/> Valid during IACK for all active interrupts (not just external)<br><input type="checkbox"/> Encoding order follows the interrupt-service fetch-packet ordering |
| INUM2                 | W4   |                |                                                                                                                                                                                                                                   |
| INUM1                 | AA2  |                |                                                                                                                                                                                                                                   |
| INUM0                 | AB1  |                |                                                                                                                                                                                                                                   |
| LENDIAN               | H3   | I              | If high, LENDIAN selects little-endian byte/half-word addressing order within a word<br>If low, LENDIAN selects big-endian addressing                                                                                             |
| PD                    | D3   | O              | Power-down mode 3 (active if high)                                                                                                                                                                                                |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

‡ PLLV and PLLG are not part of external voltage supply or ground. See the CLOCK/PLL documentation for information on how to connect these pins.

§ A = Analog Signal (PLL Filter)

¶ For emulation and normal operation, pull up EMU1 and EMU0 with a dedicated 20-kΩ resistor. For boundary scan, pull down EMU1 and EMU0 with a dedicated 20-kΩ resistor.

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### Signal Descriptions (Continued)

| SIGNAL<br>NAME                   | NO. | TYPE† | DESCRIPTION                                                                           |
|----------------------------------|-----|-------|---------------------------------------------------------------------------------------|
| <b>HOST-PORT INTERFACE (HPI)</b> |     |       |                                                                                       |
| $\overline{\text{HINT}}$         | H26 | O     | Host interrupt (from DSP to host)                                                     |
| HCNTL1                           | F23 | I     | Host control – selects between control, address, or data registers                    |
| HCNTL0                           | D25 | I     | Host control – selects between control, address, or data registers                    |
| HHWIL                            | C26 | I     | Host half-word select – first or second half-word (not necessarily high or low order) |
| HBE1                             | E23 | I     | Host byte select within word or half-word                                             |
| HBE0                             | D24 | I     | Host byte select within word or half-word                                             |
| $\overline{\text{HR/W}}$         | C23 | I     | Host read or write select                                                             |
| HD15                             | B13 | I/O/Z | Host-port data (used for transfer of data, address, and control)                      |
| HD14                             | B14 |       |                                                                                       |
| HD13                             | C14 |       |                                                                                       |
| HD12                             | B15 |       |                                                                                       |
| HD11                             | D15 |       |                                                                                       |
| HD10                             | B16 |       |                                                                                       |
| HD9                              | A17 |       |                                                                                       |
| HD8                              | B17 |       |                                                                                       |
| HD7                              | D16 |       |                                                                                       |
| HD6                              | B18 |       |                                                                                       |
| HD5                              | A19 |       |                                                                                       |
| HD4                              | C18 |       |                                                                                       |
| HD3                              | B19 |       |                                                                                       |
| HD2                              | C19 |       |                                                                                       |
| HD1                              | B20 |       |                                                                                       |
| HD0                              | B21 |       |                                                                                       |
| $\overline{\text{HAS}}$          | C22 | I     | Host address strobe                                                                   |
| $\overline{\text{HCS}}$          | B23 | I     | Host chip select                                                                      |
| $\overline{\text{HDS1}}$         | D22 | I     | Host data strobe 1                                                                    |
| $\overline{\text{HDS2}}$         | A24 | I     | Host data strobe 2                                                                    |
| $\overline{\text{HRDY}}$         | J24 | O     | Host ready (from DSP to host)                                                         |
| <b>BOOT MODE</b>                 |     |       |                                                                                       |
| BOOTMODE4                        | D8  | I     | Boot mode                                                                             |
| BOOTMODE3                        | B4  |       |                                                                                       |
| BOOTMODE2                        | A3  |       |                                                                                       |
| BOOTMODE1                        | D5  |       |                                                                                       |
| BOOTMODE0                        | C4  |       |                                                                                       |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



**Signal Descriptions (Continued)**

| SIGNAL<br>NAME NO.                                   |      | TYPE† | DESCRIPTION                                                                                                                                                                                                                                                                       |
|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EMIF – CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY |      |       |                                                                                                                                                                                                                                                                                   |
| CE3                                                  | AE22 | O/Z   | Memory space enables<br><input type="checkbox"/> Enabled by bits 24 and 25 of the word address<br><input type="checkbox"/> Only one asserted during any external data access                                                                                                      |
| CE2                                                  | AD26 | O/Z   |                                                                                                                                                                                                                                                                                   |
| CE1                                                  | AB24 | O/Z   |                                                                                                                                                                                                                                                                                   |
| CE0                                                  | AC26 | O/Z   |                                                                                                                                                                                                                                                                                   |
| BE3                                                  | AB25 | O/Z   | Byte-enable control<br><input type="checkbox"/> Decoded from the two lowest bits of the internal address<br><input type="checkbox"/> Byte-write enables for most types of memory<br><input type="checkbox"/> Can be directly connected to SDRAM read and write mask signal (SDQM) |
| BE2                                                  | AA24 | O/Z   |                                                                                                                                                                                                                                                                                   |
| BE1                                                  | Y23  | O/Z   |                                                                                                                                                                                                                                                                                   |
| BE0                                                  | AA26 | O/Z   |                                                                                                                                                                                                                                                                                   |
| EMIF – ADDRESS                                       |      |       |                                                                                                                                                                                                                                                                                   |
| EA21                                                 | J26  | O/Z   | External address (word address)                                                                                                                                                                                                                                                   |
| EA20                                                 | K25  |       |                                                                                                                                                                                                                                                                                   |
| EA19                                                 | L24  |       |                                                                                                                                                                                                                                                                                   |
| EA18                                                 | K26  |       |                                                                                                                                                                                                                                                                                   |
| EA17                                                 | M26  |       |                                                                                                                                                                                                                                                                                   |
| EA16                                                 | M25  |       |                                                                                                                                                                                                                                                                                   |
| EA15                                                 | P25  |       |                                                                                                                                                                                                                                                                                   |
| EA14                                                 | P24  |       |                                                                                                                                                                                                                                                                                   |
| EA13                                                 | R25  |       |                                                                                                                                                                                                                                                                                   |
| EA12                                                 | T26  |       |                                                                                                                                                                                                                                                                                   |
| EA11                                                 | R23  |       |                                                                                                                                                                                                                                                                                   |
| EA10                                                 | U26  |       |                                                                                                                                                                                                                                                                                   |
| EA9                                                  | U25  |       |                                                                                                                                                                                                                                                                                   |
| EA8                                                  | T23  |       |                                                                                                                                                                                                                                                                                   |
| EA7                                                  | V26  |       |                                                                                                                                                                                                                                                                                   |
| EA6                                                  | V25  |       |                                                                                                                                                                                                                                                                                   |
| EA5                                                  | W26  |       |                                                                                                                                                                                                                                                                                   |
| EA4                                                  | V24  |       |                                                                                                                                                                                                                                                                                   |
| EA3                                                  | W25  |       |                                                                                                                                                                                                                                                                                   |
| EA2                                                  | Y26  |       |                                                                                                                                                                                                                                                                                   |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### Signal Descriptions (Continued)

| SIGNAL<br>NAME NO.                 |      | TYPE† | DESCRIPTION                       |
|------------------------------------|------|-------|-----------------------------------|
| EMIF – DATA                        |      |       |                                   |
| ED31                               | AB2  | I/O/Z | External data                     |
| ED30                               | AC1  |       |                                   |
| ED29                               | AA4  |       |                                   |
| ED28                               | AD1  |       |                                   |
| ED27                               | AC3  |       |                                   |
| ED26                               | AD4  |       |                                   |
| ED25                               | AF3  |       |                                   |
| ED24                               | AE4  |       |                                   |
| ED23                               | AD5  |       |                                   |
| ED22                               | AF4  |       |                                   |
| ED21                               | AE5  |       |                                   |
| ED20                               | AD6  |       |                                   |
| ED19                               | AE6  |       |                                   |
| ED18                               | AD7  |       |                                   |
| ED17                               | AC8  |       |                                   |
| ED16                               | AF7  |       |                                   |
| ED15                               | AD9  |       |                                   |
| ED14                               | AD10 |       |                                   |
| ED13                               | AF9  |       |                                   |
| ED12                               | AC11 |       |                                   |
| ED11                               | AE10 |       |                                   |
| ED10                               | AE11 |       |                                   |
| ED9                                | AF11 |       |                                   |
| ED8                                | AE14 |       |                                   |
| ED7                                | AF15 |       |                                   |
| ED6                                | AE15 |       |                                   |
| ED5                                | AF16 |       |                                   |
| ED4                                | AC15 |       |                                   |
| ED3                                | AE17 |       |                                   |
| ED2                                | AF18 |       |                                   |
| ED1                                | AF19 |       |                                   |
| ED0                                | AC17 |       |                                   |
| EMIF – ASYNCHRONOUS MEMORY CONTROL |      |       |                                   |
| $\overline{\text{ARE}}$            | Y24  | O/Z   | Asynchronous memory read enable   |
| $\overline{\text{AOE}}$            | AC24 | O/Z   | Asynchronous memory output enable |
| $\overline{\text{AWE}}$            | AD23 | O/Z   | Asynchronous memory write enable  |
| ARDY                               | W23  | I     | Asynchronous memory ready input   |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



**Signal Descriptions (Continued)**

| SIGNAL<br>NAME NO.                           |      | TYPE† | DESCRIPTION                                        |
|----------------------------------------------|------|-------|----------------------------------------------------|
| EMIF – SYNCHRONOUS BURST SRAM CONTROL        |      |       |                                                    |
| SSADS                                        | AC20 | O/Z   | SBSRAM address strobe                              |
| SSOE                                         | AF21 | O/Z   | SBSRAM output enable                               |
| SSWE                                         | AD19 | O/Z   | SBSRAM write enable                                |
| SSCLK                                        | AD17 | O     | SBSRAM clock                                       |
| EMIF – SYNCHRONOUS DRAM CONTROL              |      |       |                                                    |
| SDA10                                        | AD21 | O/Z   | SDRAM address 10 (separate for deactivate command) |
| SDRAS                                        | AF24 | O/Z   | SDRAM row-address strobe                           |
| SDCAS                                        | AD22 | O/Z   | SDRAM column-address strobe                        |
| SDWE                                         | AF23 | O/Z   | SDRAM write enable                                 |
| SDCLK                                        | AE20 | O     | SDRAM clock                                        |
| EMIF – BUS ARBITRATION                       |      |       |                                                    |
| HOLD                                         | AA25 | I     | Hold request from the host                         |
| HOLDA                                        | A7   | O     | Hold-request-acknowledge to the host               |
| TIMERS                                       |      |       |                                                    |
| TOUT1                                        | H24  | O     | Timer 1 or general-purpose output                  |
| TINP1                                        | K24  | I     | Timer 1 or general-purpose input                   |
| TOUT0                                        | M4   | O     | Timer 0 or general-purpose output                  |
| TINP0                                        | K4   | I     | Timer 0 or general-purpose input                   |
| DMA ACTION COMPLETE                          |      |       |                                                    |
| DMAC3                                        | D2   | O     | DMA action complete                                |
| DMAC2                                        | F4   |       |                                                    |
| DMAC1                                        | D1   |       |                                                    |
| DMAC0                                        | E2   |       |                                                    |
| MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1) |      |       |                                                    |
| CLKS1                                        | E25  | I     | External clock source (as opposed to internal)     |
| CLKR1                                        | H23  | I/O/Z | Receive clock                                      |
| CLKX1                                        | F26  | I/O/Z | Transmit clock                                     |
| DR1                                          | D26  | I     | Receive data                                       |
| DX1                                          | G23  | O/Z   | Transmit data                                      |
| FSR1                                         | E26  | I/O/Z | Receive frame sync                                 |
| FSX1                                         | F25  | I/O/Z | Transmit frame sync                                |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### Signal Descriptions (Continued)

| SIGNAL<br>NAME                                      | NO. | TYPE† | DESCRIPTION                                                            |
|-----------------------------------------------------|-----|-------|------------------------------------------------------------------------|
| <b>MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP0)</b> |     |       |                                                                        |
| CLKS0                                               | L4  | I     | External clock source (as opposed to internal)                         |
| CLKR0                                               | M2  | I/O/Z | Receive clock                                                          |
| CLKX0                                               | L1  | I/O/Z | Transmit clock                                                         |
| DR0                                                 | J1  | I     | Receive data                                                           |
| DX0                                                 | R1  | O/Z   | Transmit data                                                          |
| FSR0                                                | P4  | I/O/Z | Receive frame sync                                                     |
| FSX0                                                | P3  | I/O/Z | Transmit frame sync                                                    |
| <b>RESERVED FOR TEST</b>                            |     |       |                                                                        |
| RSV0                                                | T2  | I     | Reserved for testing, pullup with a dedicated 20-kΩ resistor           |
| RSV1                                                | G2  | I     | Reserved for testing, pullup with a dedicated 20-kΩ resistor           |
| RSV2                                                | C11 | I     | Reserved for testing, pullup with a dedicated 20-kΩ resistor           |
| RSV3                                                | B9  | I     | Reserved for testing, pullup with a dedicated 20-kΩ resistor           |
| RSV4                                                | A6  | I     | Reserved for testing, <b>pulldown</b> with a dedicated 20-kΩ resistor  |
| RSV5                                                | C8  | O     | Reserved (leave unconnected, <b>do not</b> connect to power or ground) |
| RSV6                                                | C21 | I     | Reserved for testing, pullup with a dedicated 20-kΩ resistor           |
| RSV7                                                | B22 | I     | Reserved for testing, pullup with a dedicated 20-kΩ resistor           |
| RSV8                                                | A23 | I     | Reserved for testing, pullup with a dedicated 20-kΩ resistor           |
| RSV9                                                | E4  | O     | Reserved (leave unconnected, <b>do not</b> connect to power or ground) |
| <b>SUPPLY VOLTAGE PINS</b>                          |     |       |                                                                        |
| DVDD                                                | A10 | S     | 3.3-V supply voltage                                                   |
|                                                     | A15 |       |                                                                        |
|                                                     | A18 |       |                                                                        |
|                                                     | A21 |       |                                                                        |
|                                                     | A22 |       |                                                                        |
|                                                     | B7  |       |                                                                        |
|                                                     | C1  |       |                                                                        |
|                                                     | D17 |       |                                                                        |
|                                                     | F3  |       |                                                                        |
|                                                     | G24 |       |                                                                        |
|                                                     | G25 |       |                                                                        |
|                                                     | H25 |       |                                                                        |
|                                                     | J25 |       |                                                                        |
|                                                     | L25 |       |                                                                        |
|                                                     | M3  |       |                                                                        |
|                                                     | N3  |       |                                                                        |
|                                                     | N23 |       |                                                                        |
|                                                     | R26 |       |                                                                        |
|                                                     | T24 |       |                                                                        |
|                                                     | U24 |       |                                                                        |
|                                                     | W24 |       |                                                                        |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



# TMS320C6701 FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## Signal Descriptions (Continued)

| SIGNAL<br>NAME NO.              |      | TYPE† | DESCRIPTION                                                                           |
|---------------------------------|------|-------|---------------------------------------------------------------------------------------|
| SUPPLY VOLTAGE PINS (CONTINUED) |      |       |                                                                                       |
| DV <sub>DD</sub>                | Y4   | S     | 3.3-V supply voltage                                                                  |
|                                 | AB3  |       |                                                                                       |
|                                 | AB4  |       |                                                                                       |
|                                 | AB26 |       |                                                                                       |
|                                 | AC6  |       |                                                                                       |
|                                 | AC10 |       |                                                                                       |
|                                 | AC19 |       |                                                                                       |
|                                 | AC21 |       |                                                                                       |
|                                 | AC22 |       |                                                                                       |
|                                 | AC25 |       |                                                                                       |
|                                 | AD11 |       |                                                                                       |
|                                 | AD13 |       |                                                                                       |
|                                 | AD15 |       |                                                                                       |
|                                 | AD18 |       |                                                                                       |
|                                 | AE18 |       |                                                                                       |
|                                 | AE21 |       |                                                                                       |
|                                 | AF5  |       |                                                                                       |
|                                 | AF6  |       |                                                                                       |
|                                 | AF17 |       |                                                                                       |
| CV <sub>DD</sub>                | A5   | S     | 1.8-V supply voltage (for 6701-120, -150)<br>1.9-V supply voltage (for 6701-167 only) |
|                                 | A12  |       |                                                                                       |
|                                 | A16  |       |                                                                                       |
|                                 | A20  |       |                                                                                       |
|                                 | B2   |       |                                                                                       |
|                                 | B6   |       |                                                                                       |
|                                 | B11  |       |                                                                                       |
|                                 | B12  |       |                                                                                       |
|                                 | B25  |       |                                                                                       |
|                                 | C3   |       |                                                                                       |
|                                 | C15  |       |                                                                                       |
|                                 | C20  |       |                                                                                       |
|                                 | C24  |       |                                                                                       |
|                                 | D4   |       |                                                                                       |
|                                 | D6   |       |                                                                                       |
|                                 | D7   |       |                                                                                       |
|                                 | D9   |       |                                                                                       |
|                                 | D14  |       |                                                                                       |
|                                 | D18  |       |                                                                                       |
|                                 | D20  |       |                                                                                       |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



TMS320C6701  
FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

| Signal Descriptions (Continued) |      |       |                                                                                       |
|---------------------------------|------|-------|---------------------------------------------------------------------------------------|
| SIGNAL<br>NAME      NO.         |      | TYPE† | DESCRIPTION                                                                           |
| SUPPLY VOLTAGE PINS (CONTINUED) |      |       |                                                                                       |
| CV <sub>DD</sub>                | D23  | S     | 1.8-V supply voltage (for 6701-120, -150)<br>1.9-V supply voltage (for 6701-167 only) |
|                                 | E1   |       |                                                                                       |
|                                 | F1   |       |                                                                                       |
|                                 | H4   |       |                                                                                       |
|                                 | J4   |       |                                                                                       |
|                                 | J23  |       |                                                                                       |
|                                 | K1   |       |                                                                                       |
|                                 | K23  |       |                                                                                       |
|                                 | M1   |       |                                                                                       |
|                                 | M24  |       |                                                                                       |
|                                 | N4   |       |                                                                                       |
|                                 | N25  |       |                                                                                       |
|                                 | P2   |       |                                                                                       |
|                                 | P23  |       |                                                                                       |
|                                 | T3   |       |                                                                                       |
|                                 | T4   |       |                                                                                       |
|                                 | U1   |       |                                                                                       |
|                                 | V4   |       |                                                                                       |
|                                 | V23  |       |                                                                                       |
|                                 | AC4  |       |                                                                                       |
|                                 | AC9  |       |                                                                                       |
|                                 | AC12 |       |                                                                                       |
|                                 | AC13 |       |                                                                                       |
|                                 | AC18 |       |                                                                                       |
|                                 | AC23 |       |                                                                                       |
|                                 | AD3  |       |                                                                                       |
|                                 | AD8  |       |                                                                                       |
|                                 | AD14 |       |                                                                                       |
|                                 | AD24 |       |                                                                                       |
|                                 | AE2  |       |                                                                                       |
|                                 | AE8  |       |                                                                                       |
|                                 | AE12 |       |                                                                                       |
|                                 | AE25 |       |                                                                                       |
|                                 | AF12 |       |                                                                                       |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



**TMS320C6701**  
**FLOATING-POINT DIGITAL SIGNAL PROCESSOR**

SPRS067F – MAY 1998 – REVISED MARCH 2004

**Signal Descriptions (Continued)**

| SIGNAL<br>NAME NO. |     | TYPE† | DESCRIPTION |
|--------------------|-----|-------|-------------|
| GROUND PINS        |     |       |             |
| VSS                | A1  | GND   | Ground pins |
|                    | A2  |       |             |
|                    | A4  |       |             |
|                    | A13 |       |             |
|                    | A14 |       |             |
|                    | A25 |       |             |
|                    | A26 |       |             |
|                    | B1  |       |             |
|                    | B3  |       |             |
|                    | B5  |       |             |
|                    | B24 |       |             |
|                    | B26 |       |             |
|                    | C2  |       |             |
|                    | C7  |       |             |
|                    | C13 |       |             |
|                    | C16 |       |             |
|                    | C17 |       |             |
|                    | C25 |       |             |
|                    | D13 |       |             |
|                    | D19 |       |             |
|                    | E3  |       |             |
|                    | E24 |       |             |
|                    | F2  |       |             |
|                    | F24 |       |             |
|                    | G3  |       |             |
|                    | G4  |       |             |
|                    | G26 |       |             |
|                    | J3  |       |             |
|                    | L23 |       |             |
|                    | L26 |       |             |
|                    | M23 |       |             |
|                    | N1  |       |             |
|                    | N2  |       |             |
|                    | N24 |       |             |
|                    | N26 |       |             |
|                    | P1  |       |             |
|                    | P26 |       |             |
|                    | R24 |       |             |
|                    | T25 |       |             |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



TMS320C6701  
FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

| Signal Descriptions (Continued) |      |       |             |
|---------------------------------|------|-------|-------------|
| SIGNAL<br>NAME NO.              |      | TYPE† | DESCRIPTION |
| GROUND PINS (CONTINUED)         |      |       |             |
| VSS                             | U2   | GND   | Ground pins |
|                                 | U23  |       |             |
|                                 | V1   |       |             |
|                                 | V3   |       |             |
|                                 | Y3   |       |             |
|                                 | Y25  |       |             |
|                                 | AA3  |       |             |
|                                 | AA23 |       |             |
|                                 | AB23 |       |             |
|                                 | AC2  |       |             |
|                                 | AC5  |       |             |
|                                 | AC7  |       |             |
|                                 | AC14 |       |             |
|                                 | AC16 |       |             |
|                                 | AD2  |       |             |
|                                 | AD12 |       |             |
|                                 | AD16 |       |             |
|                                 | AD20 |       |             |
|                                 | AD25 |       |             |
|                                 | AE1  |       |             |
|                                 | AE3  |       |             |
|                                 | AE7  |       |             |
|                                 | AE9  |       |             |
|                                 | AE13 |       |             |
|                                 | AE16 |       |             |
|                                 | AE19 |       |             |
|                                 | AE23 |       |             |
|                                 | AE24 |       |             |
|                                 | AE26 |       |             |
|                                 | AF1  |       |             |
|                                 | AF2  |       |             |
|                                 | AF8  |       |             |
|                                 | AF10 |       |             |
|                                 | AF13 |       |             |
|                                 | AF14 |       |             |
|                                 | AF25 |       |             |
|                                 | AF26 |       |             |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

# TMS320C6701 FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## Signal Descriptions (Continued)

| SIGNAL<br>NAME      NO.    |     | TYPE† | DESCRIPTION      |
|----------------------------|-----|-------|------------------|
| REMAINING UNCONNECTED PINS |     |       |                  |
| NC                         | A8  |       | Unconnected pins |
|                            | B8  |       |                  |
|                            | C9  |       |                  |
|                            | D10 |       |                  |
|                            | D21 |       |                  |
|                            | G1  |       |                  |
|                            | H1  |       |                  |
|                            | H2  |       |                  |
|                            | J2  |       |                  |
|                            | K3  |       |                  |
|                            | R2  |       |                  |

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

---

### development support

TI offers an extensive line of development tools for the TMS320C6000 DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

#### **Software Development Tools:**

Code Composer Studio™ Integrated Development Environment (IDE): including Editor

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP BIOS), which provides the basic run-time target software needed to support any DSP application.

#### **Hardware Development Tools:**

Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug)

EVM (Evaluation Module)

The *TMS320 DSP Development Support Reference Guide* (SPRU011) contains information about development-support products for all TMS320™ DSP family member devices, including documentation. See this document for further information on TMS320™ DSP documentation or any TMS320™ DSP support products from Texas Instruments. An additional document, the *TMS320 Third-Party Support Reference Guide* (SPRU052), contains information about TMS320™ DSP-related products from other companies in the industry. To receive TMS320™ DSP literature, contact the Literature Response Center at 800/477-8924.

For a complete listing of development-support tools for the TMS320C6000 DSP platform, visit the Texas Instruments web site on the Worldwide Web at <http://www.ti.com> uniform resource locator (URL) and under “Development Tools”, select “Digital Signal Processors”. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

---

Code Composer Studio, XDS, and TMS320 are trademarks of Texas Instruments.

---



## device and development-support tool nomenclature

To designate the stages in the product-development cycle, TI assigns prefixes to the part numbers of all TMS320 DSP devices and support tools. Each TMS320 DSP family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

|            |                                                                                                                                      |
|------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <b>TMX</b> | Experimental device that is not necessarily representative of the final device's electrical specifications                           |
| <b>TMP</b> | Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification |
| <b>TMS</b> | Fully qualified production device                                                                                                    |

Support tool development evolutionary flow:

|             |                                                                                                          |
|-------------|----------------------------------------------------------------------------------------------------------|
| <b>TMDX</b> | Development-support product that has not yet completed Texas Instruments internal qualification testing. |
| <b>TMDS</b> | Fully qualified development-support product                                                              |

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GJC), the temperature range (for example, blank is the default commercial temperature range), and the device speed range in megahertz (for example, -167 is 167 MHz). Table 2 identifies the available TMS320C6701 devices by their associated orderable part numbers (P/Ns) and gives device-specific ordering information (for example, device speeds, core and I/O supply voltage values, and device operating temperature ranges). Figure 4 provides a legend for reading the complete device name for any TMS320™ DSP family member.

**Table 2. TMS320C6701 Device P/Ns and Ordering Information**

| DEVICE ORDERABLE P/N | DEVICE SPEED       | CV <sub>DD</sub><br>(CORE VOLTAGE) | DV <sub>DD</sub><br>(I/O VOLTAGE) | OPERATING CASE<br>TEMPERATURE<br>RANGE |
|----------------------|--------------------|------------------------------------|-----------------------------------|----------------------------------------|
| TMSC6701GJC16719V    | 167 MHz/1 GFLOPS   | 1.9 V                              | 3.3 V                             | 0°C to 90°C                            |
| TMS320C6701GJC150    | 150 MHz/900 MFLOPS | 1.8 V                              | 3.3 V                             | 0°C to 90°C                            |
| TMS320C6701GJCA120   | 120 MHz/720 MFLOPS | 1.8 V                              | 3.3 V                             | –40°C to 105°C                         |

TMS320C6701  
FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

device and development-support tool nomenclature (continued)

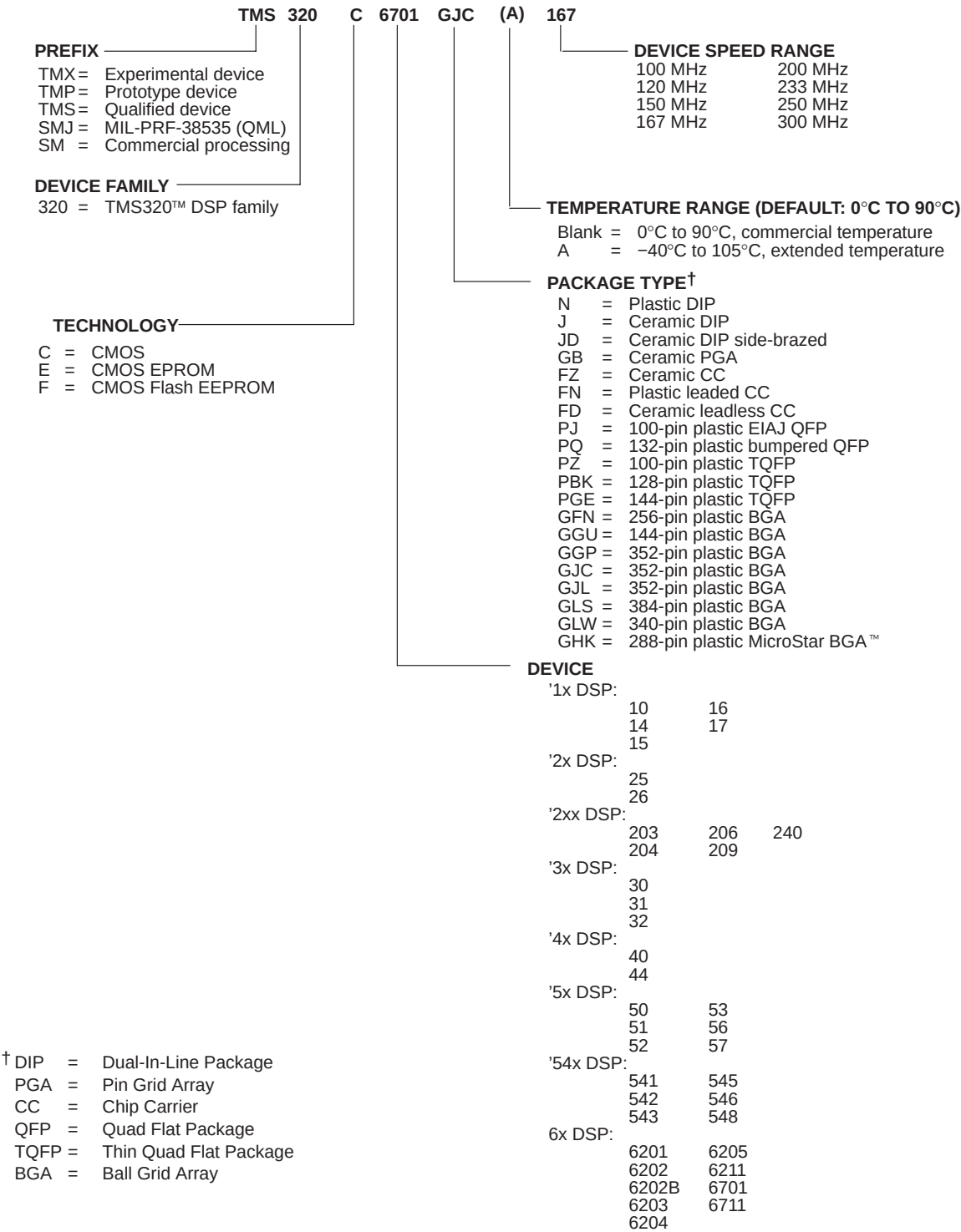


Figure 4. TMS320 DSP Device Nomenclature (Including TMS320C6701)

MicroStar BGA is a trademark of Texas Instruments.



## documentation support

Extensive documentation supports all TMS320 DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's reference guides for all devices; technical briefs; development-support tools; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6x devices:

The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the C6000 DSP CPU architecture, instruction set, pipeline, and associated interrupts.

The *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number SPRU190) briefly describes the functionality of the peripherals available on C6x devices, such as the external memory interface (EMIF), host-port interface (HPI), multichannel buffered serial ports (McBSPs), direct-memory-access (DMA), enhanced direct-memory-access (EDMA) controller, expansion bus (XB), clocking and phase-locked loop (PLL); and power-down modes.

The *TMS320C6000 Technical Brief* (literature number SPRU197) gives an introduction to the C62x/C67x devices, associated development tools, and third-party support.

The tools support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE). For a complete listing of C6000 DSP latest documentation, visit the Texas Instruments web site on the Worldwide Web at <http://www.ti.com> uniform resource locator (URL).



# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### clock PLL

All of the internal C67x clocks are generated from a single source through the CLKIN pin. This source clock either drives the PLL, which multiplies the source clock in frequency to generate the internal CPU clock, or bypasses the PLL to become the internal CPU clock.

To use the PLL to generate the CPU clock, the external PLL filter circuit must be properly designed. Table 3, Table 4, and Figure 5 show the external PLL circuitry for either x1 (PLL bypass) or x4 PLL multiply modes. Table 3 and Figure 6 show the external PLL circuitry for a system with ONLY x1 (PLL bypass) mode.

To minimize the clock jitter, a single clean power supply should power both the C67x device and the external clock oscillator circuit. Noise coupling into PLLF directly impacts PLL clock jitter. The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see the *input and output clocks* electricals section.

**Table 3. CLKOUT1 Frequency Ranges<sup>†</sup>**

| PLLFREQ3<br>(A9) | PLLFREQ2<br>(D11) | PLLFREQ1<br>(B10) | CLKOUT1 FREQUENCY RANGE<br>(MHZ) |
|------------------|-------------------|-------------------|----------------------------------|
| 0                | 0                 | 0                 | 50–140                           |
| 0                | 0                 | 1                 | 65–167                           |
| 0                | 1                 | 0                 | 130–167                          |

<sup>†</sup> Due to overlap of frequency ranges when choosing the PLLFREQ, more than one frequency range can contain the CLKOUT1 frequency. Choose the lowest frequency range that includes the desired frequency. For example, for CLKOUT1 = 133 MHz, choose PLLFREQ value of 000b. For CLKOUT1 = 167 MHz, choose PLLFREQ value of 001b. PLLFREQ values other than 000b, 001b, and 010b are reserved.

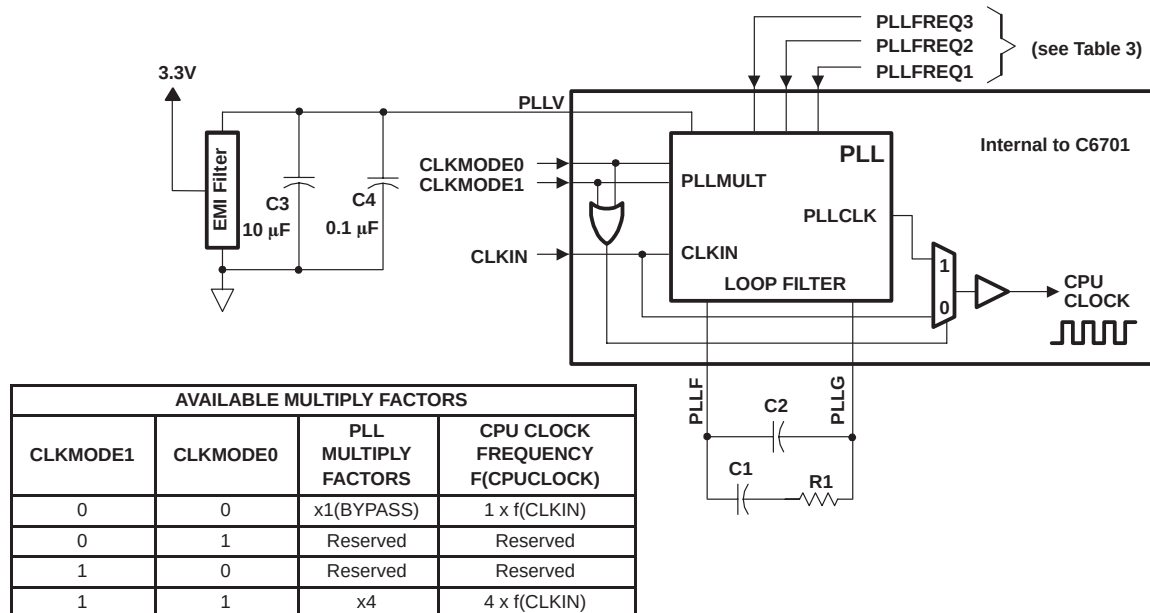
**Table 4. C6701 PLL Component Selection Table**

| CLKMODE | CLKIN<br>RANGE<br>(MHz) | CPU CLOCK<br>FREQUENCY<br>(CLKOUT1)<br>RANGE (MHz) | CLKOUT2<br>RANGE<br>(MHz) | R1<br>( $\Omega$ ) | C1<br>(nF) | C2<br>(pF) | TYPICAL<br>LOCK TIME<br>( $\mu$ s) <sup>‡</sup> |
|---------|-------------------------|----------------------------------------------------|---------------------------|--------------------|------------|------------|-------------------------------------------------|
| x4      | 12.5–41.7               | 50–167                                             | 25–83.5                   | 60.4               | 27         | 560        | 75                                              |

<sup>‡</sup> Under some operating conditions, the maximum PLL lock time may vary as much as 150% from the specified typical value. For example, if the typical lock time is specified as 100  $\mu$ s, the maximum value may be as long as 250  $\mu$ s.

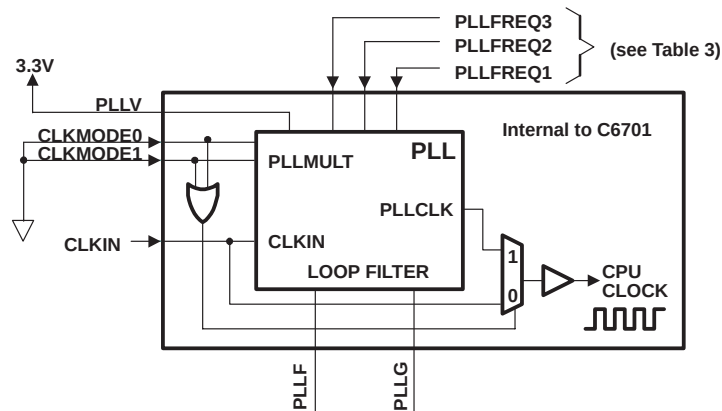


## clock PLL (continued)



- NOTES:
- A. Keep the lead length and the number of vias between the PLLF pin, the PLLG pin, and R1, C1, and C2 to a minimum. In addition, place all PLL external components (R1, C1, C2, C3, C4, and the EMI Filter) as close to the C6000™ DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown.
  - B. For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (R1, C1, C2, C3, C4, and the EMI Filter).
  - C. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV<sub>DD</sub>.
  - D. EMI filter manufacturer: TDK part number ACF451832-333, 223, 153, 103. Panasonic part number EXCET103U.

**Figure 5. External PLL Circuitry for Either PLL x4 Mode or x1 (Bypass) Mode**



- NOTES:
- A. For a system with ONLY PLL x1 (bypass) mode, short the PLLF terminal to the PLLG terminal.
  - B. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV<sub>DD</sub>.

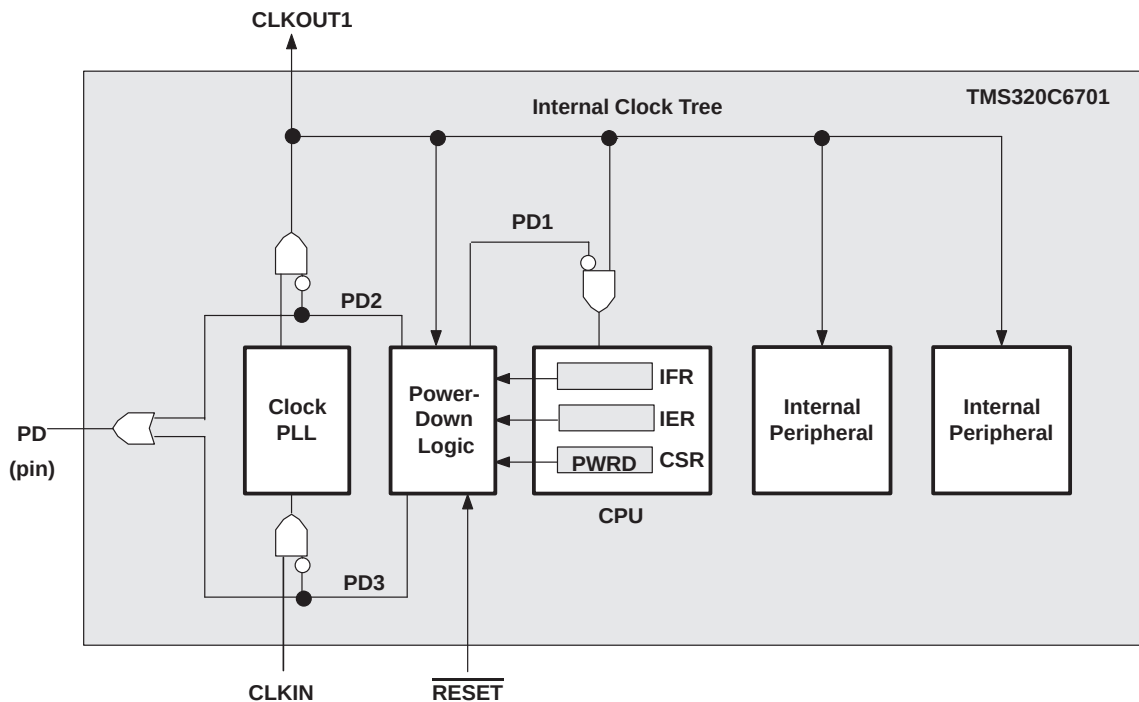
**Figure 6. External PLL Circuitry for x1 (Bypass) Mode Only**

# FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## power-down mode logic

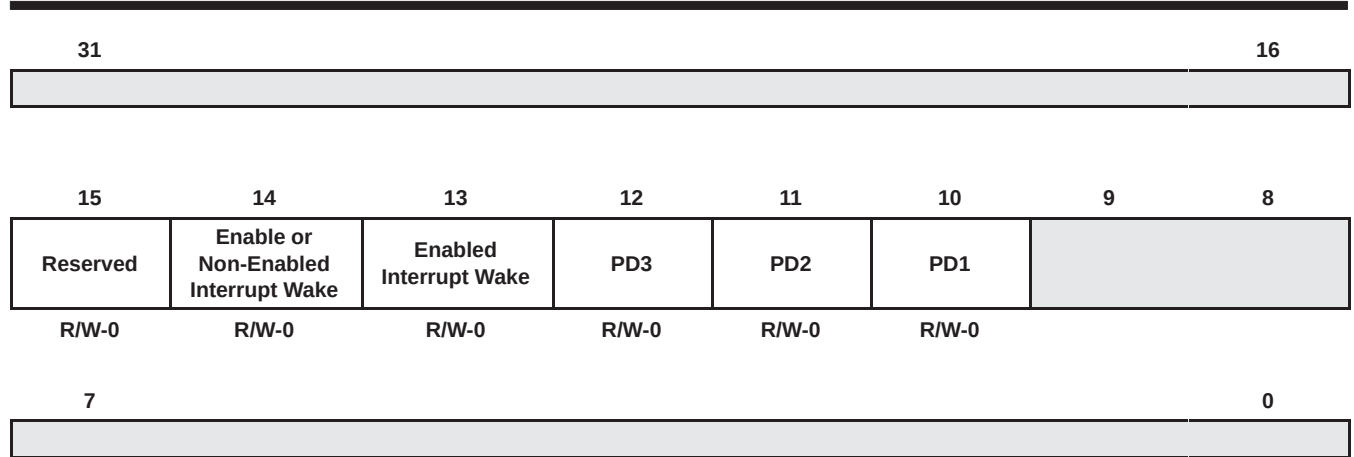
Figure 7 shows the power-down mode logic on the C6701.



### Figure 7. Power-Down Mode Logic<sup>†</sup>

## triggering, wake-up, and effects

The power-down modes and their wake-up methods are programmed by setting the PWRD field (bits 15–10) of the control status register (CSR). The PWRD field of the CSR is shown in Figure 8 and described in Table 5. When writing to the CSR, all bits of the PWRD field should be set at the same time. Logic 0 should be used when “writing” to the reserved bit (bit 15) of the PWRD field. The CSR is discussed in detail in the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189).



**Legend:** R/W-x = Read/write reset value

**NOTE:** The shadowed bits are not part of the power-down logic discussion and therefore are not covered here. For information on these other bit fields in the CSR register, see the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189).

**Figure 8. PWRD Field of the CSR Register**

Power-down mode PD1 takes effect eight to nine clock cycles after the instruction that sets the PWRD bits in the CSR.

If PD1 mode is terminated by a non-enabled interrupt, the program execution returns to the instruction where PD1 took effect. If PD1 mode is terminated by an enabled interrupt, the interrupt service routine will be executed first, then the program execution returns to the instruction where PD1 took effect. The GIE bit in CSR and the NMIE bit in the interrupt enable register (IER) must also be set in order for the interrupt service routine to execute; otherwise, execution returns to the instruction where PD1 took effect upon PD1 mode termination by an enabled interrupt.

PD2 and PD3 modes can only be aborted by device reset. Table 5 summarizes all the power-down modes.

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

**Table 5. Characteristics of the Power-Down Modes**

| PRWD FIELD<br>(BITS 15–10) | POWER-DOWN<br>MODE | WAKE-UP METHOD                              | EFFECT ON CHIP'S OPERATION                                                                                                                                                                                                                                                                                                                                           |
|----------------------------|--------------------|---------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 000000                     | No power-down      | —                                           | —                                                                                                                                                                                                                                                                                                                                                                    |
| 001001                     | PD1                | Wake by an enabled interrupt                | CPU halted (except for the interrupt logic)<br>Power-down mode blocks the internal clock inputs at the boundary of the CPU, preventing most of the CPU's logic from switching. During PD1, DMA transactions can proceed between peripherals and internal memory.                                                                                                     |
| 010001                     | PD1                | Wake by an enabled or non-enabled interrupt |                                                                                                                                                                                                                                                                                                                                                                      |
| 011010                     | PD2 <sup>†</sup>   | Wake by a device reset                      | Output clock from PLL is halted, stopping the internal clock structure from switching and resulting in the entire chip being halted. All register and internal RAM contents are preserved. All functional I/O "freeze" in the last state when the PLL clock is turned off.                                                                                           |
| 011100                     | PD3 <sup>†</sup>   | Wake by a device reset                      | Input clock to the PLL stops generating clocks. All register and internal RAM contents are preserved. All functional I/O "freeze" in the last state when the PLL clock is turned off. Following reset, the PLL needs time to re-lock, just as it does following power-up. Wake-up from PD3 takes longer than wake-up from PD2 because the PLL needs to be re-locked. |
| All others                 | Reserved           | —                                           | —                                                                                                                                                                                                                                                                                                                                                                    |

<sup>†</sup> When entering PD2 and PD3, all functional I/O remains in the previous state. However, for peripherals which are asynchronous in nature or peripherals with an external clock source, output signals may transition in response to stimulus on the inputs. Under these conditions, peripherals will not operate according to specifications.



**absolute maximum ratings over operating case temperature range (unless otherwise noted)<sup>†</sup>**

|                                                   |                 |
|---------------------------------------------------|-----------------|
| Supply voltage range, $CV_{DD}$ (see Note 1)      | –0.3 V to 2.3 V |
| Supply voltage range, $DV_{DD}$ (see Note 1)      | –0.3 V to 4 V   |
| Input voltage range                               | –0.3 V to 4 V   |
| Output voltage range                              | –0.3 V to 4 V   |
| Operating case temperature range, $T_C$ (Default) | 0°C to 90°C     |
| (A Version)                                       | –40°C to 105°C  |
| Storage temperature range, $T_{Stg}$              | –55°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to  $V_{SS}$ .

**recommended operating conditions**

|                                             |                | MIN  | NOM  | MAX  | UNIT |
|---------------------------------------------|----------------|------|------|------|------|
| $CV_{DD}$ Supply voltage, Core <sup>‡</sup> | 6701-120, -150 | 1.71 | 1.8  | 1.89 | V    |
|                                             | 6701-167 only  | 1.81 | 1.9  | 1.99 | V    |
| $DV_{DD}$ Supply voltage, I/O <sup>‡</sup>  |                | 3.14 | 3.30 | 3.46 | V    |
| $V_{SS}$ Supply ground                      |                | 0    | 0    | 0    | V    |
| $V_{IH}$ High-level input voltage           |                | 2.0  |      |      | V    |
| $V_{IL}$ Low-level input voltage            |                |      |      | 0.8  | V    |
| $I_{OH}$ High-level output current          |                |      |      | –12  | mA   |
| $I_{OL}$ Low-level output current           |                |      |      | 12   | mA   |
| $T_C$ Case temperature                      | Default        | 0    |      | 90   | °C   |
|                                             | A Version      | –40  |      | 105  | °C   |

<sup>‡</sup> TI DSP's do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long term reliability of the device. System-level concerns such as bus contention may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers. For additional power supply sequencing information, see the *Power Supply Sequencing Solutions For Dual Supply Voltage DSPs* application report (literature number SLVA073).

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

**electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)**

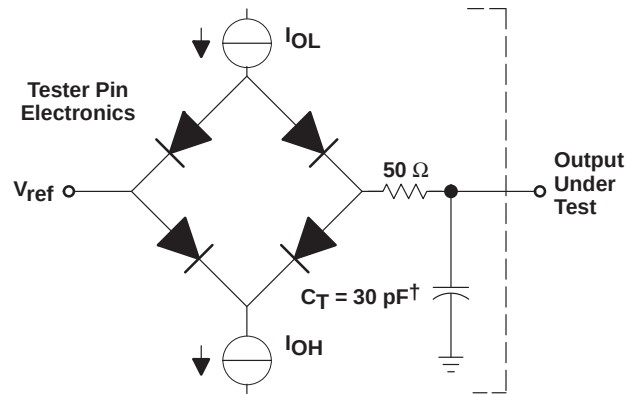
| PARAMETER                                                              | TEST CONDITIONS                                      | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------------------|------------------------------------------------------|-----|-----|-----|------|
| V <sub>OH</sub> High-level output voltage                              | DV <sub>DD</sub> = MIN, I <sub>OH</sub> = MAX        | 2.4 |     |     | V    |
| V <sub>OL</sub> Low-level output voltage                               | DV <sub>DD</sub> = MIN, I <sub>OL</sub> = MAX        |     |     | 0.6 | V    |
| I <sub>I</sub> Input current <sup>†</sup>                              | V <sub>I</sub> = V <sub>SS</sub> to DV <sub>DD</sub> |     |     | ±10 | uA   |
| I <sub>OZ</sub> Off-state output current                               | V <sub>O</sub> = DV <sub>DD</sub> or 0 V             |     |     | ±10 | uA   |
| I <sub>DD2V</sub> Supply current, CPU + CPU memory access <sup>‡</sup> | CV <sub>DD</sub> = NOM, CPU clock = 150 MHz          |     | 470 |     | mA   |
|                                                                        | CV <sub>DD</sub> = NOM, CPU clock = 120 MHz          |     | 380 |     |      |
| I <sub>DD2V</sub> Supply current, peripherals <sup>‡</sup>             | CV <sub>DD</sub> = NOM, CPU clock = 150 MHz          |     | 250 |     | mA   |
|                                                                        | CV <sub>DD</sub> = NOM, CPU clock = 120 MHz          |     | 200 |     |      |
| I <sub>DD3V</sub> Supply current, I/O pins <sup>‡</sup>                | DV <sub>DD</sub> = NOM, CPU clock = 150 MHz          |     | 85  |     | mA   |
|                                                                        | DV <sub>DD</sub> = NOM, CPU clock = 120 MHz          |     | 70  |     |      |
| C <sub>i</sub> Input capacitance                                       |                                                      |     |     | 10  | pF   |
| C <sub>o</sub> Output capacitance                                      |                                                      |     |     | 10  | pF   |

<sup>†</sup> TMS and TDI are not included due to internal pullups.

TRST is not included due to internal pulldown.

<sup>‡</sup> Measured with average activity (50% high / 50% low power). For more detailed information on CPU/peripheral/I/O activity, see the *TMS320C6000 Power Consumption Summary* application report (literature number SPRA486).

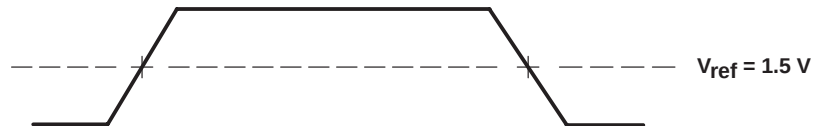
### PARAMETER MEASUREMENT INFORMATION



<sup>†</sup> Typical distributed load circuit capacitance.

### signal-transition levels

All input and output timing parameters are referenced to 1.5 V for both "0" and "1" logic levels.



**Figure 9. Input and Output Voltage Reference Levels for ac Timing Measurements**

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### INPUT AND OUTPUT CLOCKS

timing requirements for CLKIN (C6701-150, -167 devices only)<sup>†‡</sup> (see Figure 10)

| NO. |                                                 | C6701-150    |     |              |     | C6701-167    |     |              |     | UNIT |
|-----|-------------------------------------------------|--------------|-----|--------------|-----|--------------|-----|--------------|-----|------|
|     |                                                 | CLKMODE = x4 |     | CLKMODE = x1 |     | CLKMODE = x4 |     | CLKMODE = x1 |     |      |
|     |                                                 | MIN          | MAX | MIN          | MAX | MIN          | MAX | MIN          | MAX |      |
| 1   | $t_c(\text{CLKIN})$ Cycle time, CLKIN           | 26.7         |     | 6.7          |     | 24           |     | 6            |     | ns   |
| 2   | $t_w(\text{CLKINH})$ Pulse duration, CLKIN high | 0.4C         |     | 0.45C        |     | 0.4C         |     | 0.45C        |     | ns   |
| 3   | $t_w(\text{CLKINL})$ Pulse duration, CLKIN low  | 0.4C         |     | 0.45C        |     | 0.4C         |     | 0.45C        |     | ns   |
| 4   | $t_t(\text{CLKIN})$ Transition time, CLKIN      |              | 5   |              | 0.6 |              | 5   |              | 0.6 | ns   |

<sup>†</sup> The reference points for the rise and fall transitions are measured at 20% and 80%, respectively, of  $V_{IH}$ .

<sup>‡</sup> C = CLKIN cycle time in ns. For example, when CLKIN frequency is 10 MHz, use C = 100 ns.

timing requirements for CLKIN (C6701-120 device only)<sup>†‡</sup> (see Figure 10)

| NO. |                                                    | C6701-120    |     |              |     | UNIT |
|-----|----------------------------------------------------|--------------|-----|--------------|-----|------|
|     |                                                    | CLKMODE = x4 |     | CLKMODE = x1 |     |      |
|     |                                                    | MIN          | MAX | MIN          | MAX |      |
| 1   | t <sub>c</sub> (CLKIN) Cycle time, CLKIN           | 33.3         |     | 8.3          |     | ns   |
| 2   | t <sub>w</sub> (CLKINH) Pulse duration, CLKIN high | 0.4C         |     | 0.45C        |     | ns   |
| 3   | t <sub>w</sub> (CLKINL) Pulse duration, CLKIN low  | 0.4C         |     | 0.45C        |     | ns   |
| 4   | t <sub>t</sub> (CLKIN) Transition time, CLKIN      |              | 5   |              | 0.6 | ns   |

<sup>†</sup> The reference points for the rise and fall transitions are measured at 20% and 80%, respectively, of  $V_{IH}$ .

<sup>‡</sup> C = CLKIN cycle time in ns. For example, when CLKIN frequency is 10 MHz, use C = 100 ns.

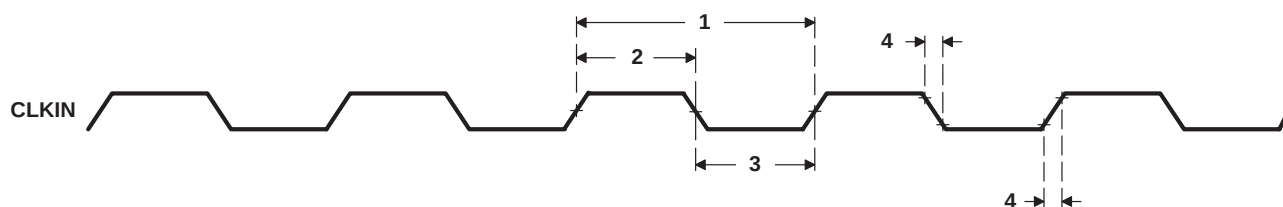


Figure 10. CLKIN Timings



## INPUT AND OUTPUT CLOCKS (CONTINUED)

### switching characteristics for CLKOUT1<sup>†‡</sup> (see Figure 11)

| NO. | PARAMETER                                              | C6701-120<br>C6701-150<br>C6701-167 |             |              |          | UNIT |
|-----|--------------------------------------------------------|-------------------------------------|-------------|--------------|----------|------|
|     |                                                        | CLKMODE = X4                        |             | CLKMODE = X1 |          |      |
|     |                                                        | MIN                                 | MAX         | MIN          | MAX      |      |
| 1   | t <sub>c</sub> (CKO1)    Cycle time, CLKOUT1           | P – 0.7                             | P + 0.7     | P – 0.7      | P + 0.7  | ns   |
| 2   | t <sub>w</sub> (CKO1H)    Pulse duration, CLKOUT1 high | (P/2) – 0.5                         | (P/2) + 0.5 | PH – 0.5     | PH + 0.5 | ns   |
| 3   | t <sub>w</sub> (CKO1L)    Pulse duration, CLKOUT1 low  | (P/2) – 0.5                         | (P/2) + 0.5 | PL – 0.5     | PL + 0.5 | ns   |
| 4   | t <sub>t</sub> (CKO1)    Transition time, CLKOUT1      | 0.6                                 |             | 0.6          |          | ns   |

<sup>†</sup>  $P = 1/\text{CPU clock frequency}$  in nanoseconds (ns).

<sup>‡</sup> PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.

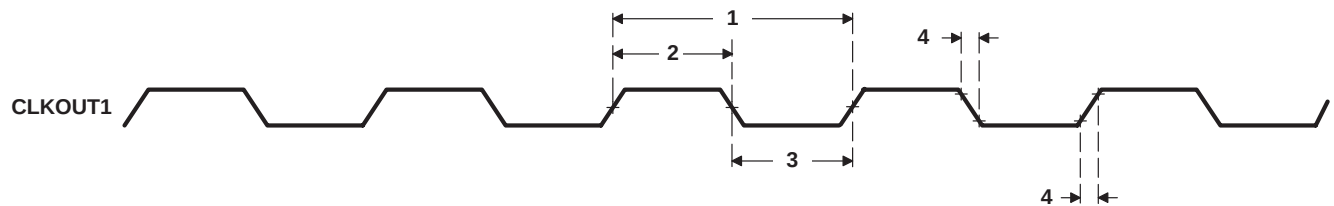


Figure 11. CLKOUT1 Timings

### switching characteristics for CLKOUT2<sup>§</sup> (see Figure 12)

| NO. | PARAMETER                                        | C6701-120<br>C6701-150<br>C6701-167 |            | UNIT |
|-----|--------------------------------------------------|-------------------------------------|------------|------|
|     |                                                  | MIN                                 | MAX        |      |
| 1   | $t_c(\text{CKO2})$ Cycle time, CLKOUT2           | $2P - 0.7$                          | $2P + 0.7$ | ns   |
| 2   | $t_w(\text{CKO2H})$ Pulse duration, CLKOUT2 high | $P - 0.7$                           | $P + 0.7$  | ns   |
| 3   | $t_w(\text{CKO2L})$ Pulse duration, CLKOUT2 low  | $P - 0.7$                           | $P + 0.7$  | ns   |
| 4   | $t_t(\text{CKO2})$ Transition time, CLKOUT2      | 0.6                                 |            | ns   |

<sup>§</sup>  $P = 1/\text{CPU clock frequency}$  in ns.

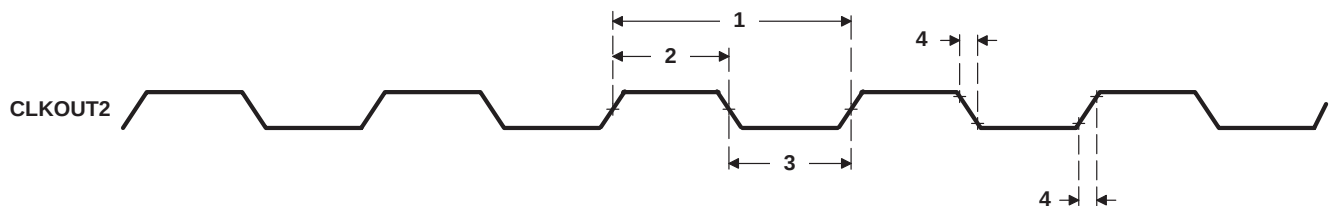


Figure 12. CLKOUT2 Timings

TMS320C6701  
FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

INPUT AND OUTPUT CLOCKS (CONTINUED)

SDCLK, SSCLK timing parameters

SDCLK timing parameters are the same as CLKOUT2 parameters.

SSCLK timing parameters are the same as CLKOUT1 or CLKOUT2 parameters, depending on SSCLK configuration.

switching characteristics for the relation of SSCLK, SDCLK, and CLKOUT2 to CLKOUT1  
(see Figure 13)

| NO. | PARAMETER                                                                           | C6701-120<br>C6701-150<br>C6701-167 |     | UNIT |
|-----|-------------------------------------------------------------------------------------|-------------------------------------|-----|------|
|     |                                                                                     | MIN                                 | MAX |      |
| 1   | $t_d(\text{CKO1-SSCLK})$ Delay time, CLKOUT1 edge to SSCLK edge                     | -0.8                                | 3.4 | ns   |
| 2   | $t_d(\text{CKO1-SSCLK1/2})$ Delay time, CLKOUT1 edge to SSCLK edge (1/2 clock rate) | -1.0                                | 3.0 | ns   |
| 3   | $t_d(\text{CKO1-CKO2})$ Delay time, CLKOUT1 edge to CLKOUT2 edge                    | -1.5                                | 2.5 | ns   |
| 4   | $t_d(\text{CKO1-SDCLK})$ Delay time, CLKOUT1 edge to SDCLK edge                     | -1.5                                | 1.9 | ns   |

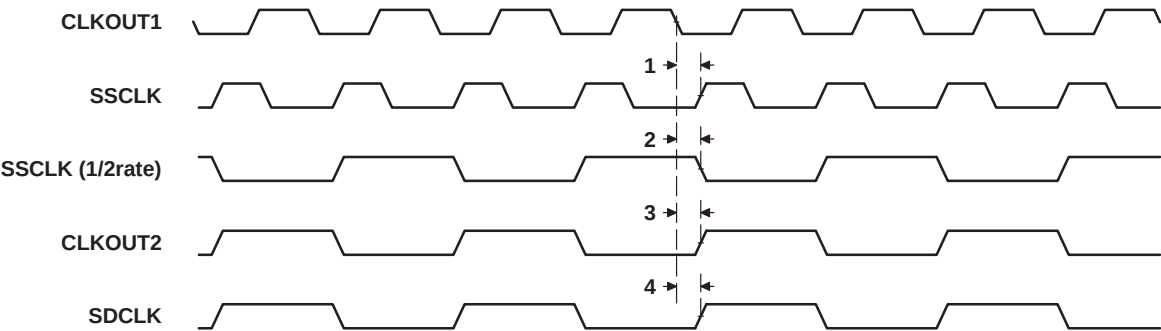


Figure 13. Relation of CLKOUT2, SDCLK, and SSCLK to CLKOUT1

## ASYNCHRONOUS MEMORY TIMING

**timing requirements for asynchronous memory cycles<sup>†</sup> (see Figure 14 and Figure 15)**

| NO. |                      |                                                | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|----------------------|------------------------------------------------|-------------------------------------|------|
|     |                      |                                                | MIN MAX                             |      |
| 6   | $t_{su}(EDV-CKO1H)$  | Setup time, read EDx valid before CLKOUT1 high | 4.5                                 | ns   |
| 7   | $t_h(CKO1H-EDV)$     | Hold time, read EDx valid after CLKOUT1 high   | 1.5                                 | ns   |
| 10  | $t_{su}(ARDY-CKO1H)$ | Setup time, ARDY valid before CLKOUT1 high     | 3.5                                 | ns   |
| 11  | $t_h(CKO1H-ARDY)$    | Hold time, ARDY valid after CLKOUT1 high       | 1.5                                 | ns   |

<sup>†</sup> To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. If ARDY does not meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, ARDY can be an asynchronous input.

**switching characteristics for asynchronous memory cycles<sup>‡</sup> (see Figure 14 and Figure 15)**

| NO. | PARAMETER          |                                                      | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|--------------------|------------------------------------------------------|-------------------------------------|------|
|     |                    |                                                      | MIN MAX                             |      |
| 1   | $t_d(CKO1H-CEV)$   | Delay time, CLKOUT1 high to $\overline{CE}x$ valid   | -1.0 4.5                            | ns   |
| 2   | $t_d(CKO1H-BEV)$   | Delay time, CLKOUT1 high to $\overline{B}Ex$ valid   | 4.5                                 | ns   |
| 3   | $t_d(CKO1H-BEIV)$  | Delay time, CLKOUT1 high to $\overline{B}Ex$ invalid | -1.0                                | ns   |
| 4   | $t_d(CKO1H-EAV)$   | Delay time, CLKOUT1 high to EAx valid                | 4.5                                 | ns   |
| 5   | $t_d(CKO1H-EAIV)$  | Delay time, CLKOUT1 high to EAx invalid              | -1.0                                | ns   |
| 8   | $t_d(CKO1H-AOE V)$ | Delay time, CLKOUT1 high to $\overline{AOE}$ valid   | -1.0 4.5                            | ns   |
| 9   | $t_d(CKO1H-ARE V)$ | Delay time, CLKOUT1 high to $\overline{ARE}$ valid   | -0.5 4.5                            | ns   |
| 12  | $t_d(CKO1H-EDV)$   | Delay time, CLKOUT1 high to EDx valid                | 4.5                                 | ns   |
| 13  | $t_d(CKO1H-EDIV)$  | Delay time, CLKOUT1 high to EDx invalid              | -1.0                                | ns   |
| 14  | $t_d(CKO1H-AWE V)$ | Delay time, CLKOUT1 high to $\overline{AWE}$ valid   | -1.0 4.5                            | ns   |

<sup>‡</sup> The minimum delay is also the minimum output hold after CLKOUT1 high.

# TMS320C6701 FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## ASYNCHRONOUS MEMORY TIMING (CONTINUED)

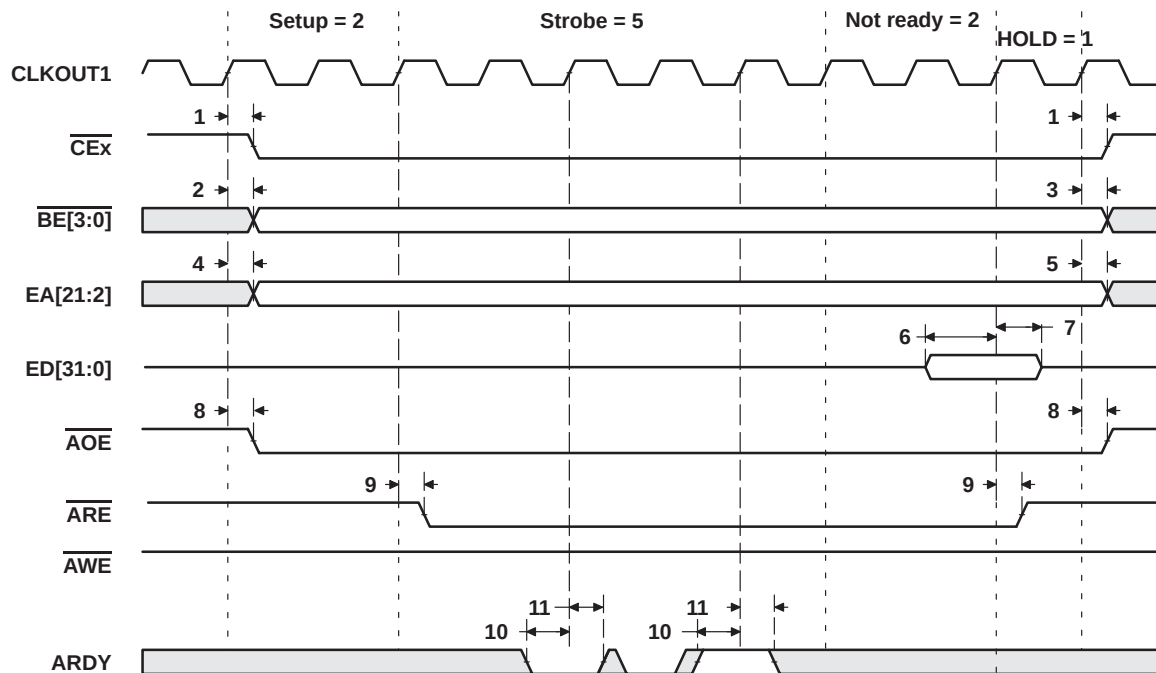


Figure 14. Asynchronous Memory Read Timing

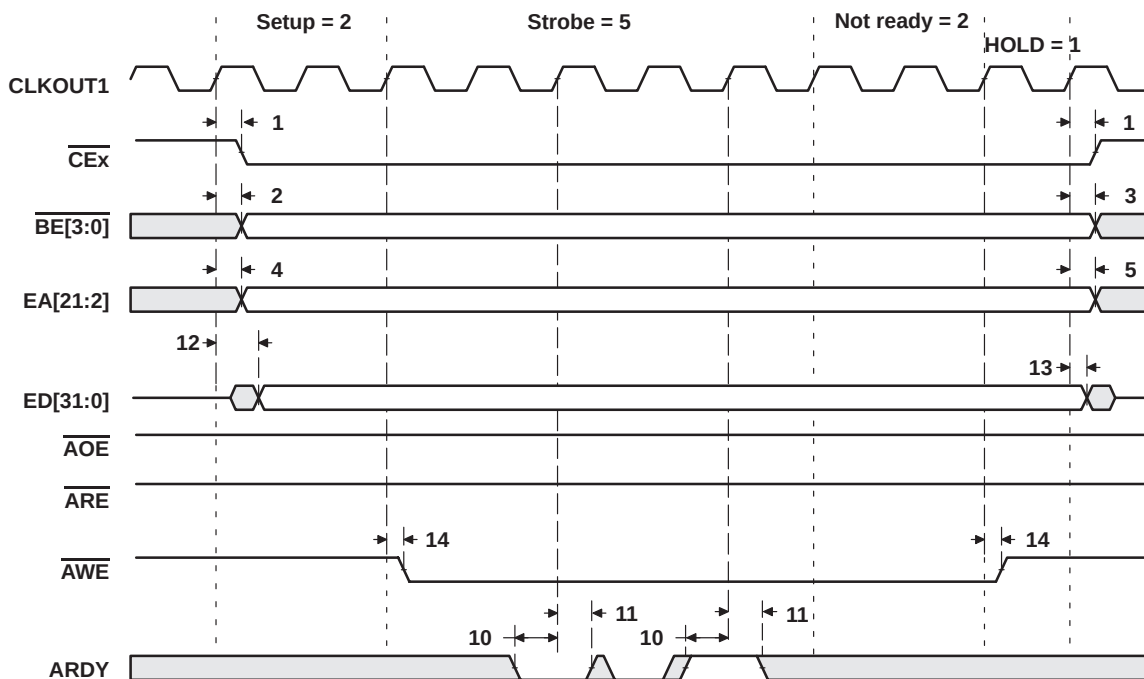


Figure 15. Asynchronous Memory Write Timing

## SYNCHRONOUS-BURST MEMORY TIMING

**timing requirements for synchronous-burst SRAM cycles (full-rate SSCLK) (see Figure 16)**

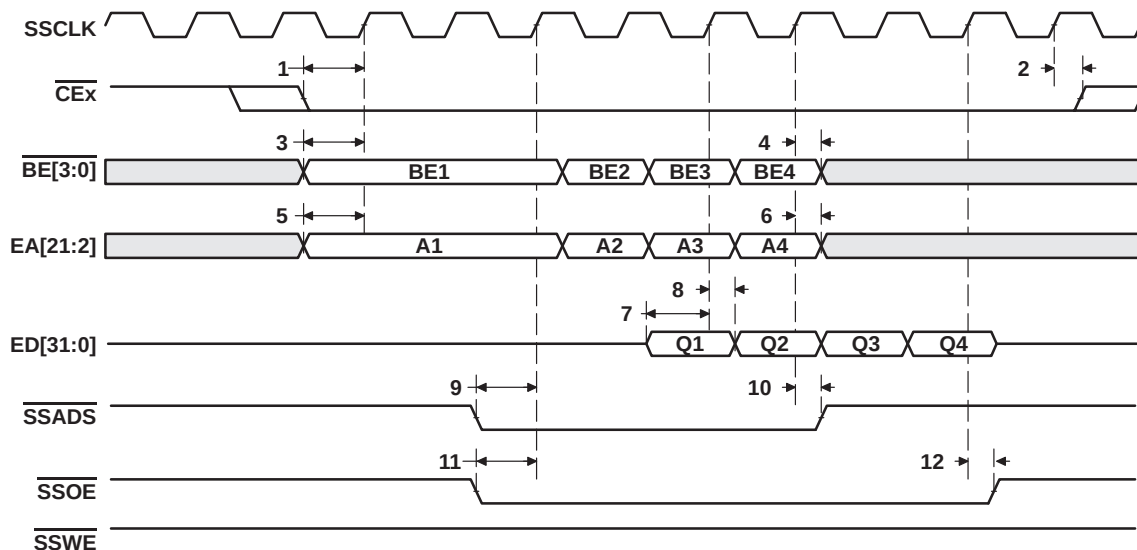
| NO. |                                                                   | 'C6701-120 |     | C6701-150<br>C6701-167 |     | UNIT |
|-----|-------------------------------------------------------------------|------------|-----|------------------------|-----|------|
|     |                                                                   | MIN        | MAX | MIN                    | MAX |      |
| 7   | $t_{su}(EDV-SSCLKH)$ Setup time, read EDx valid before SSCLK high | 2.0        |     | 2.0                    |     | ns   |
| 8   | $t_h(SSCLKH-EDV)$ Hold time, read EDx valid after SSCLK high      | 2.9        |     | 2.1                    |     | ns   |

**switching characteristics for synchronous-burst SRAM cycles<sup>†</sup> (full-rate SSCLK)  
(see Figure 16 and Figure 17)**

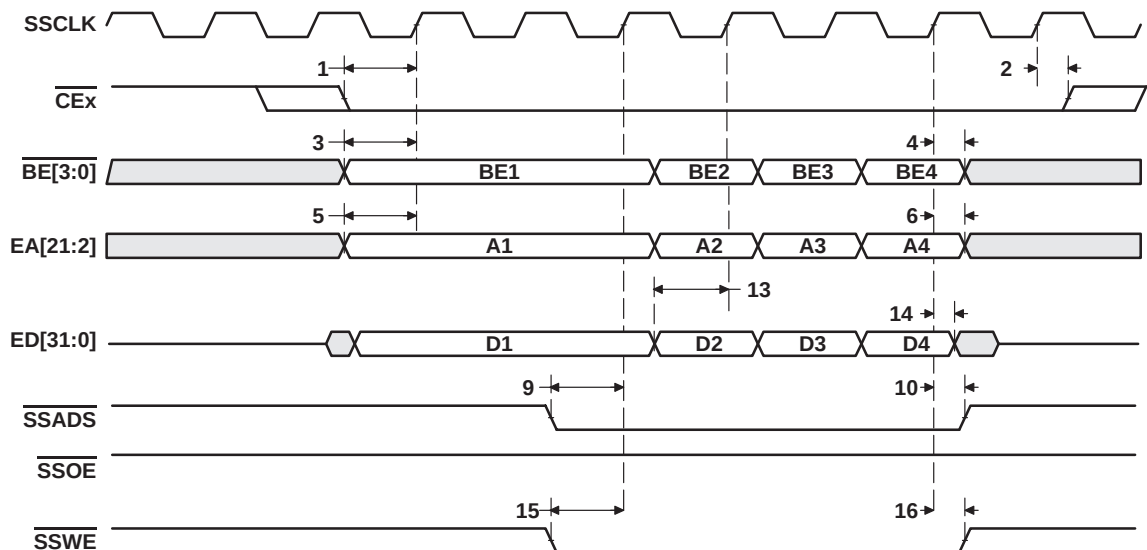
| NO. | PARAMETER                                                                            | 'C6701-120 |     | C6701-150<br>C6701-167 |     | UNIT |
|-----|--------------------------------------------------------------------------------------|------------|-----|------------------------|-----|------|
|     |                                                                                      | MIN        | MAX | MIN                    | MAX |      |
| 1   | $t_{osu}(CEV-SSCLKH)$ Output setup time, $\overline{CEx}$ valid before SSCLK high    | 0.5P – 1.3 |     | 0.5P – 1.3             |     | ns   |
| 2   | $t_{oh}(SSCLKH-CEV)$ Output hold time, $\overline{CEx}$ valid after SSCLK high       | 0.5P – 2.9 |     | 0.5P – 2.3             |     | ns   |
| 3   | $t_{osu}(BEV-SSCLKH)$ Output setup time, $\overline{BEx}$ valid before SSCLK high    | 0.5P – 1.3 |     | 0.5P – 1.6             |     | ns   |
| 4   | $t_{oh}(SSCLKH-BEIV)$ Output hold time, $\overline{BEx}$ invalid after SSCLK high    | 0.5P – 2.9 |     | 0.5P – 2.3             |     | ns   |
| 5   | $t_{osu}(EAV-SSCLKH)$ Output setup time, EAx valid before SSCLK high                 | 0.5P – 1.3 |     | 0.5P – 1.7             |     | ns   |
| 6   | $t_{oh}(SSCLKH-EAIV)$ Output hold time, EAx invalid after SSCLK high                 | 0.5P – 2.9 |     | 0.5P – 2.3             |     | ns   |
| 9   | $t_{osu}(ADSV-SSCLKH)$ Output setup time, $\overline{SSADS}$ valid before SSCLK high | 0.5P – 1.3 |     | 0.5P – 1.3             |     | ns   |
| 10  | $t_{oh}(SSCLKH-ADSV)$ Output hold time, $\overline{SSADS}$ valid after SSCLK high    | 0.5P – 2.9 |     | 0.5P – 2.3             |     | ns   |
| 11  | $t_{osu}(OEV-SSCLKH)$ Output setup time, $\overline{SSOE}$ valid before SSCLK high   | 0.5P – 1.3 |     | 0.5P – 1.3             |     | ns   |
| 12  | $t_{oh}(SSCLKH-OEV)$ Output hold time, $\overline{SSOE}$ valid after SSCLK high      | 0.5P – 2.9 |     | 0.5P – 2.3             |     | ns   |
| 13  | $t_{osu}(EDV-SSCLKH)$ Output setup time, EDx valid before SSCLK high                 | 0.5P – 1.3 |     | 0.5P – 1.3             |     | ns   |
| 14  | $t_{oh}(SSCLKH-EDIV)$ Output hold time, EDx invalid after SSCLK high                 | 0.5P – 2.9 |     | 0.5P – 2.3             |     | ns   |
| 15  | $t_{osu}(WEV-SSCLKH)$ Output setup time, $\overline{SSWE}$ valid before SSCLK high   | 0.5P – 1.3 |     | 0.5P – 1.3             |     | ns   |
| 16  | $t_{oh}(SSCLKH-WEV)$ Output hold time, $\overline{SSWE}$ valid after SSCLK high      | 0.5P – 2.9 |     | 0.5P – 2.3             |     | ns   |

<sup>†</sup> When the PLL is used (CLKMODE x4), P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.  
For CLKMODE x1, 0.5P is defined as PH (pulse duration of CLKIN high) for all output setup times; 0.5P is defined as PL (pulse duration of CLKIN low) for all output hold times.

**SYNCHRONOUS-BURST MEMORY TIMING (CONTINUED)**



**Figure 16. SBSRAM Read Timing (Full-Rate SSCLK)**



**Figure 17. SBSRAM Write Timing (Full-Rate SSCLK)**

## SYNCHRONOUS-BURST MEMORY TIMING (CONTINUED)

timing requirements for synchronous-burst SRAM cycles (half-rate SSCLK) (see Figure 18)

| NO. |                      |                                              | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|----------------------|----------------------------------------------|-------------------------------------|------|
|     |                      |                                              | MIN    MAX                          |      |
| 7   | $t_{su}(EDV-SSCLKH)$ | Setup time, read EDx valid before SSCLK high | 3.6                                 | ns   |
| 8   | $t_h(SSCLKH-EDV)$    | Hold time, read EDx valid after SSCLK high   | 1.5                                 | ns   |

switching characteristics for synchronous-burst SRAM cycles<sup>†</sup> (half-rate SSCLK)  
(see Figure 18 and Figure 19)

| NO. | PARAMETER              | C6701-120                                                     |     | C6701-150<br>C6701-167 |     | UNIT |
|-----|------------------------|---------------------------------------------------------------|-----|------------------------|-----|------|
|     |                        | MIN                                                           | MAX | MIN                    | MAX |      |
| 1   | $t_{osu}(CEV-SSCLKH)$  | Output setup time, $\overline{CEx}$ valid before SSCLK high   |     | 1.5P – 4.5             |     | ns   |
| 2   | $t_{oh}(SSCLKH-CEV)$   | Output hold time, $\overline{CEx}$ valid after SSCLK high     |     | 0.5P – 2               |     | ns   |
| 3   | $t_{osu}(BEV-SSCLKH)$  | Output setup time, $\overline{BEx}$ valid before SSCLK high   |     | 1.5P – 4.5             |     | ns   |
| 4   | $t_{oh}(SSCLKH-BEIV)$  | Output hold time, $\overline{BEx}$ invalid after SSCLK high   |     | 0.5P – 2               |     | ns   |
| 5   | $t_{osu}(EAV-SSCLKH)$  | Output setup time, EAx valid before SSCLK high                |     | 1.5P – 4.5             |     | ns   |
| 6   | $t_{oh}(SSCLKH-EAIV)$  | Output hold time, EAx invalid after SSCLK high                |     | 0.5P – 2               |     | ns   |
| 9   | $t_{osu}(ADSV-SSCLKH)$ | Output setup time, $\overline{SSADS}$ valid before SSCLK high |     | 1.5P – 4.5             |     | ns   |
| 10  | $t_{oh}(SSCLKH-ADSV)$  | Output hold time, $\overline{SSADS}$ valid after SSCLK high   |     | 0.5P – 2               |     | ns   |
| 11  | $t_{osu}(OEV-SSCLKH)$  | Output setup time, $\overline{SSOE}$ valid before SSCLK high  |     | 1.5P – 4.5             |     | ns   |
| 12  | $t_{oh}(SSCLKH-OEV)$   | Output hold time, $\overline{SSOE}$ valid after SSCLK high    |     | 0.5P – 2               |     | ns   |
| 13  | $t_{osu}(EDV-SSCLKH)$  | Output setup time, EDx valid before SSCLK high                |     | 1.5P – 4.5             |     | ns   |
| 14  | $t_{oh}(SSCLKH-EDIV)$  | Output hold time, EDx invalid after SSCLK high                |     | 0.5P – 2               |     | ns   |
| 15  | $t_{osu}(WEV-SSCLKH)$  | Output setup time, $\overline{SSWE}$ valid before SSCLK high  |     | 1.5P – 4.5             |     | ns   |
| 16  | $t_{oh}(SSCLKH-WEV)$   | Output hold time, $\overline{SSWE}$ valid after SSCLK high    |     | 0.5P – 2               |     | ns   |

<sup>†</sup> When the PLL is used (CLKMODE x4), P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

For CLKMODE x1:

1.5P = P + PH, where P = 1/CPU clock frequency, and PH = pulse duration of CLKIN high.

0.5P = PL, where PL = pulse duration of CLKIN low.

# TMS320C6701 FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## SYNCHRONOUS-BURST MEMORY TIMING (CONTINUED)

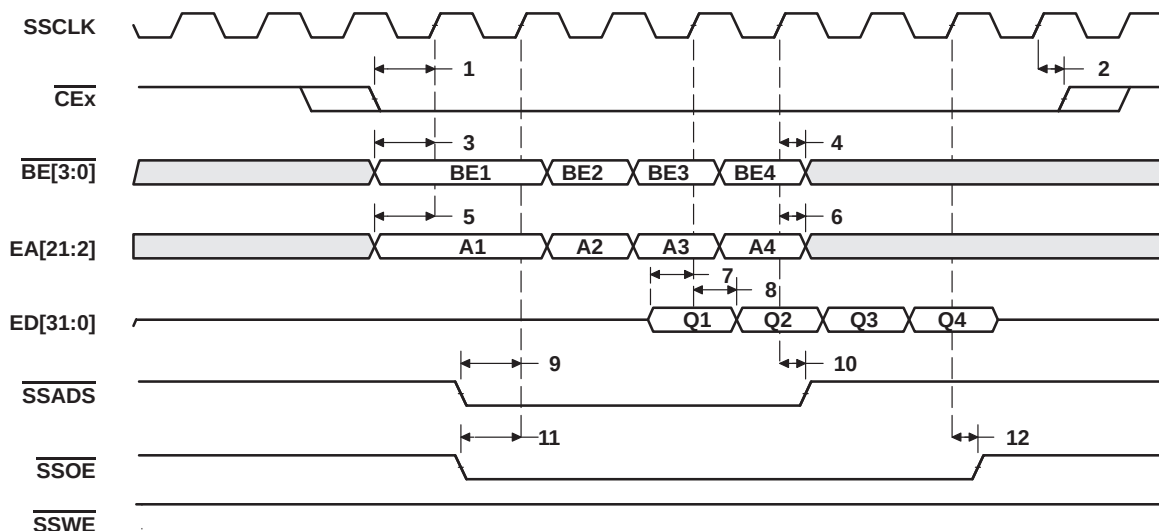


Figure 18. SBSRAM Read Timing (1/2 Rate SSCLK)

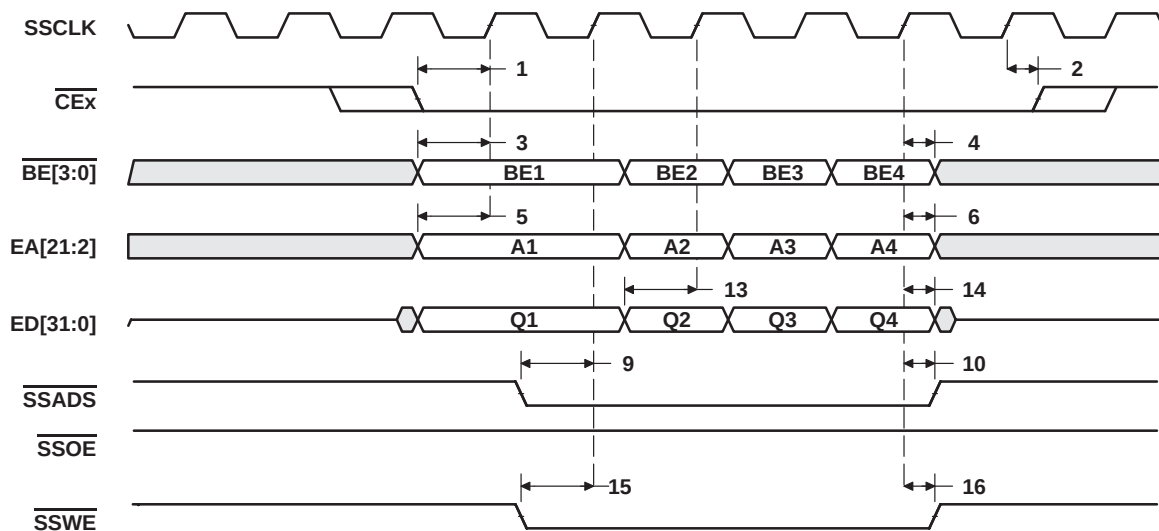


Figure 19. SBSRAM Write Timing (1/2 Rate SSCLK)



## SYNCHRONOUS DRAM TIMING

timing requirements for synchronous DRAM cycles (see Figure 20)

| NO. |                                                                   | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|-------------------------------------------------------------------|-------------------------------------|------|
|     |                                                                   | MIN MAX                             |      |
| 7   | $t_{su}(EDV-SDCLKH)$ Setup time, read EDx valid before SDCLK high | 1.8                                 | ns   |
| 8   | $t_h(SDCLKH-EDV)$ Hold time, read EDx valid after SDCLK high      | 3                                   | ns   |

switching characteristics for synchronous DRAM cycles<sup>†</sup> (see Figure 20–Figure 25)

| NO. | PARAMETER                                                                             | C6701-120  |     | C6701-150<br>C6701-167 |     | UNIT |
|-----|---------------------------------------------------------------------------------------|------------|-----|------------------------|-----|------|
|     |                                                                                       | MIN        | MAX | MIN                    | MAX |      |
| 1   | $t_{osu}(CEV-SDCLKH)$ Output setup time, $\overline{CEx}$ valid before SDCLK high     | 1.5P – 4   |     | 1.5P – 4               |     | ns   |
| 2   | $t_{oh}(SDCLKH-CEV)$ Output hold time, $\overline{CEx}$ valid after SDCLK high        | 0.5P – 1.9 |     | 0.5P – 1.5             |     | ns   |
| 3   | $t_{osu}(BEV-SDCLKH)$ Output setup time, $\overline{BEx}$ valid before SDCLK high     | 1.5P – 4   |     | 1.5P – 4               |     | ns   |
| 4   | $t_{oh}(SDCLKH-BEIV)$ Output hold time, $\overline{BEx}$ invalid after SDCLK high     | 0.5P – 1.9 |     | 0.5P – 1.5             |     | ns   |
| 5   | $t_{osu}(EAV-SDCLKH)$ Output setup time, EAx valid before SDCLK high                  | 1.5P – 4   |     | 1.5P – 4               |     | ns   |
| 6   | $t_{oh}(SDCLKH-EAIV)$ Output hold time, EAx invalid after SDCLK high                  | 0.5P – 1.9 |     | 0.5P – 1.5             |     | ns   |
| 9   | $t_{osu}(SDCAS-SDCLKH)$ Output setup time, $\overline{SDCAS}$ valid before SDCLK high | 1.5P – 4   |     | 1.5P – 4               |     | ns   |
| 10  | $t_{oh}(SDCLKH-SDCAS)$ Output hold time, $\overline{SDCAS}$ valid after SDCLK high    | 0.5P – 1.9 |     | 0.5P – 1.5             |     | ns   |
| 11  | $t_{osu}(EDV-SDCLKH)$ Output setup time, EDx valid before SDCLK high                  | 1.5P – 4   |     | 1.5P – 4               |     | ns   |
| 12  | $t_{oh}(SDCLKH-EDIV)$ Output hold time, EDx invalid after SDCLK high                  | 0.5P – 1.9 |     | 0.5P – 1.5             |     | ns   |
| 13  | $t_{osu}(SDWE-SDCLKH)$ Output setup time, $\overline{SDWE}$ valid before SDCLK high   | 1.5P – 4   |     | 1.5P – 4               |     | ns   |
| 14  | $t_{oh}(SDCLKH-SDWE)$ Output hold time, $\overline{SDWE}$ valid after SDCLK high      | 0.5P – 1.9 |     | 0.5P – 1.5             |     | ns   |
| 15  | $t_{osu}(SDA10V-SDCLKH)$ Output setup time, SDA10 valid before SDCLK high             | 1.5P – 4   |     | 1.5P – 4               |     | ns   |
| 16  | $t_{oh}(SDCLKH-SDA10V)$ Output hold time, SDA10 invalid after SDCLK high              | 0.5P – 1.9 |     | 0.5P – 1.5             |     | ns   |
| 17  | $t_{osu}(SDRAS-SDCLKH)$ Output setup time, $\overline{SDRAS}$ valid before SDCLK high | 1.5P – 4   |     | 1.5P – 4               |     | ns   |
| 18  | $t_{oh}(SDCLKH-SDRAS)$ Output hold time, $\overline{SDRAS}$ valid after SDCLK high    | 0.5P – 1.9 |     | 0.5P – 1.5             |     | ns   |

<sup>†</sup> When the PLL is used (CLKMODE x4), P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.  
For CLKMODE x1:

1.5P = P + PH, where P = 1/CPU clock frequency, and PH = pulse duration of CLKIN high.

0.5P = PL, where PL = pulse duration of CLKIN low.

# TMS320C6701 FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## SYNCHRONOUS DRAM TIMING (CONTINUED)

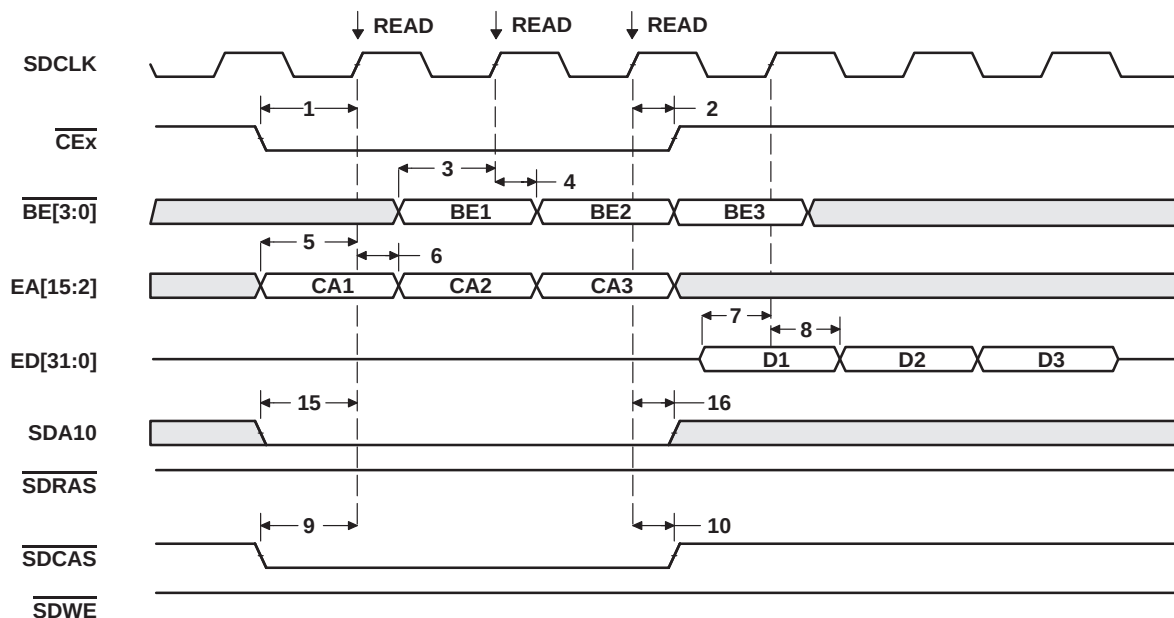


Figure 20. Three SDRAM Read Commands

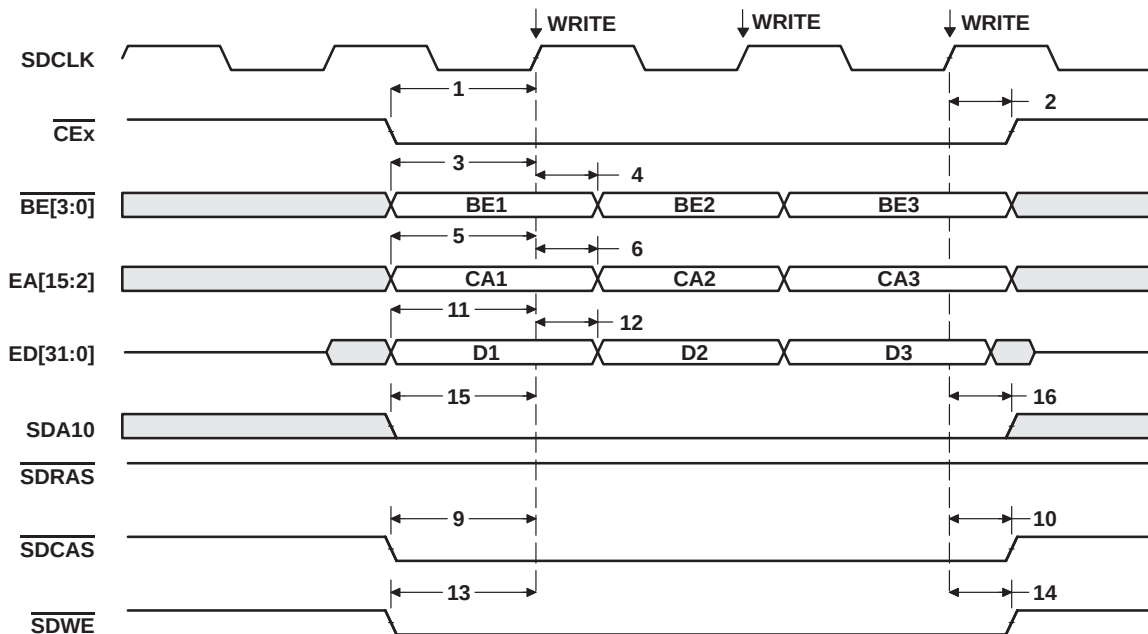


Figure 21. Three SDRAM Write Commands

### SYNCHRONOUS DRAM TIMING (CONTINUED)

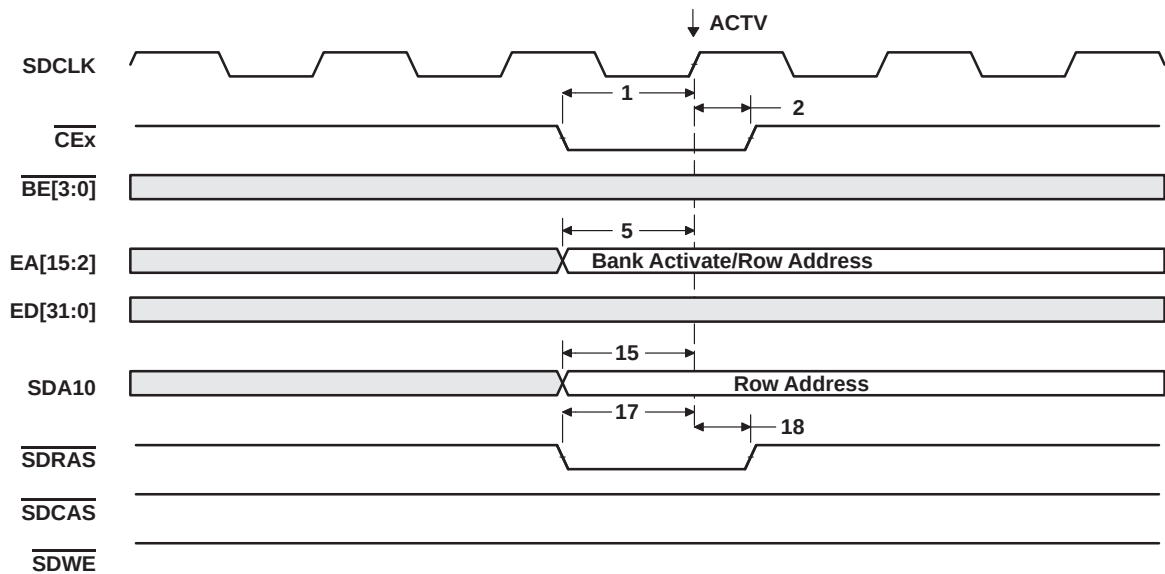


Figure 22. SDRAM ACTV Command

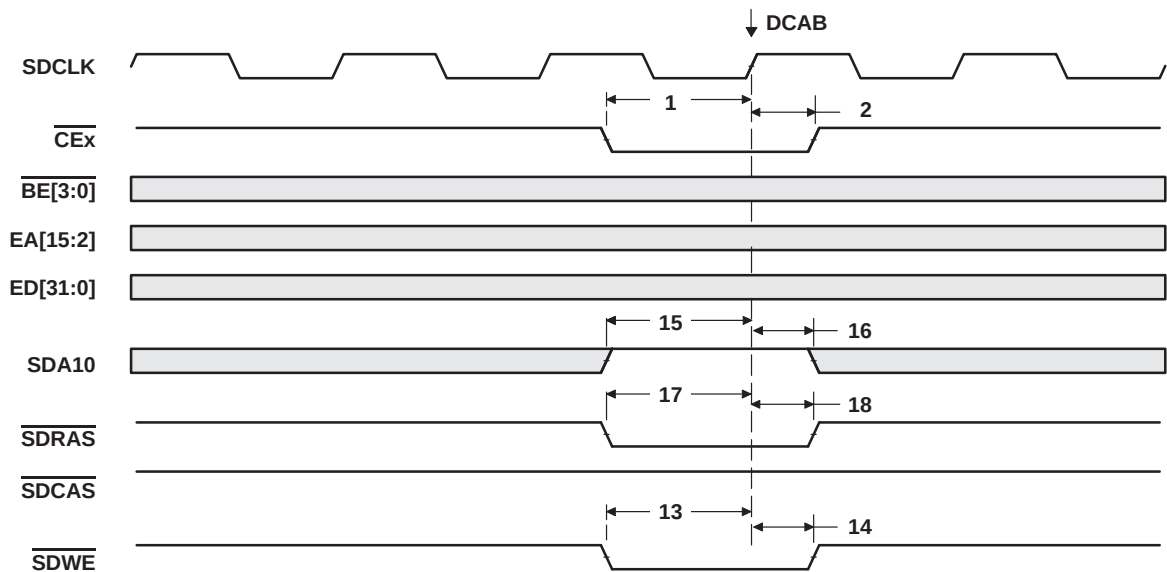
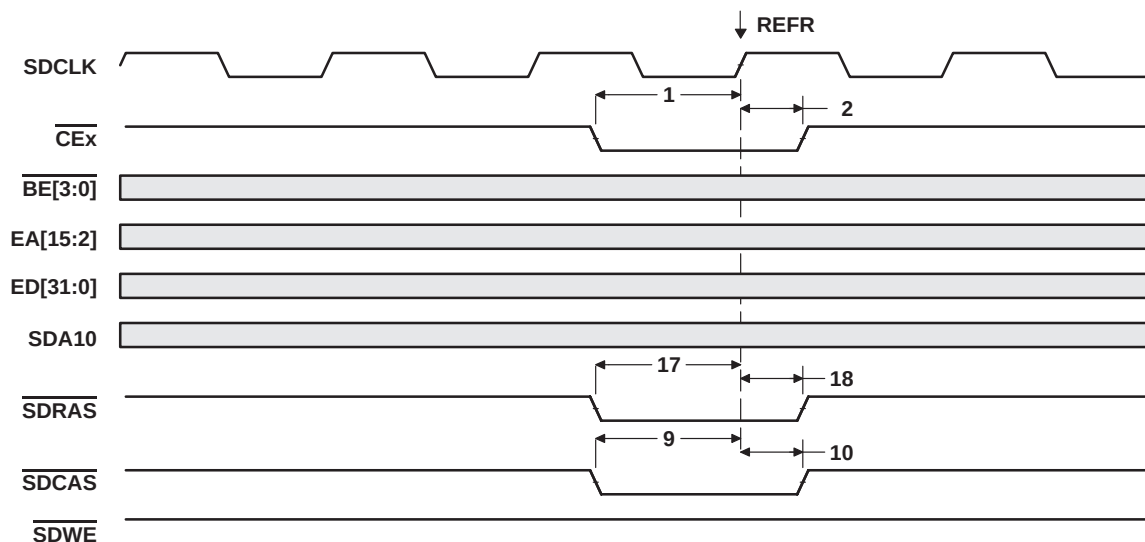
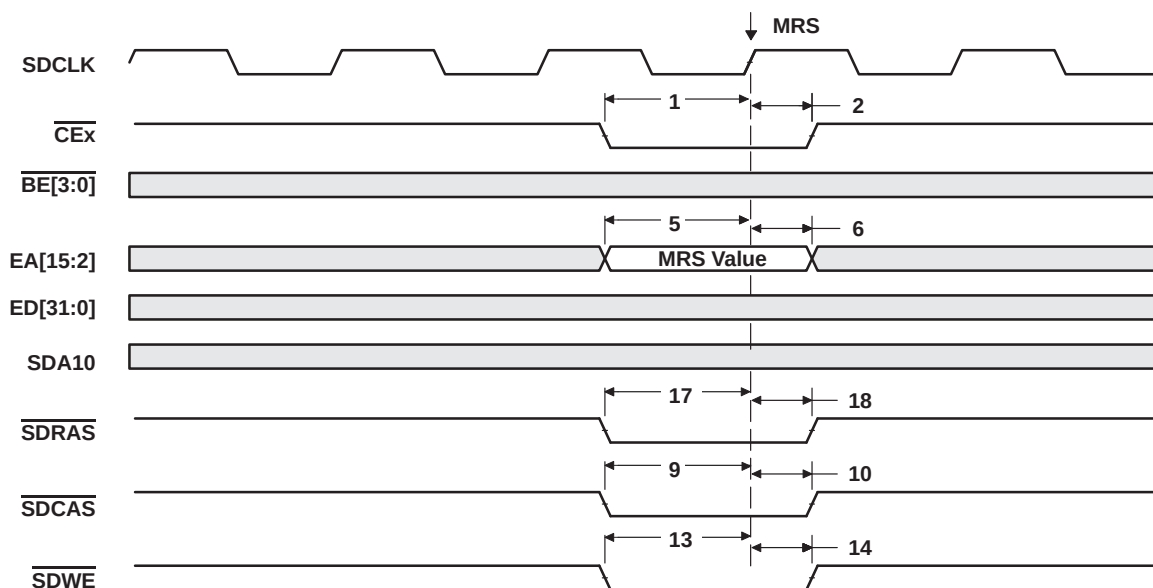


Figure 23. SDRAM DCAB Command

**SYNCHRONOUS DRAM TIMING (CONTINUED)**



**Figure 24. SDRAM REFR Command**



**Figure 25. SDRAM MRS Command**

## HOLD/HOLDA TIMING

timing requirements for the hold/hold acknowledge cycles<sup>†</sup> (see Figure 26)

| NO. |                                                                                            | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|--------------------------------------------------------------------------------------------|-------------------------------------|------|
|     |                                                                                            | MIN MAX                             |      |
| 1   | $t_{su}(\text{HOLDH-CKO1H})$ Setup time, $\overline{\text{HOLD}}$ high before CLKOUT1 high | 5                                   | ns   |
| 2   | $t_h(\text{CKO1H-HOLDL})$ Hold time, $\overline{\text{HOLD}}$ low after CLKOUT1 high       | 2                                   | ns   |

<sup>†</sup> HOLD is synchronized internally. Therefore, if setup and hold times are not met, it will either be recognized in the current cycle or in the next cycle. Thus, HOLD can be an asynchronous input.

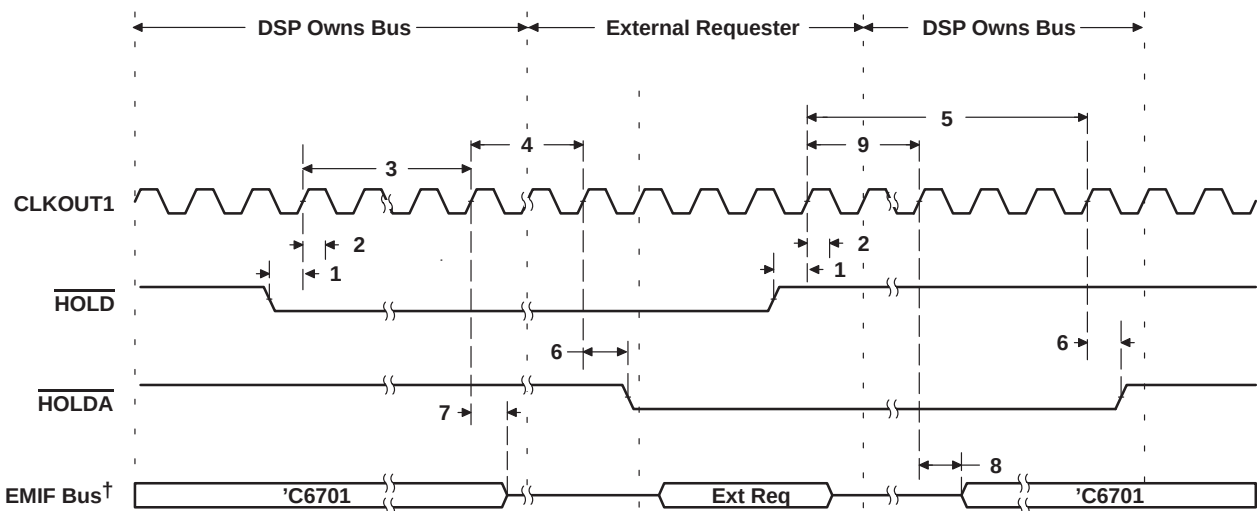
switching characteristics for the hold/hold acknowledge cycles<sup>‡</sup> (see Figure 26)

| NO. | PARAMETER                                                                                                   | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|-------------------------------------------------------------------------------------------------------------|-------------------------------------|------|
|     |                                                                                                             | MIN MAX                             |      |
| 3   | $t_R(\text{HOLDL-EMHZ})$ Response time, $\overline{\text{HOLD}}$ low to EMIF high impedance                 | 4P                                  | ns   |
| 4   | $t_R(\text{EMHZ-HOLDAL})$ Response time, EMIF high impedance to $\overline{\text{HOLDA}}$ low               | 2P                                  | ns   |
| 5   | $t_R(\text{HOLDH-HOLDAH})$ Response time, $\overline{\text{HOLD}}$ high to $\overline{\text{HOLDA}}$ high   | 4P                                  | ns   |
| 6   | $t_d(\text{CKO1H-HOLDAL})$ Delay time, CLKOUT1 high to $\overline{\text{HOLDA}}$ valid                      | 1 8                                 | ns   |
| 7   | $t_d(\text{CKO1H-BHZ})$ Delay time, CLKOUT1 high to EMIF Bus high impedance <sup>¶</sup>                    | 1 8                                 | ns   |
| 8   | $t_d(\text{CKO1H-BLZ})$ Delay time, CLKOUT1 high to EMIF Bus low impedance <sup>¶</sup>                     | 1 12                                | ns   |
| 9   | $t_R(\text{HOLDH-BLZ})$ Response time, $\overline{\text{HOLD}}$ high to EMIF Bus low impedance <sup>¶</sup> | 3P                                  | ns   |

<sup>‡</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

<sup>§</sup> All pending EMIF transactions are allowed to complete before  $\overline{\text{HOLDA}}$  is asserted. The worst cases for this is an asynchronous read or write with external ARDY used or a minimum of eight consecutive SDRAM reads or writes when RBTR8 = 1. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting the NOHOLD = 1.

<sup>¶</sup> EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE, AOE, AWE, SSADS, SSOE, SSWE, SDA10, SDRAS, SDCAS, and SDWE.



<sup>†</sup> EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE, AOE, AWE, SSADS, SSOE, SSWE, SDA10, SDRAS, SDCAS, and SDWE.

**Figure 26. HOLD/HOLDA Timing**

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### RESET TIMING

#### timing requirements for reset (see Figure 27)

| NO. |                     |                                                                                  | C6701-120<br>C6701-150<br>C6701-167 | UNIT           |
|-----|---------------------|----------------------------------------------------------------------------------|-------------------------------------|----------------|
|     |                     |                                                                                  | MIN MAX                             |                |
| 1   | $t_W(\text{RESET})$ | Width of the $\overline{\text{RESET}}$ pulse (PLL stable) <sup>†</sup>           | 10                                  | CLKOUT1 cycles |
|     |                     | Width of the $\overline{\text{RESET}}$ pulse (PLL needs to sync up) <sup>‡</sup> | 250                                 | μs             |

<sup>†</sup> This parameter applies to CLKMODE x1 when CLKIN is stable and applies to CLKMODE x4 when CLKIN and PLL are stable.

<sup>‡</sup> This parameter only applies to CLKMODE x4. The  $\overline{\text{RESET}}$  signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 μs to stabilize following device powerup or after PLL configuration has been changed. During that time,  $\overline{\text{RESET}}$  must be asserted to ensure proper device operation. See the *clock PLL* section for PLL lock times.

#### switching characteristics during reset<sup>§</sup> (see Figure 27)

| NO. | PARAMETER                                                                                | C6701-120<br>C6701-150<br>C6701-167 | UNIT           |
|-----|------------------------------------------------------------------------------------------|-------------------------------------|----------------|
|     |                                                                                          | MIN MAX                             |                |
| 2   | $t_R(\text{RESET})$ Response time to change of value in $\overline{\text{RESET}}$ signal | 1                                   | CLKOUT1 cycles |
| 3   | $t_d(\text{CKO1H-CKO2IV})$ Delay time, CLKOUT1 high to CLKOUT2 invalid                   | -1                                  | ns             |
| 4   | $t_d(\text{CKO1H-CKO2V})$ Delay time, CLKOUT1 high to CLKOUT2 valid                      | 10                                  | ns             |
| 5   | $t_d(\text{CKO1H-SDCLKIV})$ Delay time, CLKOUT1 high to SDCLK invalid                    | -1                                  | ns             |
| 6   | $t_d(\text{CKO1H-SDCLKV})$ Delay time, CLKOUT1 high to SDCLK valid                       | 10                                  | ns             |
| 7   | $t_d(\text{CKO1H-SSCKIV})$ Delay time, CLKOUT1 high to SSCLK invalid                     | -1                                  | ns             |
| 8   | $t_d(\text{CKO1H-SSCKV})$ Delay time, CLKOUT1 high to SSCLK valid                        | 10                                  | ns             |
| 9   | $t_d(\text{CKO1H-LOWIV})$ Delay time, CLKOUT1 high to low group invalid                  | -1                                  | ns             |
| 10  | $t_d(\text{CKO1H-LOWV})$ Delay time, CLKOUT1 high to low group valid                     | 10                                  | ns             |
| 11  | $t_d(\text{CKO1H-HIGHIV})$ Delay time, CLKOUT1 high to high group invalid                | -1                                  | ns             |
| 12  | $t_d(\text{CKO1H-HIGHV})$ Delay time, CLKOUT1 high to high group valid                   | 10                                  | ns             |
| 13  | $t_d(\text{CKO1H-ZHZ})$ Delay time, CLKOUT1 high to Z group high impedance               | -1                                  | ns             |
| 14  | $t_d(\text{CKO1H-ZV})$ Delay time, CLKOUT1 high to Z group valid                         | 10                                  | ns             |

<sup>§</sup> Low group consists of:  $\overline{\text{IACK}}$ ,  $\text{INUM}[3:0]$ ,  $\text{DMAC}[3:0]$ ,  $\text{PD}$ ,  $\text{TOUT0}$ , and  $\text{TOUT1}$ .

High group consists of:  $\text{HINT}$ .

Z group consists of:  $\text{EA}[21:2]$ ,  $\text{ED}[31:0]$ ,  $\text{CE}[3:0]$ ,  $\text{BE}[3:0]$ ,  $\text{ARE}$ ,  $\text{AWE}$ ,  $\text{AOE}$ ,  $\text{SSADS}$ ,  $\text{SSOE}$ ,  $\text{SSWE}$ ,  $\text{SDA10}$ ,  $\text{SDRAS}$ ,  $\text{SDCAS}$ ,  $\text{SDWE}$ ,  $\text{HD}[15:0]$ ,  $\text{CLKX0}$ ,  $\text{CLKX1}$ ,  $\text{FSX0}$ ,  $\text{FSX1}$ ,  $\text{DX0}$ ,  $\text{DX1}$ ,  $\text{CLKR0}$ ,  $\text{CLKR1}$ ,  $\text{FSR0}$ , and  $\text{FSR1}$ .

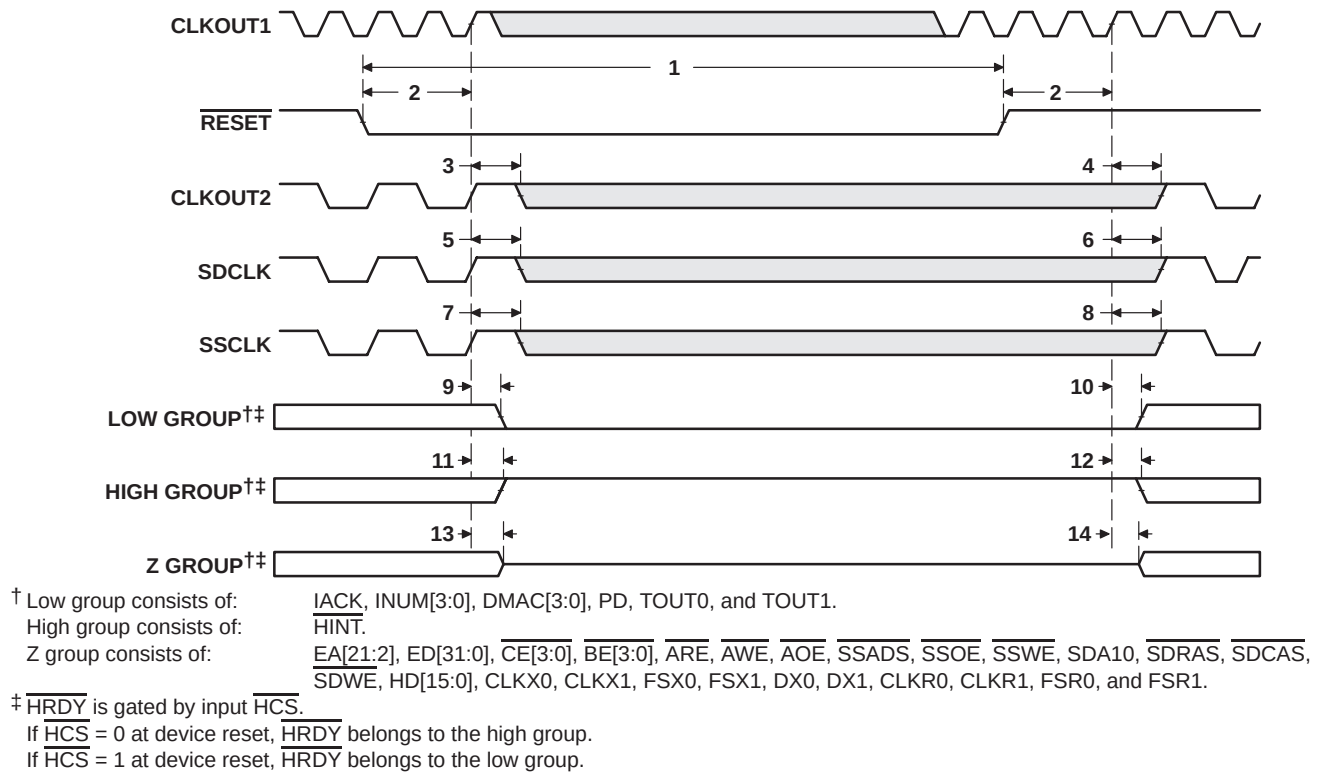
<sup>¶</sup>  $\text{HRDY}$  is gated by input  $\overline{\text{HCS}}$ .

If  $\overline{\text{HCS}} = 0$  at device reset,  $\text{HRDY}$  belongs to the high group.

If  $\overline{\text{HCS}} = 1$  at device reset,  $\text{HRDY}$  belongs to the low group.



### RESET TIMING (CONTINUED)



**Figure 27. Reset Timing**

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### EXTERNAL INTERRUPT TIMING

timing requirements for interrupt response cycles<sup>†‡</sup> (see Figure 28)

| NO. |                                                  | C6701-120<br>C6701-150<br>C6701-167 |     | UNIT |
|-----|--------------------------------------------------|-------------------------------------|-----|------|
|     |                                                  | MIN                                 | MAX |      |
| 2   | $t_{w(ILOW)}$ Width of the interrupt pulse low   | 2P                                  |     | ns   |
| 3   | $t_{w(IHIGH)}$ Width of the interrupt pulse high | 2P                                  |     | ns   |

<sup>†</sup> Interrupt signals are synchronized internally and are potentially recognized one cycle later if setup and hold times are violated. Thus, they can be connected to asynchronous inputs.

<sup>‡</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

switching characteristics during interrupt response cycles<sup>§</sup> (see Figure 28)

| NO. | PARAMETER                                                      | C6701-120<br>C6701-150<br>C6701-167 |           | UNIT |
|-----|----------------------------------------------------------------|-------------------------------------|-----------|------|
|     |                                                                | MIN                                 | MAX       |      |
| 1   | $t_{R(EINTH-IACKH)}$ Response time, EXT_INTx high to IACK high | 9P                                  |           | ns   |
| 4   | $t_{d(CKO2L-IACKV)}$ Delay time, CLKOUT2 low to IACK valid     | -0.5P                               | 13 - 0.5P | ns   |
| 5   | $t_{d(CKO2L-INUMV)}$ Delay time, CLKOUT2 low to INUMx valid    |                                     | 10 - 0.5P | ns   |
| 6   | $t_{d(CKO2L-INUMIV)}$ Delay time, CLKOUT2 low to INUMx invalid | -0.5P                               |           | ns   |

<sup>§</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

When the PLL is used (CLKMODE x4), 0.5P = 1/(2 × CPU clock frequency).

For CLKMODE x1: 0.5P = PH, where PH is the high period of CLKIN.

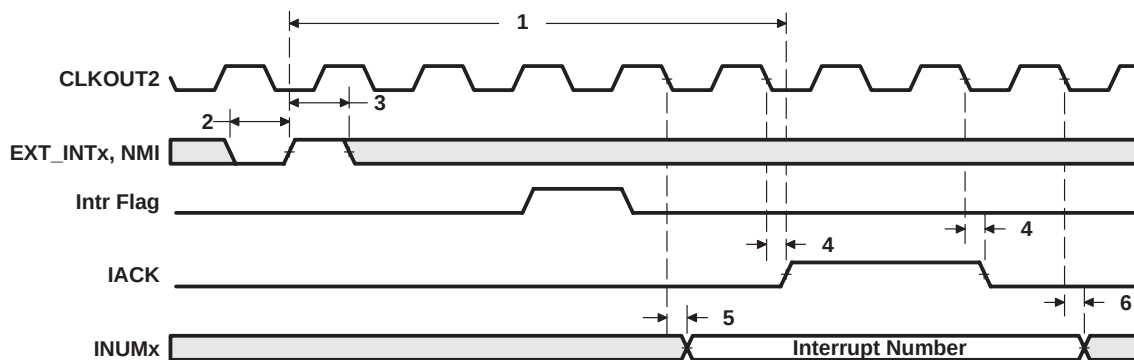


Figure 28. Interrupt Timing



## HOST-PORT INTERFACE TIMING

**timing requirements for host-port interface cycles<sup>†‡</sup> (see Figure 29, Figure 30, Figure 31, and Figure 32)**

| NO. |                             |                                                                                                                                                                                                                                        | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|------|
|     |                             |                                                                                                                                                                                                                                        | MIN MAX                             |      |
| 1   | $t_{su}(\text{SEL-HSTBL})$  | Setup time, select signals <sup>§</sup> valid before $\overline{\text{HSTROBE}}$ low                                                                                                                                                   | 4                                   | ns   |
| 2   | $t_h(\text{HSTBL-SEL})$     | Hold time, select signals <sup>§</sup> valid after $\overline{\text{HSTROBE}}$ low                                                                                                                                                     | 2                                   | ns   |
| 3   | $t_w(\text{HSTBL})$         | Pulse duration, $\overline{\text{HSTROBE}}$ low                                                                                                                                                                                        | 2P                                  | ns   |
| 4   | $t_w(\text{HSTBH})$         | Pulse duration, $\overline{\text{HSTROBE}}$ high between consecutive accesses                                                                                                                                                          | 2P                                  | ns   |
| 10  | $t_{su}(\text{SEL-HASL})$   | Setup time, select signals <sup>§</sup> valid before $\overline{\text{HAS}}$ low                                                                                                                                                       | 4                                   | ns   |
| 11  | $t_h(\text{HASL-SEL})$      | Hold time, select signals <sup>§</sup> valid after $\overline{\text{HAS}}$ low                                                                                                                                                         | 2                                   | ns   |
| 12  | $t_{su}(\text{HDV-HSTBH})$  | Setup time, host data valid before $\overline{\text{HSTROBE}}$ high                                                                                                                                                                    | 3                                   | ns   |
| 13  | $t_h(\text{HSTBH-HDV})$     | Hold time, host data valid after $\overline{\text{HSTROBE}}$ high                                                                                                                                                                      | 2                                   | ns   |
| 14  | $t_h(\text{HRDYL-HSTBL})$   | Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be inactivated until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly. | 1                                   | ns   |
| 18  | $t_{su}(\text{HASL-HSTBL})$ | Setup time, $\overline{\text{HAS}}$ low before $\overline{\text{HSTROBE}}$ low                                                                                                                                                         | 2                                   | ns   |
| 19  | $t_h(\text{HSTBL-HASL})$    | Hold time, $\overline{\text{HAS}}$ low after $\overline{\text{HSTROBE}}$ low                                                                                                                                                           | 2                                   | ns   |

<sup>†</sup>  $\overline{\text{HSTROBE}}$  refers to the following logical operation on  $\overline{\text{HCS}}$ ,  $\overline{\text{HDS1}}$ , and  $\overline{\text{HDS2}}$ :  $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$ .

<sup>‡</sup>  $P = 1/\text{CPU clock frequency}$  in ns. For example, when running parts at 167 MHz, use  $P = 6$  ns.

<sup>§</sup> Select signals include:  $\overline{\text{HCNTRL}}[1:0]$ ,  $\overline{\text{HR/W}}$ , and  $\overline{\text{HHWIL}}$ .

**switching characteristics during host-port interface cycles<sup>†‡</sup> (see Figure 29, Figure 30, Figure 31, and Figure 32)**

| NO. | PARAMETER                  |                                                                                             | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|----------------------------|---------------------------------------------------------------------------------------------|-------------------------------------|------|
|     |                            |                                                                                             | MIN MAX                             |      |
| 5   | $t_d(\text{HCS-HRDY})$     | Delay time, $\overline{\text{HCS}}$ to $\overline{\text{HRDY}}^{\text{¶}}$                  | 1 12                                | ns   |
| 6   | $t_d(\text{HSTBL-HRDYH})$  | Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ high <sup>#</sup>   | 1 12                                | ns   |
| 7   | $t_d(\text{HSTBL-HDLZ})$   | Delay time, $\overline{\text{HSTROBE}}$ low to HD low impedance for an HPI read             | 4                                   | ns   |
| 8   | $t_d(\text{HDV-HRDYL})$    | Delay time, HD valid to $\overline{\text{HRDY}}$ low                                        | $P - 3$ $P + 3$                     | ns   |
| 9   | $t_{oh}(\text{HSTBH-HDV})$ | Output hold time, HD valid after $\overline{\text{HSTROBE}}$ high                           | 3 12                                | ns   |
| 15  | $t_d(\text{HSTBH-HDHZ})$   | Delay time, $\overline{\text{HSTROBE}}$ high to HD high impedance                           | 3 12                                | ns   |
| 16  | $t_d(\text{HSTBL-HDV})$    | Delay time, $\overline{\text{HSTROBE}}$ low to HD valid                                     | 3 12                                | ns   |
| 17  | $t_d(\text{HSTBH-HRDYH})$  | Delay time, $\overline{\text{HSTROBE}}$ high to $\overline{\text{HRDY}}$ high <sup>¶¶</sup> | 1 12                                | ns   |
| 20  | $t_d(\text{HASL-HRDYH})$   | Delay time, $\overline{\text{HAS}}$ low to $\overline{\text{HRDY}}$ high                    | 3 12                                | ns   |

<sup>†</sup>  $\overline{\text{HSTROBE}}$  refers to the following logical operation on  $\overline{\text{HCS}}$ ,  $\overline{\text{HDS1}}$ , and  $\overline{\text{HDS2}}$ :  $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$ .

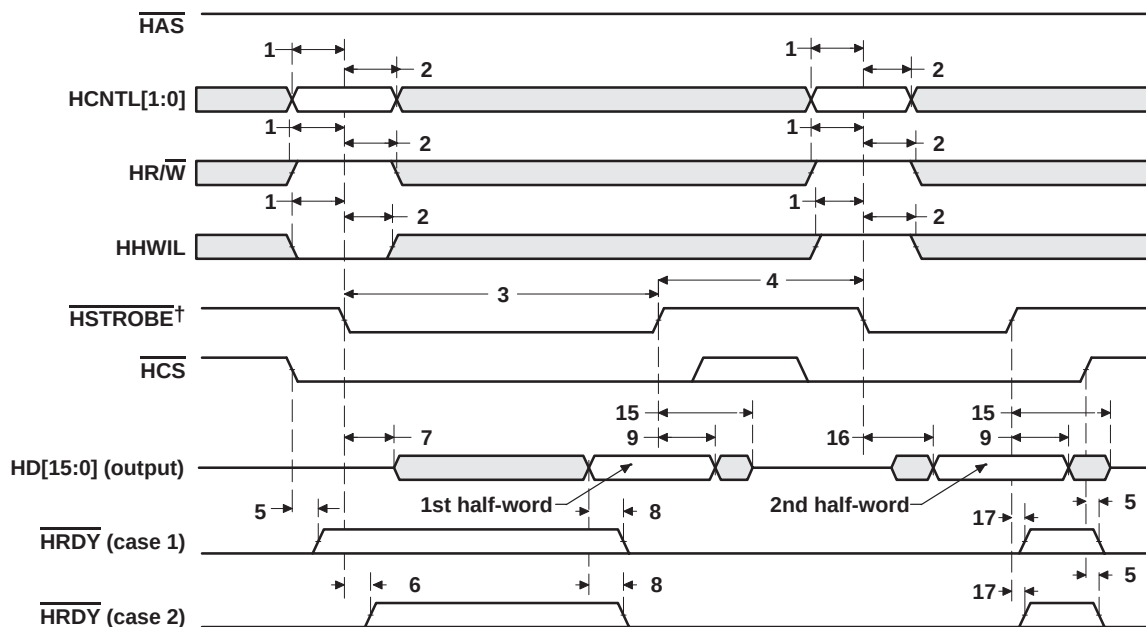
<sup>‡</sup>  $P = 1/\text{CPU clock frequency}$  in ns. For example, when running parts at 167 MHz, use  $P = 6$  ns.

<sup>¶</sup>  $\overline{\text{HCS}}$  enables  $\overline{\text{HRDY}}$ , and  $\overline{\text{HRDY}}$  is always low when  $\overline{\text{HCS}}$  is high. The case where  $\overline{\text{HRDY}}$  goes high when  $\overline{\text{HCS}}$  falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.

<sup>#</sup> This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of  $\overline{\text{HSTROBE}}$ , the HPI sends the request to the DMA auxiliary channel, and  $\overline{\text{HRDY}}$  remains high until the DMA auxiliary channel loads the requested data into HPID.

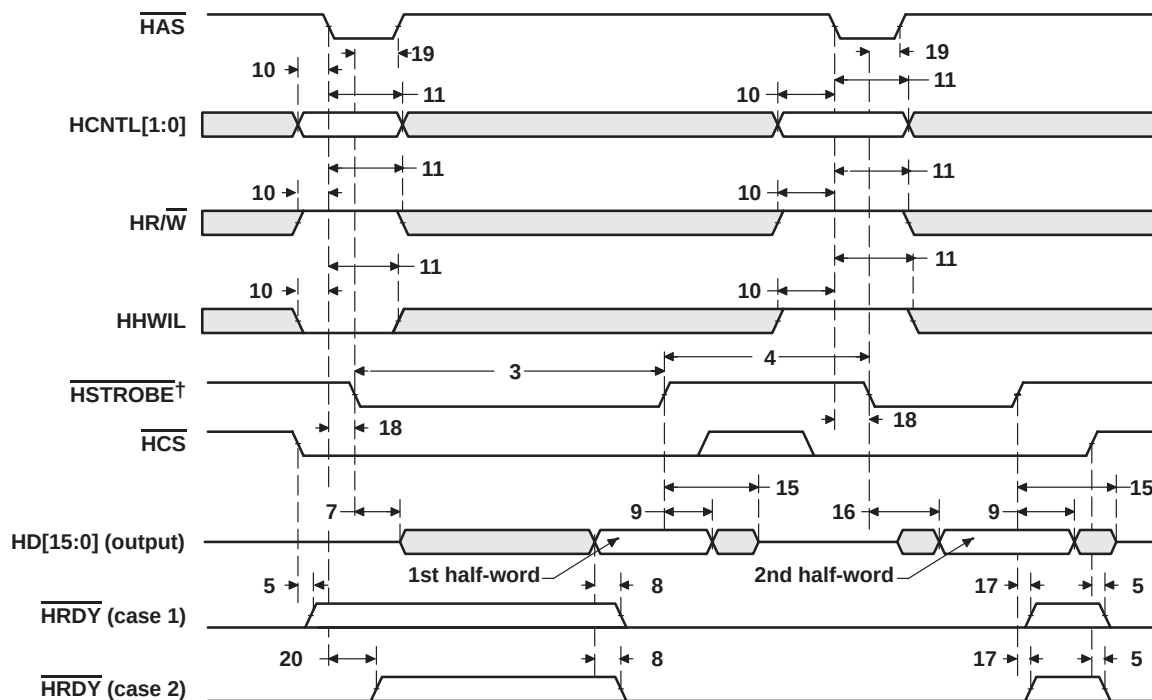
<sup>¶¶</sup> This parameter is used after the second half-word of an HPID write or autoincrement read.  $\overline{\text{HRDY}}$  remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the  $\overline{\text{HRDY}}$  signal.

**HOST-PORT INTERFACE TIMING (CONTINUED)**



† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2:  $[\text{NOT}(\text{HDS1 XOR HDS2})] \text{ OR HCS}$ .

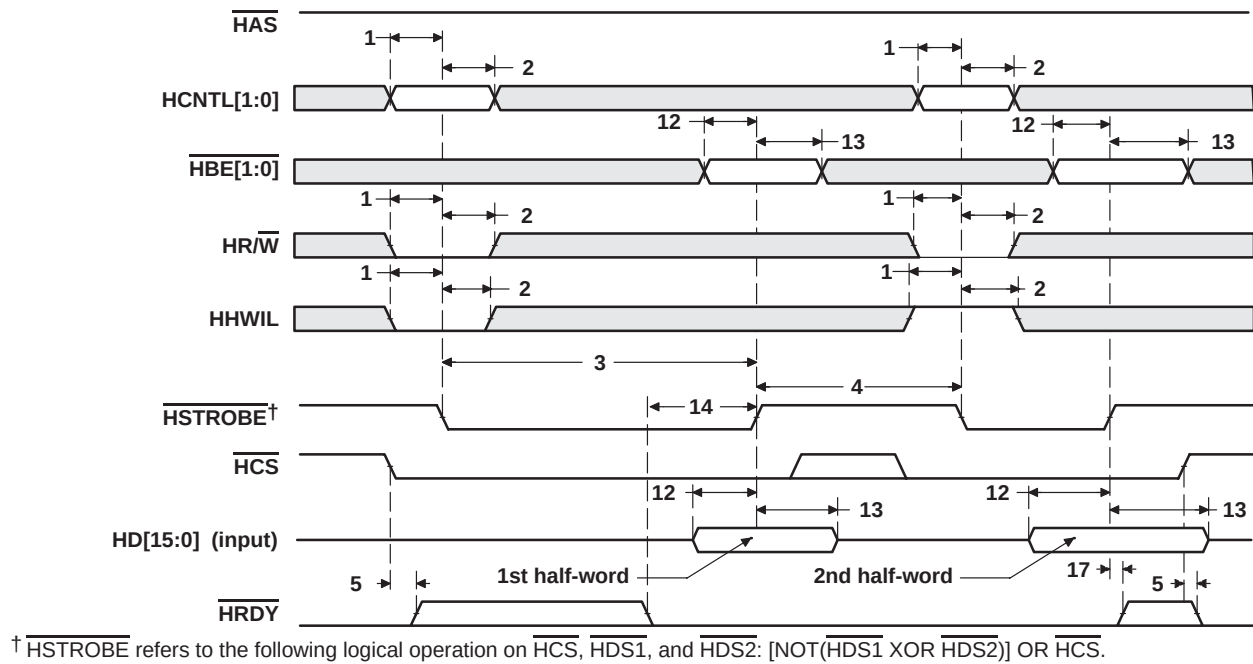
**Figure 29. HPI Read Timing ( $\overline{\text{HAS}}$  Not Used, Tied High)**



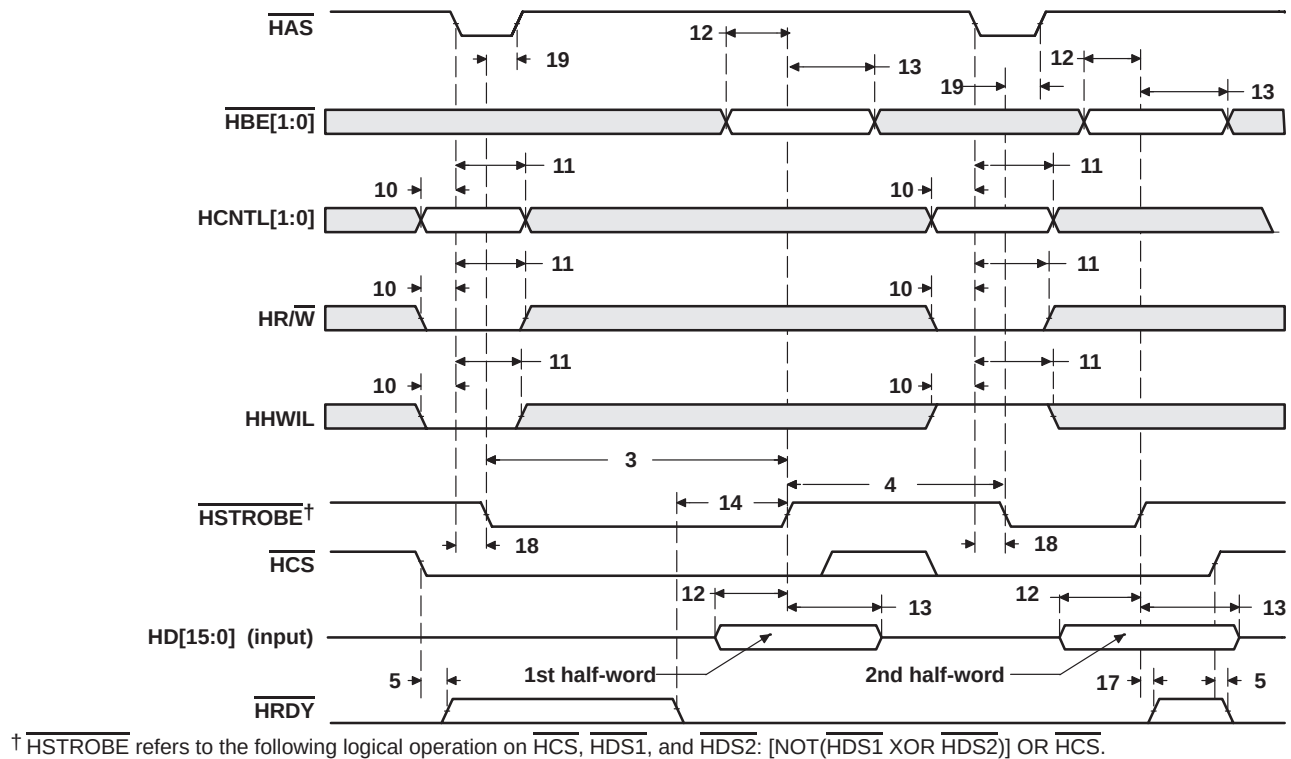
† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2:  $[\text{NOT}(\text{HDS1 XOR HDS2})] \text{ OR HCS}$ .

**Figure 30. HPI Read Timing ( $\overline{\text{HAS}}$  Used)**

### HOST-PORT INTERFACE TIMING (CONTINUED)



**Figure 31. HPI Write Timing ( $\overline{\text{HAS}}$  Not Used, Tied High)**



**Figure 32. HPI Write Timing ( $\overline{\text{HAS}}$  Used)**

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### MULTICHANNEL BUFFERED SERIAL PORT TIMING

timing requirements for McBSP<sup>†‡</sup> (see Figure 33)

| NO. |                           |                                               |            | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|---------------------------|-----------------------------------------------|------------|-------------------------------------|------|
|     |                           |                                               |            | MIN MAX                             |      |
| 2   | $t_c(\text{CKRX})$        | Cycle time, CLKR/X                            | CLKR/X ext | $2P^{\S}$                           | ns   |
| 3   | $t_w(\text{CKRX})$        | Pulse duration, CLKR/X high or CLKR/X low     | CLKR/X ext | $P - 1^{\parallel}$                 | ns   |
| 5   | $t_{su}(\text{FRH-CKRL})$ | Setup time, external FSR high before CLKR low | CLKR int   | 13                                  | ns   |
|     |                           |                                               | CLKR ext   | 4                                   |      |
| 6   | $t_h(\text{CKRL-FRH})$    | Hold time, external FSR high after CLKR low   | CLKR int   | 7                                   | ns   |
|     |                           |                                               | CLKR ext   | 4                                   |      |
| 7   | $t_{su}(\text{DRV-CKRL})$ | Setup time, DR valid before CLKR low          | CLKR int   | 10                                  | ns   |
|     |                           |                                               | CLKR ext   | 1                                   |      |
| 8   | $t_h(\text{CKRL-DRV})$    | Hold time, DR valid after CLKR low            | CLKR int   | 4                                   | ns   |
|     |                           |                                               | CLKR ext   | 4                                   |      |
| 10  | $t_{su}(\text{FXH-CKXL})$ | Setup time, external FSX high before CLKX low | CLKX int   | 13                                  | ns   |
|     |                           |                                               | CLKX ext   | 4                                   |      |
| 11  | $t_h(\text{CKXL-FXH})$    | Hold time, external FSX high after CLKX low   | CLKX int   | 7                                   | ns   |
|     |                           |                                               | CLKX ext   | 3                                   |      |

<sup>†</sup>  $P = 1/\text{CPU clock frequency}$  in ns. For example, when running parts at 167 MHz, use  $P = 6$  ns.

<sup>‡</sup>  $\text{CLKRP} = \text{CLKXP} = \text{FSRP} = \text{FSXP} = 0$ . If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

<sup>§</sup> The maximum McBSP bit rate is 50 MHz; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time ( $2P$ ), or 20 ns (50 MHz), whichever value is larger. For example, when running parts at 167 MHz ( $P = 6$  ns), use 20 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 80 MHz ( $P = 12.5$  ns), use  $2P = 25$  ns (40 MHz) as the minimum CLKR/X clock cycle. The maximum McBSP bit rate applies when the serial port is a master of clock and frame syncs and the other device the McBSP communicates to is a slave.

<sup>||</sup> The minimum CLKR/X pulse duration is either  $(P - 1)$  or 9 ns, whichever is larger. For example, when running parts at 167 MHz ( $P = 6$  ns), use 9 ns as the minimum CLKR/X pulse duration. When running parts at 80 MHz ( $P = 12.5$  ns), use  $(P - 1) = 11.5$  ns as the minimum CLKR/X pulse duration.



## MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

### switching characteristics for McBSP<sup>†‡</sup> (see Figure 33)

| NO. | PARAMETER                    |                                                                                           |            | C6701-120<br>C6701-150<br>C6701-167 |                    | UNIT |
|-----|------------------------------|-------------------------------------------------------------------------------------------|------------|-------------------------------------|--------------------|------|
|     |                              |                                                                                           |            | MIN                                 | MAX                |      |
| 1   | t <sub>d</sub> (CKSH-CKRXH)  | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input        |            | 3                                   | 15                 | ns   |
| 2   | t <sub>c</sub> (CKRX)        | Cycle time, CLKR/X                                                                        | CLKR/X int | 2P <sup>§</sup> ¶                   |                    | ns   |
| 3   | t <sub>w</sub> (CKRX)        | Pulse duration, CLKR/X high or CLKR/X low                                                 | CLKR/X int | C – 1 <sup>#</sup>                  | C + 1 <sup>#</sup> | ns   |
| 4   | t <sub>d</sub> (CKRH-FRV)    | Delay time, CLKR high to internal FSR valid                                               | CLKR int   | –4                                  | 4                  | ns   |
| 9   | t <sub>d</sub> (CKXH-FXV)    | Delay time, CLKX high to internal FSX valid                                               | CLKX int   | –4                                  | 5                  | ns   |
|     |                              |                                                                                           | CLKX ext   | 3                                   | 16                 |      |
| 12  | t <sub>dis</sub> (CKXH-DXHZ) | Disable time, DX high impedance following last data bit from CLKX high                    | CLKX int   | –3                                  | 2                  | ns   |
|     |                              |                                                                                           | CLKX ext   | 2                                   | 9                  |      |
| 13  | t <sub>d</sub> (CKXH-DXV)    | Delay time, CLKX high to DX valid.                                                        | CLKX int   | –2                                  | 4                  | ns   |
|     |                              |                                                                                           | CLKX ext   | 3                                   | 16                 |      |
| 14  | t <sub>d</sub> (FXH-DXV)     | Delay time, FSX high to DX valid. ONLY applies when in data delay 0 (XDATDLY = 00b) mode. | FSX int    | –2                                  | 4                  | ns   |
|     |                              |                                                                                           | FSX ext    | 2                                   | 10                 |      |

<sup>†</sup> CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

<sup>‡</sup> Minimum delay times also represent minimum output hold times.

<sup>§</sup>  $P = 1/\text{CPU clock frequency}$  in ns. For example, when running parts at 167 MHz, use  $P = 6$  ns.

<sup>¶</sup> The maximum McBSP bit rate is 50 MHz; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time ( $2P$ ), or 20 ns (50 MHz), whichever value is larger. For example, when running parts at 167 MHz ( $P = 6$  ns), use 20 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 80 MHz ( $P = 12.5$  ns), use  $2P = 25$  ns (40 MHz) as the minimum CLKR/X clock cycle. The maximum McBSP bit rate applies when the serial port is a master of clock and frame syncs and the other device the McBSP communicates to is a slave.

<sup>#</sup>  $C = H$  or  $L$

$S =$  sample rate generator input clock =  $P$  if  $\text{CLKSM} = 1$  ( $P = 1/\text{CPU clock frequency}$ )

$=$  sample rate generator input clock =  $P_{\text{clks}}$  if  $\text{CLKSM} = 0$  ( $P_{\text{clks}} = \text{CLKS period}$ )

$H =$  CLKX high pulse width =  $(\text{CLKGDV}/2 + 1) * S$  if CLKGDV is even

$= (\text{CLKGDV} + 1)/2 * S$  if CLKGDV is odd or zero

$L =$  CLKX low pulse width =  $(\text{CLKGDV}/2) * S$  if CLKGDV is even

$= (\text{CLKGDV} + 1)/2 * S$  if CLKGDV is odd or zero

CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the 50 MHz limit.

# TMS320C6701 FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

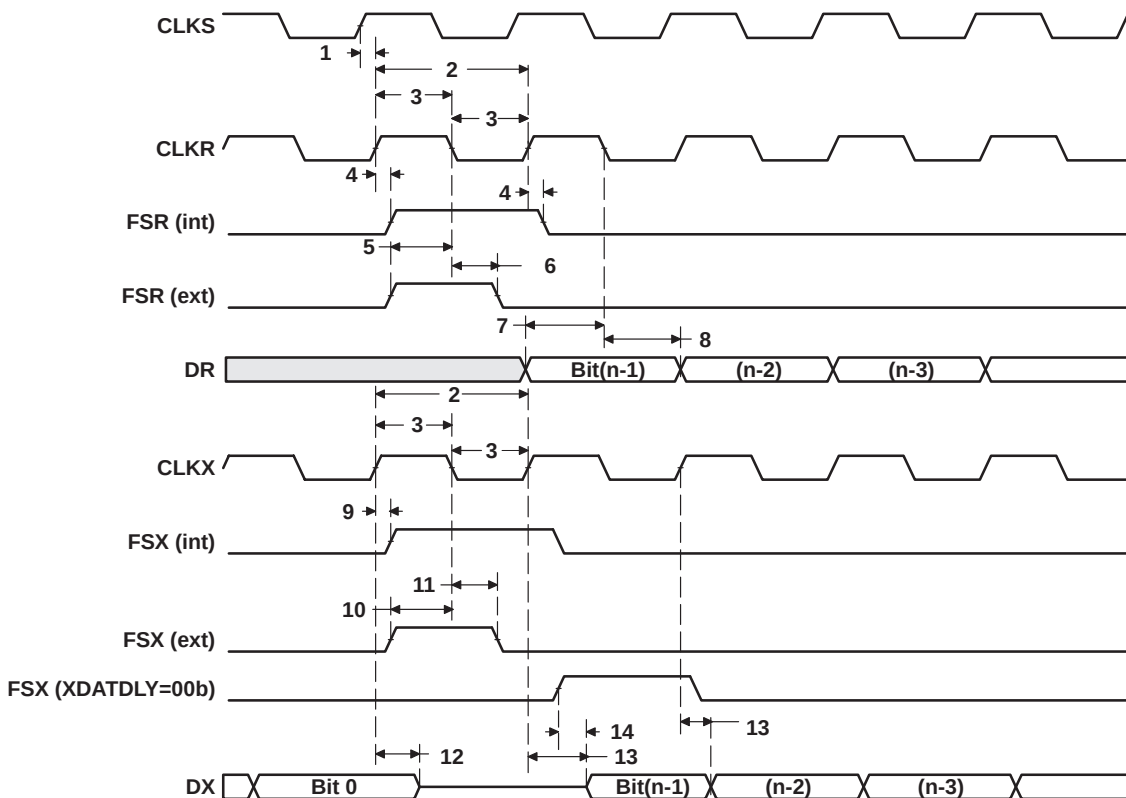
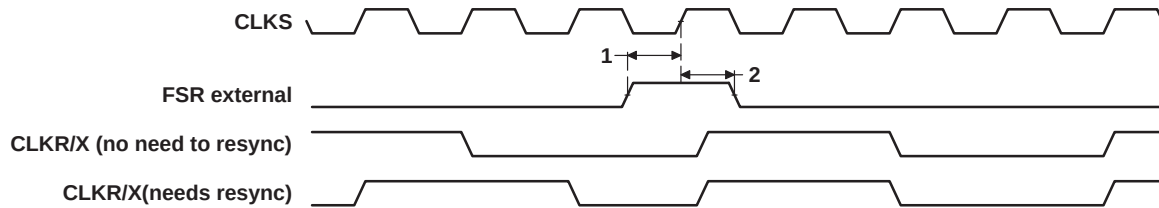


Figure 33. McBSP Timings

**MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)**

**timing requirements for FSR when GSYNC = 1 (see Figure 34)**

| NO. |                                                          | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|----------------------------------------------------------|-------------------------------------|------|
|     |                                                          | MIN    MAX                          |      |
| 1   | $t_{su}(FRH-CKSH)$ Setup time, FSR high before CLKS high | 4                                   | ns   |
| 2   | $t_h(CKSH-FRH)$ Hold time, FSR high after CLKS high      | 4                                   | ns   |



**Figure 34. FSR Timing When GSYNC = 1**

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0<sup>†‡</sup> (see Figure 35)

| NO. |                                                                 | C6701-120<br>C6701-150<br>C6701-167 |     |        |     | UNIT |
|-----|-----------------------------------------------------------------|-------------------------------------|-----|--------|-----|------|
|     |                                                                 | MASTER                              |     | SLAVE  |     |      |
|     |                                                                 | MIN                                 | MAX | MIN    | MAX |      |
| 4   | t <sub>su</sub> (DRV-CKXL) Setup time, DR valid before CLKX low | 12                                  |     | 2 – 3P |     | ns   |
| 5   | t <sub>h</sub> (CKXL-DRV) Hold time, DR valid after CLKX low    | 4                                   |     | 5 + 6P |     | ns   |

<sup>†</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

<sup>‡</sup> For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0<sup>†‡</sup> (see Figure 35)

| NO. | PARAMETER                    |                                                                       | C6701-120<br>C6701-150<br>C6701-167 |       |        |         | UNIT |
|-----|------------------------------|-----------------------------------------------------------------------|-------------------------------------|-------|--------|---------|------|
|     |                              |                                                                       | MASTER <sup>§</sup>                 |       | SLAVE  |         |      |
|     |                              |                                                                       | MIN                                 | MAX   | MIN    | MAX     |      |
| 1   | t <sub>h</sub> (CKXL-FXL)    | Hold time, FSX low after CLKX low <sup>¶</sup>                        | T – 4                               | T + 4 |        |         | ns   |
| 2   | t <sub>d</sub> (FXL-CKXH)    | Delay time, FSX low to CLKX high <sup>#</sup>                         | L – 4                               | L + 4 |        |         | ns   |
| 3   | t <sub>d</sub> (CKXH-DXV)    | Delay time, CLKX high to DX valid                                     | –4                                  | 4     | 3P + 1 | 5P + 17 | ns   |
| 6   | t <sub>dis</sub> (CKXL-DXHZ) | Disable time, DX high impedance following last data bit from CLKX low | L – 2                               | L + 3 |        |         | ns   |
| 7   | t <sub>dis</sub> (FXH-DXHZ)  | Disable time, DX high impedance following last data bit from FSX high |                                     |       | P + 4  | 3P + 17 | ns   |
| 8   | t <sub>d</sub> (FXL-DXV)     | Delay time, FSX low to DX valid                                       |                                     |       | 2P + 1 | 4P + 13 | ns   |

<sup>†</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

<sup>‡</sup> For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

<sup>§</sup> S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)

= sample rate generator input clock = P<sub>clks</sub> if CLKSM = 0 (P<sub>clks</sub> = CLKS period)

T = CLKX period = (1 + CLKGDV) \* S

H = CLKX high pulse width = (CLKGDV/2 + 1) \* S if CLKGDV is even

= (CLKGDV + 1)/2 \* S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) \* S if CLKGDV is even

= (CLKGDV + 1)/2 \* S if CLKGDV is odd or zero

<sup>¶</sup> FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

<sup>#</sup> FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).





**MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)**

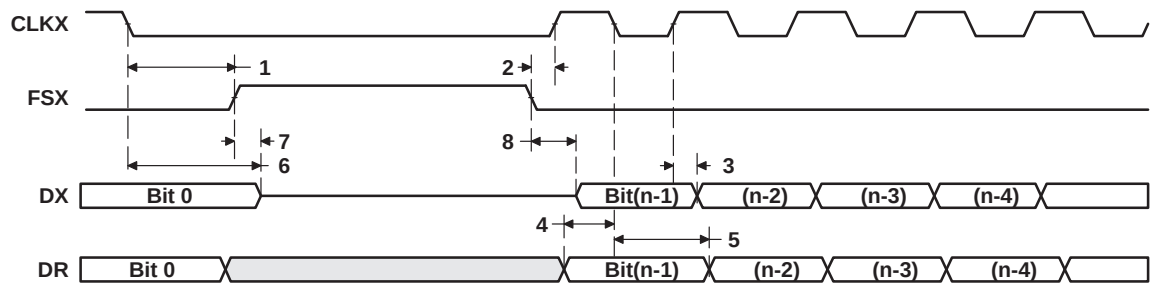


Figure 35. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

# TMS320C6701

## FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

### MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0<sup>†‡</sup> (see Figure 36)

| NO. |                                                                  | C6701-120<br>C6701-150<br>C6701-167 |     |        |     | UNIT |
|-----|------------------------------------------------------------------|-------------------------------------|-----|--------|-----|------|
|     |                                                                  | MASTER                              |     | SLAVE  |     |      |
|     |                                                                  | MIN                                 | MAX | MIN    | MAX |      |
| 4   | t <sub>su</sub> (DRV-CKXH) Setup time, DR valid before CLKX high | 12                                  |     | 2 – 3P |     | ns   |
| 5   | t <sub>h</sub> (CKXH-DRV) Hold time, DR valid after CLKX high    | 4                                   |     | 5 + 6P |     | ns   |

<sup>†</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

<sup>‡</sup> For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0<sup>†‡</sup> (see Figure 36)

| NO. | PARAMETER                    |                                                                       | C6701-120<br>C6701-150<br>C6701-167 |       |        |         | UNIT |
|-----|------------------------------|-----------------------------------------------------------------------|-------------------------------------|-------|--------|---------|------|
|     |                              |                                                                       | MASTER <sup>§</sup>                 |       | SLAVE  |         |      |
|     |                              |                                                                       | MIN                                 | MAX   | MIN    | MAX     |      |
| 1   | t <sub>h</sub> (CKXL-FXL)    | Hold time, FSX low after CLKX low <sup>¶</sup>                        | L – 4                               | L + 4 |        |         | ns   |
| 2   | t <sub>d</sub> (FXL-CKXH)    | Delay time, FSX low to CLKX high <sup>#</sup>                         | T – 4                               | T + 4 |        |         | ns   |
| 3   | t <sub>d</sub> (CKXL-DXV)    | Delay time, CLKX low to DX valid                                      | –4                                  | 4     | 3P + 1 | 5P + 17 | ns   |
| 6   | t <sub>dis</sub> (CKXL-DXHZ) | Disable time, DX high impedance following last data bit from CLKX low | –2                                  | 4     | 3P + 4 | 5P + 17 | ns   |
| 7   | t <sub>d</sub> (FXL-DXV)     | Delay time, FSX low to DX valid                                       | H – 2                               | H + 3 | 2P + 1 | 4P + 13 | ns   |

<sup>†</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

<sup>‡</sup> For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

<sup>§</sup> S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)

= sample rate generator input clock = P<sub>clks</sub> if CLKSM = 0 (P<sub>clks</sub> = CLKS period)

T = CLKX period = (1 + CLKGDV) \* S

H = CLKX high pulse width = (CLKGDV/2 + 1) \* S if CLKGDV is even

= (CLKGDV + 1)/2 \* S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) \* S if CLKGDV is even

= (CLKGDV + 1)/2 \* S if CLKGDV is odd or zero

<sup>¶</sup> FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

<sup>#</sup> FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

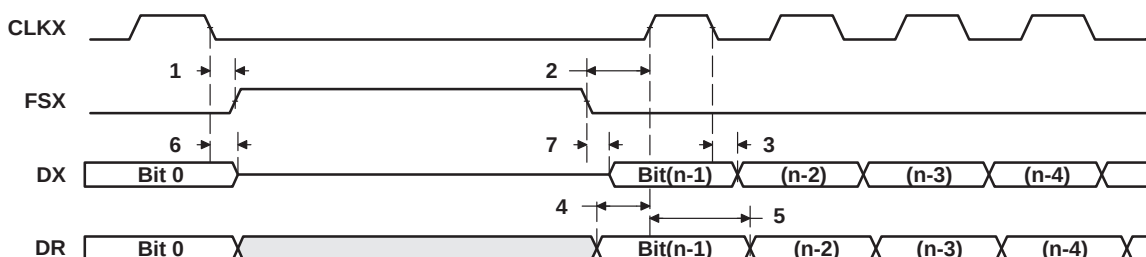


Figure 36. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

### MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

**timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1<sup>†‡</sup> (see Figure 37)**

| NO. |                                                          | C6701-120<br>C6701-150<br>C6701-167 |     |        |     | UNIT |
|-----|----------------------------------------------------------|-------------------------------------|-----|--------|-----|------|
|     |                                                          | MASTER                              |     | SLAVE  |     |      |
|     |                                                          | MIN                                 | MAX | MIN    | MAX |      |
| 4   | $t_{su}(DRV-CKXH)$ Setup time, DR valid before CLKX high | 12                                  |     | 2 – 3P | ns  |      |
| 5   | $t_h(CKXH-DRV)$ Hold time, DR valid after CLKX high      | 4                                   |     | 5 + 6P | ns  |      |

<sup>†</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

<sup>‡</sup> For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

**switching characteristics for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1<sup>†‡</sup> (see Figure 37)**

| NO. | PARAMETER                    |                                                                        | C6701-120<br>C6701-150<br>C6701-167 |       |        |         | UNIT |
|-----|------------------------------|------------------------------------------------------------------------|-------------------------------------|-------|--------|---------|------|
|     |                              |                                                                        | MASTER <sup>§</sup>                 |       | SLAVE  |         |      |
|     |                              |                                                                        | MIN                                 | MAX   | MIN    | MAX     |      |
| 1   | t <sub>h</sub> (CKXH-FXL)    | Hold time, FSX low after CLKX high <sup>¶</sup>                        | T – 4                               | T + 4 |        |         | ns   |
| 2   | t <sub>d</sub> (FXL-CKXL)    | Delay time, FSX low to CLKX low <sup>#</sup>                           | H – 4                               | H + 4 |        |         | ns   |
| 3   | t <sub>d</sub> (CKXL-DXV)    | Delay time, CLKX low to DX valid                                       | –4                                  | 4     | 3P + 1 | 5P + 17 | ns   |
| 6   | t <sub>dis</sub> (CKXH-DXHZ) | Disable time, DX high impedance following last data bit from CLKX high | H – 2                               | H + 3 |        |         | ns   |
| 7   | t <sub>dis</sub> (FXH-DXHZ)  | Disable time, DX high impedance following last data bit from FSX high  |                                     |       | P + 4  | 3P + 17 | ns   |
| 8   | t <sub>d</sub> (FXL-DXV)     | Delay time, FSX low to DX valid                                        |                                     |       | 2P + 1 | 4P + 13 | ns   |

<sup>†</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

<sup>‡</sup> For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

<sup>§</sup> S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)

= sample rate generator input clock = P\_clks if CLKSM = 0 (P\_clks = CLKS period)

T = CLKX period = (1 + CLKGDV) \* S

H = CLKX high pulse width = (CLKGDV/2 + 1) \* S if CLKGDV is even

= (CLKGDV + 1)/2 \* S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) \* S if CLKGDV is even

= (CLKGDV + 1)/2 \* S if CLKGDV is odd or zero

<sup>¶</sup> FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

<sup>#</sup> FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

# TMS320C6701 FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

## MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

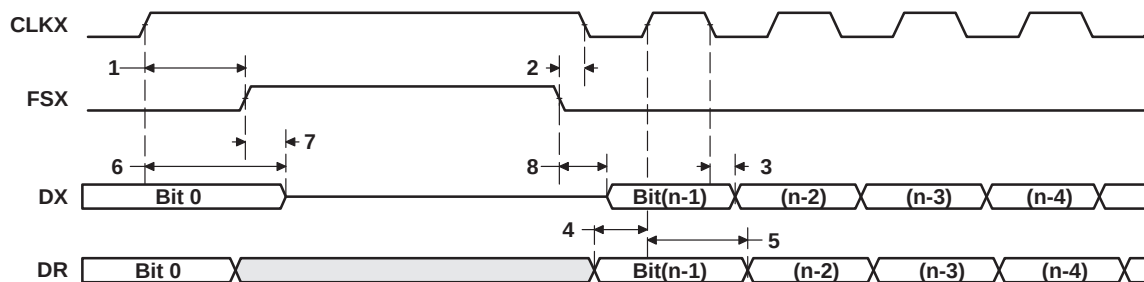


Figure 37. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

**MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)**

**timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1<sup>†‡</sup> (see Figure 38)**

| NO. |                                                                 | C6701-120<br>C6701-150<br>C6701-167 |     |        |     | UNIT |
|-----|-----------------------------------------------------------------|-------------------------------------|-----|--------|-----|------|
|     |                                                                 | MASTER                              |     | SLAVE  |     |      |
|     |                                                                 | MIN                                 | MAX | MIN    | MAX |      |
| 4   | t <sub>su</sub> (DRV-CKXL) Setup time, DR valid before CLKX low | 12                                  |     | 2 – 3P |     | ns   |
| 5   | t <sub>h</sub> (CKXL-DRV) Hold time, DR valid after CLKX low    | 4                                   |     | 5 + 6P |     | ns   |

<sup>†</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

<sup>‡</sup> For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

**switching characteristics for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1<sup>†‡</sup> (see Figure 38)**

| NO. | PARAMETER                    |                                                                        | C6701-120<br>C6701-150<br>C6701-167 |       |        |         | UNIT |
|-----|------------------------------|------------------------------------------------------------------------|-------------------------------------|-------|--------|---------|------|
|     |                              |                                                                        | MASTER <sup>§</sup>                 |       | SLAVE  |         |      |
|     |                              |                                                                        | MIN                                 | MAX   | MIN    | MAX     |      |
| 1   | t <sub>h</sub> (CKXH-FXL)    | Hold time, FSX low after CLKX high <sup>¶</sup>                        | H – 4                               | H + 4 |        |         | ns   |
| 2   | t <sub>d</sub> (FXL-CKXL)    | Delay time, FSX low to CLKX low <sup>#</sup>                           | T – 4                               | T + 4 |        |         | ns   |
| 3   | t <sub>d</sub> (CKXH-DXV)    | Delay time, CLKX high to DX valid                                      | –4                                  | 4     | 3P + 1 | 5P + 17 | ns   |
| 6   | t <sub>dis</sub> (CKXH-DXHZ) | Disable time, DX high impedance following last data bit from CLKX high | –2                                  | 4     | 3P + 4 | 5P + 17 | ns   |
| 7   | t <sub>d</sub> (FXL-DXV)     | Delay time, FSX low to DX valid                                        | L – 2                               | L + 3 | 2P + 1 | 4P + 13 | ns   |

<sup>†</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

<sup>‡</sup> For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

<sup>§</sup> S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)

= sample rate generator input clock = P\_clks if CLKSM = 0 (P\_clks = CLKX period)

T = CLKX period = (1 + CLKGDV) \* S

H = CLKX high pulse width = (CLKGDV/2 + 1) \* S if CLKGDV is even

= (CLKGDV + 1)/2 \* S if CLKGDV is odd or zero

L = CLKX low pulse width = (CLKGDV/2) \* S if CLKGDV is even

= (CLKGDV + 1)/2 \* S if CLKGDV is odd or zero

<sup>¶</sup> FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

<sup>#</sup> FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

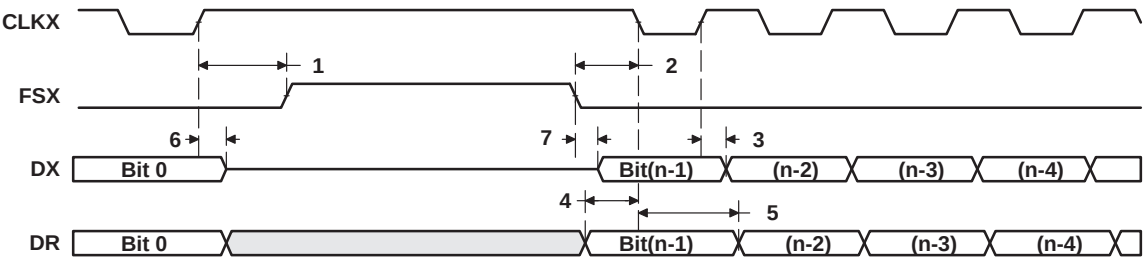
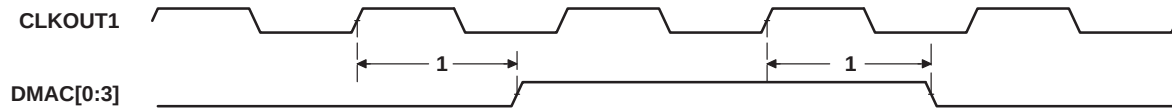


Figure 38. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

## DMAC, TIMER, POWER-DOWN TIMING

### switching characteristics for DMAC outputs (see Figure 39)

| NO. | PARAMETER                                                        | C6701-120<br>C6701-150<br>C6701-167 |     | UNIT |
|-----|------------------------------------------------------------------|-------------------------------------|-----|------|
|     |                                                                  | MIN                                 | MAX |      |
| 1   | $t_d(\text{CKO1H-DMACV})$ Delay time, CLKOUT1 high to DMAC valid | 2                                   | 11  | ns   |



**Figure 39. DMAC Timing**

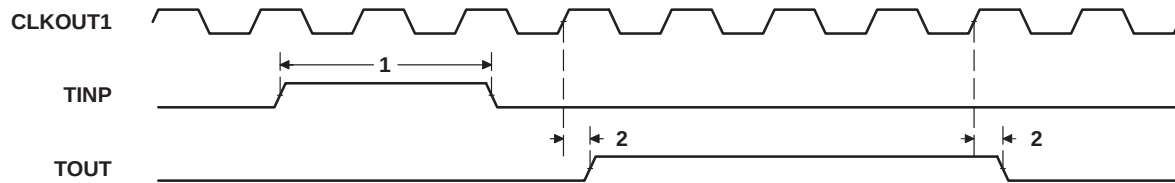
### timing requirements for timer inputs (see Figure 40)<sup>†</sup>

| NO. | PARAMETER                                     | C6701-120<br>C6701-150<br>C6701-167 |     | UNIT |
|-----|-----------------------------------------------|-------------------------------------|-----|------|
|     |                                               | MIN                                 | MAX |      |
| 1   | $t_w(\text{TINPH})$ Pulse duration, TINP high | 2P                                  |     | ns   |

<sup>†</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

### switching characteristics for timer outputs (see Figure 40)

| NO. | PARAMETER                                                        | C6701-120<br>C6701-150<br>C6701-167 |     | UNIT |
|-----|------------------------------------------------------------------|-------------------------------------|-----|------|
|     |                                                                  | MIN                                 | MAX |      |
| 2   | $t_d(\text{CKO1H-TOUTV})$ Delay time, CLKOUT1 high to TOUT valid | 1                                   | 10  | ns   |



**Figure 40. Timer Timing**

TMS320C6701

FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

DMAC, TIMER, POWER-DOWN TIMING (CONTINUED)

switching characteristics for power-down outputs (see Figure 41)

| NO. | PARAMETER                                               | C6701-120<br>C6701-150<br>C6701-167 |     | UNIT |
|-----|---------------------------------------------------------|-------------------------------------|-----|------|
|     |                                                         | MIN                                 | MAX |      |
| 1   | $t_{d(CKO1H-PDV)}$ Delay time, CLKOUT1 high to PD valid | 1                                   | 9   | ns   |

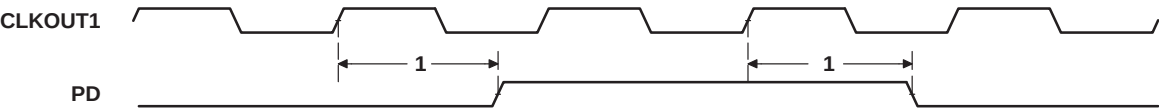


Figure 41. Power-Down Timing



## JTAG TEST-PORT TIMING

timing requirements for JTAG test port (see Figure 42)

| NO. |                                                                           | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|---------------------------------------------------------------------------|-------------------------------------|------|
|     |                                                                           | MIN MAX                             |      |
| 1   | $t_c(\text{TCK})$ Cycle time, TCK                                         | 35                                  | ns   |
| 3   | $t_{su}(\text{TDIV-TCKH})$ Setup time, TDI/TMS/TRST valid before TCK high | 10                                  | ns   |
| 4   | $t_h(\text{TCKH-TDIV})$ Hold time, TDI/TMS/TRST valid after TCK high      | 9                                   | ns   |

switching characteristics for JTAG test port (see Figure 42)

| NO. | PARAMETER                                                | C6701-120<br>C6701-150<br>C6701-167 | UNIT |
|-----|----------------------------------------------------------|-------------------------------------|------|
|     |                                                          | MIN MAX                             |      |
| 2   | $t_d(\text{TCKL-TDOV})$ Delay time, TCK low to TDO valid | -3 12                               | ns   |

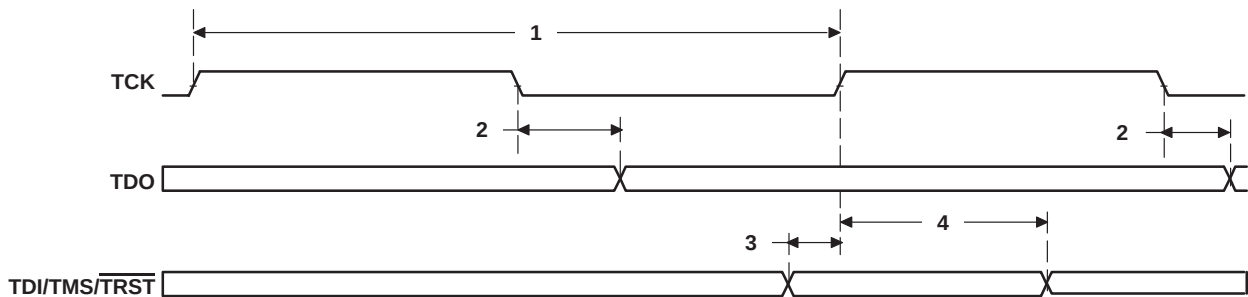


Figure 42. JTAG Test-Port Timing

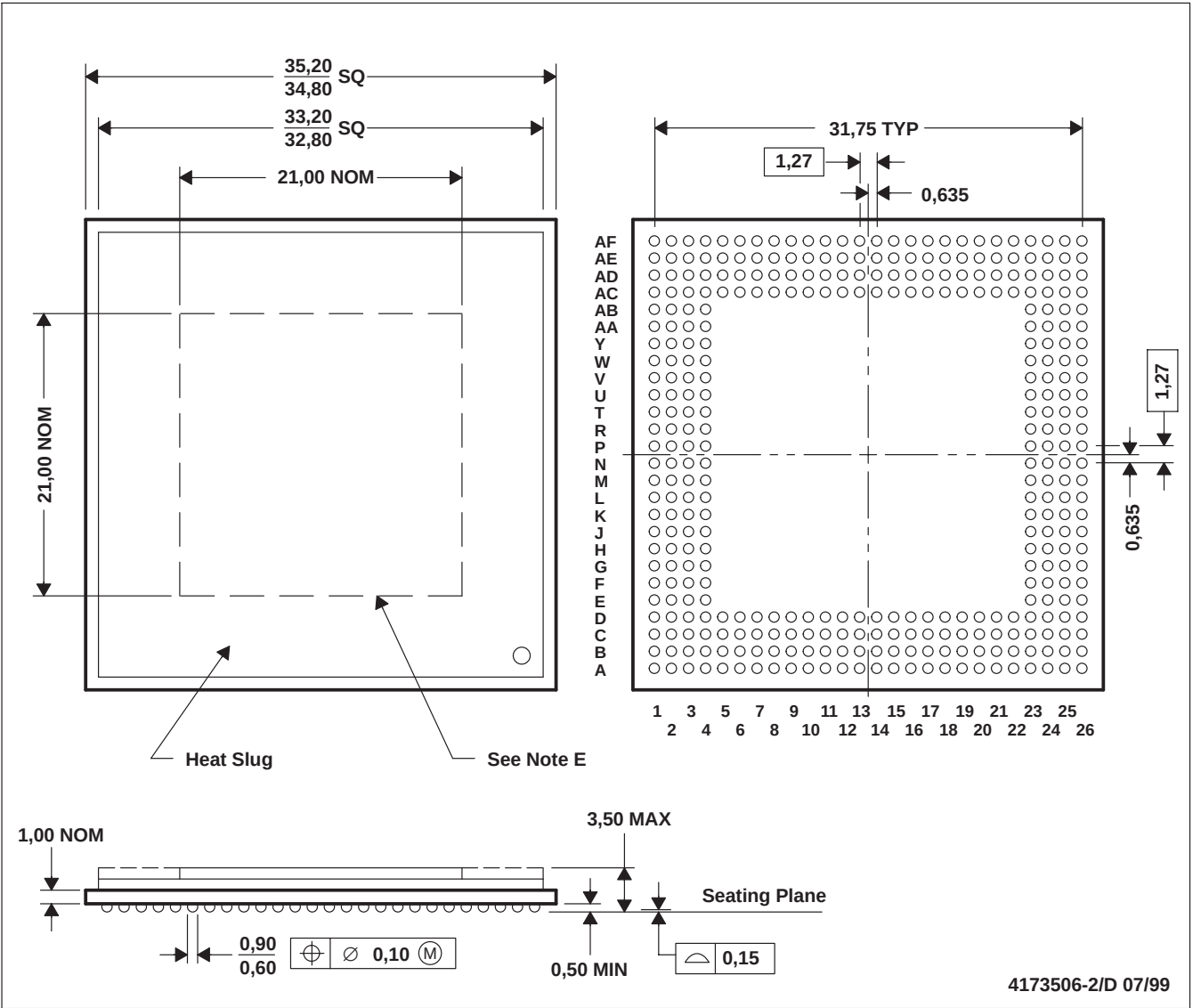
TMS320C6701  
FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS067F – MAY 1998 – REVISED MARCH 2004

MECHANICAL DATA

GJC (S-PBGA-N352)

PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Thermally enhanced plastic package with heat slug (HSL).  
D. Flip chip application only  
E. Possible protrusion in this area, but within 3,50 max package height specification  
F. Falls within JEDEC MO-151/BAR-2

thermal resistance characteristics (S-PBGA package)

| NO |                                       | °C/W  | Air Flow LFPM <sup>†</sup> |
|----|---------------------------------------|-------|----------------------------|
| 1  | R <sub>θJC</sub> Junction-to-case     | 0.74  | N/A                        |
| 2  | R <sub>θJA</sub> Junction-to-free air | 11.31 | 0                          |
| 3  | R <sub>θJA</sub> Junction-to-free air | 9.60  | 100                        |
| 4  | R <sub>θJA</sub> Junction-to-free air | 8.34  | 250                        |
| 5  | R <sub>θJA</sub> Junction-to-free air | 7.30  | 500                        |

<sup>†</sup> LFPM = Linear Feet Per Minute



## REVISION HISTORY

This data sheet revision history highlights the technical changes made to the SPR067E device-specific data sheet to make it an SPRS067F revision.

**Scope:** Applicable updates to the C67x device family, specifically relating to the C6701 device, have been incorporated.

| PAGE(S)<br>NO. | ADDITIONS/CHANGES/DELETIONS                                                                                 |
|----------------|-------------------------------------------------------------------------------------------------------------|
| All            | Updated the title for literature number SPRU190 to:<br>TMS320C6000 DSP Peripherals Overview Reference Guide |
| 26             | Added the power-down mode logic section and accompanying information.                                       |

**PACKAGING INFORMATION**

| Orderable Device   | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| TMS320C6701GJC150  | ACTIVE                | FCBGA        | GJC             | 352  | 21          | TBD                     | SNPB                 | Level-4-220C-72 HR           |                             |
| TMS320C6701GJC167  | OBSOLETE              | FCBGA        | GJC             | 352  |             | TBD                     | Call TI              | Call TI                      |                             |
| TMS320C6701GJCA120 | ACTIVE                | FCBGA        | GJC             | 352  | 21          | TBD                     | SNPB                 | Level-4-220C-72 HR           |                             |
| TMSC6701GJC16719V  | ACTIVE                | FCBGA        | GJC             | 352  | 21          | TBD                     | SNPB                 | Level-4-220C-72 HR           |                             |
| TMX320C6701GJC     | OBSOLETE              | FCBGA        | GJC             | 352  |             | TBD                     | Call TI              | Call TI                      |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TMS320C6701 :**

- Catalog: [SM320C6701](#)

- Enhanced Product: [SM320C6701-EP](#)

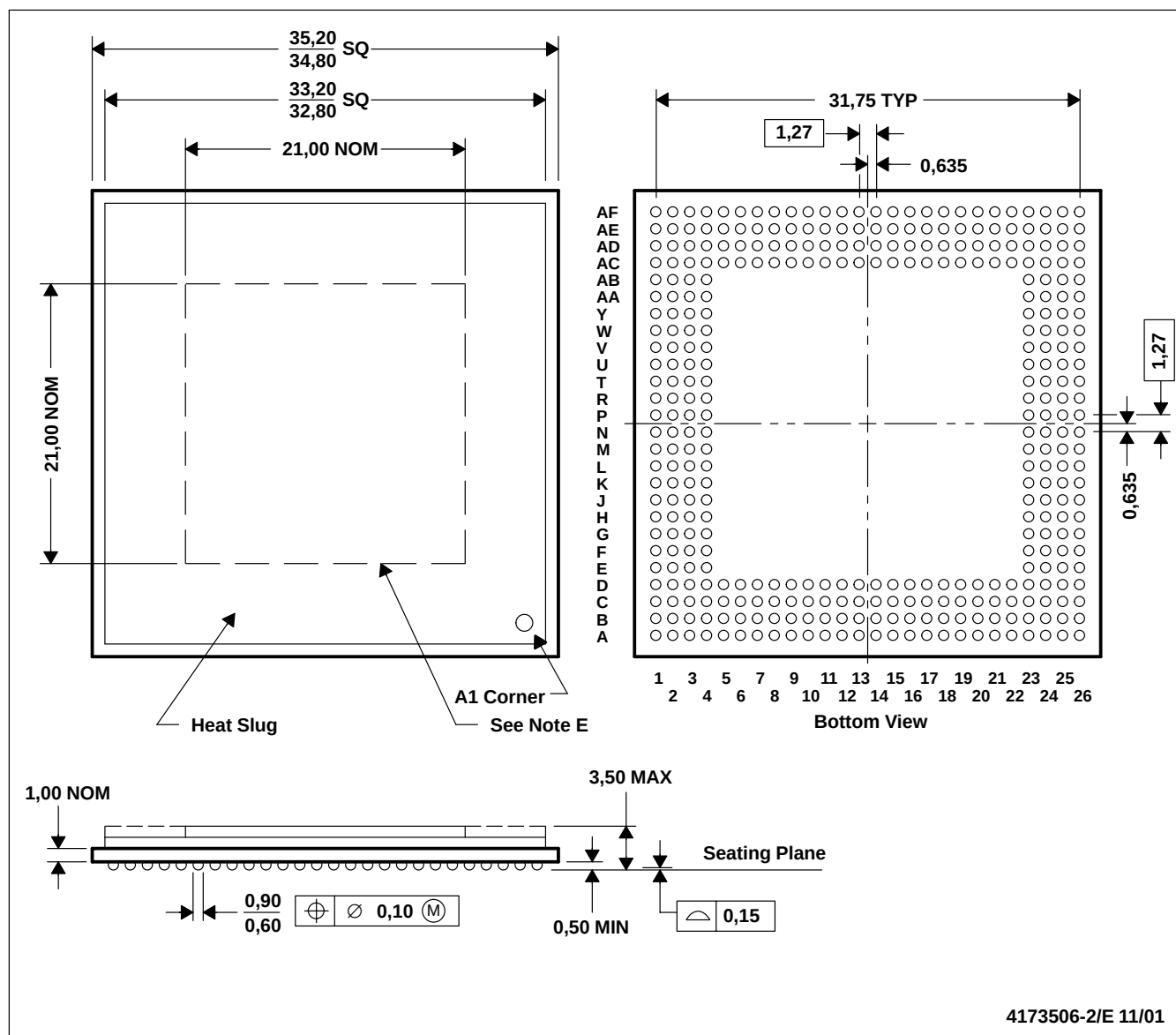
- Military: [SMJ320C6701](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## GJC (S-PBGA-N352)

## PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Thermally enhanced plastic package with heat slug (HSL).
  - D. Flip chip application only
  - E. Possible protrusion in this area, but within 3,50 max package height specification
  - F. Falls within JEDEC MO-151/BAR-2

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

|                        |                                                                                      |
|------------------------|--------------------------------------------------------------------------------------|
| Audio                  | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers             | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters        | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products          | <a href="http://www.dlp.com">www.dlp.com</a>                                         |
| DSP                    | <a href="http://dsp.ti.com">dsp.ti.com</a>                                           |
| Clocks and Timers      | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface              | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                  | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt             | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers       | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                   | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Mobile Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity  | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |                                                                                          |
|-------------------------------|------------------------------------------------------------------------------------------|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

TI E2E Community Home Page

[e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2012, Texas Instruments Incorporated



**Стандарт  
Электрон  
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

**Наши контакты:**

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331