GS2961 3Gb/s, HD, SD SDI Receiver, with Integrated Adaptive Cable Equalizer complete with SMPTE Video Processing

Key Features

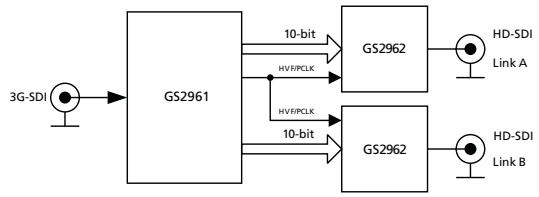
- Operation at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE 425M (Level A and Level B), SMPTE 424M, SMPTE 292M, SMPTE 259M-C and DVB-ASI
- Integrated adaptive cable equalizer
- Typical equalized length of Belden 1694A cable:
  - 150m at 2.97Gb/s
  - 250m at 1.485Gb/s
  - 480m at 270Mb/s
- Integrated Reclocker with low phase noise, integrated VCO
- Serial digital reclocked, or non-reclocked output
- Ancillary data extraction
- Optional conversion from SMPTE 425M Level B to Level A for 1080p 50/60 4:2:2 10-bit
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 Timing Signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI Host Interface
- -20°C to +85°C operating temperature range
- Low power operation (typically 515mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and ROHS compliant

Errata

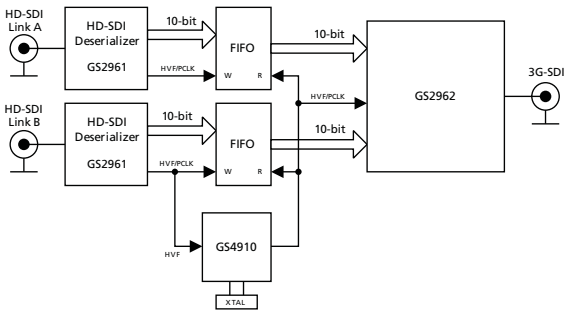
Refer to Errata document entitled **GS2960/GS2961 Errata** for this device (document number **53117**).

Applications

Application: Single Link (3G-SDI) to Dual Link (HD-SDI) Converter



Application: Dual Link (HD-SDI) to Single Link (3G-SDI) Converter



Description

The GS2961 is a multi-rate SDI integrated Receiver which includes complete SMPTE processing, as per SMPTE 425M, 292M and SMPTE 259M-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The GS2961 integrates Gennum's adaptive cable equalizer technology, achieving unprecedented cable lengths and jitter tolerance. It features DC restoration to compensate for the DC content of SMPTE pathological signals.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop-through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The serial digital output can be connected to an external cable driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode (the default operating mode), the GS2961 performs full SMPTE processing, and features a number of data integrity checks and measurement capabilities.

The device also supports ancillary data extraction, and can provide entire ancillary data packets through host-accessible registers. It also provides a variety of other packet detection and error handling features. All of these processing features are optional, and may be individually enabled or disabled through register programming.

Both SMPTE 425M Level A and Level B inputs are supported with optional conversion from Level B to Level A for 1080p 50/59.94/60 4:2:2 10-bit inputs.

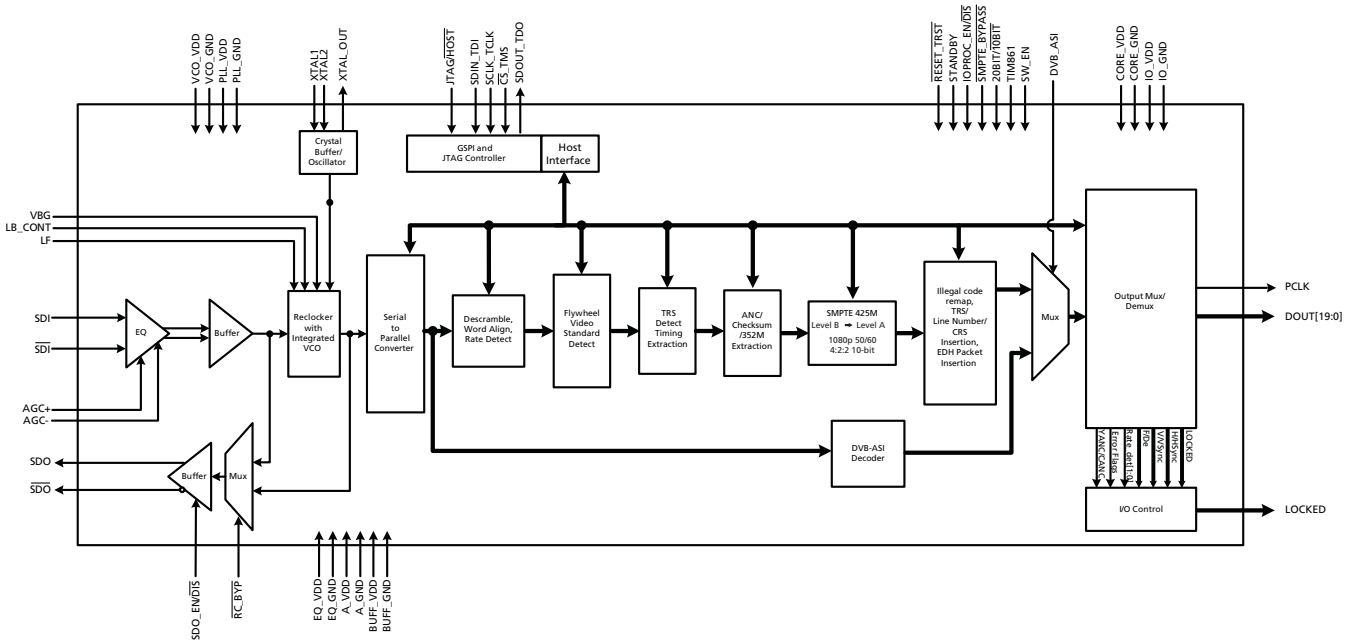
In DVB-ASI mode, sync word detection, alignment and 8b/10b decoding is applied to the received data stream.

In Data-Through mode all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

The device can also operate in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static.

Parallel data outputs are provided in 20-bit or 10-bit format for 3Gb/s, HD and SD video rates, with a variety of mapping options. As such, this parallel bus can interface directly with video processor ICs, and output data can be multiplexed onto 10 bits for a low pin count interface.

Functional Block Diagram



GS2961 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
2	153143	53865	November 2009	Added reference to GS2960/GS2961 Errata (document number 53117). Converted to Data Sheet.
1	152698	–	October 2009	Updated Power numbers in Table 2-3: DC Electrical Characteristics.
0	151888	–	June 2009	Conversion to Preliminary Data Sheet. Corrections to Timing Diagrams in Figure 4-5, Figure 4-6 and Figure 4-7. Clarification to Section 4.18.8. Updates to all sections.
C	151697	–	April 2009	Updated equalized cable lengths and power numbers in Key Features, Table 2-4: AC Electrical Characteristics and Section 4.3.1.
B	151504	–	March 2009	Changed pin H3 from 'RSV' to 'CORE_GND' in 1.1 Pin Assignment, 1.2 Pin Descriptions and 5.3 Typical Application Circuit.
A	151219	–	February 2009	New Document.

Contents

List of Figures

List of Tables

1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_ VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	A_VDD	PLL_ VDD	RSV	VCO_ GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	A_GND	PLL_ VDD	PLL_ VDD	STAT4	STAT5	$\overline{\text{RESET}}$ _$\overline{\text{TRST}}$	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	A_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SW_EN	JTAG/ $\overline{\text{HOST}}$	IO_GND	IO_VDD
E	EQ_VDD	EQ_GND	A_GND	PLL_ GND	CORE _GND	CORE _VDD	SDOUT_ TDO	SDIN_ TDI	DOUT10	DOUT11
F	AGCP	RSV	A_GND	PLL_ GND	CORE _GND	CORE _VDD	$\overline{\text{CS}}$_ TMS	SCLK_ TCK	DOUT8	DOUT9
G	AGCN	A_GND	$\overline{\text{RC\_BYP}}$	CORE _GND	CORE _GND	CORE _VDD	$\overline{\text{SMPTE}}$_ $\overline{\text{BYPASS}}$	DVB_ASI	IO_GND	IO_VDD
H	BUFF_ VDD	BUFF_ GND	CORE _GND	RSV	TIM_861	XTAL_ OUT	20bit/ $\overline{\text{10bit}}$	IOPROC_ EN/$\overline{\text{DIS}}$	DOUT6	DOUT7
J	SDO	SDO_ EN/$\overline{\text{DIS}}$	RSV	RSV	RSV	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STANDBY	RSV	RSV	RSV	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
A1	VBG		Analog Input	Band Gap voltage filter connection.
A2	LF		Analog Input	Loop Filter component connection.
A3	LB_CONT		Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD		Input Power	POWER pin for the VCO. Connect to 1.2V DC analog through an RC filter (see 5. Application Reference Design). VCO_VDD is nominally 0.7V. (Do not connect directly to 0.7V).

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A5, A6, B5, B6, C5, C6	STAT[0:5]		Output	MULTI-FUNCTIONAL OUTPUT PORT. Signal levels are LVCMOS/LVTTL compatible. Each of the STAT [0:5] pins can be configured individually to output one of the following signals:

Signal	Default
H/HSYNC	STAT0
V/VSYNC	STAT1
F/DE	STAT2
LOCKED	STAT3
Y/1ANC	STAT4
C/2ANC	–
DATA ERROR	STAT5
EDH DETECTED	–
CARRIER DETECT	–
RATE_DET0	–
RATE_DET1	–

A7, D10, G10, K7	IO_VDD		Input Power	POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.
A8	PCLK		Output	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS/LVTTL compatible.

3G 10-bit or 20-bit mode	PCLK @ 148.5 or 148.5/1.001MHz
HD 10-bit mode	PCLK @ 148.5 or 148.5/1.001MHz
HD 20-bit mode	PCLK @ 74.25 or 74.25/1.001MHz
SD 10-bit mode	PCLK @ 27MHz
SD 20-bit mode	PCLK @ 13.5MHz

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
A9, A10, B8, B9, B10,C8, C9, C10, E9, E10	DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11		Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible.	
				20-bit mode 20bit/$\overline{10bit}$ = HIGH	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Luma data output for SD and HD data rates; Data Stream 1 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
				10-bit mode 20bit/$\overline{10bit}$ = LOW	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1&2 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): 8b/10b decoded DVB-ASI data Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
B1	A_VDD		Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.	
B2, C3, C4	PLL_VDD		Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.	
B3, F2, H4, J3, J4, J5, K3, K4, K5	RSV			These pins must be left unconnected.	
B4	VCO_GND		Input Power	GND pin for the VCO. Connect to analog GND.	
B7, D9, G9, J7	IO_GND		Input Power	GND connection for digital I/O. Connect to digital GND.	
C1, D1	SDI, $\overline{SDI}$		Analog Input	Serial Digital Differential Input.	
C2, D2, D3, E3, F3, G2	A_GND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
C7	$\overline{\text{RESET\_TRST}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG/$\overline{\text{HOST}}$ = LOW): When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG/$\overline{\text{HOST}}$ = HIGH): When LOW, all functional blocks are set to default and the JTAG test sequence is reset. When HIGH, normal operation of the JTAG test sequence resumes after $\overline{\text{RESET\_TRST}}$ is de-asserted.
D4, E4, F4	PLL_GND		Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G4, G5, H3	CORE_GND		Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD		Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	SW_EN		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable switch-line locking, as described in Section 4.10.1.
D8	JTAG/$\overline{\text{HOST}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG test mode or host interface mode. When JTAG/$\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/$\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes.
E1	EQ_VDD		Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	EQ_GND		Input Power	GND pin for SDI buffer. Connect to analog GND.
E7	SDOUT_TDO		Output	COMMUNICATION SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. GSPI serial data output/test data out. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test results from the device. In host interface mode, this pin is used to read status and configuration data from the device.
E8	SDIN_TDI		Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. GSPI serial data in/test data in. In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test data into the device. In host interface mode, this pin is used to write address and configuration data words into the device.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description	
F1, G1	AGCP, AGCN			Automatic Gain Control for the equalizer. Attach the AGC capacitor between these pins.	
F7	$\overline{CS}$_TMS		Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip select / test mode start. In JTAG mode (JTAG/$\overline{HOST}$ = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test. In host interface mode (JTAG/$\overline{HOST}$ = LOW), this pin operates as the host interface chip select and is active LOW.	
F8	SCLK_TCK		Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial data clock signal. In JTAG mode (JTAG/$\overline{HOST}$ = HIGH), this pin is the JTAG clock. In host interface mode (JTAG/$\overline{HOST}$ = LOW), this pin is the host interface serial bit clock. All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.	
F9, F10, H9, H10, J8, J9, J10, K8, K9, K10	DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3		Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible.	
				20-bit mode 20bit/$\overline{10bit}$ = HIGH	SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for 3G data rate DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH): Not defined Data-Through mode ($\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW): Data output
				10-bit mode 20bit/$\overline{10bit}$ = LOW	Forced LOW
G3	$\overline{RC\_BYP}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G7	$\overline{\text{SMPTE\_BYPASS}}$		Input/Output	CONTROL SIGNAL INPUT/OUTPUT Signal levels are LVCMOS/LVTTL compatible. Indicates the presence of valid SMPTE data. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{\text{SMPTE\_BYPASS}}$ is HIGH when the device locks to a SMPTE compliant input. $\overline{\text{SMPTE\_BYPASS}}$ is LOW under all other conditions. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface register is LOW, this pin is an INPUT: No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ is set HIGH, the device carries out SMPTE scrambling and I/O processing. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode.
G8	DVB_ASI		Input/Output	CONTROL SIGNAL INPUT Signal Levels are LVCMOS/LVTTL compatible. Used to enable/disable DVB-ASI data extraction in manual mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is LOW, this pin is an input and when the DVB_ASI pin is set HIGH the device will carry out DVB_ASI data extraction and processing. The $\overline{\text{SMPTE\_BYPASS}}$ pin must be set LOW. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode. When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is HIGH (default), DVB-ASI is configured as a status output (set LOW), and DVB-ASI input streams are not supported or recognized.
H1	BUFF_VDD		Input Power	POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND		Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H5	TIM_861		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select CEA-861 timing mode. When TIM_861 is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.
H6	XTAL_OUT		Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.
H7	20bit/$\overline{\text{10bit}}$		Input	CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to select the output bus width. HIGH = 20-bit, LOW = 10-bit.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H8	IOPROC_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to enable or disable video processing features. When IOPROC_EN is HIGH, the video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.
J1, K1	SDO, $\overline{\text{SDO}}$		Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable the serial digital output stage. When SDO_EN/$\overline{\text{DIS}}$ is LOW, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH. When SDO_EN/$\overline{\text{DIS}}$ is HIGH, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are enabled.
J6, K6	XTAL2, XTAL1		Analog Input	Input connection for 27MHz crystal.
K2	STANDBY		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (EQ_VDD, BUFF_VDD, A_VDD)	-0.3V to +4.0V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Ambient Operating Temperature (T_A)	$-40°C \leq T_A \leq 95°C$
Storage Temperature (T_{STG})	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

NOTES:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	2
Supply Voltage, Serial Digital Input	EQ_VDD	–	3.13	3.3	3.47	V	–

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	2

NOTES

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor. See Typical Application Circuit on page 99.
2. The 3.3V supplies must track the 3.3V supply of an external CD.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10bit 3G	–	200	240	mA	–
		20bit 3G	–	190	240	mA	–
		10/20bit HD	–	160	200	mA	–
		10/20bit SD	–	130	170	mA	–
		DVB_ASI	–	130	170	mA	–
+1.8V Supply Current	I_{1V8}	10bit 3G	–	37	45	mA	–
		20bit 3G	–	16	20	mA	–
		10/20bit HD	–	15	21	mA	–
		10/20bit SD	–	4	7	mA	–
		DVB_ASI	–	4	6	mA	–
+3.3V Supply Current	I_{3V3}	10bit 3G	–	150	180	mA	–
		20bit 3G	–	115	130	mA	–
		10/20bit HD	–	110	135	mA	–
		10/20bit SD	–	90	100	mA	–
		DVB_ASI	–	90	95	mA	–
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10bit 3G	–	540	640	mW	–
		20bit 3G	–	500	600	mW	–
		10/20bit HD	–	460	560	mW	–
		10/20bit SD	–	410	490	mW	–
		DVB_ASI	–	410	490	mW	–
		Reset	–	390	–	mW	–
		Standby	–	23	45	mW	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10bit 3G	–	720	890	mW	–
		20bit 3G	–	600	720	mW	–
		10/20bit HD	–	550	700	mW	–
		10/20bit SD	–	440	540	mW	–
		DVB_ASI	–	440	530	mW	–
		Reset	–	410	–	mW	–
		Standby	–	23	45	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VSS -0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD +0.3	V	–
Output Logic LOW	V_{OL}	IOL = 5mA, 1.8V operation	–	–	0.2	V	–
		IOL = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOH = 5mA, 1.8V operation	1.4	–	–	V	–
		IOH = 8mA, 3.3V operation	2.4	–	–	V	–
Serial Input							
Serial Input Common Mode Voltage	–	75Ω load	–	2.2	–	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD -(0.6/2)	BUFF_VDD -(0.45/2)	BUFF_VDD -(0.35/2)	V	–

Notes:

The output drive strength of the digital outputs can be programmed through the host interface. please see Table 4-18: Configuration and Status Registers, register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
System								
Device Latency	–	3G		–	47	–	PCLK	–
		HD		–	47	–	PCLK	–
		SD		–	46	–	PCLK	–
		DVB-ASI		–	14	–	PCLK	–
Reset Pulse Width	t_{reset}	–		1	–	–	ms	–
Parallel Output								
Parallel Clock Frequency	f_{PCLK}	–		13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–		40	–	60	%	–
Output Data Hold Time (1.8V)	t_{oh}	3G 10-bit 6pF Cload	SPI	1.5	–	–	ns	1
			DBUS	0.4	–	–	ns	1
			STAT	0.45	–	–	ns	1
		3G 20-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		HD 10-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		HD 20-bit 6pF Cload	DBUS	1.0	–	–	ns	1
			STAT	1.0	–	–	ns	1
		SD 10-bit 6pF Cload	DBUS	19.4	–	–	ns	1
			STAT	19.4	–	–	ns	1
		SD 20-bit 6pF Cload	DBUS	38.0	–	–	ns	1
			STAT	38.0	–	–	ns	1

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Hold Time (3.3V)	t_{oh}	3G 10-bit 6pF Cload	SPI	1.5	–	–	ns	2
			DBUS	0.45	–	–	ns	2
			STAT	0.45	–	–	ns	2
		3G 20-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		HD 10-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		HD 20-bit 6pF Cload	DBUS	1.0	–	–	ns	2
			STAT	1.0	–	–	ns	2
		SD 10-bit 6pF Cload	DBUS	19.4	–	–	ns	2
			STAT	19.4	–	–	ns	2
		SD 20-bit 6pF Cload	DBUS	38.0	–	–	ns	2
			STAT	38.0	–	–	ns	2
Output Data Delay Time (1.8V)	t_{od}	3G 10-bit 15pF Cload	SPI	–	–	14.0	ns	3
			DBUS	–	–	1.8	ns	3
			STAT	–	–	2.5	ns	3
		3G 20-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		HD 10-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		HD 20-bit 15pF Cload	DBUS	–	–	3.7	ns	3
			STAT	–	–	4.4	ns	3
		SD 10-bit 15pF Cload	DBUS	–	–	22.2	ns	3
			STAT	–	–	22.2	ns	3
		SD 20-bit 15pF Cload	DBUS	–	–	41.0	ns	3
			STAT	–	–	41.0	ns	3

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Delay Time (3.3V)	t_{od}	3G 10-bit 15pF Cload	SPI	–	–	14.0	ns	4
			DBUS	–	–	1.9	ns	4
			STAT	–	–	2.2	ns	4
		3G 20-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		HD 10-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		HD 20-bit 15pF Cload	DBUS	–	–	3.7	ns	4
			STAT	–	–	4.1	ns	4
		SD 10-bit 15pF Cload	DBUS	–	–	22.2	ns	4
			STAT	–	–	22.2	ns	4
		SD 20-bit 15pF Cload	DBUS	–	–	41.0	ns	4
			STAT	–	–	41.0	ns	4
Output Data Rise/Fall Time (1.8V)	t_r/t_f	3G 10-bit 6pF Cload	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.3	ns	1
		All other modes 6pF Cload	STAT	–	–	0.4	ns	1
			DBUS	–	–	0.4	ns	1
		3G 10-bit 15pF Cload	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.1	ns	3
		All other modes 15pF Cload	STAT	–	–	1.5	ns	3
			DBUS	–	–	1.4	ns	3
Output Data Rise/Fall Time (3.3V)	t_r/t_f	3G 10-bit 6pF Cload	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
		All other modes 6pF Cload	STAT	–	–	0.5	ns	2
			DBUS	–	–	0.4	ns	2
Output Data Rise/Fall Time (3.3V)	t_r/t_f	3G 10-bit 15pF Cload	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.5	ns	4
		All other modes 15pF Cload	STAT	–	–	1.6	ns	4
			DBUS	–	–	1.4	ns	4

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Digital Input							
Serial Input Data Rate	DR_{SDI}	–	0.27	–	2.97	Gb/s	–
Serial Input Voltage Swing	ΔV_{SDI}	T_A =25°C, differential, 270Mb/s & 1.485Gb/s	720	800	950	mV_{p-p}	6
		T_A =25°C, differential, 2.97Gb/s	720	800	880	mV_{p-p}	6
Achievable Cable Length	–	Belden 1694A cable, 3G	–	150	–	m	–
		Belden 1694A cable, HD	–	230	–	m	–
		Belden 1694A cable, SD	–	440	–	m	–
Input Return Loss	–	single ended	15	21	–	dB	7
Input Resistance	–	single ended	–	1.52	–	kΩ	–
Input Capacitance	–	single ended	–	1	–	pF	–
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	0.27	–	2.97	Gb/s	–
Serial Output Swing	ΔV_{SDO}	Differential with 100Ω load	320	–	600	mVp-p	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	–	–	–	180	ps	–
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	–	–	–	180	ps	–
Serial Output Jitter with loop-through mode	t_{OJ}	SMPTE colour bar 3G, 150m	–	–	100	ps	–
		SMPTE colour bar HD, 250m	–	–	100	ps	–
		SMPTE colour bar SD, 480m	–	–	470	ps	–
Serial Output Duty Cycle Distortion	DCD_{SDD}	3G	–	10	–	ps	–
		HD	–	10	–	ps	–
		SD	–	20	–	ps	–
Synchronous lock time	–	–	–	–	25	µs	–
Asynchronous lock time	–	–	0.1	–	20	ms	–
Lock time from power-up	–	After 20 minutes at -20°C	–	–	5	s	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	60	MHz	5
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	5
GSPI Input Data Setup Time	–		1.5	–	–	ns	5
GSPI Input Data Hold Time	–		1.5	–	–	ns	5
GSPI Output Data Hold Time	–	–	1.5	–	–	ns	5
$\overline{CS}$ low before SCLK rising edge	–	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	5
$\overline{CS}$ high after SCLK falling edge	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	5

Notes:

1. 1.89V and 0°C.
2. 3.47V and 0°C.
3. 1.71V and 85°C
4. 3.13V and 85°C
5. Timing parameters defined in Section 4.19.3
6. 0m cable length
7. Tested on a 2961 board from 5MHz to 3GHz.

3. Input/Output Circuits

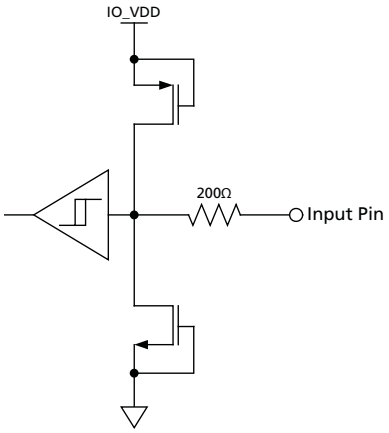


Figure 3-1: Digital Input Pin with Schmitt Trigger (20bit/$\overline{10bit}$, $\overline{CS}$_TMS, SW_EN, IOPROC_EN/$\overline{DIS}$, JTAG/$\overline{HOST}$, $\overline{RC\_BYP}$, $\overline{RESET\_TRST}$, SCLK_TCK, SDIN_TDI, SDO_EN/$\overline{DIS}$, STANDBY, TIM_861)

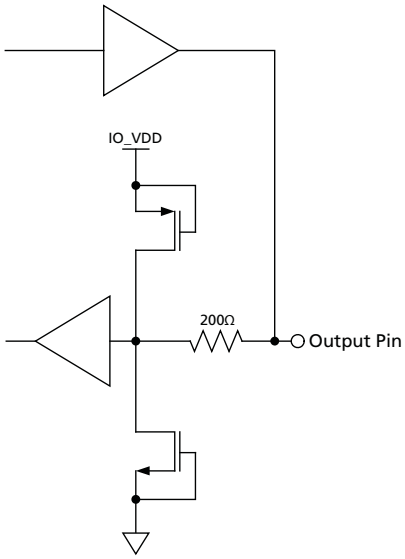


Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (DVB_ASI, $\overline{SMPTE\_BYPASS}$)

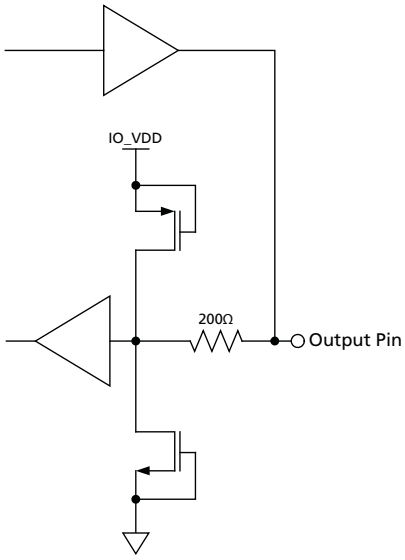


Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output unless in Reset Mode; in which case they are high-impedance. The drive strength can be set by writing to address 06Dh in the host interface register. (DOUT0, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, DOUT6, DOUT7, DOUT8, DOUT9, SDOUT_TDO, STAT0, STAT1, STAT2, STAT3, STAT4, STAT5, XTAL_OUT, DOUT10, DOUT11, DOUT12, DOUT13, DOUT14, DOUT15, DOUT16, DOUT17, DOUT18, DOUT19, PCLK)

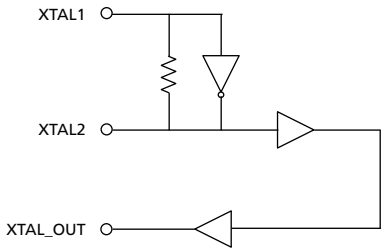


Figure 3-4: XTAL1/XTAL2/XTAL-OUT

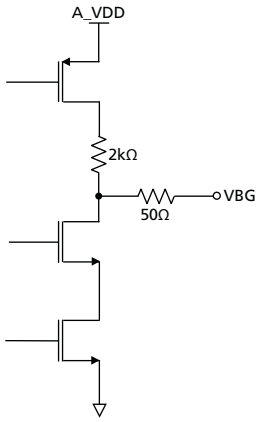


Figure 3-5: VBG

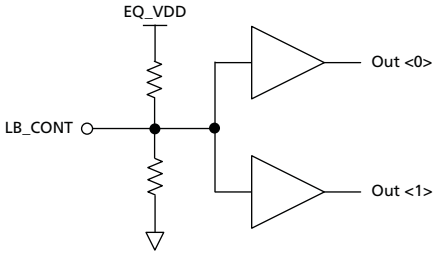


Figure 3-6: LB_CONT

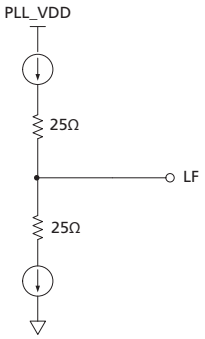


Figure 3-7: Loop Filter

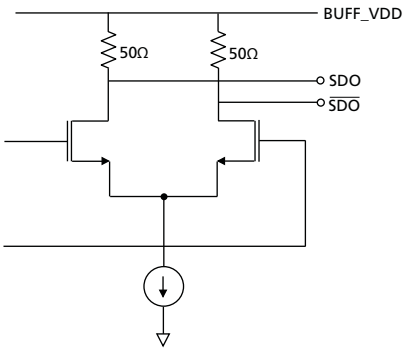


Figure 3-8: SDO/$\overline{\text{SDO}}$

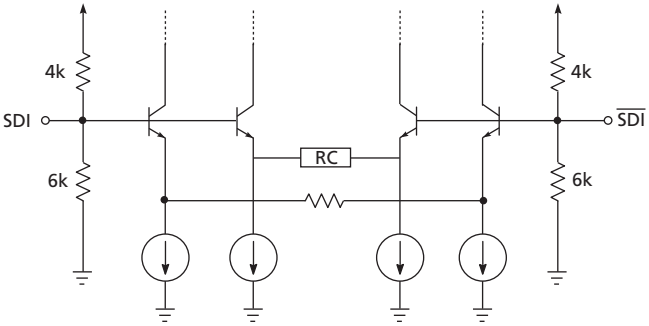


Figure 3-9: Equalizer Input Equivalent Circuit

4. Detailed Description

Refer to the document entitled **GS2960/GS2961 Errata** for this device (document number **53117**).

4.1 Functional Overview

The GS2961 is a multi-rate SDI integrated Receiver which includes complete SMPTE processing, as per SMPTE 425M, 292M and SMPTE 259M-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The GS2961 integrates Gennum's adaptive cable equalizer technology, achieving unprecedented cable lengths and jitter tolerance. It features DC restoration to compensate for the DC content of SMPTE pathological signals.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The Serial Digital Output can be connected to an external Cable Driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode, the GS2961 performs SMPTE de-scrambling and NRZI to NRZ decoding and word alignment. Line-based CRC errors, line number errors, TRS errors and ancillary data check sum errors can all be detected. The GS2961 also provides ancillary data extraction. The entire ancillary data packet is extracted, and written to host-accessible registers. Other processing functions include H:V:F timing extraction, Luma and Chroma ancillary data indication, video standard detection, and SMPTE 352M packet detection and decoding. All of the processing features are optional, and may be enabled or disabled via the Host Interface.

Both SMPTE 425M Level A and Level B inputs are supported. The GS2961 also provides user-selectable conversion from Level B to Level A for 1080p 50/60 4:2:2 10-bit formats only.

In DVB-ASI mode, 8b/10b decoding is applied to the received data stream.

In Data-Through mode, all forms of SMPTE and DVB-ASI decoding are disabled, and the device can be used as a simple serial to parallel converter.

The device can also be placed in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static. Placing the Receiver in Standby mode will automatically place the integrated equalizer in power down mode as well.

Parallel data outputs are provided in 20-bit or 10-bit multiplexed format for 3Gb/s, HD and SD video rates. For 1080p 50/60 4:2:2 10-bit, the parallel data is output on the 20-bit parallel bus as Y on 10 bits and Cb/Cr on the other 10 bits. As such, this parallel bus can interface directly with video processor ICs. For other SMPTE 425M mapping structures,

the video data is mapped to a 20-bit virtual interface as described in SMPTE 425M. In all cases this 20-bit parallel bus can be multiplexed onto 10 bits for a low pin count interface with downstream devices. The associated Parallel Clock input signal operates at 148.5 or 148.5/1.001MHz (for all 3Gb/s HD 10-bit multiplexed modes), 74.25 or 74.25/1.001MHz (for HD 20-bit mode), 27MHz (for SD 10-bit mode) and 13.5MHz (for SD 20-bit mode).

Note: for 3Gb/s 10-bit mode the device operates in Dual Data Rate (DDR) mode, where the data is sampled at both the rising and falling edges of the clock. This reduces the I/O speed requirements of the downstream devices.

4.2 SMPTE 425M Mapping - 3G Level A and Level B Formats

4.2.1 Level A Mapping

Direct image format mapping - the mapping structure used to define 1080p/50/59.94/60 4:2:2 YCbCr 10 bit data, as supported by the GS2961. See Figure 4-1:

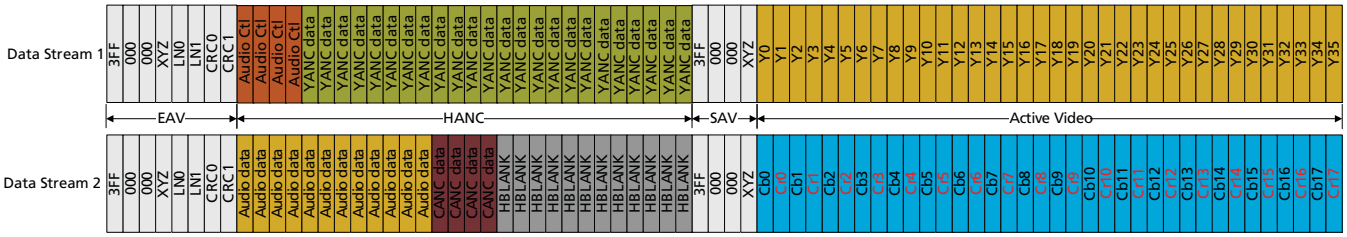


Figure 4-1: Level A Mapping

4.2.2 Level B Mapping

The 2 x 292 HD SDI interface - this can be two distinct links running at 1.5Gb/s or one 3Gb/s link formatted according to SMPTE 292 on two 10-bit links (Y/C interleaved). For 1080p/50/59.94/60 4:2:2 video formats, each link should be line-interleaved as per SMPTE 372M. See Figure 4-2:

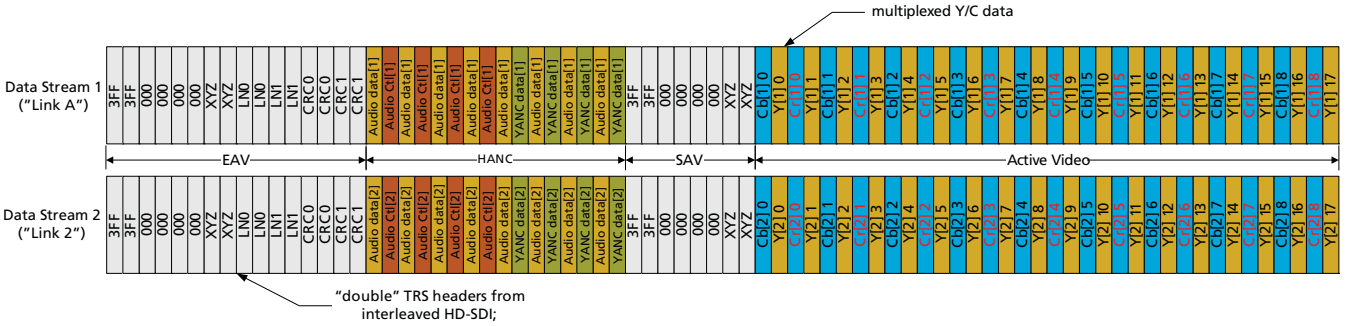


Figure 4-2: Level B Mapping

The GS2961 distinguishes between Level A and Level B mappings at 3Gb/s. When Level B data is detected, each 10-bit link is demultiplexed into its individual component streams, and most video processing features, including error detection and correction are enabled separately for Data Stream 1 and Data Stream 2 (Link A and Link B, respectively). Note that ancillary data extraction can only be enabled for one link for 3Gb/s Level B data. Data Stream 1 or Data Stream 2 can be selected via the host interface.

4.3 Serial Digital Input

The GS2961 can accept serial digital inputs compliant with SMPTE 424M, SMPTE 292 and SMPTE 259M-C.

4.3.1 Integrated Adaptive Cable Equalizer

The GS2961 integrates Gennum's adaptive cable equalizer technology.

The integrated adaptive equalizer can equalize 3Gb/s, HD and SD serial digital signals, and will typically equalize 150m of Belden 1694A cable at 2.97Gb/s, 250m at 1.485Gb/s and 480m at 270Mb/s.The integrated adaptive equalizer is powered from a single +3.3V power supply and consumes approximately 195mW of power.

The equalizer can be bypassed by programming register 073h through the GSPI interface.

4.3.1.1 Serial Digital Inputs

The Serial Data Signal may be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

4.3.1.2 Cable Equalization

The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling.

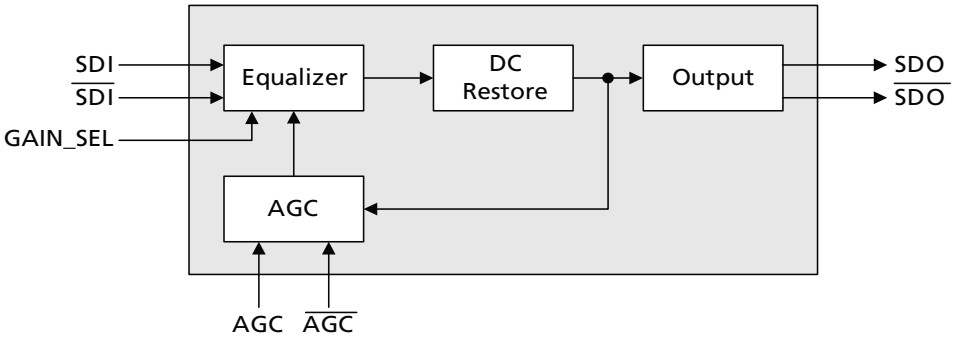


Figure 4-3: GS2961 Integrated EQ Block Diagram

4.4 Serial Digital Loop-Through Output

The GS2961 contains a 100Ω differential serial output buffer which can be configured to output either a retimed or a buffered version of the serial digital input. The SDO and $\overline{\text{SDO}}$ outputs of this buffer can interface directly to a 3Gb/s-capable, SMPTE compliant Gennum cable driver. See 5.3 Typical Application Circuit on page 99.

When the $\overline{\text{RC\_BYP}}$ pin is set HIGH, the serial digital output is the re-timed version of the serial input.

When the $\overline{\text{RC\_BYP}}$ pin is set LOW, the serial digital output is simply the buffered version of the serial input, bypassing the internal reclocker.

The output can be disabled by setting the SDO_EN/$\overline{\text{DIS}}$ pin LOW. The output is also disabled when the STANDBY pin is asserted HIGH. When the output is disabled, both SDO and $\overline{\text{SDO}}$ pins are set to VDD and remain static.

The SDO output is muted when the $\overline{\text{RC\_BYP}}$ pin is set HIGH and the PLL is unlocked (LOCKED pin is LOW). When muted, the output is held static at logic '0' or logic '1'.

Table 4-1: Serial Digital Output

SDO_EN/$\overline{\text{DIS}}$	$\overline{\text{RC\_BYP}}$	SDO/$\overline{\text{SDO}}$
0	X	Disabled
1	1	Re-timed
1	0	Buffered (not re-timed)

NOTE: the serial digital output is muted when the GS2961 is unlocked.

4.5 Serial Digital Reclocker

The GS2961 includes both a PLL stage and a sampling stage.

The PLL is comprised of two distinct loops:

- A coarse frequency acquisition loop sets the centre frequency of the integrated Voltage Controlled Oscillator (VCO) using an external 27MHz reference clock
- A fine frequency and phase locked loop aligns the VCO's phase and frequency to the input serial digital stream

The frequency lock loop results in a very fast lock time.

The sampling stage re-times the serial digital input with the locked VCO clock. This generates a clean serial digital stream, which may be output on the SDO/$\overline{\text{SDO}}$ output pins and converted to parallel data for further processing. Parallel data is not affected by $\overline{\text{RC\_BYP}}$. Only the SDO is affected by this pin.

4.5.1 PLL Loop Bandwidth

The fine frequency and phase lock loop in the GS2961 reclocker is non-linear. The PLL loop bandwidth scales with the jitter amplitude of the input data stream; automatically reduces bandwidth in response to higher jitter. This allows the PLL to reject more of the jitter in the input data stream and produce a very clean reclocked output.

The loop bandwidth of the GS2961 PLL is defined with 0.2UI input jitter. The bandwidth is controlled by the LB_CONT pin. Under nominal conditions, with the LB_CONT pin floating and 0.2UI input jitter applied, the loop bandwidth is set to 1/1000 of the frequency of the input data stream. Connecting the LB_CONT pin to 3.3V reduces the bandwidth to half of the nominal setting. Connecting the LB_CONT pin to GND increases the bandwidth to double the nominal setting. Table 4-2 below summarizes this information.

Table 4-2: PLL Loop Bandwidth

Input Data Rate	LB_CONT Pin Connection	Loop Bandwidth (MHz)[1]
SD	3.3V	0.135
	Floating	0.27
	0V	0.54
HD	3.3V	0.75
	Floating	1.5
	0V	3.0
3G	3.3V	1.5
	Floating	3.0
	0V	6.0

[1]Measured with 0.2UI input jitter applied

4.6 External Crystal/Reference Clock

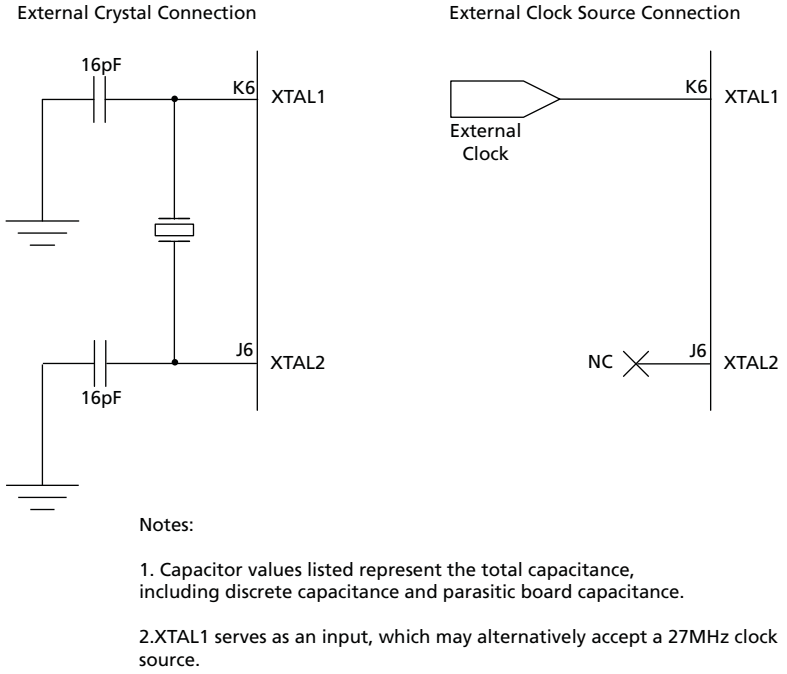
The GS2961 requires an external 27MHz reference clock for correct operation. This reference clock is generated by connecting a crystal to the XTAL1 and XTAL2 pins of the device. See Application Reference Design on page 98. Table 4-3 shows XTAL characteristics.

Alternately, a 27MHz external clock source can be connected to the XTAL1 pin of the device, as shown in Figure 4-4.

The frequency variation of the crystal including aging, supply and temperature variation, should be less than +/-100ppm.

The equivalent series resistance (or motional resistance) should be a maximum of 50Ω.

The external crystal is used in the frequency acquisition process. It has no impact on the output jitter performance of the part when the part is locked to incoming data. Because of this, the only key parameter is the frequency variation of the crystal that is stated above.



Notes:

1. Capacitor values listed represent the total capacitance, including discrete capacitance and parasitic board capacitance.

2.XTAL1 serves as an input, which may alternatively accept a 27MHz clock source.

Figure 4-4: 27MHz Clock Sources

Table 4-3: Input Clock Requirements

Parameter	Min	Typ	Max	UOM	Notes
XTAL1 Low Level Input Voltage (V_{il})	–	–	20% of VDD_IO	V	3
XTAL1 High Level Input Voltage (V_{ih})	80% of VDDIO	–	–	V	3

Table 4-3: Input Clock Requirements

Parameter	Min	Typ	Max	UOM	Notes
XTAL1 Input Slew Rate	2	–	–	V/ns	3
XTAL1 to XOUT Prop. Delay (High to Low)	1.3	1.5	2.3	ns	3
XTAL1 to XOUT Prop. Delay (Low to High)	1.3	1.6	2.3	ns	3

NOTES:

Valid when the cell is used to buffer an external clock source which is connected to the XTAL1 pin, then nothing should be connected to the XTAL2 pin.

4.7 Lock Detect

The LOCKED output signal is available by default on the STAT3 output pin, but may be programmed to be output through any one of the six programmable multi-functional pins of the device; STAT[5:0].

The LOCKED output signal is set HIGH by the Lock Detect block under the following conditions:

Table 4-4: Lock Detect Conditions

Mode of Operation	Mode Setting	Condition for Locked
Data-Through Mode	$\overline{\text{SMPTE\_BYPASS}}$ = LOW DVB_ASI = LOW	Reclocker PLL is locked.
SMPTE Mode	$\overline{\text{SMPTE\_BYPASS}}$ = HIGH DVB_ASI = LOW	Reclocker PLL is locked 2 consecutive TRS words are detected in a 2-line window.
DVB_ASI Mode	$\overline{\text{SMPTE\_BYPASS}}$ = LOW DVB_ASI = HIGH Bit AUTO/$\overline{\text{MAN}}$ = LOW	Reclocker PLL is locked 32 consecutive DVB_ASI words with no errors are detected within a 128-word window.

All other combinations result in the LOCKED signal being LOW.

NOTE: In Standby mode, the reclocker PLL unlocks. However, the LOCKED signal retains whatever state it previously held. So, if before Standby assertion, the LOCKED signal is HIGH, then during standby, it remains HIGH regardless of the status of the PLL.

4.7.1 Asynchronous Lock

The lock detection algorithm is a continuous process, beginning at device power-up or after a system reset. It continues until the device is powered down or held in reset.

The device first determines if a valid serial digital input signal has been presented to the device. If no valid serial data stream has been detected, the serial data into the device is considered invalid, and the LOCKED signal is LOW.

Once a valid input signal has been detected, the asynchronous lock algorithm enters a "hunt" phase, in which the device attempts to detect the presence of either TRS words or DVB-ASI sync words.

By default, the device powers up in auto mode (the AUTO/$\overline{\text{MAN}}$ bit in the host interface is set HIGH). In this mode, the device operating frequency toggles between 3G, HD and SD rates as it attempts to lock to the incoming data rate. The PCLK output continues to operate, and the frequency may switch between 148.5MHz, 74.25MHz, 27MHz and 13.5MHz.

When the device is operating in manual mode (AUTO/$\overline{\text{MAN}}$ bit in the host interface is LOW), the operating frequency needs to be set through the host interface using the RATE_DET[1:0] bits. In this mode, the asynchronous lock algorithm does not toggle the operating rate of the device and attempts to lock within a single standard. Lock is achieved within three lines of the selected standard.

4.7.2 Signal Interruption

The device tolerates a signal interruption of up to 10µs without unlocking, as long as no TRS words are deleted by this interruption. If a signal interruption of greater than 10µs is detected, the lock detection algorithm may lose the current data rate, and LOCKED will de-assert until the data rate is re-acquired by the lock detection block.

4.8 SMPTE Functionality

4.8.1 Descrambling and Word Alignment

The GS2961 performs NRZI to NRZ decoding and data descrambling according to SMPTE 424M/SMPTE 292/SMPTE 259M-C and word aligns the data to TRS sync words.

When operating in manual mode (AUTO/$\overline{\text{MAN}}$ = LOW), the device only carries out SMPTE decoding, descrambling and word alignment when the $\overline{\text{SMPTE\_BYPASS}}$ pin is set HIGH and the DVB_ASI pin is set LOW.

When operating in Auto mode (AUTO/$\overline{\text{MAN}}$ = HIGH), the GS2961 carries out descrambling and word alignment to enable the detection of TRS sync words. When two consecutive valid TRS words (SAV and EAV), with the same bit alignment have been detected, the device word-aligns the data to the TRS ID words.

TRS ID word detection is a continuous process. The device remains in SMPTE mode until TRS ID words fail to be detected.

NOTE 1: Both 8-bit and 10-bit TRS headers are identified by the device.

NOTE 2: In 3G Level B mode, the device only supports Data Stream 1 and Data Stream 2 having the same bit width (i.e. both data streams contain 8-bit data, or both data streams contain 10-bit data). If the bit widths between the two data streams are different, the GS2961 cannot word align the input stream, and switches in Data-Through mode.

4.9 Parallel Data Outputs

The parallel data outputs are aligned to the rising edge of the PCLK.

4.9.1 Parallel Data Bus Buffers

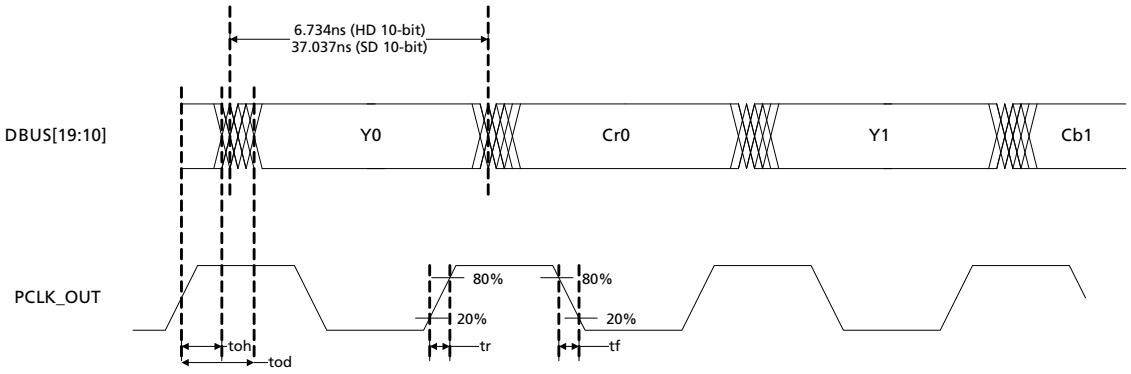
The parallel data bus, status signal outputs and control signal input pins are all connected to high-impedance buffers.

The device supports 1.8 or 3.3V (LVTTL and LVCMOS levels) supplied at the IO_VDD and IO_GND pins.

All output buffers (including the PCLK output), are set to high-impedance in Reset mode ($\overline{\text{RESET\_TRST}}$ = LOW).

I/O Timing Specs:

10-bit SDR Mode:



10bHD Mode

	3.3V						1.8V					
	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload
dbus	1.000ns	0.400ns	6 pF	3.700ns	1.400ns	15 pF	1.000ns	0.400ns	6 pF	3.700ns	1.400ns	15 pF
stat	1.000ns	0.500ns		4.100ns	1.600ns		1.000ns	0.400ns		4.400ns	1.500ns	

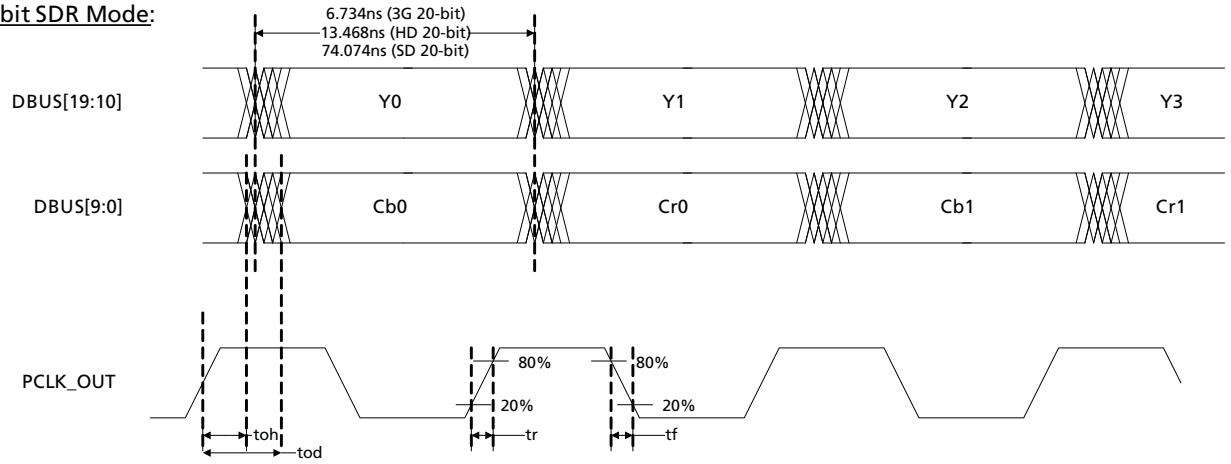
10bSD Mode

	3.3V						1.8V					
	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload
dbus	19.400ns	0.400ns	6 pF	22.200ns	1.400ns	15 pF	19.400ns	0.400ns	6 pF	22.200ns	1.400ns	15 pF
stat	19.400ns	0.500ns		22.200ns	1.600ns		19.400ns	0.400ns		22.200ns	1.500ns	

Figure 4-5: PCLK to Data and Control Signal Output Timing - SDR Mode 1

I/O Timing Specs:

20-bit SDR Mode:



20b3G and 20bHD Modes

	3.3V						1.8V					
	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload
dbus	1.000ns	0.400ns	6 pF	3.700ns	1.400ns	15 pF	1.000ns	0.400ns	6 pF	3.700ns	1.400ns	15 pF
stat	1.000ns	0.500ns		4.100ns	1.600ns		1.000ns	0.400ns		4.400ns	1.500ns	

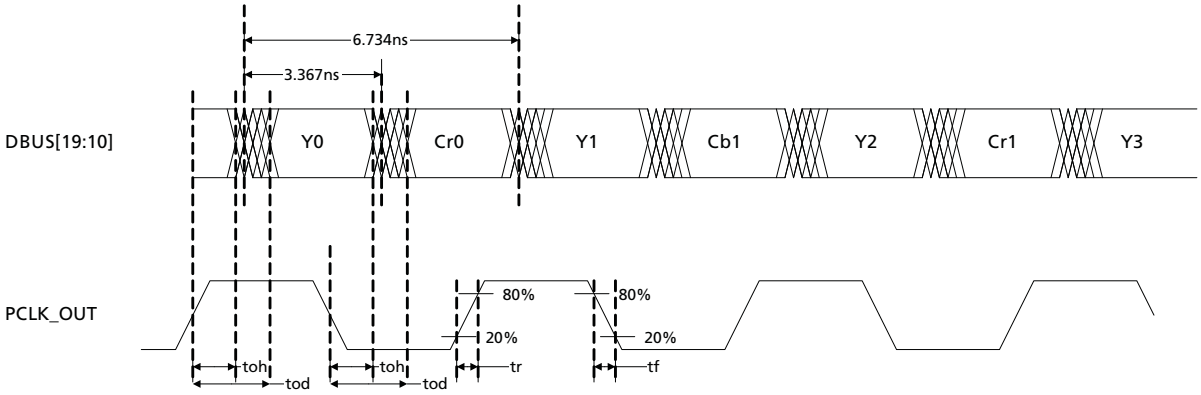
20bSD Mode

	3.3V						1.8V					
	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload
dbus	38.000ns	0.400ns	6 pF	41.000ns	1.400ns	15 pF	38.000ns	0.400ns	6 pF	41.000ns	1.400ns	15 pF
stat	38.000ns	0.500ns		41.000ns	1.600ns		38.000ns	0.400ns		41.000ns	1.500ns	

Figure 4-6: PCLK to Data and Control Signal Output Timing - SDR Mode 2

I/O Timing Specs:

DDR Mode:



10b3G Mode

	3.3V						1.8V					
	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload	toh	tr/tf (min)	Cload	tod	tr/tf (max)	Cload
dbus	0.450ns	0.400ns	6 pF	1.900ns	1.500ns	15 pF	0.400ns	0.300ns	6 pF	1.800ns	1.100ns	15 pF
stat	0.450ns	0.500ns		2.200ns	1.600ns		0.450ns	0.400ns		2.500ns	1.500ns	

Figure 4-7: PCLK to Data and Control Signal Output Timing - DDR Mode

The GS2961 has a 20-bit output parallel bus, which can be configured for different output formats as shown in Table 4-5.

Table 4-5: GS2961 Output Video Data Format Selections

Output Data Format	Pin/Register Bit Settings					DOUT[9:0]	DOUT[19:10]
	20BIT /10BIT	RATE_ SEL0	RATE_ SEL1	SMPTE_ BYPASS	DVB-ASI		
20-bit demultiplexed HD format	HIGH	LOW	LOW	HIGH	LOW	Chroma	Luma
20-bit data output HD format	HIGH	LOW	LOW	LOW	LOW	DATA	DATA
20-bit demultiplexed SD format	HIGH	HIGH	X	HIGH	LOW	Chroma	Luma
20-bit data output SD format	HIGH	HIGH	X	LOW	LOW	DATA	DATA
10-bit multiplexed 3G DDR format	LOW	LOW	HIGH	HIGH	LOW	Driven LOW	Data Stream One/ Data Stream Two*
10-bit multiplexed HD format	LOW	LOW	LOW	HIGH	LOW	Driven LOW	Luma/Chroma

Table 4-5: GS2961 Output Video Data Format Selections

Output Data Format	Pin/Register Bit Settings					DOUT[9:0]	DOUT[19:10]
	20BIT /10BIT	RATE_ SEL0	RATE_ SEL1	SMPTE_ BYPASS	DVB-ASI		
10-bit data output HD format	LOW	LOW	LOW	LOW	LOW	Driven LOW	DATA
10-bit multiplexed SD format	LOW	HIGH	X	HIGH	LOW	Driven LOW	Luma/Chroma
10-bit data output SD format	LOW	HIGH	X	LOW	LOW	Driven LOW	DATA
20-bit demultiplexed 3G format	HIGH	LOW	HIGH	HIGH	LOW	Data Stream Two*	Data Stream One*
DVB-ASI format	LOW	HIGH	X	–	HIGH	DOUT19 = WORD_ERR DOUT18 = SYNC_OUT DOUT17 = H_OUT DOUT16 = G_OUT DOUT15 = F_OUT DOUT14 = E_OUT DOUT13 = D_OUT DOUT12 = C_OUT DOUT11 = B_OUT DOUT10 = A_OUT	

*In 3G Mode, the data streams can be swapped at the output through the host interface.

NOTE: When in Auto Mode, swap RATE_SEL with RATE_DET.

4.9.2 Parallel Output in SMPTE Mode

When the device is operating in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB_ASI = LOW), data is output in either Multiplexed or Demultiplexed form depending on the setting of the 20bit/$\overline{\text{10bit}}$ pin.

When operating in 20-bit mode (20bit/$\overline{\text{10bit}}$ = HIGH), the output data is demultiplexed Luma and Chroma data for SD and HD data rates, and Data Stream 1 and Data Stream 2 for the 3G data.

When operating in 10-bit mode (20bit/$\overline{\text{10bit}}$ = LOW), the output data is multiplexed Luma and Chroma data for SD and HD data rates, and multiplexed Data Stream 1 and Data Stream 2 for the 3G data. In this mode, the data is presented on the DOUT[19:10] pins, with DOUT[9:0] being forced LOW.

4.9.3 Parallel Output in DVB-ASI Mode

In DVB-ASI mode, the 20bit/$\overline{\text{10bit}}$ pin must be set LOW to configure the output parallel bus for 10-bit operation.

DVB-ASI mode is enabled when the AUTO/$\overline{\text{MAN}}$ bit is LOW, $\overline{\text{SMPTE\_BYPASS}}$ pin is LOW and the DVB_ASI pin is HIGH.

The extracted 8-bit data is presented on DOUT[17:10] such that DOUT[17:10] = HOUT ~ AOUT, where AOUT is the least significant bit of the decoded transport stream data.

In addition, the DOUT19 and DOUT18 pins are configured as DVB-ASI status signals WORDERR and SYNCOUT respectively.

SYNCOUT is HIGH whenever a K28.5 sync character is output from the device.

WORDERR is HIGH whenever the device has detected a running disparity error or illegal code word.

4.9.4 Parallel Output in Data-Through Mode

This mode is enabled when the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins are LOW.

In this mode, data is passed to the output bus without any decoding, descrambling or word-alignment.

The output data width (10-bit or 20-bit) is controlled by the setting of the 20bit/$\overline{\text{10bit}}$ pin.

4.9.5 Parallel Output Clock (PCLK)

The frequency of the PCLK output signal of the GS2961 is determined by the output data rate and the 20bit/$\overline{\text{10bit}}$ pin setting. Table 4-6 lists the output signal formats according to the data format selected in Manual mode (AUTO/$\overline{\text{MAN}}$ bit in the host interface is set LOW), or detected in Auto Mode (AUTO/$\overline{\text{MAN}}$ bit in the host interface is set HIGH).

Table 4-6: GS2961 PCLK Output Rates

Output Data Format	Pin/Control Bit Settings					PCLK Rate
	20bit/$\overline{\text{10bit}}$	RATE_DET0	RATE_DET1	$\overline{\text{SMPTE\_BYPASS}}$	DVB-ASI	
20-bit demultiplexed HD format	HIGH	LOW	LOW	HIGH	LOW	74.25 or 74.25/1.001MHz
20-bit data output HD format	HIGH	LOW	LOW	LOW	LOW	74.25 or 74.25/1.001MHz
20-bit demultiplexed SD format	HIGH	HIGH	X	HIGH	LOW	13.5MHz
20-bit data output SD format	HIGH	HIGH	X	LOW	LOW	13.5MHz
20-bit demultiplexed 3G format	HIGH	LOW	HIGH	HIGH	LOW	148.5 or 148.5/1.001MHz
10-bit multiplexed 3G DDR format	LOW	LOW	HIGH	HIGH	LOW	148.5 or 148.5/1.001MHz
10-bit multiplexed HD format	LOW	LOW	LOW	HIGH	LOW	148.5 or 148.5/1.001MHz
10-bit data output HD format	LOW	LOW	LOW	LOW	LOW	148.5 or 148.5/1.001MHz

Table 4-6: GS2961 PCLK Output Rates

Output Data Format	Pin/Control Bit Settings					PCLK Rate
	20bit/ $\overline{\text{10bit}}$	RATE_DET0	RATE_DET1	$\overline{\text{SMPTE\_BYPASS}}$	DVB-ASI	
10-bit multiplexed SD format	LOW	HIGH	X	HIGH	LOW	27MHz
10-bit data output SD format	LOW	HIGH	X	LOW	LOW	27MHz
10-bit ASI output SD format	LOW	HIGH	X	LOW	HIGH	27MHz

4.9.6 DDR Parallel Clock Timing

The GS2961 has the ability to transmit 10-bit parallel video data with a DDR (Dual Data Rate) pixel clock over a single-ended interface. DDR Mode can be enabled when the SDI data bandwidth is 3Gb/s. In this case, the 10-bit parallel data rate is 297Mb/s, and the frequency of the DDR clock is 148.5MHz (10-bit output in 3G mode).

The DDR pixel clock avoids the need to operate a high-drive pixel clock at 297MHz. This reduces power consumption, clock drive strength, and noise generation, and precludes from generating excessive EMI had PCLK on the board have to run at 297MHz. It also enables easier board routing and avoids the need to use the higher-speed I/Os on FPGAs, which may require more expensive speed grades.

Figure 4-8 shows how the DDR interface operates. The pixel clock is transmitted at half the data rate, and the interleaved data is sampled at the receiver on both clock edges.

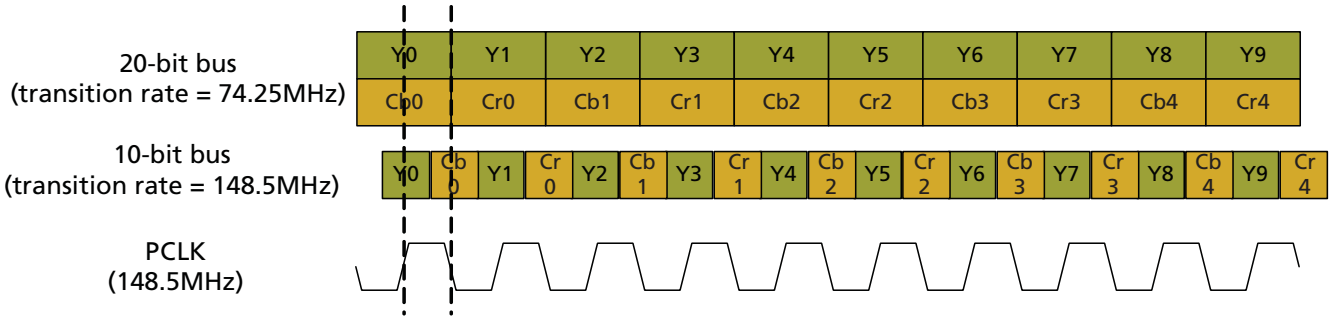


Figure 4-8: DDR Video Interface

The GS2961 has the ability to shift the Setup/Hold window on the receive interface, by using an on-chip delay line to shift the phase of PCLK with respect to the data bus.

The timing of the PCLK output, relative to the data, can be adjusted through the host interface registers. Address 06Ch contains the delay line controls:

Bit[5] (DEL_LINE_CLK_SEL) is a coarse delay adjustment that selects between the default (nominal) PCLK phase and a quadrature phase, for a 90° phase shift.

Bits[4:0] (DEL_LINE_OFFSET) comprise a fine delay adjustment to shift the PCLK in 40ps increments (typical conditions). The maximum fine delay adjustment is approximately 1.2ns under nominal conditions.

An example delay adjustment over min/typ/max conditions is illustrated in Figure 4-9. The target delay is 0.84 ns under typical conditions (approximately 45° PCLK phase shift), and requires a control word setting of 0x0014 for address 0x006C.

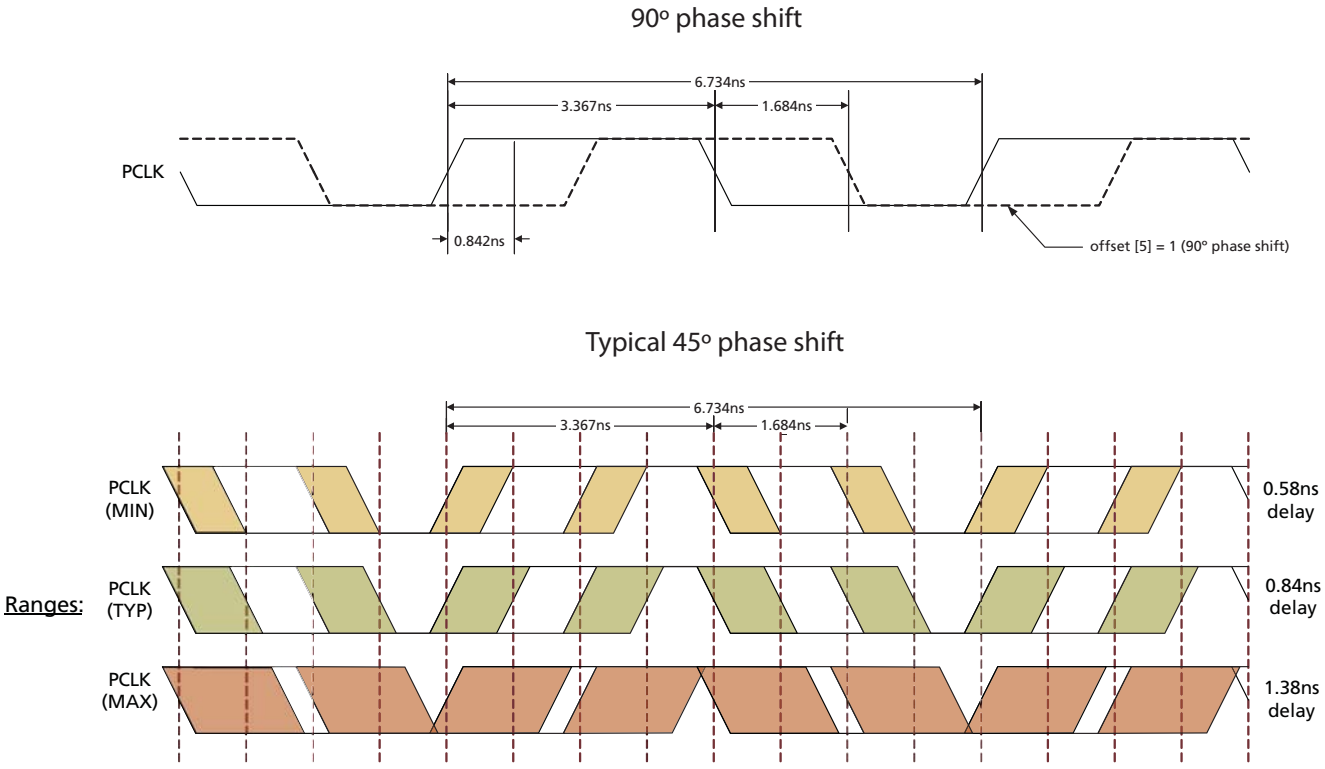


Figure 4-9: Delay Adjustment Ranges

4.10 Timing Signal Generator

The GS2961 has an internal timing signal generator which is used to generate digital FVH timing reference signals, to detect and correct certain error conditions and automatic video standard detection.

The timing signal generator is only operational in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH).

The timing signal generator consists of a number of counters and comparators operating at video pixel and video line rates. These counters maintain information about the total line length, active line length, total number of lines per field/frame and total active lines per field/frame for the received video standard.

It takes one video frame to obtain full synchronization to the received video standard.

NOTE: Both 8-bit and 10-bit TRS words are identified by the device. Once synchronization has been achieved, the timing signal generator continues to monitor the received TRS timing information to maintain synchronization.

The timing signal generator re-synchronizes all pixel and line based counters on every received TRS ID. Note that for correct operation of the timing signal generator, the SW_EN input pin must be set LOW, unless manual synchronous switching is enabled (Section 4.10.1).

4.10.1 Manual Switch Line Lock Handling

The principle of switch line lock handling is that the switching of synchronous video sources will only disturb the horizontal timing and alignment, whereas the vertical timing remains in synchronization - i.e. switching between video sources of the same format.

To account for the horizontal disturbance caused by a synchronous switch, the word alignment block and timing signal generator automatically re-synchronizes to the new timing immediately if the synchronous switch happens during the designated switch line, as defined in SMPTE recommended practice RP168-2002.

The device samples the SW_EN pin on every PCLK cycle. When a Logic LOW to HIGH transition on this pin is detected anywhere within the active line, the word alignment block and timing signal generator re-synchronize immediately to the next TRS word.

This allows the system to force immediate lock on any line, if the switch point is non-standard.

To ensure proper switch line lock handling, the SW_EN signal should be asserted HIGH anywhere within the active portion of the line on which the switch has taken place, and should be held HIGH for approximately one video line. After this time period, SW_EN should be de-asserted. SW_EN should be held LOW during normal device operation.

NOTE: It is the rising edge of the SW_EN signal, which generates the switch line lock re-synchronization. This edge must be in the active portion of the line containing the video switch point.

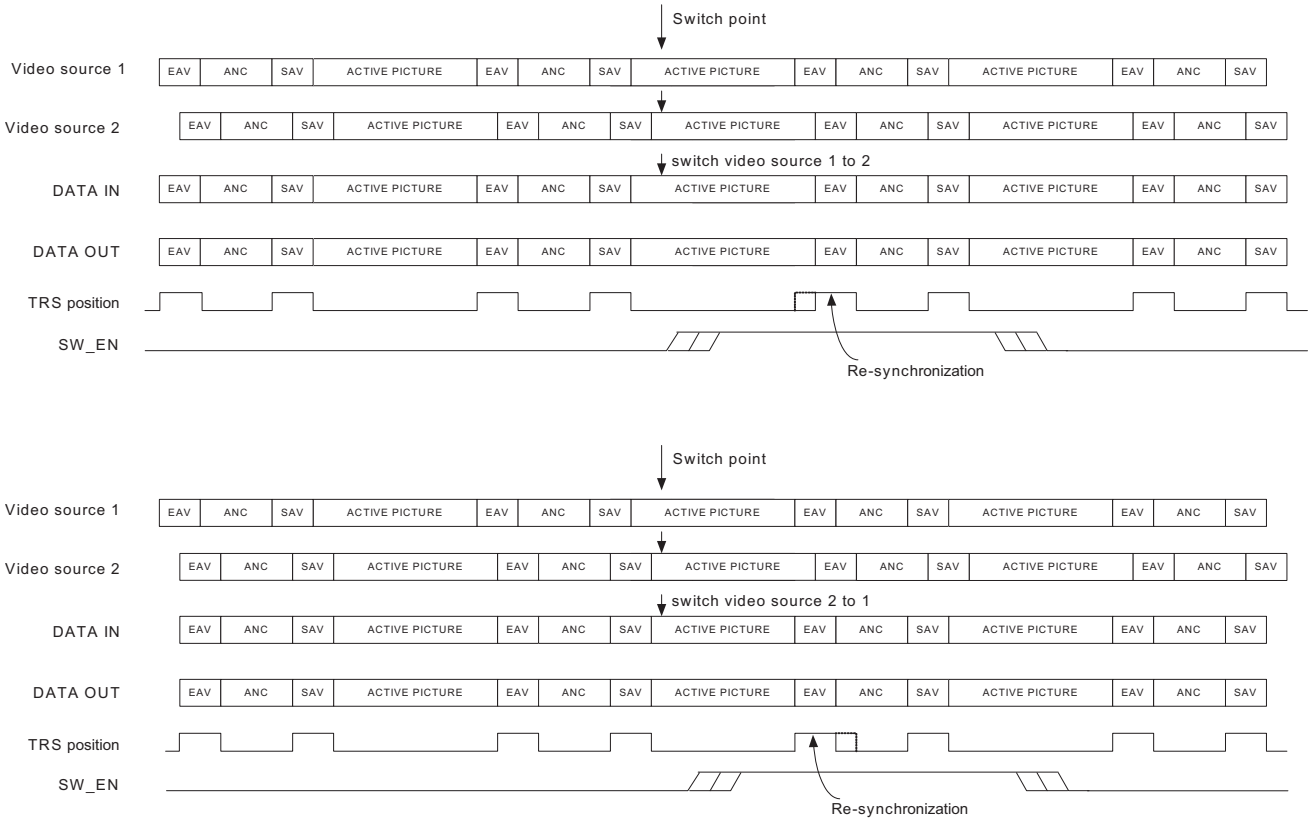


Figure 4-10: Switch Line Locking on a Non-Standard Switch Line

4.10.2 Automatic Switch Line Lock Handling

The synchronous switch point is defined for all major video standards in SMPTE RP168-2002. The device automatically re-synchronizes the word alignment block and timing signal generator at the switch point, based on the detected video standard.

The device, as described in Section 4.10.1 and Figure 4-10 above, implements the re-synchronization process automatically, every field/frame. The switch line is defined as follows:

- For 525 line interlaced systems: resynchronization takes place at then end of lines 10 & 273
- For 525 line progressive systems: resynchronization takes place at then end of line 10
- For 625 line interlaced systems: resynchronization takes place at then end of lines 6 & 319
- For 625 line progressive systems: resynchronization takes place at then end of line 6
- For 750 line progressive systems: resynchronization takes place at then end of line 7
- For 1125 line interlaced systems: resynchronization takes place at then end of lines 7 & 568
- For 1125 line progressive systems: resynchronization takes place at then end of line 7

NOTE: Unless indicated by SMPTE 352M payload identifier packets, the GS2961 does not distinguish between 1125-line progressive segmented-frame (PsF) video and

1125-line interlaced video operating at 25 or 30fps. However. PsF video operating at 24fps is detected by the device.

A full list of all major video standards and switching lines is shown in Table 4-7.

4.10.3 Switch Line Lock Handling During Level B to Level A Conversion

When 3G data is detected by the GS2961, and Level B to Level A conversion is enabled, the device only supports a limited phase offset between two synchronous video sources if a synchronous switch is implemented.

If the synchronous switch point results in an "extended" active video period, the GS2961 only re-synchronizes to the following TRS ID if the phase difference between the two sources is less than or equal to 10µs. If the phase difference is greater than 10µs, the GS2961 takes one additional line to re-synchronize. In this case, the user may observe a missing H pulse on the line following the switch line, on the H timing output.

Note that this 10µs constraint is only valid when Level B to Level A conversion is enabled, and only when the synchronous switch point results in an extended active video area.

Table 4-7: Switch Line Position for Digital Systems

System	Frame Rate & Structure	Pixel Structure		Signal Standard	Parallel Interface	Serial Interface	Line No.
1125	60/P	1920x1080	4:2:2	274M + RP211		292	7
	50/P			274M + RP211			
	60/I			274M + RP211			7/569
	50/I			274M + RP211			
	30/P			274M + RP211			7
	25/P			274M + RP211			
	24/P			274M + RP211			
	30/PsF			274M + RP211			
	25/PsF			274M + RP211			
	24/PsF			274M + RP211			
750	60/P	1280x720	4:2:2	296M		292	7
	50/P			296M			
	30/P			296M			
	25/P			296M			
	24/P			296M			

Table 4-7: Switch Line Position for Digital Systems

System	Frame Rate & Structure	Pixel Structure		Signal Standard	Parallel Interface	Serial Interface	Line No.
625	50/P	720x576	4:2:2	BT.1358	349M	292	6
				BT.1358	347M	344M	
				BT.1358	BT.1358	BT.1362	
			4:2:0	BT.1358	349M	292	
				BT.1358	BT.1358	BT.1362	
	50/I	960x576	4:2:2	BT.601	349M	292	6/319
				BT.601	BT.656	259M	
		720x576	4:4:4:4	BT.799	349M	292	
				BT.799	347M	344M	
				BT.799	BT.799	344M	
				BT.799	BT.799	–	
			4:2:2	BT.601	349M	292	
				BT.601	125M	259M	
525	59.94/P	720x483	4:2:2	293M	349M	292	10
				293M	347M	344M	
				293M	293M	294M	
			4:2:0	293M	349M	292	
				293M	293M	294M	
	59.94/I	960x483	4:2:2	267M	349M	292	10/273
				267M	267M	259M	
		720x483	4:4:4	267M	349M	292	
				267M	347M	344M	
				267M	RP174	344M	
				267M	RP175	RP175	
			4:2:2	125M	349M	292	
				125M	125M	259M	
HD-SDTI	P or PsF structure	1920x1080	4:2:2	274M	274M + 348M	292	7
	I structure			274M			7/569
	P structure	1280x720		296M	296M + 348M		7
SDTI	50/I	720x576	4:2:2	BT.656	BT.656 + 305M	259M	6/319
	59.94/I	720x483		125M	125M + 305M		10/273

4.11 Programmable Multi-function Outputs

The GS2961 has 6 multi-function output pins, STAT [5:0], which are programmable via the host interface to output one of the following signals:

Table 4-8: Output Signals Available on Programmable Multi-Function Pins

Status Signal	Selection Code	Default Output Pin
H/HSYNC (according to TIM_861 Pin) Section 4.12	0000	STAT 0
V/VSYNC (according to TIM_861 Pin) Section 4.12	0001	STAT 1
F/DE (according to TIM_861 Pin) Section 4.12	0010	STAT 2
LOCKED Section 4.7	0011	STAT 3
Y/1ANC Section 4.17	0100	STAT 4
C/2ANC Section 4.17	0101	–
$\overline{\text{DATA ERROR}}$ Section 4.16	0110	STAT 5
EDH DETECTED	1001	–
CARRIER DETECT	1010	–
RATE_DET0	1011	–
RATE_DET1	1100	–

Each of the STAT[5:0] pins are configurable individually using the register bits in the host interface; STAT[5:0]_CONFIG (008h/009h).

4.12 H:V:F Timing Signal Generation

The GS2961 extracts critical timing parameters from the received TRS words.

Horizontal blanking (H), Vertical blanking (V), and Field odd/even (F) timing are output on the STAT[2:0] pins by default.

Using the H_CONFIG bit in the host interface, the H signal timing can be selected as one of the following:

1. Active line blanking (H_CONFIG = LOW) - the H output is HIGH for the horizontal blanking period, including the EAV TRS words.
2. TRS based blanking (H_CONFIG = HIGH) - the H output is set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS signals.

The timing of these signals is shown in Figure 4-14 below.

NOTE: Both 8-bit and 10-bit TRS words are identified by the device.

Figure 4-11: H:V:F Output Timing - 3G Level A and HDTV 20-bit Mode

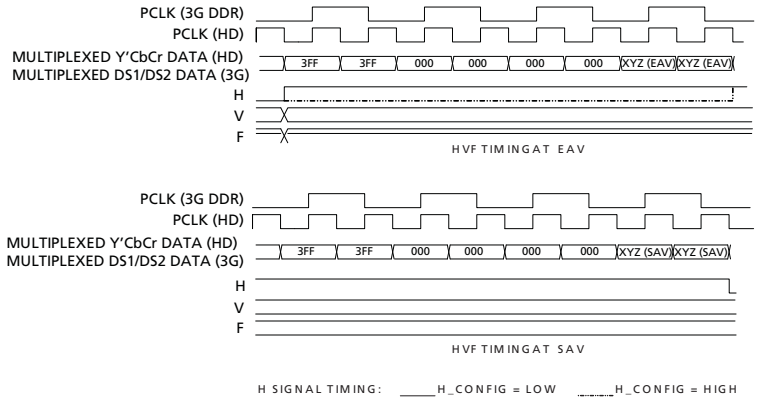


Figure 4-12: H:V:F Output Timing - 3G Level A and HDTV 10-bit Mode
3G Level B 20-bit Mode, each 10-bit stream

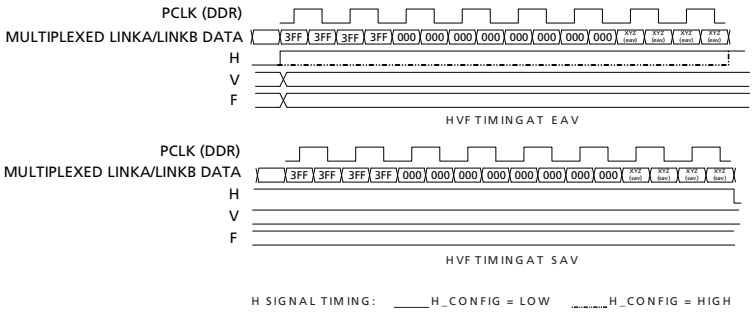


Figure 4-13: H:V:F Output Timing - 3G Level B 10-bit Mode

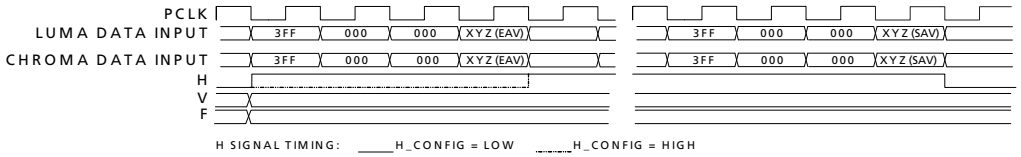


Figure 4-14: H:V:F Output Timing - HD 20-bit Output Mode

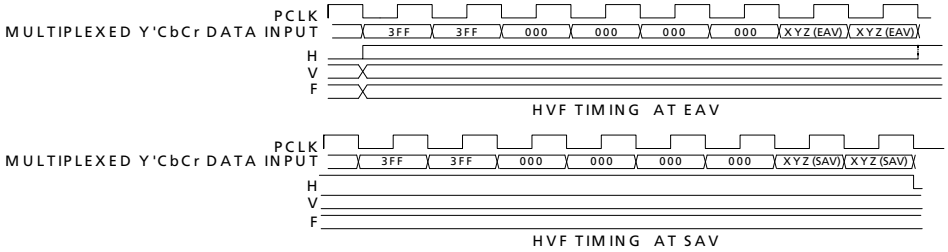


Figure 4-15: H:V:F Output Timing - HD 10-bit Output Mode

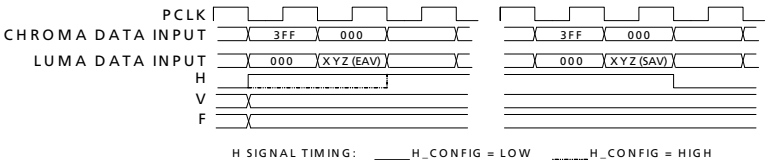


Figure 4-16: H:V:F Output Timing - SD 20-bit Output Mode

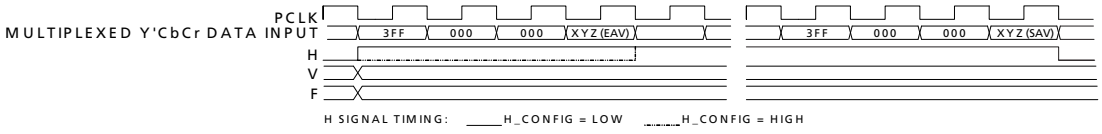


Figure 4-17: H:V:F Output Timing - SD 10-bit Output Mode

4.12.1 CEA-861 Timing Generation

The GS2961 is capable of generating CEA 861 timing instead of SMPTE HVF timing for all of the supported video formats.

This mode is selected when the TIM_861 pin is HIGH.

Horizontal sync (HSYNC), Vertical sync (VSYNC), and Data Enable (DE) timing are output on the STAT[2:0] pins by default.

Table 4-9 shows the CEA-861 formats supported by the GS2961:

Table 4-9: Supported CEA-861 Formats

Format	CEA-861 Format	VD_STD[5:0]
720(1440) x 480i @ 59.94/60Hz	6 & 7	16h, 17h, 19h, 1Bh
720(1440) x 576i @ 50Hz	21 & 22	18h, 1Ah
1280 x 720p @ 59.94/60Hz	4	20h, 00h
1280 x 720p @ 50Hz	19	24h, 04h
1920 x 1080i @ 59.94/60Hz	5	2Ah, 0Ah
1920 x 1080i @ 50Hz	20	2Ch, 0Ch
1920 x 1080p @ 29.97/30Hz	34[1]	2Bh, 0Bh
1920 x 1080p @ 25Hz	33[2]	2Dh, 0Dh
1920 x 1080p @ 23.98/24Hz	32	30h, 10h
1920 x 1080p @ 59.94/60Hz	16[1]	2Bh
1920 x 1080p @ 50Hz	31[2]	2Dh

NOTES:
1,2: Timing is identical for the corresponding formats.

4.12.1.1 Vertical Timing

When CEA861 timing is selected, the device outputs standards compliant CEA861 timing signals as shown in the figures below; for example 240 active lines per field for SMPTE 125M.

The register bit TRS_861 is used to select DFP timing generator mode which follows the vertical blanking timing as defined by the embedded TRS code words. This setting is helpful for 525i. When TRS_861 is set LOW, DE will go HIGH for 480 lines out of 525. When TRS_861 is set HIGH, DE will go HIGH for 487 lines out of 525.

The timing of the CEA 861 timing reference signals can be found in the CEA 861 specificaitons. For information, they are included in the following diagrams. These diagrams may not be comprehensive.

Table 4-10: CEA861 Timing Formats

Format	Parameters
4	H:V:DE Input Timing 1280 x 720p @ 59.94/60Hz
5	H:V:DE Input Timing 1920 x 1080i @ 59.94/60Hz
6&7	H:V:DE Input Timing 720 (1440) x 480i @ 59.94/60Hz
19	H:V:DE Input Timing 1280 x 720p @ 50Hz
20	H:V:DE Input Timing 1920 x 1080i @ 50Hz
21&22	H:V:DE Input Timing 720 (1440) x 576 @ 50Hz
16	H:V:DE Input Timing 1920 x 1080p @ 59.94/60Hz
31	H:V:DE Input Timing 1920 x 1080p @ 50Hz
32	H:V:DE Input Timing 1920 x 1080p @ 23.94/24Hz
33	H:V:DE Input Timing 1920 x 1080p @ 25Hz
34	H:V:DE Input Timing 1920 x 1080p @ 29.97/30Hz

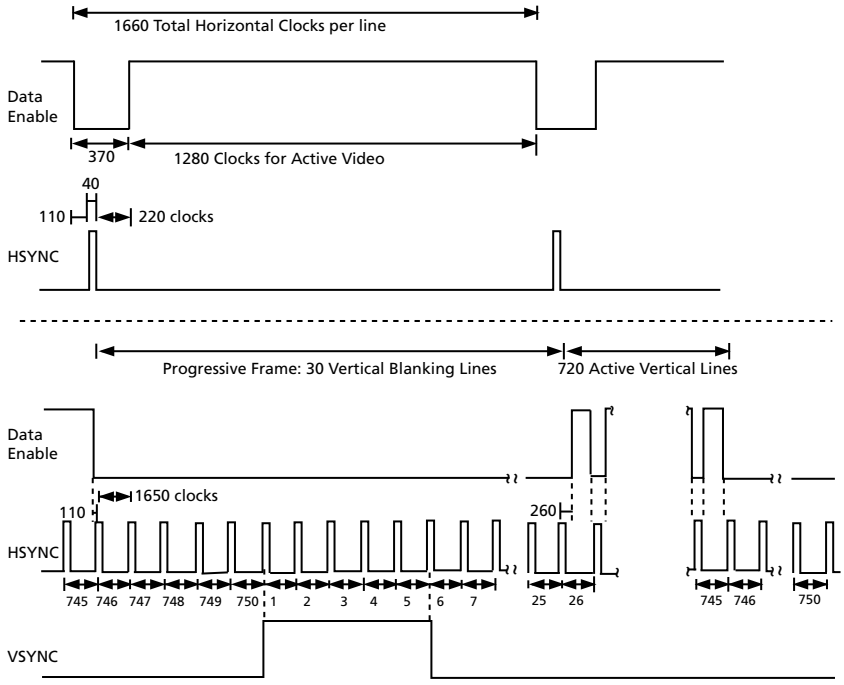


Figure 4-18: H:V:DE Output Timing 1280 x 720p @ 59.94/60 (Format 4)

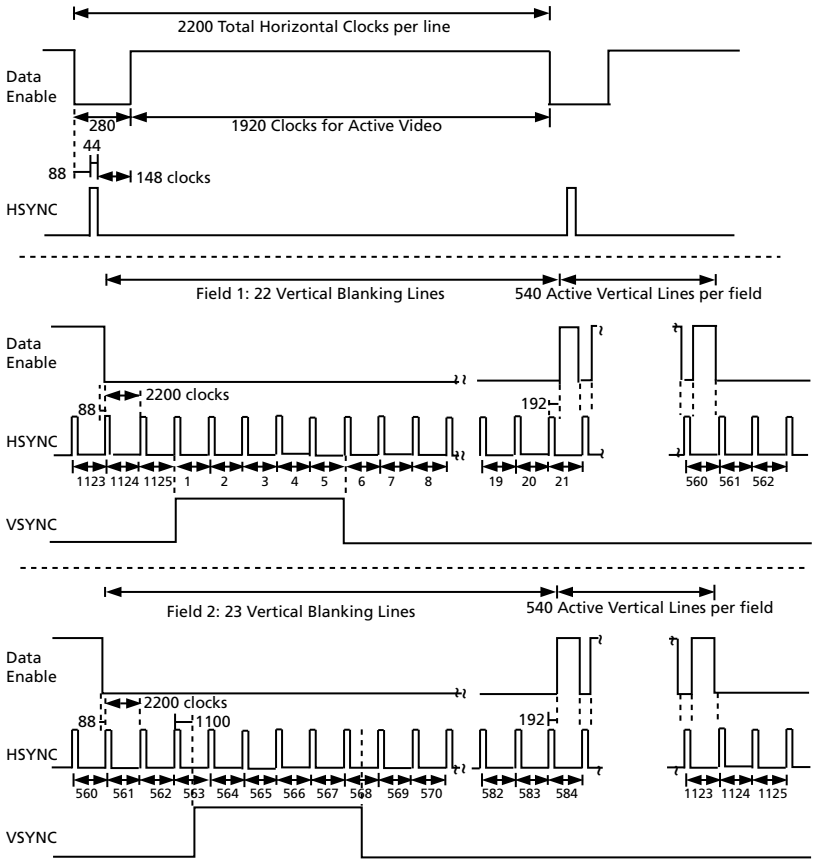


Figure 4-19: H:V:DE Output Timing 1920 x 1080i @ 59.94/60 (Format 5)

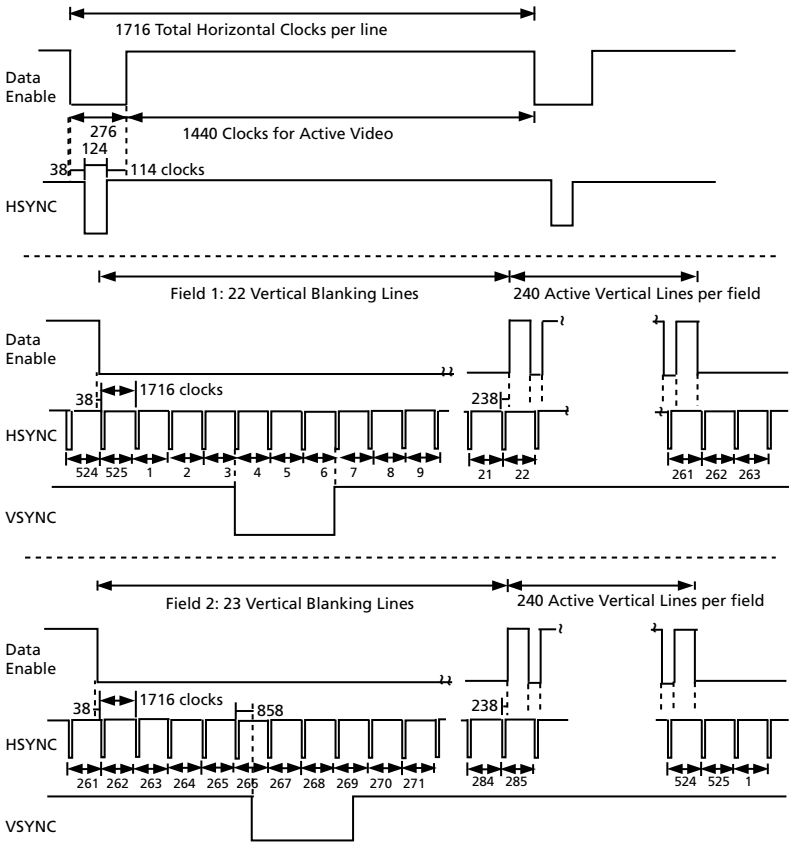


Figure 4-20: H:V:DE Output Timing 720 (1440) x 480i @ 59.94/60 (Format 6&7)

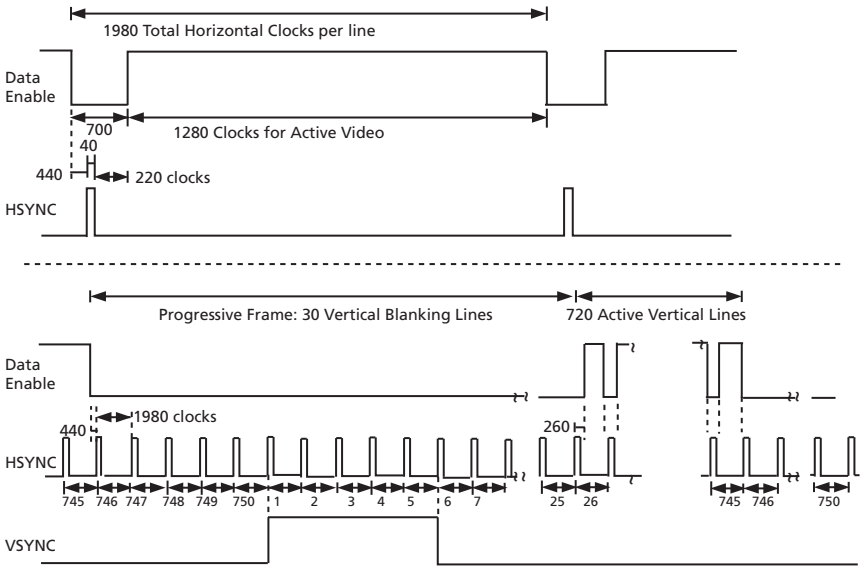


Figure 4-21: H:V:DE Output Timing 1280 x 720p @ 50 (Format 19)

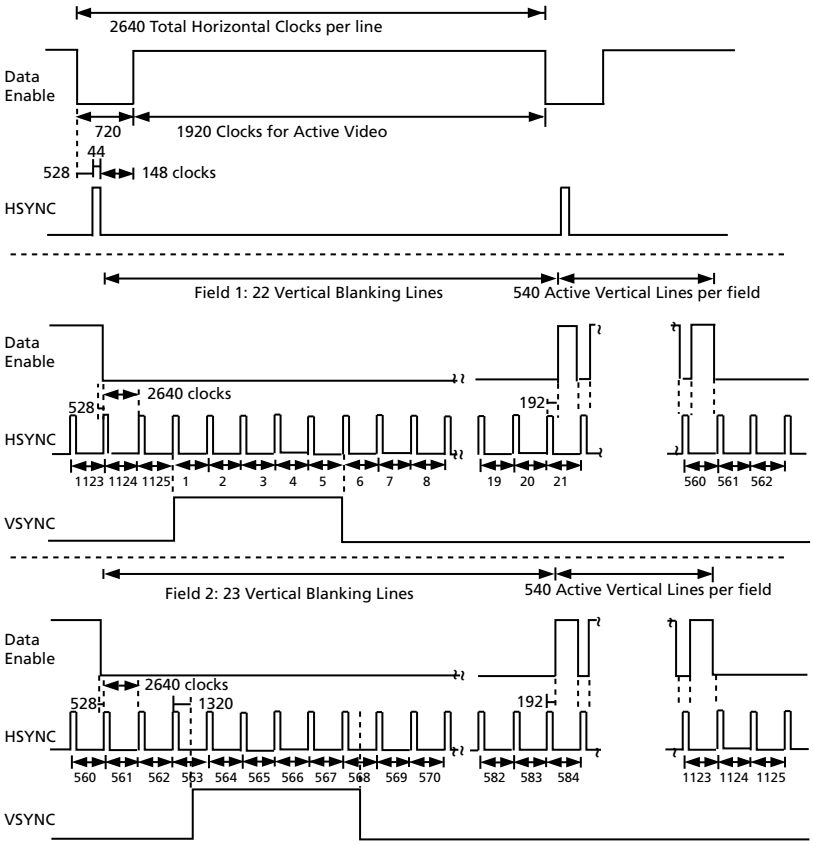


Figure 4-22: H:V:DE Output Timing 1920 x 1080i @ 50 (Format 20)

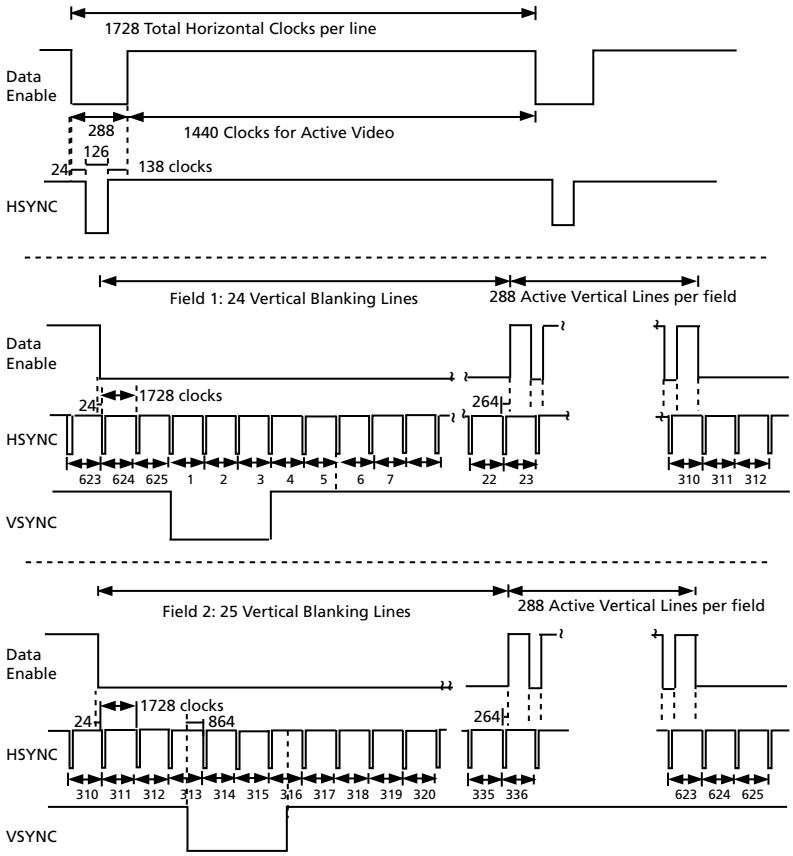


Figure 4-23: H:V:DE Output Timing 720 (1440) x 576 @ 50 (Format 21 & 22)

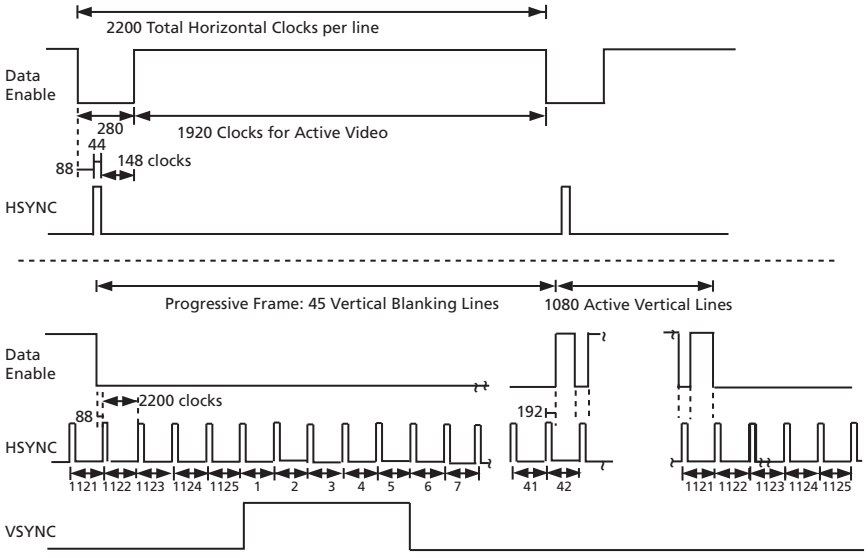


Figure 4-24: H:V:DE Output Timing 1920 x 1080p @ 59.94/60 (Format 16)

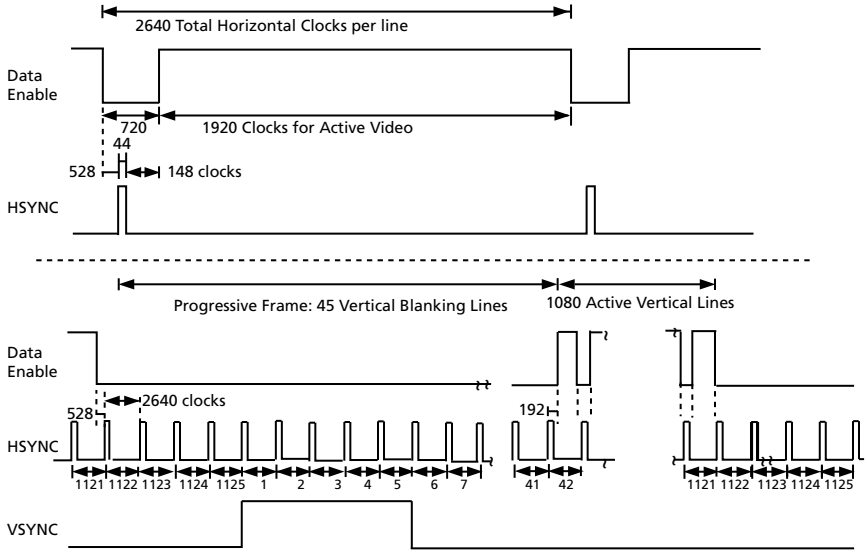


Figure 4-25: H:V:DE Output Timing 1920 x 1080p @ 50 (Format 31)

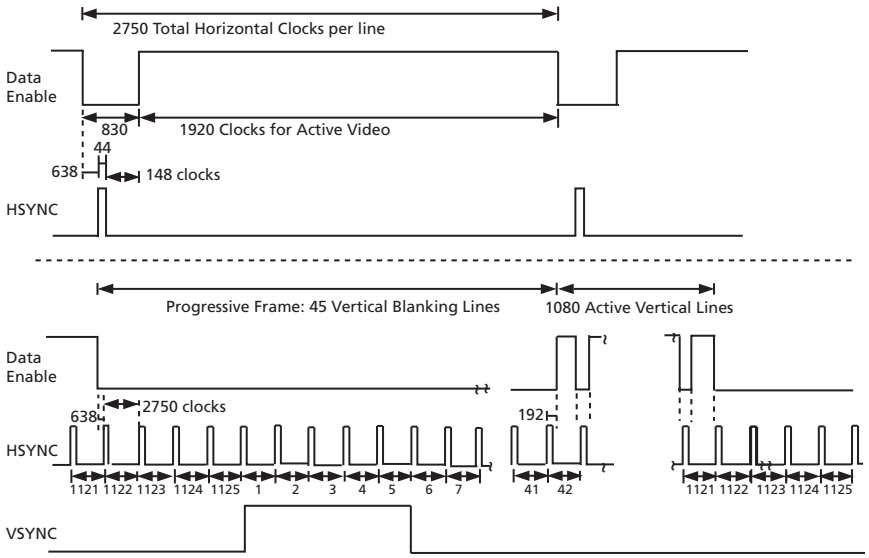


Figure 4-26: H:V:DE Output Timing 1920 x 1080p @ 23.94/24 (Format 32)

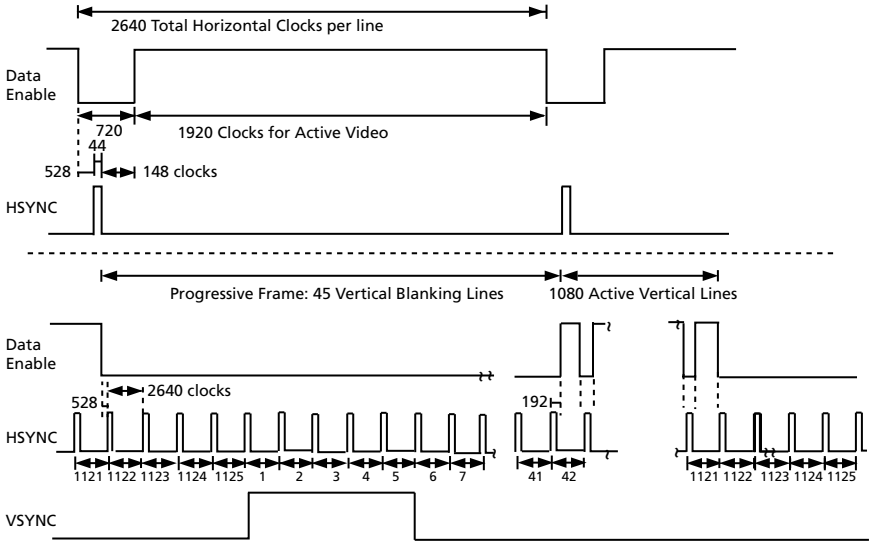


Figure 4-27: H:V:DE Output Timing 1920 x 1080p @ 25 (Format 33)

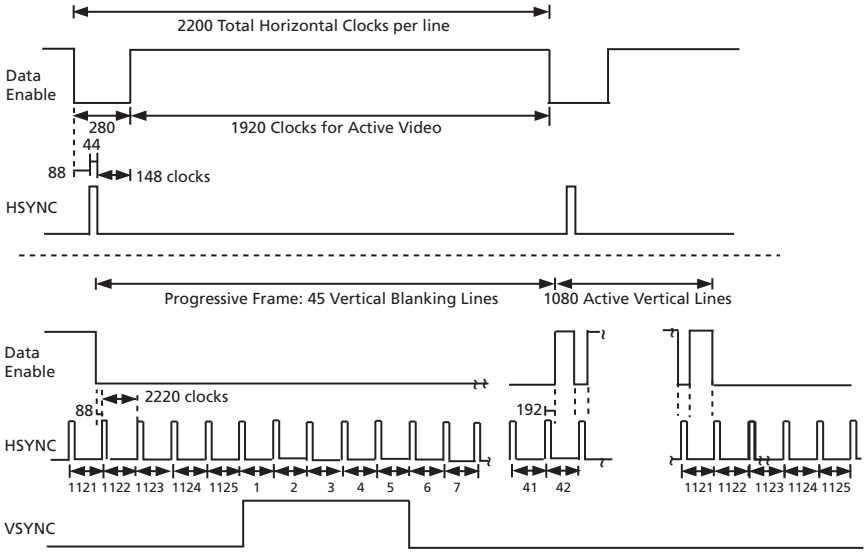


Figure 4-28: H:V:DE Output Timing 1920 x 1080p @ 29.97/30 (Format 34)

4.13 Automatic Video Standards Detection

Using the timing extracted from the received TRS signals, the GS2961 is able to identify the received video standard.

In 3G input mode, the GS2961 measures the timing parameters of one of the two identical data streams. The Rate Selection/Indication bits and the VD_STD code may be used in combination to determine the video standard.

The total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are all measured.

Four registers are provided to allow the system to read the video standard information from the device. These raster structure registers are provided in addition to the VIDEO_FORMAT_352_A_X and VIDEO_FORMAT_352_B_X registers, and are updated once per frame at the end of line 12.

The raster structure registers also contain three status bits: STD_LOCK, INT/$\overline{\text{PROG}}$ and M. The STD_LOCK bit is set HIGH whenever the timing signal generator is fully synchronized to the incoming standard, and detects it as one of the supported formats. The INT/$\overline{\text{PROG}}$ bit is set HIGH if the detected video standard is interlaced and LOW if the detected video standard is progressive. M is set HIGH if the clock frequency includes the "1000/1001" factor denoting a 23.98, 29.97 or 59.94Hz frame rate.

The video standard code is reported in the VD_STD bits of the host interface register. Table 4-11 describes the 5-bit codes for the recognized video standards.

Table 4-11: Supported Video Standard Codes

SMPTE Standard	Active Video Area	RATE_DET[1] $\overline{\text{HD}}$/3G	RATE_DET[0] SD/$\overline{\text{HD}}$	Lines per Field	Active Lines per Field	Words per Active Line	Words per Line	VD_STD [5:0]
425M (3G) 4:2:2	1920x1080/60 (1:1)	1	0	1125	1080	1920	2200	2Bh
	1920x1080/50 (1:1)	1	0	1125	1080	1920	2640	2Dh
425M (3G) 4:4:4	1920x1080/60 (2:1) or 1920x1080/30 (PsF)	1	0	1125	1080	3840	4400	2Ah
	1920x1080/50 (2:1) or 1920x1080/25 (PsF)	1	0	1250	1080	3840	5280	2Ch
	1280x720/60 (1:1)	1	0	750	720	2560	3300	20h
	1280x720/50 (1:1)	1	0	750	720	2560	3960	24h
	1920x1080/30 (1:1)	1	0	1125	1080	3840	4400	2Bh
	1920x1080/25 (1:1)	1	0	1125	1080	3840	5280	2Dh
	1280x720/25 (1:1)	1	0	750	720	2560	7920	26h
	1920x1080/24 (1:1)	1	0	1125	1080	3840	5500	30h
	1280x720/24 (1:1)	1	0	750	720	2560	8250	28h
260M (HD)	1920x1035/60 (2:1)	0	0	1125	1035	1920	2200	15h
295M (HD)	1920x1080/50 (2:1)	0	0	1250	1080	1920	2376	14h

Table 4-11: Supported Video Standard Codes

SMPTE Standard	Active Video Area	RATE_DET[1] HD/3G	RATE_DET[0] SD/HD	Lines per Field	Active Lines per Field	Words per Active Line	Words per Line	VD_STD [5:0]
274M (HD)	1920x1080/60 (2:1) or 1920x1080/30 (PsF)	0	0	1125	1080	1920	2200	0Ah
	1920x1080/50 (2:1) or 1920x1080/25 (PsF)	0	0	1250	1080	1920	2640	0Ch
	1920x1080/30 (1:1)	0	0	1125	1080	1920	2200	0Bh
	1920x1080/25 (1:1)	0	0	1125	1080	1920	2640	0Dh
	1920x1080/24 (1:1)	0	0	1125	1080	1920	2750	10h
	1920x1080/24 (PsF)	0	0	1125	1080	1920	2750	11h
	1920x1080/25 (1:1) –	0	0	1125	1080	2304	2640	0Eh
	1920x1080/25 (PsF) – EM	0	0	1125	1080	2304	2640	0Fh
	1920x1080/24 (1:1) –	0	0	1125	1080	2400	2750	12h
	1920x1080/24 (PsF) – EM	0	0	1125	1080	2400	2750	13h
296M (HD)	1280x720/30 (1:1)	0	0	750	720	1280	3300	02h
	1280x720/30 (1:1) – EM	0	0	750	720	2880	3300	03h
	1280x720/50 (1:1)	0	0	750	720	1280	1980	04h
296M (HD)	1280x720/50 (1:1) – EM	0	0	750	720	1728	1980	05h
	1280x720/25 (1:1)	0	0	750	720	1280	3960	06h
	1280x720/25 (1:1) – EM	0	0	750	720	3456	3960	07h
	1280x720/24 (1:1)	0	0	750	720	1280	4125	08h
	1280x720/24 (1:1) – EM	0	0	750	720	3600	4125	09h
	1280x720/60 (1:1)	0	0	750	720	1280	1650	00h
	1280x720/60 (1:1) – EM	0	0	750	720	1440	1650	01h
125M (SD)	1440x487/60 (2:1)	x	1	525	244 or 243	1440	1716	16h
	1440x507/60	x	1	525	254 or 253	1440	1716	17h
	525-line 487 generic	x	1	525	–	–	1716	19h
	525-line 507 generic	x	1	525	–	–	1716	1Bh

Table 4-11: Supported Video Standard Codes

SMPTE Standard	Active Video Area	RATE_DET[1] HD/3G	RATE_DET[0] SD/HD	Lines per Field	Active Lines per Field	Words per Active Line	Words per Line	VD_STD [5:0]
ITU-R BT.656 (SD)	1440x576/50 (2:1) Or dual link progressive)	x	1	625	–	1440	1728	18h
	625-line generic	x	1	625	–	–	1728	1Ah
Unknown HD	SD/HD = 0	0	0	–	–	–	–	1Dh
Unknown SD	SD/HD = 1	x	1	–	–	–	–	1Eh
Unknown 3G	SD/HD = 0	1	0	–	–	–	–	3Ch
Reserved		–	–	–	–	–	–	1Fh

Notes:

1. The Line Numbers in brackets refer to version zero SMPTE 352M packet locations, if they are different from version 1.
2. The part may provide full or limited functionality with standards that are not included in this table. Please consult a Gennum technical representative.

NOTE: The part may provide full or limited functionality with standards that are not included in this table. Please consult a Gennum technical representative.

By default (after power up or after systems reset), the four RASTER_STRUCTURE, VD_STD, STD_LOCK and INT/PROG fields are set to zero. These fields are also cleared when the SMPTE_BYPASS pin is LOW.

4.14 Data Format Detection & Indication

In addition to detecting the video standard, the GS2961 detects the data format, i.e. SDTI, SDI, TDM data (SMPTE 346M), etc.

This information is represented by bits in the DATA_FORMAT_DSX register accessible through the host interface.

Data format detection is only carried out when the LOCKED signal is HIGH.

By default (at power up or after system reset), the DATA_FORMAT_DSX register is set to Fh (undefined). This register is also set as undefined when the LOCKED signal is LOW and/or the SMPTE_BYPASS pin is LOW.

Table 4-12: Data Format Register Codes

YDATA_FORMAT[3:0] or CDATA_FORMAT[3:0]	Data Format	Remarks
0h ~ 05h	SDTI	SMPTE 321M, SMPTE 322M, SMPTE 326M
6h	SDI	–
7h	Reserved	–
8h	TDM	SMPTE 346M
9h	HD-SDTI	–
Ah ~ Eh	Reserved	–
Fh	Non-SMPTE data format	Detected data format is not SMPTE. $\overline{\text{SMPTE\_BYPASS}}$ = LOW *or* LOCKED = LOW

The data format is determined using the following criteria:

- If TRS ID words are detected but no SDTI header or TDM header is detected, then the data format is SDI
- If TRS ID words are detected and the SDTI header is available then the format is SDTI
- If TRS ID words are detected and the TDM data header is detected then the format is TDM video
- If DVB-ASI sync words are detected then the data format is DVB-ASI
- No TRS words or DVB-ASI sync words are detected, but the PLL is locked, then the data format is unknown

NOTE: Two data format sets are provided for HD video rates. This is because the Y and Cr/Cb channels can be used separately to carry SDTI data streams of different data formats. In SD video mode or DVB-ASI mode, only the Y data format register contains the data, and the C register is set to Fh (undefined format).

4.15 EDH Detection

4.15.1 EDH Packet Detection

The GS2961 determines if EDH packets are present in the incoming video data and asserts the EDH_DETECT status according to the SMPTE standard.

EDH_DETECT is set HIGH when EDH packets have been detected and remains HIGH until EDH packets are no longer present. It is set LOW at the end of the vertical blanking (falling edge of V) if an EDH packet has not been detected during vertical blanking.

EDH_DETECT can be programmed to be output on the multi-function output port pins. The EDH_DETECT bit is also available in the host interface.

4.15.2 EDH Flag Detection

The EDH flags for ancillary data, active picture, and full field regions are extracted from the detected EDH packets and placed in the EDH_FLAG_IN register.

When the EDH_FLAG_UPDATE_MASK bit in the host interface is set HIGH, the GS2961 updates the Ancillary Data, Full Field, and Active Picture EDH flags according to SMPTE RP165. The updated EDH flags are available in the EDH_FLAG_OUT register. The EDH packet output from the device contains these updated flags.

One set of flags is provided for both fields 1 and 2. The field 1 flag data is overwritten by the field 2 flag data.

When EDH packets are not detected, the UES flags in the EDH_FLAG_OUT register are set HIGH to signify that the received signal does not support Error Detection and Handling. In addition, the EDH_DETECT bit is set LOW. These flags are set regardless of the setting of the EDH_FLAG_UPDATE_MASK bit.

EDH_FLAG_OUT and EDH_FLAG_IN may be read via the host interface at any time during the received frame except on the lines defined in SMPTE RP165, when these flags are updated.

The GS2961 indicates the CRC validity for both active picture and full field CRCs. The AP_CRC_V bit in the host interface indicates the active picture CRC validity, and the FF_CRC_V bit indicates the full field CRC validity. When EDH_DETECT = LOW, these bits are cleared.

The EDH_FLAG_OUT and EDH_FLAG_IN register values remain set until overwritten by the decoded flags in the next received EDH packet. When an EDH packet is not detected during vertical blanking, the flag registers are cleared at the end of the vertical blanking period.

4.16 Video Signal Error Detection & Indication

The GS2961 includes a number of video signal error detection functions. These are provided to enhance operation of the device when operating in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH). These features are not available in the other operating modes of the device (i.e. when $\overline{\text{SMPTE\_BYPASS}}$ = LOW).

Signal errors that can be detected include:

1. TRS errors.
2. HD line based CRC errors.
3. EDH errors.
4. HD line number errors.
5. Video standard errors.

The device maintains an ERROR_STAT_X register. Each error condition has a specific flag in the ERROR_STAT_X register, which is set HIGH whenever an error condition is detected.

An ERROR_MASK register is also provided, allowing the user to select which error conditions are reported. Each bit of the ERROR_MASK register corresponds to a unique error type.

Each bit of each ERROR_MASK register corresponds to a unique error type.

By default (at power up or after system reset), all bits of the ERROR_MASK registers are zero, enabling all errors to be reported. Individual error detection may be disabled by setting the corresponding bit HIGH in the mask registers.

Error conditions are indicated by a $\overline{\text{DATA\_ERROR}}$ signal , which are available for output on the multifunction I/O output pins. This signal is normally HIGH, but is set LOW by the device when an error condition has been detected.

This signal is a logical 'NOR' of the appropriate error status flags stored in the ERROR_STAT_X register, which are gated by the bit settings in the ERROR_MASK registers. When an error status bit is HIGH and the corresponding error mask bit is LOW, the corresponding $\overline{\text{DATA\_ERROR}}$ signal is set LOW by the device.

The ERROR_STAT_X registers, and correspondingly the $\overline{\text{DATA\_ERROR}}$ signal, are cleared at the start of the next video field or when read via the host interface, which ever condition occurs first.

All bits of the ERROR_STAT_X registers are also cleared under any of the following conditions:

1. LOCKED signal = LOW.
2. $\overline{\text{SMPTE\_BYPASS}}$ = LOW.
3. When a change in video standard has been detected.
4. $\overline{\text{RESET\_TRST}}$ = LOW

Table 4-13 shows the ERROR_STAT_X register and ERROR_MASK_X register.

NOTE: Since the error indication registers are cleared once per field, if an external host micro is polling the error registers periodically, an error flag may be missed if it is intermittent, and the polling frequency is less than the field rate.

Table 4-13: Error Status Register and Error Mask Register

Video Error Status Register	Video Error Mask Register
SAV_ERR (02h, 03h)	SAV_ERR_MASK (037h, 038h)
EAV_ERR (02h, 03h)	EAV_ERR_MASK (037h, 038h)
YCRC_ERR (02h, 03h)	YCRC_ERR_MASK (037h, 038h)
CCRC_ERR (02h, 03h)	CCRC_ERR_MASK (037h, 038h)
LNUM_ERR (02h, 03h)	LNUM_ERR_MASK (037h, 038h)
YCS_ERR (02h, 03h)	YCS_ERR_MASK (037h, 038h)
CCS_ERR (02h, 03h)	CCS_ERR_MASK (037h, 038h)
AP_CRC_ERR (02h)	AP_CRC_ERR_MASK (037h)

Table 4-13: Error Status Register and Error Mask Register

Video Error Status Register	Video Error Mask Register
FF_CRC_ERR (02h)	FF_CRC_ERR_MASK (037h)
VD_STD_ERR (02h, 03h)	VD_STD_ERR_MASK (037h)

NOTE: In 3G Level B mode, separate Video Error Mask registers exist for Link A and Link B. The GS2961 distinguishes between Level A and Level B mappings at 3Gb/s. When Level B data is detected, error detection is enabled separately for Data Stream 1 and Data Stream 2 (Link A and Link B, respectively). Therefore, a second set of error status and mask registers is available for Data Stream 2, and is only valid when 3Gb/s Level B data is detected by the device.

4.16.1 TRS Error Detection

TRS error flags are generated by the GS2961 under the following two conditions:

1. A phase shift in received TRS timing is observed on a non-switching line.
2. The received TRS Hamming codes are incorrect.

Both SAV and EAV TRS words are checked for timing and data integrity errors.

For HD mode, only the Y channel TRS codes are checked for errors.

For 3G mode Level A signals, only data stream one TRS codes are checked for errors. For 3G Level B signals, the Y channel TRS codes of both Link A and Link B are checked for errors.

Both 8-bit and 10-bit TRS code words are checked for errors.

The SAV_ERR bit of the ERROR_STAT_X register is set HIGH when an SAV TRS error is detected.

The EAV_ERR bit of the ERROR_STAT_X register is set HIGH when an EAV TRS error is detected.

4.16.2 Line Based CRC Error Detection

The GS2961 calculates line based CRCs for HD and 3G video signals. CRC calculations are done for each 10-bit channel (Y and C for HD video, DS1 and DS2 for 3G video).

These calculated CRC values are compared with the received CRC values.

If a mismatch in the calculated and received CRC values is detected for Y channel data (Data Stream 1 for 3G video), the YCRC_ERR bit in the ERROR_STAT_X register is set HIGH.

If a mismatch in the calculated and received CRC values is detected for C channel data (Data Stream 2 for 3G video), the CCRC_ERR bit in the ERROR_STAT_X register is set HIGH.

Y or C CRC errors are also generated if CRC values are not embedded.

Line based CRC errors are only generated when the device is operating in HD and 3G modes.

NOTE: By default, 8-bit to 10-bit TRS remapping is enabled. If an 8-bit input is used, the HD CRC check is based on the 10-bit remapped value, not the 8-bit value, so the CRC Error Flag is incorrectly asserted and should be ignored. If 8-bit to 10-bit remapping is enabled, then CRC correction and insertion should be enabled by setting the CRC_INS_MASK bit in the IOPROC_DISABLE register LOW. This ensures that the CRC values are updated.

4.16.3 EDH CRC Error Detection

The GS2961 also calculates Full Field (FF) and Active Picture (AP) CRC's according to SMPTE RP165 in support of Error Detection and Handling packets in SD signals.

These calculated CRC values are compared with the received CRC values.

Error flags for AP and FF CRC errors are provided and each error flag is a logical OR of field 1 and field 2 error conditions.

The AP_CRC_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH when an Active Picture CRC mismatch has been detected in field 1 or 2.

The FF_CRC_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH when a Full Field CRC mismatch has been detected in field 1 or 2.

EDH CRC errors are only indicated when the device is operating in SD mode and when the device has correctly received EDH packets.

4.16.4 HD & 3G Line Number Error Detection

If a mismatch in the calculated and received line numbers is detected, the LNUM_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH.

4.17 Ancillary Data Detection & Indication

The GS2961 detects ancillary data in both the vertical and horizontal ancillary data spaces. Status signal outputs Y/1ANC and C/2ANC are provided to indicate the position of ancillary data in the output data streams. These signals may be selected for output on the multi-function I/O port pins (STAT[5:0]).

The GS2961 indicates the presence of all types of ancillary data by detecting the 000h, 3FFh, 3FFh (00h, FFh, FFh for 8-bit video) ancillary data preamble.

NOTE: Both 8 and 10-bit ancillary data preambles are detected by the device.

By default (at power up or after system reset) the GS2961 indicates all types of ancillary data. Up to 5 types of ancillary data can be specifically programmed for recognition.

For HD video signals, ancillary data may be placed in both the Y and Cb/Cr video data streams separately. For SD video signals, the ancillary data is multiplexed and combined into the YCbCr data space.

For 3G signals, ancillary data may be placed in either or both of the virtual interface data streams. Both data streams are examined for ancillary data.

For a 3G data stream formatted as per Level A mapping:

- The ancillary data is placed in Data Stream 1 first, with overflow into Data Stream 2
- SMPTE 352M packets are duplicated in both data streams

For a 3G data stream formatted as per Level B mapping:

- Each multiplexed data stream forming the 3G signal contains ancillary data embedded according to SMPTE 291M
- Each multiplexed data stream forming the 3G signal contains SMPTE 352M packets embedded according to SMPTE 425M

When operating in HD mode, the Y/1ANC signal is HIGH whenever ancillary data is detected in the Luma data stream, and C/2ANC is HIGH whenever ancillary data is detected in the Chroma data stream. The signals are asserted HIGH at the start of the ancillary data preamble, and remain HIGH until after the ancillary data checksum.

When detecting ancillary data in 3G Level A data, the Y/1ANC status output is HIGH whenever Data Stream 1 ancillary data is detected and the C/2ANC status output is HIGH whenever Data Stream 2 ancillary data is detected.

When detecting ancillary data in 3G Level B data, the Y/1ANC status output is HIGH whenever Data Stream 1 ancillary data is detected on either Y or C channels and the C/2ANC status output is HIGH whenever Data Stream 2 ancillary data is detected on either Y or C channels.

When operating in SD mode, the Y/1ANC and C/2ANC signals depend on the output data format. For 20-bit demultiplexed data, the Y/1ANC and C/2ANC signals operate independently to indicate the first and last ancillary Data Word position in the Luma and/or Chroma data streams. For 10-bit multiplexed data, the Y/1ANC signal is HIGH whenever ancillary data is detected, and the C/2ANC signal is always LOW.

When operating in 3G modes, the Y/1ANC and C/2ANC flags are both zero if the 10-bit multiplexed output format is selected.

These status signal outputs are synchronous with PCLK and may be used as clock-enables for external logic, or as write-enables for an external FIFO or other memory devices.

The operation of the Y/1ANC and C/2ANC signals is shown below in Figure 4-29.

NOTE 1: When I/O processing is disabled, the Y/1ANC and C/2ANC flags may toggle, but they are invalid and should be ignored.

NOTE 2: In 3G Level B mode, if the ANC_EXT_SEL_DS2_$\overline{DS1}$ bit is HIGH and the ANC_DATA_DELETE bit is HIGH, the Y/1ANC and C/2ANC flags are not valid.

NOTE3: For 3G Level B data, the Y/1ANC flag identifies all ANC data on Data Stream 1 (Link A), whether it is embedded in the Y or C component – ANC data is not identified separately for each component. Similarly, the C/2ANC flag identifies all ANC data on Data Stream 2 (Link B), whether it is embedded in the Y or C component.

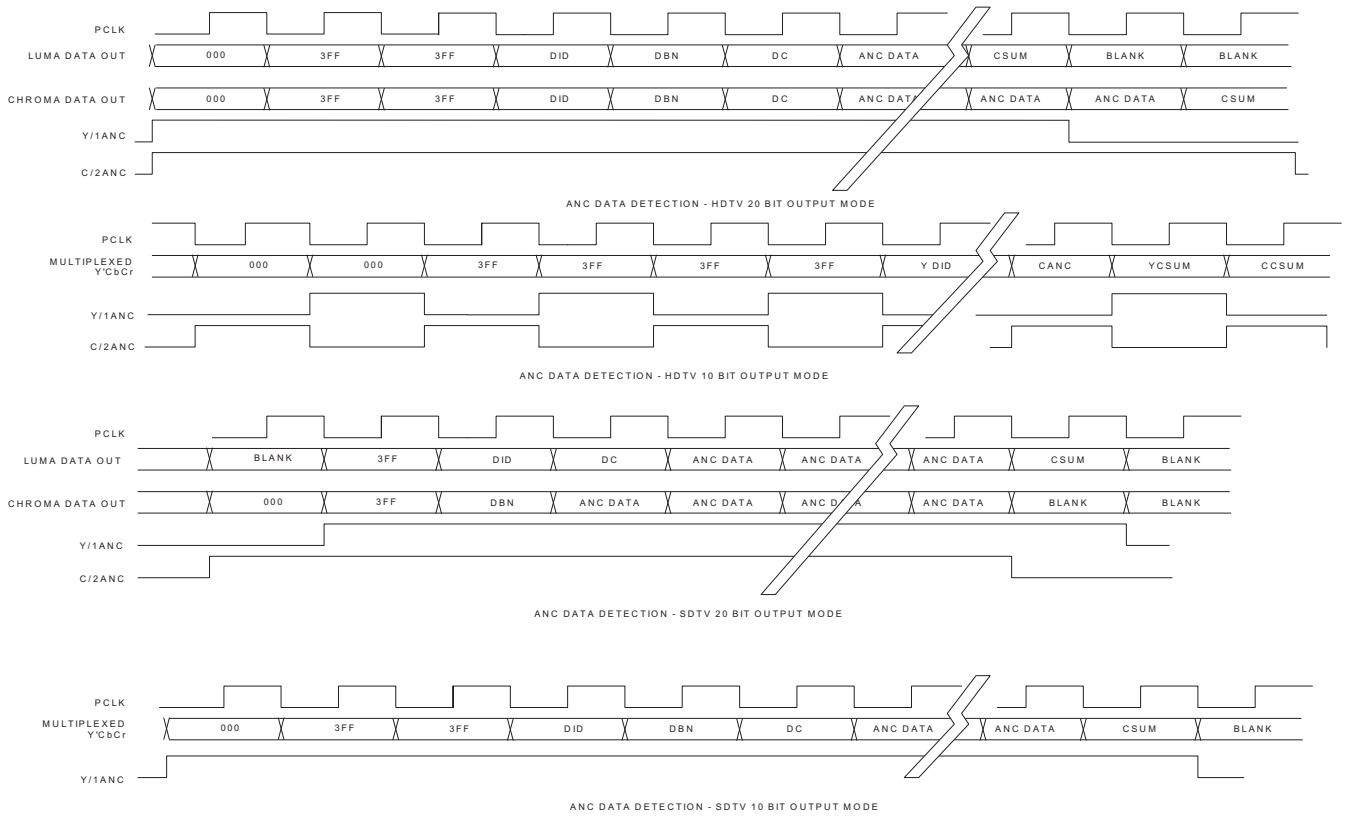


Figure 4-29: Y/1ANC and C/2ANC Signal Timing

4.17.1 Programmable Ancillary Data Detection

As described above in Section 4.17, the GS2961 detects and indicates all ancillary data types by default.

It is possible to program which ancillary data types are to be detected and indicated. Up to 5 different ancillary data types may be programmed for detection by the GS2961 in the ANC_TYPE_DS1 registers for SD, HD and 3G Level A data.

When so programmed, the GS2961 only indicates the presence of the specified ancillary data types, ignoring all other ancillary data. For each data type to be detected, the user must program the DID and/or SDID of that ancillary data type. In the case where no DID or SDID values are programmed, the GS2961 indicates the presence of all ancillary data. In the case where one or more, DID and/or SDID values have been programmed, then only those matching data types are detected and indicated.

The timing of the Y/1ANC and C/2ANC signals in this case is as shown in Figure 4-29.

The GS2961 compares the received DID and/or SDID with the programmed values. If a match is found, ancillary data is indicated.

For any DID or SDID value set to zero, no comparison or match is made. For example, if the DID is programmed and the SDID is not programmed, the GS2961 only detects a match to the DID value.

If both DID and SDID values are non-zero, then the received ancillary data type must match both the DID and SDID before Y/1ANC and/or C/2ANC is set HIGH.

NOTE 1: For 3G Level B data, the ANC_TYPE_DS1 registers are valid for Data Stream 1, and a second set of five ANC_TYPE registers (ANC_TYPE_DS2) is provided for detection of specific ancillary data in Data Stream 2.

NOTE 2: SMPTE 352M Payload Identifier packets and Error Detection and Handling (EDH) Packets are always detected by the GS2961, irrespective of the settings of the ANC_TYPE registers.

4.17.2 SMPTE 352M Payload Identifier

The GS2961 automatically extracts the SMPTE 352M payload identifier present in the input data stream for SD, HD, and 3G Level A signals. The four word payload identifier packets are written to VIDEO_FORMAT_X_DS1 and VIDEO_FORMAT_X_DS2 bits accessible through the host interface.

The device also indicates the version of the payload packet in the VERSION_352M bit of the DATA_FORMAT_DSX register. When the SMPTE 352M packet is formatted as a "version 1" packet, the VERSION_352M bit is set HIGH, when the packet is formatted as a "version 2" packet, this bit is set LOW.

The VIDEO_FORMAT_352_A_X and VIDEO_FORMAT_352_B_X registers are only updated if there are no checksum errors in the received SMPTE 352M packets.

By default (at power up or after system reset), the VIDEO_FORMAT_X_DS1 and VIDEO_FORMAT_X_DS2 bits are set to 0, indicating an undefined format.

NOTE 1: When 3G Level B data is detected by the device, the user needs to extract the SMPTE 352M Payload Identifier packets by using the ANC packet extraction block - they are not detected and extracted automatically. In this case:

- The VD_STD_ERR bit is not valid
- 352M extraction is only done on one data stream or the other, not both simultaneously (Link A or Link B selected via the host interface)
- Previously embedded 352M packets can be deleted on one data stream only (using the ANC_DATA_DELETE bit, see Section 4.18.8), but these packets are replaced with 10-bit Y/C blanking values only
- It is necessary to manually extract the SMPTE 352M data by programming the DID, SDID and line number information into the ANC data extraction block

NOTE 2: SMPTE 352M packet regeneration is enabled by default for 3G Level B inputs, and should be disabled through the host interface if Level B to Level A conversion is not enabled.

4.17.2.1 SMPTE 352M Payload Identifier Usage

The SMPTE 352M Payload Identifier is used to confirm the video format identified by the Automatic Video Standards Detection block (see Section 4.17.4)

Table 4-14: SMPTE 352M Packet Data

Bit Name	Bit	Name	Description	R/W	Default
VIDEO_FORMAT_4_DS1 Address: 01Ah	15-8	SMPTE 352M Byte 4	Data is available in this register when Video Payload Identification Packets are detected in the data stream.	R	0
VIDEO_FORMAT_3_DS1 Address: 01Ah	7-0	SMPTE 352M Byte 3		R	0
VIDEO_FORMAT_2_DS1 Address: 019h	15-8	SMPTE 352M Byte 2		R	0
VIDEO_FORMAT_2_DS1 Address: 019h	7-0	SMPTE 352M Byte 1		R	0

4.17.2.2 3G SMPTE 352M Packets Following Level B to Level A Conversion

After Level B to Level A conversion, modified payload data must be programmed via the host interface into the VIDEO_FORMAT_352_X_X registers and automatically inserted by the GS2961 on the correct SMPTE 352M Line Number.

SMPTE 352M Packets are embedded in both data streams.

Previously embedded 352M packets may be deleted from one data stream only (using the ANC_DATA_DELETE bit, see Section 4.18.8), but these packets are replaced with 10-bit Y/C blanking values.

NOTE: Pre-existing SMPTE 352M Packets that are not deleted are re-mapped to different line numbers during conversion to Level A formatting. These packets should be ignored by the system, since they are on non-standard SMPTE 352M lines.

4.17.3 Ancillary Data Checksum Error

The GS2961 calculates checksums for all received ancillary data.

These calculated checksums are compared with the received ancillary data checksum words.

If a mismatch in the calculated and received checksums is detected, then a checksum error is indicated.

When operating in HD mode, the device makes comparisons on both the Y and C channels separately. If an error condition in the Y channel is detected, the YCS_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH. If an error condition in the C channel is detected, the CCS_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH.

When operating in 3G Level A mode, the device makes comparisons on both the Y (Data Stream 1) and C (Data Stream 2) channels separately. If an error condition in the Y channel is detected, the YCS_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH.

If an error condition in the C channel is detected, the CCS_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH.

When operating in 3G Level B mode, the device makes comparisons on both the Y channel and the C channel of both Link A and Link B.

When operating in SD mode, only the YCS_ERR bit is set HIGH when checksum errors are detected.

4.17.3.1 Programmable Ancillary Data Checksum Calculation

As described above, the GS2961 calculates and compares checksum values for all ancillary data types by default. It is possible to program which ancillary data types are checked as described in Section 4.17.1.

When so programmed, the GS2961 only checks ancillary data checksums for the specified data types, ignoring all other ancillary data.

The YCS_ERR and/or CCS_ERR bits in the VIDEO_ERROR_STAT_X register are only set HIGH if an error condition is detected for the programmed ancillary data types.

4.17.4 Video Standard Error

If a mismatch between the received SMPTE 352M packets and the calculated video standard occurs, the GS2961 indicates a video standard error by setting the VD_STD_ERR bit of the VIDEO_ERROR_STAT_X register HIGH.

The device detects the SMPTE 352M Packet version as defined in the SMPTE 352M standard. If the incoming packet is Version Zero, then no comparison is made with the internally generated payload information and the VD_STD_ERR bit is not set HIGH.

NOTE 1: If the received SMPTE 352M packet indicates 25, 30 or 29.97PsF formats, the device only indicates an error when the video format is actually progressive. The device detects 24 and 23.98PsF video standards and perform error checking at these rates.

NOTE 2: The VD_STD_ERR bit should be ignored in all 3G modes.

4.18 Signal Processing

In addition to error detection and indication, the GS2961 can also correct errors, inserting corrected code words, checksums and CRC values into the data stream.

The following processing can be performed by the GS2961:

1. TRS error correction and insertion.
2. HD line based CRC correction and insertion.
3. EDH CRC error correction and insertion.
4. HD line number error correction and insertion.
5. Illegal code re-mapping.
6. Ancillary data checksum error correction and insertion.

7. SMPTE 372M (Level B to Level A) Conversion.

All of the above features are only available in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH).

To enable these features, the IOPROC_EN/$\overline{\text{DIS}}$ pin must be set HIGH, and the individual feature must be enabled via bits in the IOPROC_DISABLE register.

The IOPROC_DISABLE register contains one bit for each processing feature allowing each one to be enabled/disabled individually.

By default (at power up or after system reset), all of the IOPROC_DISABLE register bits are LOW, enabling all of the processing features.

To disable an individual processing feature, set the corresponding IOPROC_DISABLE bit HIGH in the IOPROC_DISABLE register.

Table 4-15: IOPROC_DISABLE Register Bits

Processing Feature	IOPROC_DISABLE Register Bit
TRS error correction and insertion	TRS_INS
Y and C line based CRC error correction	CRC_INS
Y and C line number error correction	LNUM_INS
Ancillary data check sum correction	ANC_CHECKSUM_INSERTION
EDH CRC error correction	EDH_CRC_INS
Illegal code re-mapping	ILLEGAL_WORD_REMAP
H timing signal configuration	H_CONFIG
Update EDH Flags	EDH_FLAG_UPDATE_MASK
Ancillary Data Extraction	ANC_DATA_EXT
Regeneration of 352M packets	$\overline{\text{REGEN\_352M}}$

4.18.1 TRS Correction & Insertion

When TRS Error Correction and Insertion is enabled, the GS2961 generates and overwrites TRS code words as required.

TRS Word Generation and Insertion is performed using the timing generated by the Timing Signal Generator, providing an element of noise immunity over using just the received TRS information.

This feature is enabled when the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and the TRS_INS_DISABLE bit in the IOPROC_DISABLE register is set LOW.

NOTE: Inserted TRS code words are always 10-bit compliant, irrespective of the bit depth of the incoming video stream.

4.18.2 Line Based CRC Correction & Insertion

When CRC Error Correction and Insertion is enabled, the GS2961 generates and inserts line based CRC words into both the Y and C channels of the data stream.

Line based CRC word generation and insertion only occurs in HD and 3G modes, and is enabled in when the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and the CRC_INS_DSX_MASK bit in the IOPROC_X register is set LOW.

4.18.3 Line Number Error Correction & Insertion

When Line Number Error Correction and Insertion is enabled, the GS2961 calculates and inserts line numbers into the output data stream. Re-calculated line numbers are inserted into both the Y and C channels.

Line number generation is in accordance with the relevant HD or 3G video standard as determined by the Automatic Standards Detection block.

This feature is enabled when the device is operating in HD or 3G modes, the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and the LNUM_INS_DSX_MASK bit in the IOPROC_X register is set LOW.

4.18.4 ANC Data Checksum Error Correction & Insertion

When ANC data Checksum Error Correction and Insertion is enabled, the GS2961 generates and inserts ancillary data checksums for all ancillary data words by default.

Where user specified ancillary data has been programmed (see Section 4.17.1), only the checksums for the programmed ancillary data are corrected.

This feature is enabled when the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and the ANC_CHECKSUM_INSERTION_DSX_MASK bit in the IOPROC_X register is set LOW.

4.18.5 EDH CRC Correction & Insertion

When EDH CRC Error Correction and Insertion is enabled, the GS2961 generates and overwrites full field and active picture CRC check-words.

Additionally, the device sets the active picture and full field CRC 'V' bits HIGH in the EDH packet. The AP_CRC_V and FF_CRC_V register bits only report the received EDH validity flags.

EDH FF and AP CRC's are only inserted when the device is operating in SD mode, and if the EDH data packet is detected in the received video data.

Although the GS2961 modifies and inserts EDH CRC's and EDH packet checksums, EDH error flags are only updated when the EDH_FLAG_UPDATE_MASK bit is LOW.

This feature is enabled in SD mode, when the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and the EDH_CRC_INS_MASK bit in the IOPROC_1 register is set LOW.

4.18.6 Illegal Word Re-mapping

All words within the active picture (outside the horizontal and vertical blanking periods), between the values of 3FCh and 3FFh are re-mapped to 3FBh. All words within the active picture area between the values of 000h and 003h are remapped to 004h.

This feature is enabled when the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and the ILLEGAL_WORD_REMAP_DSX_MASK bit in the IOPROC_X register is set LOW.

4.18.7 TRS and Ancillary Data Preamble Remapping

8-bit TRS and ancillary data preambles are re-mapped to 10-bit values. 8-bit to 10-bit mapping of TRS headers is only supported if the TRS values are 3FC 000 000. Other values such as 3FD, 3FE, 3FF, 001, 002 and 003 are not supported. This feature is enabled by default, and cannot be disabled via the IOPROC_X register.

4.18.8 Ancillary Data Extraction

Ancillary data may be extracted externally from the GS2961 output stream using the Y/1ANC and C/2ANC signals, and external logic.

As an alternative, the GS2961 includes a FIFO, which extracts ancillary data using read access via the host interface to ease system implementation. The FIFO stores up to 2048 x 16 bit words of ancillary data in two separate 1024 word memory banks.

The device writes the contents of ANC packets into the FIFO, starting with the first Ancillary Data Flag (ADF), followed by up to 1024 words.

All Data Identification (DID), Secondary Data Identification (SDID), Data Count (DC), user data, and checksum words are written into the device memory.

The device detects ancillary data packet DID's placed anywhere in the video data stream, including the active picture area.

Ancillary data from the Y channel or Data Stream One is placed in the Least Significant Word (LSW) of the FIFO, allocated to the lower 8 bits of each FIFO address.

Ancillary data from the C channel or Data Stream Two is placed in the Most Significant Word (MSW) (upper 8 bits) of each FIFO address.

In SD mode, ancillary data is placed in the LSW of the FIFO. The MSW is set to zero.

If the ANC_TYPE registers are all set to zero, the device extracts all types of ancillary data. If programmable ancillary data extraction is required, then up to five types of ancillary data to be extracted can be programmed in the ANC_TYPE registers (see Section 4.17.1).

Additionally, the lines from which the packets are to be extracted can be programmed into the ANC_LINEA[10:0] and ANC_LINEB[10:0] registers, allowing ancillary data from a maximum of two lines per frame to be extracted. If only one line number register is programmed (with the other set to zero), ancillary data packets are extracted from one line per frame only. When both registers are set to zero, the device extracts packets from all lines.

To start Ancillary Data Extraction, the ANC_DATA_EXT_MASK bit of the host interface must be set LOW. Ancillary data packet extraction begins in the following frame (see Figure 4-30: Ancillary Data Extraction - Step A).

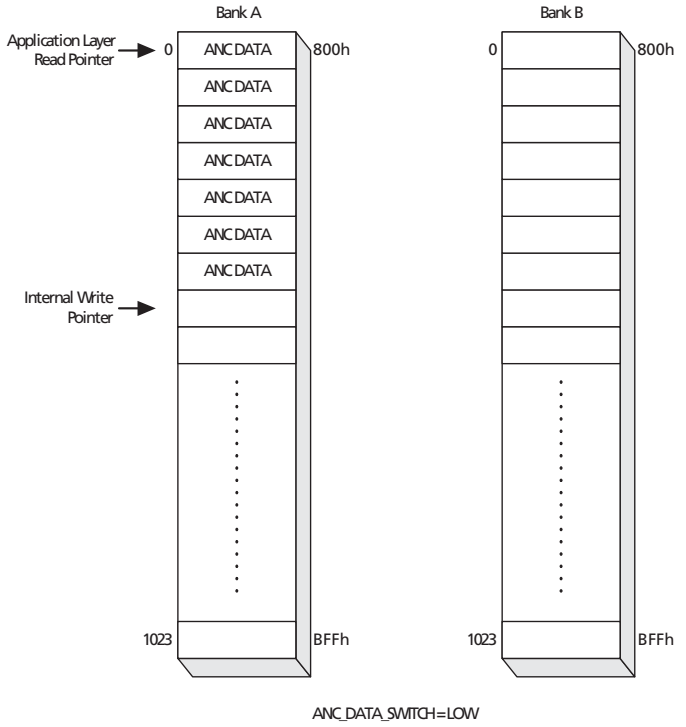


Figure 4-30: Ancillary Data Extraction - Step A

Ancillary data is written into Bank A until full. The Y/1ANC and C/2ANC output flags can be used to determine the length of the ancillary data extracted and when to begin reading the extracted data from memory.

While the ANC_DATA_EXT_MASK bit is set LOW, the ANC_DATA_SWITCH bit can be set HIGH during or after reading the extracted data. New data is then written into Bank B (up to 1024 x 16-bit words), at the corresponding host interface addresses (see Figure 4-31: Ancillary Data Extraction - Step B).

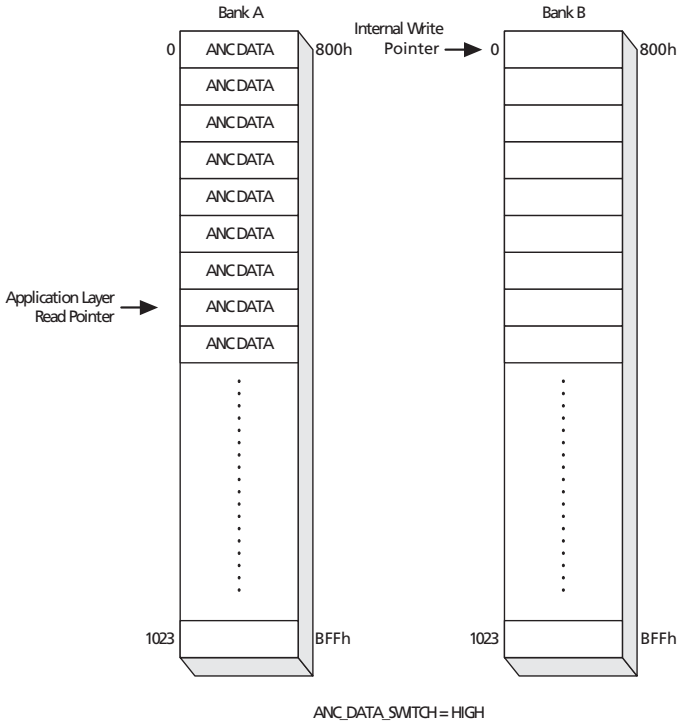


Figure 4-31: Ancillary Data Extraction - Step B

To read the new data, toggle the ANC_DATA_SWITCH bit LOW. The old data in Bank A is cleared to zero and extraction continues in Bank B (see Figure 4-32: Ancillary Data Extraction - Step C).

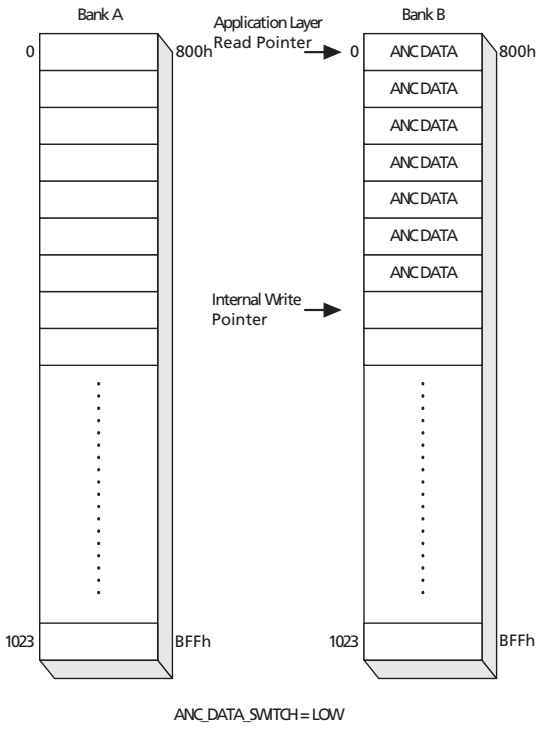


Figure 4-32: Ancillary Data Extraction - Step C

If the ANC_DATA_SWITCH bit is not toggled, extracted data is written into Bank B until full. To continue extraction in Bank A, the ANC_DATA_SWITCH bit must be toggled HIGH (see Figure 4-33: Ancillary Data Extraction - Step D).

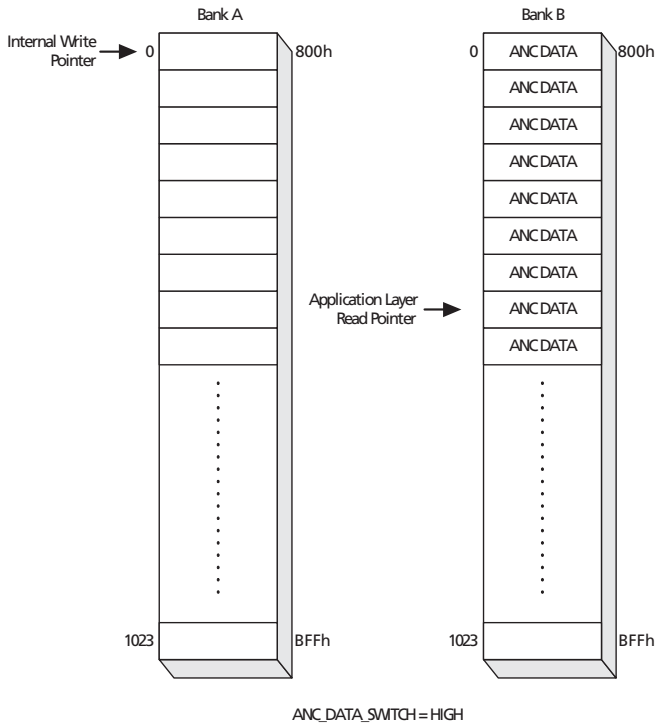


Figure 4-33: Ancillary Data Extraction - Step D

Toggling the ANC_DATA_SWITCH bit LOW returns the process to step A (Figure 4-30).

NOTE: Toggling the ANC_DATA_SWITCH must occur at a time when no extraction is taking place, i.e. when the both the Y/1ANC and C/2ANC signals are LOW.

To turn extraction off, the ANC_DATA_EXT_MASK bit must be set HIGH.

In HD mode, the device can detect ancillary data packets in the Luma video data only, Chroma video data only, or both. By default (at power-up or after a system reset), the device extracts ancillary data packets from the luma channel only.

In 3G mode Level A, the device can detect ancillary data packets in Luma video (Data Stream One) only, Chroma video (Data Stream Two) only, or both. By default (at power-up or after a system reset), the device extracts ancillary data packets from Data Stream One only.

In 3G mode Level B mode, the device can detect ancillary data packets in Luma video only, Chroma video only, or both from either Link A or Link B. Selection of Link A or Link B for ANC data extraction is done via the host interface. By default (at power-up or after a system reset), the device extracts ancillary data packets from Link A Luma only.

To extract packets from the Chroma/Data Stream Two channel only, the HD_ANC_C2 bit of the host interface must be set HIGH. To extract packets from both Luma/Data Stream One and Chroma/Data Stream Two video data, the HD_ANC_Y1_C2 bit must be set HIGH (the setting of the HD_ANC_C2 bit is ignored).

The default setting of both the HD_ANC_C2 and HD_ANC_Y1_C2 is LOW. The setting of these bits is ignored when the device is configured for SD video standards.

Ancillary data packet extraction and deletion is disabled when the IOPROC_EN/$\overline{DIS}$ pin is set LOW.

After extraction, the ancillary data may be deleted from the video stream by setting the ANC_DATA_DEL bit of the host interface HIGH. When set HIGH, all existing ancillary data is removed and replaced with blanking values. If any of the ANC_TYPE registers are programmed with a DID and/or DID and SDID, only the ancillary data packets with the matching IDs are deleted from the video stream.

NOTE1: After the ancillary data determined by the ANC_TYPE_X_APX registers has been deleted, other existing ancillary data may not be contiguous. The device does not concatenate the remaining ancillary data.

NOTE2: Reading extracted ancillary data from the host interface must be performed while there is a valid video signal present at the serial input and the device is locked (LOCKED signal is HIGH).

4.18.9 Level B to Level A Conversion

When IOPROC_2 register bit LEVEL_B2A_CONV_DISABLE_MASK is HIGH (default), the GS2961 does not convert 3G LEVEL B streams between Level A and Level B mapping formats.

When LEVEL_B2A_CONV_DISABLE_MASK is LOW, the GS2961 converts a 3G 1080p Level B stream to the Level A mapping format, as per SMPTE 425M.

The device assumes that Link A and Link B are phase-aligned at the transmitter.

The output data are line multiplexed such that the data content from Link A and Link B are assembled in a continuous fashion, at twice the input data rate. Extracted timing reference information is used to trigger a line counter which embeds the correct line number according to SMPTE 425M.

NOTE 1: If Level B/A conversion is enabled, previous 352M Payload ID packets are not deleted from the data stream.

NOTE 2: When Level B/A conversion is enabled, timing reference information (FVH) present on the STAT outputs is not phase-aligned with the output video data, and should not be used for line or frame synchronization activities. During Level B to Level A conversion, it is advised that the user generates the H and V timing signals from the embedded TRS words.

NOTE 3: If the GS2961 sees a synchronous switch where the difference in phases between two Level B inputs is greater than ~10.7µs, the user may observe a missing H pulse on the line following the switch line, when Level B/A conversion is enabled.

4.19 GSPI - HOST Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the system to access additional status and control information through configuration registers in the GS2961.

The GSPI is comprised of a Serial Data Input signal (SDIN), Serial Data Output signal (SDOUT), an active low Chip Select ($\overline{CS}$), and a Burst Clock (SCLK).

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided.

When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled. When JTAG/$\overline{HOST}$ is HIGH, the JTAG interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals must be provided by the system. The SDOUT pin is a non-clocked loop-through of SDIN and may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. See Section 4.19.2 for details. The interface is illustrated in the Figure 4-34 below.

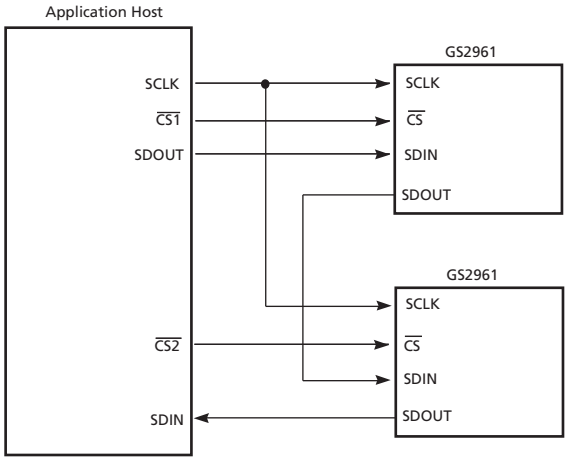


Figure 4-34: GSPI Application Interface Connection

All read or write access to the GS2961 is initiated and terminated by the system host processor. Each access always begins with a Command/Address Word, followed by a data write to, or data read from, the GS2961.

4.19.1 Command Word Description

The Command Word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address.

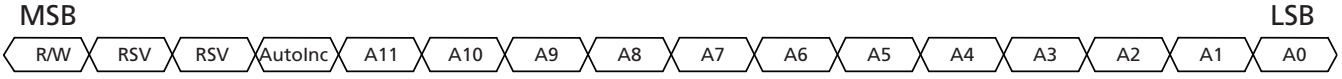


Figure 4-35: Command Word Format

Command Words are clocked into the GS2961 on the rising edge of the Serial Clock SCLK, which operates in a burst fashion. The chip select ($\overline{CS}$) signal must be set low a minimum of 1.5ns (t0 in Figure 4-37) before the first clock edge to ensure proper operation.

When the Auto-Increment bit is set LOW, each Command Word must be followed by only one Data Word to ensure proper operation.

If the Auto-Increment bit is set HIGH, the following Data Word is written into the address specified in the Command Word, and subsequent Data Words are written into incremental addresses from the first Data Word. This facilitates multiple address writes without sending a Command Word for each Data Word.

4.19.2 Data Read or Write Access

During a read sequence (Command Word R/W bit set HIGH) serial data is transmitted or received MSB first, synchronous with the rising edge of the serial clock SCLK. The Chip Select ($\overline{CS}$) signal must be set low a minimum of 1.5ns (t0 in Figure 4-37) before the first clock edge to ensure proper operation. The first bit (MSB) of the Serial Output (SDOUT) is available (t5 in Figure 4-38) following the last falling SCLK edge of the read Command Word, the remaining bits are clocked out on the negative edges of SCLK.

NOTE1: When several devices are connected to the GSPI chain, only one $\overline{CS}$ may be asserted during a read sequence.

During a write sequence (Command Word R/W bit set LOW), a wait state of 37.1ns (t4 in Figure 4-37) is required between the Command Word and the following Data Word. This wait state must also be maintained between successive Command Word/Data Word write sequences. When Auto Increment mode is selected (AutoInc = 1), the wait state must be maintained between successive Data Words after the initial Command Word/Data Word sequence.

During the write sequence, all Command and following Data Words input at the SDIN pin are output at the SDOUT pin unchanged. When several devices are connected to the GSPI chain, data can be written simultaneously to all the devices which have $\overline{CS}$ set LOW.

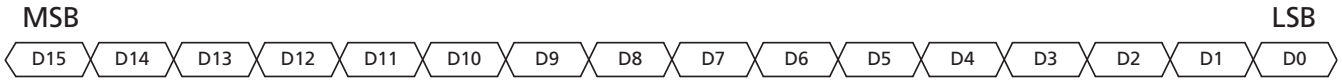


Figure 4-36: Data Word Format

4.19.3 GSPI Timing

Write and Read Mode timing for the GSPI interface;

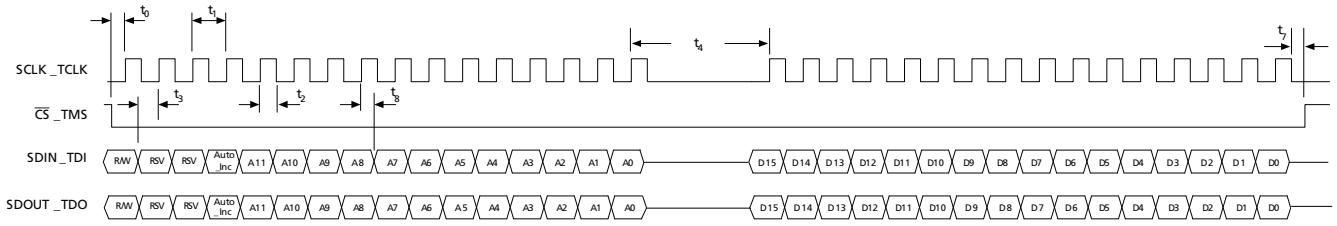


Figure 4-37: Write Mode

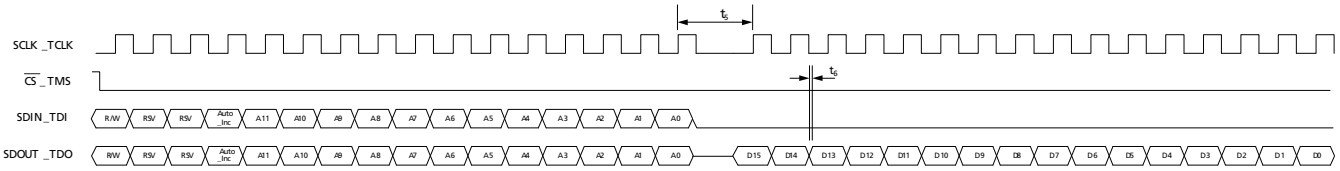


Figure 4-38: Read Mode

SDIN_TDI to SDOUT_TDO combinational path for daisy chain connection of multiple GS2961.

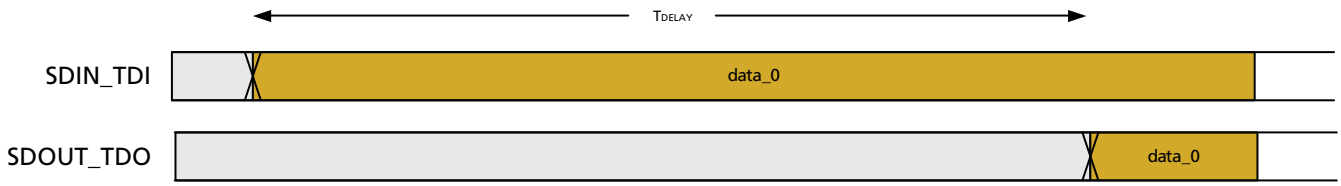


Figure 4-39: GSPI Time Delay

Table 4-16: GSPI Time Delay

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Delay time	t_{DELAY}	50% levels; 1.8V operation	–	–	13.1	ns
Delay time	t_{DELAY}	50% levels; 3.3V operation	–	–	9.7	ns

Table 4-17: GSPI Timing Parameters (50% levels; 3.3V or 1.8V operation)

Parameter	Symbol	Min		Typ	Max	Units
$\overline{CS}$ low before SCLK rising edge	t_0	1.5		–	–	ns
SCLK period	t_1	16.67		–	–	ns
SCLK duty cycle	t_2	40		50	60	%
Input data setup time	t_3	1.5		–	–	ns
Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – write cycle	t_4	PCLK (MHz)	ns	–	–	ns
		unlocked	100			
		27.0	37.1			
		74.25	13.5			
		148.5	6.7			
Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – read cycle.	t_5	PCLK (MHz)	ns	–	–	ns
		unlocked	–			
		27.0	148.4			
		74.25	53.9			
		148.5	27			
Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – read cycle - ANC FIFO Read	t_5	222.6		–	–	ns
Output hold time (15pF load)	t_6	1.5		–	–	ns
$\overline{CS}$ high after last SCLK rising edge	t_7	PCLK (MHz)	ns	–	–	ns
		unlocked	445			
		27.0	37.1			
		74.25	13.5			
		148.5	6.7			
Input data hold time	t_8	1.5		–	–	ns

This timing must be satisfied across all ambient temperature and power supply operating conditions, as described in the Electrical Characteristics on page 15.

4.20 Host Interface Register Maps

Table 4-18: Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
000h	IOPROC_1	RSVD	15	Reserved.	R	0
		TRS_WORD_REMAP_DS1 _DISABLE	14	Disables 8-bit TRS word remapping for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.	R/W	0
		RSVD	13	Reserved.	R/W	0
		EDH_FLAG_UPDATE _MASK	12	Disables updating of EDH error flags.	R/W	0
		EDH_CRC_INS_MASK	11	Disables EDH_CRC error correction and insertion.	R/W	0
		H_CONFIG	10	Selects the H blanking indication: 0: Active line blanking - the H output is HIGH for all the horizontal blanking period, including the EAV and SAV TRS words. 1: TRS based blanking - the H output is set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS signals. This signal is only valid when TIM_861 is set to '0' (via pin or host interface).	R/W	0
		ANC_DATA_EXT_MASK	9	Disables ancillary data extraction FIFO.	R/W	0
		RSVD	8	Reserved.	R/W	0
		TIM_861_PIN_DISABLE	7	Disable TIM_861 pin control when set to '1', and use TIMING_861 bit instead.	R/W	0
		TIMING_861	6	Selects the output timing reference format: 0 = Digital FVH timing output; 1 = CEA-861 timing output.	R/W	0
		RSVD	5	Reserved.	R/W	0
		ILLEGAL_WORD_REMAP _DS1_MASK	4	Disables illegal word remapping for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.	R/W	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
000h	IOPROC_1	ANC_CHECKSUM _INSERTION_DS1_MASK	3	Disables insertion of ancillary data checksums for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.	R/W	0
		CRC_INS_DS1_MASK	2	Disables insertion of HD/3G CRC words for 3G Level B Data Stream 1, 3G Level A, and HD inputs.	R/W	0
		LNUM_INS_DS1_MASK	1	Disables insertion of line numbers for 3G Level B Data Stream 1, 3G Level A, and HD inputs.	R/W	0
		TRS_INS_DS1_MASK	0	Disables insertion of TRS words for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.	R/W	0
001h	IOPROC_2	RSVD	15-13	Reserved.	R/W	N/A
		TRS_WORD_REMAP_DS2 _DISABLE	12	Disables 8-bit TRS word remapping in Data Stream 2 (3G Level B only).	R/W	0
		RSVD	11	Reserved.	R/W	0
		REGEN_352M_MASK	10	Disables regeneration of the SMPTE 352M packet for 3G Level B data. Note: this bit needs to be enabled via the host interface to disable SMPTE 352M packet generation. It is strongly recommended to set this bit LOW only when Level B to Level A conversion is enabled.	R/W	0
		DS_SWAP_3G	9	Swaps Data Stream 1 (DS1) and Data Stream 2 (DS2) at the output in 3G mode. In 20-bit output mode, DS1 shall be present on DOUT pins [19:10] and DS2 shall be present on DOUT pins [9:0] by default. When DS_SWAP_3G is set to '1', DS2 shall be present on DOUT pins [19:10] and DS1 shall be present on DOUT pins [9:0] In 10-bit (DDR) output mode, DS2 shall precede DS1 by default. When DS_SWAP_3G is set to '1', DS1 shall precede DS2.	R/W	0
		LEVEL_B2A_CONV _DISABLE_MASK	8	Disable conversion of a 3G Level B input to a 3G Level A format. Only effective if in 3G Level B mode. Default is active HIGH (disabled), so Level B inputs are formatted as Level B outputs.	R/W	1

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
001h	IOPROC_2	ANC_EXT_SEL_DS2_$\overline{DS1}$	7	Selects data stream to extract ANC data from (valid for 3G Level B data).	R/W	0
		RSVD	6-5	Reserved.	R/W	0
		ILLEGAL_WORD_REMAP _DS2_MASK	4	Disables illegal word remapping in Data Stream 2 (3G Level B only).	R/W	0
		ANC_CHECKSUM _INSERTION_DS2_MASK	3	Disables insertion of ancillary data checksums in Data Stream 2 (3G Level B only).	R/W	0
		CRC_INS_DS2_MASK	2	Disables insertion of CRC words in Data Stream 2 (3G Level B only).	R/W	0
		LNUM_INS_DS2_MASK	1	Disables insertion of line numbers in Data Stream 2 (3G Level B only).	R/W	0
		TRS_INS_DS2_MASK	0	Disable insertion of TRS words in Data Stream 2 (3G Level B only).	R/W	0
002h	ERROR_STAT_1	RSVD	15-11	Reserved.	ROCW	0
		VD_STD_ERR_DS1	10	Video Standard Error indication for HD and SD inputs.	ROCW	0
		FF_CRC_ERR	9	EDH Full Frame CRC error indication.	ROCW	0
		AP_CRC_ERR	8	EDH Active Picture CRC error indication.	ROCW	0
		RSVD	7	Reserved.	ROCW	0
		CCS_ERR_DS1	6	Chroma ancillary data checksum error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.	ROCW	0
		YCS_ERR_DS1	5	Luma ancillary data checksum error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.	ROCW	0
		CCRC_ERR_DS1	4	Chroma CRC error indication for 3G Level B Data Stream 1, 3G Level A, and HD inputs.	ROCW	0
		YCRC_ERR_DS1	3	Luma CRC error indication for 3G Level B Data Stream 1, 3G Level A, and HD inputs.	ROCW	0
		LNUM_ERR_DS1	2	Line number error indication for 3G Level B Data Stream 1, 3G Level A, and HD inputs.	ROCW	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
002h	ERROR_STAT_1	SAV_ERR_DS1	1	SAV error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.	ROCW	0
		EAV_ERR_DS1	0	EAV error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.	ROCW	0
003h	ERROR_STAT_2	RSVD	15-7	Reserved.	ROCW	0
		CCS_ERR_DS2	6	Chroma ancillary data checksum error indication for Data Stream 2 (3G Level B only).	ROCW	0
		YCS_ERR_DS2	5	Luma ancillary data checksum error indication for Data Stream 2 (3G Level B only).	ROCW	0
		CCRC_ERR_DS2	4	Chroma CRC error indication for Data Stream 2 (3G Level B only).	ROCW	0
		YCRC_ERR_DS2	3	Luma CRC error indication for Data Stream 2 (3G Level B only).	ROCW	0
		LNUM_ERR_DS2	2	Line number error indication for Data Stream 2 (3G Level B only).	ROCW	0
		SAV_ERR_DS2	1	SAV error indication for Data Stream 2 (3G Level B only).	ROCW	0
		EAV_ERR_DS2	0	EAV error indication for Data Stream 2 (3G Level B only).	ROCW	0
004h	EDH_FLAG_IN	EDH_DETECT	15	Embedded EDH packet detected.	R	0
		ANC_UES_IN	14	Ancillary data – unknown error status flag.	R	0
		ANC_IDA_IN	13	Ancillary data – internal error detected already flag.	R	0
		ANC_IDH_IN	12	Ancillary data – internal error detected here flag	R	0
		ANC_EDA_IN	11	Ancillary data – error detected already flag.	R	0
		ANC_EDH_IN	10	Ancillary data – error detected here flag.	R	0
		FF_UES_IN	9	EDH Full Field – unknown error status flag.	R	0
		FF_IDA_IN	8	EDH Full Field – internal error detected already flag.	R	0
		FF_IDH_IN	7	EDH Full Field – internal error detected here flag.	R	0
		FF_EDA_IN	6	EDH Full Field – error detected already flag.	R	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
004h	EDH_FLAG_IN	FF_EDH_IN	5	EDH Full Field – error detected here flag.	R	0
		AP_UES_IN	4	EDH Active Picture – unknown error status flag.	R	0
		AP_IDA_IN	3	EDH Active Picture – internal error detected already flag.	R	0
		AP_IDH_IN	2	EDH Active Picture – internal error detected here flag.	R	0
		AP_EDA_IN	1	EDH Active Picture – error detected already flag.	R	0
		AP_EDH_IN	0	EDH Active Picture – error detected here flag.	R	0
005h	EDH_FLAG_OUT	RSVD	15	Reserved.	R	0
		ANC_UES	14	Ancillary data – Unknown Error Status flag.	R	1
		ANC_IDA	13	Ancillary data – Internal error Detected Already flag.	R	0
		ANC_IDH	12	Ancillary data – Internal error Detected Here flag.	R	0
		ANC_EDA	11	Ancillary data – Error Detected Already flag.	R	0
		ANC_EDH	10	Ancillary data – Error Detected Here flag.	R	0
		FF_UES	9	EDH Full Field – Unknown Error Status flag.	R	1
		FF_IDA	8	EDH Full Field – Internal error Detected Already flag.	R	0
		FF_IDH	7	EDH Full Field – Internal error Detected Here flag.	R	0
		FF_EDA	6	EDH Full Field – Error Detected Already flag.	R	0
		FF_EDH	5	EDH Full Field – Error Detected Here flag.	R	0
		AP_UES	4	EDH Active Picture – Unknown Error Status flag.	R	1
		AP_IDA	3	EDH Active Picture – Internal error Detected Already flag.	R	0
		AP_IDH	2	EDH Active Picture – Internal error Detected Here flag.	R	0
		AP_EDA	1	EDH Active Picture – Error Detected Already flag.	R	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
005h	EDH_FLAG_OUT	AP_EDH	0	EDH Active Picture – Error Detected Here flag.	R	0
006h	DATA_FORMAT_DS1	FF_CRC_V	15	EDH Full Field CRC Validity bit.	R	0
		AP_CRC_V	14	EDH Active Picture CRC Validity bit.	R	0
		VD_STD_DS1	13-8	Detected Video Standard for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.	R	29
		CDATA_FORMAT_DS1	7-4	Data format as indicated in Chroma channel for 3G Level B Data Stream 1, HD and SD inputs; Data format as indicated in Data Stream 2 for 3G Level A inputs.	R	15
		YDATA_FORMAT_DS1	3-0	Data format as indicated in Luma channel for 3G Level B Data Stream 1, HD and SD inputs; Data format as indicated in Data Stream 1 for 3G Level A inputs.	R	15
007h	DATA_FORMAT_DS2	RSVD	15-14	Reserved.	R	0
		VD_STD_DS2	13-8	Detected Video Standard for Data Stream 2 (3G Level B only).	R	0
		CDATA_FORMAT_DS2	7-4	Data Format as indicated in Chroma channel for Data Stream 2 (3G Level B only).	R	0
		YDATA_FORMAT_DS2	3-0	Data Format as indicated in Luma channel for Data Stream 2 (3G Level B only).	R	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
008h	IO_CONFIG	RSVD	15	Reserved.	RW	0
		STAT2_CONFIG	14-10	Configure STAT2 output pin: 00000: H Blanking when TIM_861 = 0; HSYNC when TIM_861 = 1 00001: V Blanking when TIM_861 = 0; VSYNC when TIM_861 = 1 00010: F bit when TIM_861 = 0; Data Enable (DE) when TIM_861 = 1 00011: LOCKED 00100: Y/1ANC: ANC indication (SD), Luma ANC indication (HD), Data Stream 1 ANC data indication (3G) 00101: C/2ANC: Chroma ANC indication (HD) or Data Stream 2 ANC data indication (3G) 00110: Data Error 00111: Video Error 01000: Reserved 01001: EDH Detected 01010: Carrier Detect 01011: RATE_DET0 01100: RATE_DET1 01101 - 11111: Reserved	RW	2
		STAT1_CONFIG	9-5	Configure STAT1 output pin. (Refer to above for decoding)	RW	1
		STAT0_CONFIG	4-0	Configure STAT0 output pin. (Refer to above for decoding)	RW	0
009h	IO_CONFIG2	RSVD	15	Reserved.	RW	0
		STAT5_CONFIG	14-10	Configure STAT5 output pin. (Refer to above for decoding)	RW	6
		STAT4_CONFIG	9-5	Configure STAT4 output pin. (Refer to above for decoding)	RW	4
		STAT3_CONFIG	4-0	Configure STAT3 output pin. (Refer to above for decoding)	RW	3

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
00Ah	ANC_CONTROL	RSVD	15-4	Reserved.	RW	0
		ANC_DATA_SWITCH	3	Switches between FIFO memories.	RW	0
		ANC_DATA_DEL	2	Remove Ancillary Data from output video stream, set to Luma and Chroma blanking values.	RW	0
		HD_ANC_Y1_C2	1	Extract Ancillary data from Luma and Chroma channels (HD inputs) Extract Ancillary data from Data Stream 1 and Data Stream 2 (3G Level A inputs) Extract Ancillary data from Luma and Chroma channels of Data Stream 1 (3G Level B inputs, when ANC_EXT_SEL_DS2_$\overline{DS1}$ = 0) Extract Ancillary data from Luma and Chroma channels of Data Stream 2 (3G Level B inputs, when ANC_EXT_SEL_DS2_$\overline{DS1}$ = 1)	RW	0
		HD_ANC_C2	0	Extract Ancillary data only from Chroma channel (HD inputs) Extract Ancillary data only from Data Stream 2 (3G Level A inputs) Extract Ancillary data only from Chroma channel of Data Stream 1 (3G Level B inputs, when ANC_EXT_SEL_DS2_$\overline{DS1}$ = 0) Extract Ancillary data only from Chroma channel of Data Stream 2 (3G Level B inputs, when ANC_EXT_SEL_DS2_$\overline{DS1}$ = 1)	RW	0
00Bh	ANC_LINE_A	RSVD	15-11	Reserved.	R/W	0
		ANC_LINE_A	10-0	Video Line to extract Ancillary data from.	R/W	0
00Ch	ANC_LINE_B	RSVD	15-11	Reserved.	R/W	0
		ANC_LINE_B	10-0	Second video Line to extract Ancillary data from.	R/W	0
00Dh - 00Eh	RSVD	RSVD	15-0	Reserved.	R	0
00Fh	ANC_TYPE1_AP2	ANC_TYPE1_DS1	15-0	Programmable DID/SDID pair #1 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats.	R/W	0
010h	ANC_TYPE2_AP2	ANC_TYPE2_DS1	15-0	Programmable DID/SDID pair #2 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats.	R/W	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
011h	ANC_TYPE_3 _AP1	ANC_TYPE3_DS1	15-0	Programmable DID/SDID pair #3 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats.	R/W	0
012h	ANC_TYPE_4 _AP1	ANC_TYPE4_DS1	15-0	Programmable DID/SDID pair #4 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats.	R/W	0
013h	ANC_TYPE_5 _AP1	ANC_TYPE5_DS1	15-0	Programmable DID/SDID pair #5 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats.	R/W	0
014h	ANC_TYPE_1 _AP2	ANC_TYPE1_DS2	15-0	Programmable DID/SDID pair #1 to extract from 3G Level B Data Stream 2.	R/W	0
015h	ANC_TYPE_2 _AP2	ANC_TYPE2_DS2	15-0	Programmable DID/SDID pair #2 to extract from 3G Level B Data Stream 2.	R/W	0
016h	ANC_TYPE_3 _AP2	ANC_TYPE3_DS2	15-0	Programmable DID/SDID pair #3 to extract from 3G Level B Data Stream 2.	R/W	0
017h	ANC_TYPE_4 _AP2	ANC_TYPE4_DS2	15-0	Programmable DID/SDID pair #4 to extract from 3G Level B Data Stream 2.	R/W	0
018h	ANC_TYPE_5 _AP2	ANC_TYPE5_DS2	15-0	Programmable DID/SDID pair #5 to extract from 3G Level B Data Stream 2.	R/W	0
019h	VIDEO_FORMAT _352_A_1	VIDEO_FORMAT_2_DS1	15-8	SMPTE 352M embedded packet – byte 2.	R	0
		VIDEO_FORMAT_1_DS1	7-0	SMPTE 352M embedded packet – byte 1: [7]: Version identifier [6:0]: Video Payload Identifier.	R	0
01Ah	VIDEO_FORMAT _352_B_1	VIDEO_FORMAT_4_DS1	15-8	SMPTE 352M embedded packet – byte 4.	R	0
		VIDEO_FORMAT_3_DS1	7-0	SMPTE 352M embedded packet – byte 3.	R	0
01Bh	VIDEO_FORMAT _352_A_2	VIDEO_FORMAT_2_DS2	15-8	SMPTE 352M embedded packet – byte 2 (3G Data Stream 2 only).	R	0
		VIDEO_FORMAT_1_DS2	7-0	SMPTE 352M embedded packet – byte 1 (3G Data Stream 2 only): [7]: Version identifier [6:0]: Video Payload Identifier.	R	0
01Ch	VIDEO_FORMAT _352_B_2	VIDEO_FORMAT_4_DS2	15-8	SMPTE 352M embedded packet – byte 4 (3G Data Stream 2 only).	R	0
		VIDEO_FORMAT_3_DS2	7-0	SMPTE 352M embedded packet – byte 3 (3G Data Stream 2 only).	R	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
01Dh	VIDEO_FORMAT_352_INS_A	VIDEO_FORMAT_2_INS	15-8	SMPTE 352M packet - byte 2 to be embedded after Level B to Level A conversion.	R/W	0
		VIDEO_FORMAT_1_INS	7-0	SMPTE 352M packet - byte 1 to be embedded after Level B to Level A conversion.	R/W	0
01Eh	VIDEO_FORMAT_352_INS_B	VIDEO_FORMAT_4_INS	15-8	SMPTE 352M packet - byte 4 to be embedded after Level B to Level A conversion.	R/W	0
		VIDEO_FORMAT_3_INS	7-0	SMPTE 352M packet - byte 3 to be embedded after Level B to Level A conversion.	R/W	0
01Fh	RASTER_STRUC_1	RSVD	15-14	Reserved.	R	0
		WORDS_PER_ACTLINE	13-0	Words Per Active Line.	R	0
020h	RASTER_STRUC_2	RSVD	15-14	Reserved.	R	0
		WORDS_PER_LINE	13-0	Total Words Per Line.	R	0
021h	RASTER_STRUC_3	RSVD	15-11	Reserved.	R	0
		LINES_PER_FRAME	10-0	Total Lines Per Frame.	R	0
022h	RASTER_STRUC_4	RATE_SEL_READBACK	15-14	Read back detected data rate: 0 = HD, 1,3=SD, 2=3G	R	0
		M	13	Specifies detected M value 0: 1.000 1: 1.001	R	0
		STD_LOCK	12	Video standard lock.	R	0
		INT_$\overline{\text{PROG}}$	11	Interlaced or progressive.	R	0
		ACTLINE_PER_FIELD	10-0	Active lines per frame.	R	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
023h	FLYWHEEL _STATUS	RSVD	15-5	Reserved.	R	0
		V_LOCK_DS2	4	Indicates that the timing signal generator is locked to vertical timing (3G Level B Data Stream 2 only).	R	0
		H_LOCK_DS2	3	Indicates that the timing signal generator is locked to horizontal timing (3G Level B Data Stream 2 only).	R	0
		RSVD	2	Reserved.	R	0
		V_LOCK_DS1	1	Indicates that the timing signal generator is locked to vertical timing (3G Level B Data Stream 1, 3G Level A, HD and SD inputs).	R	0
		H_LOCK_DS1	0	Indicates that the timing signal generator is locked to horizontal timing (3G Level B Data Stream 1, 3G Level A, HD and SD inputs).	R	0
024h	RATE_SEL	RSVD	15-3	Reserved.	R	0
		AUTO/$\overline{\text{MAN}}$	2	Detect data rate automatically (1) or program manually (0).	R/W	1
		RATE_SEL_TOP	1-0	Programmable rate select in manual mode: 0 = HD, 1,3=SD, 2=3G	R/W	0
025h	TIM_861_ FORMAT	RSVD	15-7	Reserved.	R	0
		FORMAT_ERR	6	Indicates standard is not recognized for CEA 861 conversion.	R	1
		FORMAT_ID_861	5-0	CEA-861 format ID of input video stream. Refer to Table 4-9.	R	0
026h	TIM_861_CFG	RSVD	15-3	Reserved.	R	0
		VSYNC_INVERT	2	Invert output VSYNC pulse.	R/W	0
		HSYNC_INVERT	1	Invert output HSYNC pulse.	R/W	0
		TRS_861	0	Sets the timing reference outputs to DFP timing mode when set to '1'. By default, the timing reference outputs follow CEA-861 timing mode. Only valid when TIM_861 is set to '1'.	R/W	0
027h - 036h	RSVD	RSVD	–	Reserved.	R	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
037h	ERROR_MASK_1	RSVD	15-11	Reserved.	R	0
		ERROR_MASK_1	10-0	Error mask for global error vector (3G Level B Data Stream 1, 3G Level A, HD, SD): bit[0]: EAV_ERR_DS1 mask bit[1]: SAV_ERR_DS1 mask bit[2]: LNUM_ERR_DS1 mask bit[3]: YCRC_ERR_DS1 mask bit[4]: CCRC_ERR_DS1 mask bit[5]: YCS_ERR_DS1 mask bit[6]: CCS_ERR_DS1 mask bit[7]: Reserved bit[8]: AP_CRC_ERR mask bit[9]: FF_CRC_ERR mask bit[10]: VD_STD_ERR_DS1 mask	R/W	0
038h	ERROR_MASK_2	RSVD	15-7	Reserved.	R	0
		ERROR_MASK_2	6-0	Error mask for global error vector (3G Level B Data Stream 2 only): bit[0]: EAV_ERR_DS2 mask bit[1]: SAV_ERR_DS2 mask bit[2]: LNUM_ERR_DS2 mask bit[3]: YCRC_ERR_DS2 mask bit[4]: CCRC_ERR_DS2 mask bit[5]: YCS_ERR_DS2 mask bit[6]: CCS_ERR_DS2 mask	R/W	0
039h -6Bh	RSVD	RSVD	15-0	Reserved.	R	0
06Ch	CLK_GEN	RSVD	15-6	Reserved.	R/W	0
		DEL_LINE_CLK_SEL	5	Choses between the in-phase (0) and quadrature (1) clocks for DDR mode.	R/W	0
		DEL_LINE_OFFSET	4-0	Controls the offset for the delay line.	R/W	0

Table 4-18: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
06Dh	IO_DRIVE _STRENGTH	RSVD	15-6	Reserved.	R/W	0
		IO_DS_CTRL_DOUT_MSB	5-4	Drive strength adjustment for DOUT[19:10] outputs and PCLK output: 00: 4mA; 01: 8mA; 10: 10mA(1.8V), 12mA(3.3V); 11: 12mA(1.8V), 16mA(3.3V)	R/W	2
		IO_DS_CTRL_STAT	3-2	Drive strength adjustment for STAT[5:0] outputs: 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V)	R/W	2
		IO_DS_CTRL_DOUT_LSB	1-0	Drive strength adjustment for DOUT[9:0] outputs: 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V)	R/W	3
06Eh - 072h	RSVD	RSVD	–	Reserved.	R/W	0
073h	EQ_BYPASS	RSVD	15-10	Reserved.	R/W	0
		EQ_BYPASS	9	0: non-bypass EQ 1: bypass EQ	R/W	0
		RSVD	8-0	Reserved.	R/W	0
074h -085h	RSVD	RSVD	15-0	Reserved.	R/W	0

Table 4-19: ANC Extraction FIFO Access Registers

Address	Register Name	Bit	Description	R/W	Default
800h - BFFh	ANC_PACKET_BANK	15-0	Extracted Ancillary Data 91024 words. Bit 15-8: Most Significant Word (MSW). Bit 7-0: Least Significant Word (LSW). See Section 4.18.8.	R	0

Legend:

R = Read only
ROCW = Read Only, Clear on Write
R/W = Read or Write
W = Write only

4.21 JTAG Test Operation

When the JTAG/$\overline{\text{HOST}}$ pin of the GS2961 is set HIGH, the host interface port is configured for JTAG test operation. In this mode, pins E7, F8, F7, and E8 become TDO, TCK, TMS, and TDI. In addition, the $\overline{\text{RESET\_TRST}}$ pin operates as the test reset pin.

Boundary scan testing using the JTAG interface is enabled in this mode.

There are two ways in which JTAG can be used:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly.
2. Under control of a host processor for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the JTAG/$\overline{\text{HOST}}$ input signal. This is shown in Figure 4-40.

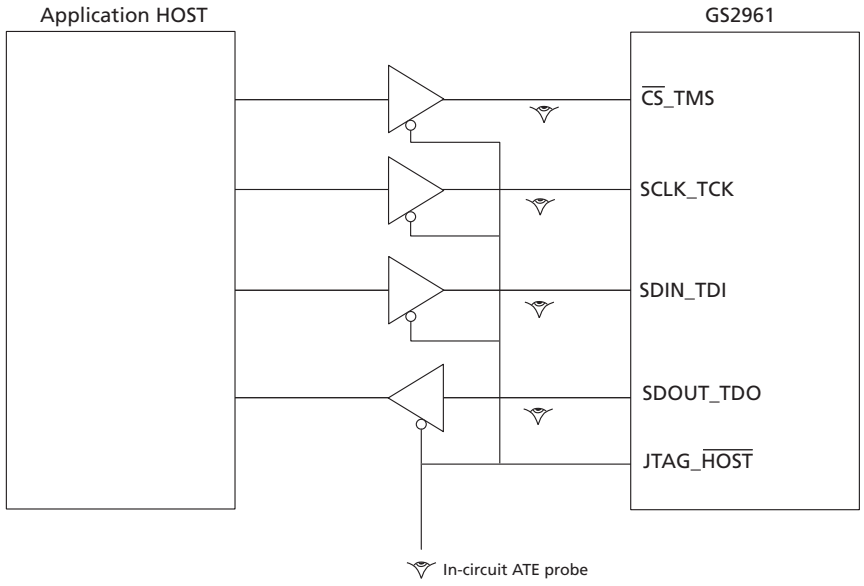


Figure 4-40: In-Circuit JTAG

Alternatively, if the test capabilities are to be used in the system, the host processor may still control the JTAG/$\overline{\text{HOST}}$ input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 4-41.

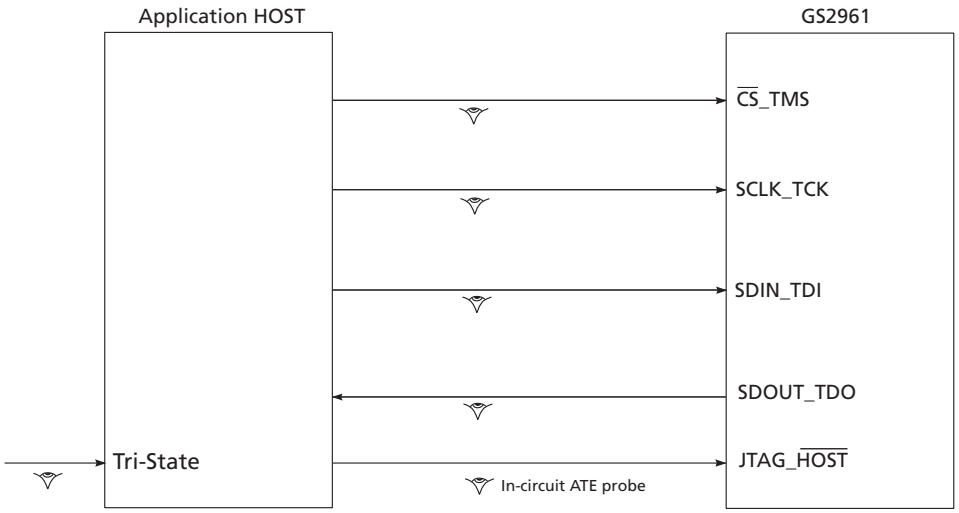


Figure 4-41: System JTAG

Scan coverage is limited to digital pins only. There is no scan coverage for analog pins VCO, SDO/SDO, RSET, LF, and CP_RES.

The JTAG/HOST pin must be held LOW during scan and therefore has no scan coverage.

Please contact your Gennum representative to obtain the BSDL model for the GS2961.

4.22 Device Power-up

Because the GS2961 is designed to operate in a multi-voltage environment, any power-up sequence is allowed. The charge pump, phase detector, core logic, serial digital output and I/O buffers can all be powered up in any order.

4.23 Device Reset

NOTE: At power-up, the device must be reset to operate correctly.

In order to initialize all internal operating conditions to their default states, hold the $\overline{\text{RESET\_TRST}}$ signal LOW for a minimum of t_{reset} = 10ms after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs are driven to a high-impedance state.

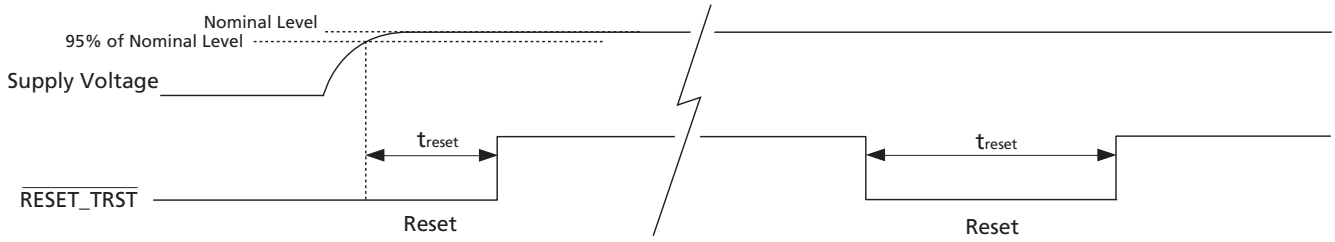


Figure 4-42: Reset Pulse

4.24 Standby Mode

The STANDBY pin reduces power to a minimum by disabling all circuits except for the register configuration. Upon removal of the signal to the STANDBY pin, the device returns to its previous operating condition within 1 second, without requiring input from the host interface.

5. Application Reference Design

5.1 High Gain Adaptive Cable Equalizers

The GS2961 has an integrated adaptive cable equalizer. In order to extend the cable length that an equalizer will remain operational at, it is necessary for the equalizer to have high gain.

A video cable equalizer must provide wide band gain over a range of frequencies in order to accommodate the range of data rates and signal patterns that are present in a SMPTE compliant serial video stream.

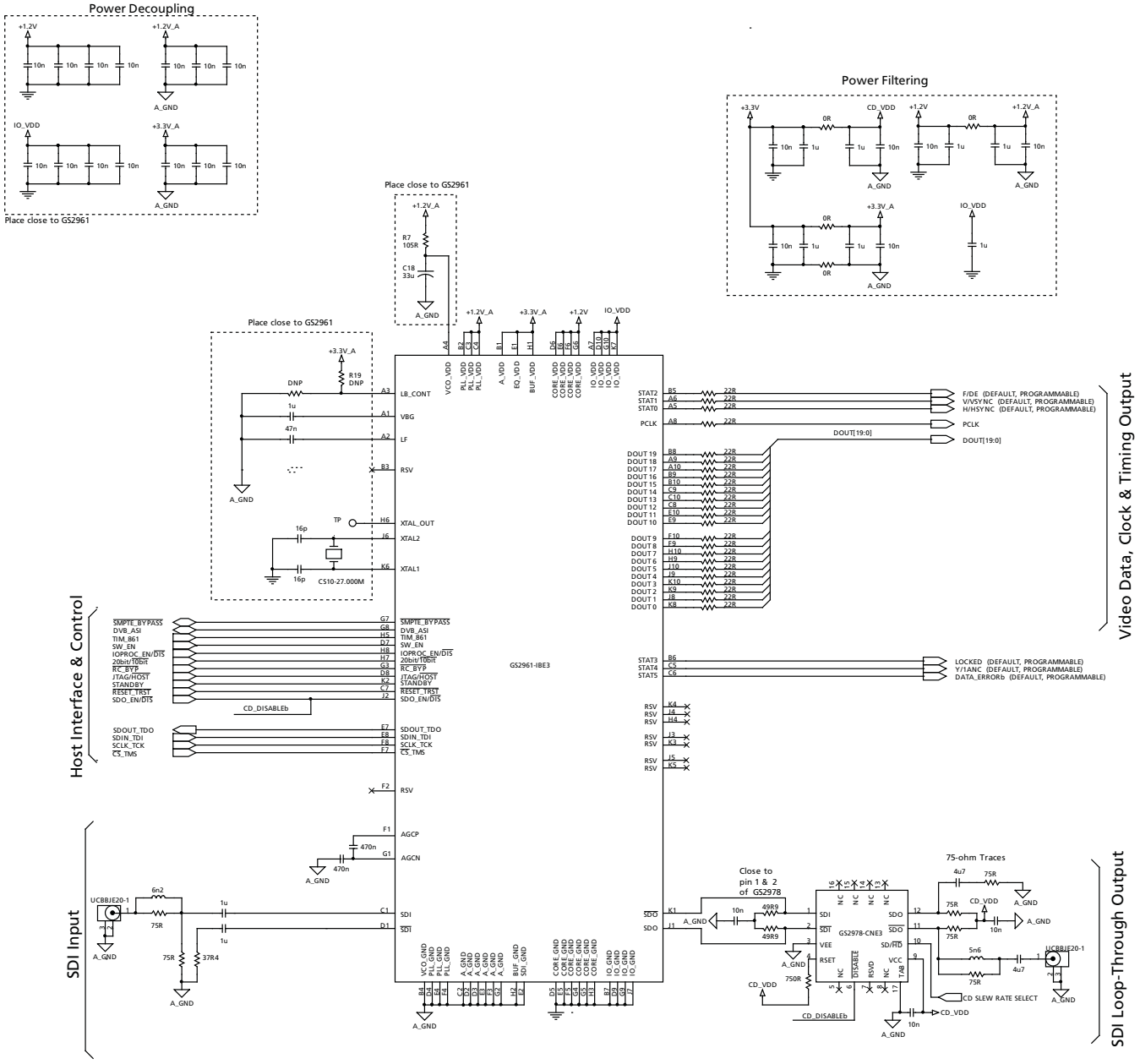
Small levels of signal or noise present at the input pins of the GS2961 may cause chatter at the output. In order to prevent this from happening, particular attention must be paid to board layout.

5.2 PCB Layout

Special attention must be paid to component layout when designing Serial Digital Interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for 3Gb/s rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- The PCB ground plane is removed under the GS2961 input components to minimize parasitic capacitance.
- High speed traces are curved to minimize impedance changes.

5.3 Typical Application Circuit

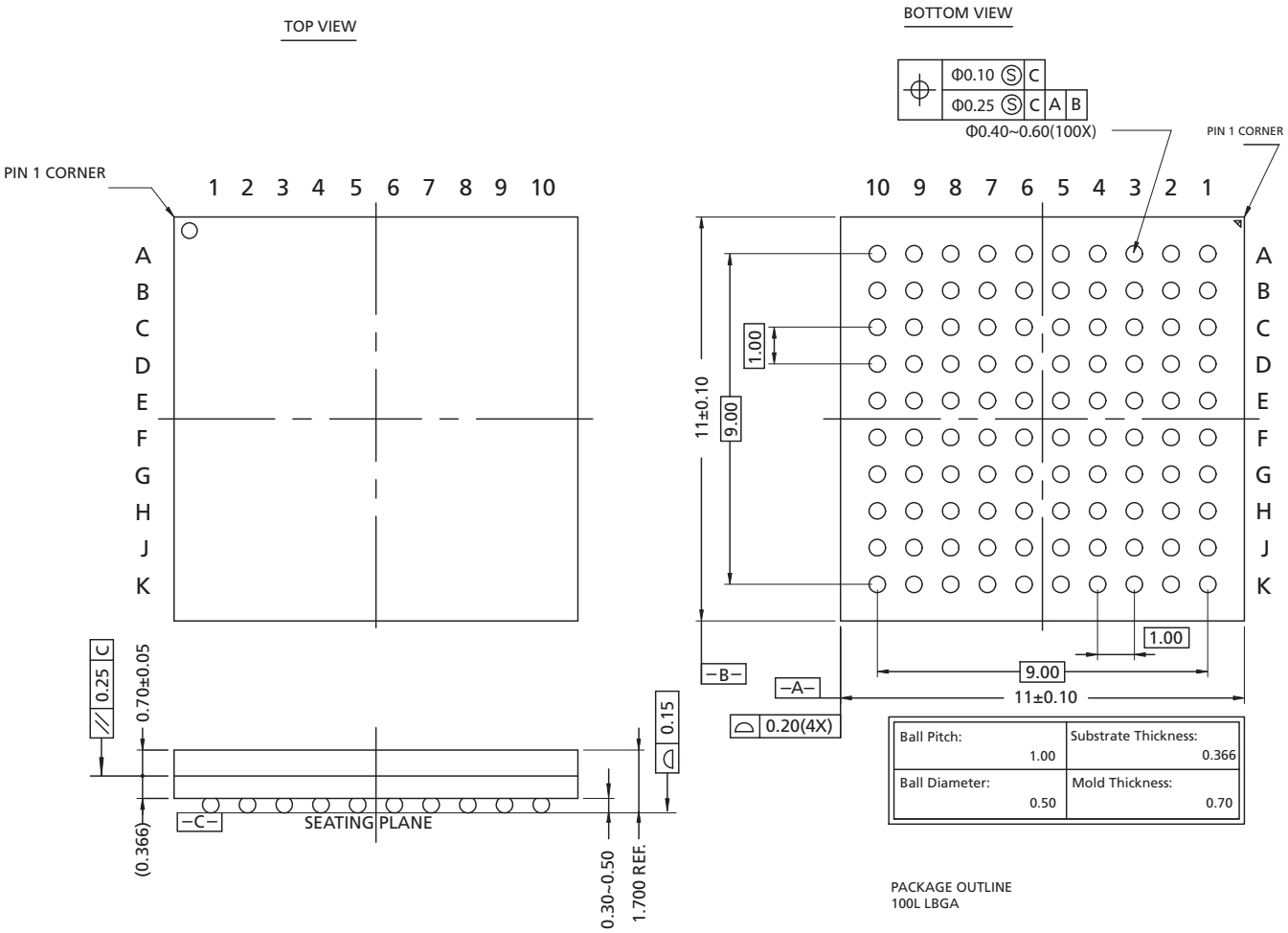


6. References & Relevant Standards

SMPTE 125M	Component video signal 4:2:2 – bit parallel interface
SMPTE 259M	10-bit 4:2:2 Component and 4fsc Composite Digital Signals - Serial Digital Interface
SMPTE 260M	1125 / 60 high definition production system – digital representation and bit parallel interface
SMPTE 267M	Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio
SMPTE 272M	Formatting AES/EBU Audio and Auxiliary Data into Digital Video Ancillary Data Space
SMPTE 274M	1920 x 1080 scanning analog and parallel digital interfaces for multiple picture rates
SMPTE 291M	Ancillary Data Packet and Space Formatting
SMPTE 292M	Bit-Serial Digital Interface for High-Definition Television Systems
SMPTE 293M	720 x 483 active line at 59.94Hz progressive scan production – digital representation
SMPTE 296M	1280 x 720 scanning, analog and digital representation and analog interface
SMPTE 299M	24-Bit Digital Audio Format for HDTV Bit-Serial Interface
SMPTE 305M	Serial Data Transport Interface
SMPTE 348M	High Data-Rate Serial Data Transport Interface (HD-SDTI)
SMPTE 352M	Video Payload Identification for Digital Television Interfaces
SMPTE 372M	Dual Link 292M Interface for 1920 x 1080 Picture Raster
SMPTE 424M	Television - 3Gb/s Signal/Data Serial Interface
SMPTE 425M	Television - 3Gb/s Signal/Data Serial Interface - Source Image Format Mapping
SMPTE RP165	Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
SMPTE RP168	Definition of Vertical Interval Switching Point for Synchronous Video Switching
CEA 861	Video Timing Requirements

7. Package & Ordering Information

7.1 Package Dimensions



PACKAGE OUTLINE
100L LBGA

PACKAGE SIZE: 11 x 11 x 1.71mm

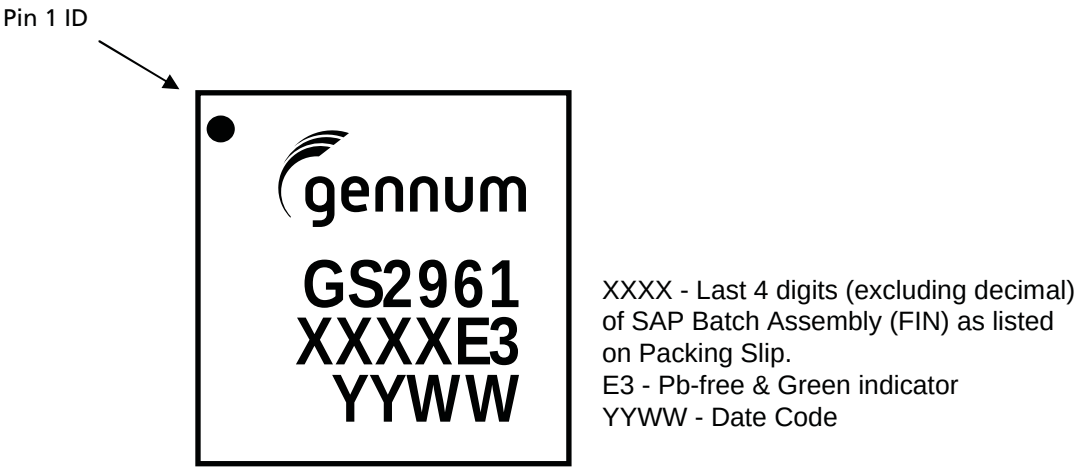
*THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

7.2 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	11mm x 11mm 100-ball LBGA
Package Drawing Reference	JEDEC M0192 (with exceptions noted in Package Dimensions on page 101).
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	15.4°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	37.1°C/W
Junction to Board Thermal Resistance, θ_{j-b}	26.4°C/W
Psi, ψ	0.4°C/W
Pb-free and RoHS Compliant	Yes

7.3 Marking Diagram



7.4 Solder Reflow Profiles

The GS2961 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 7-1.

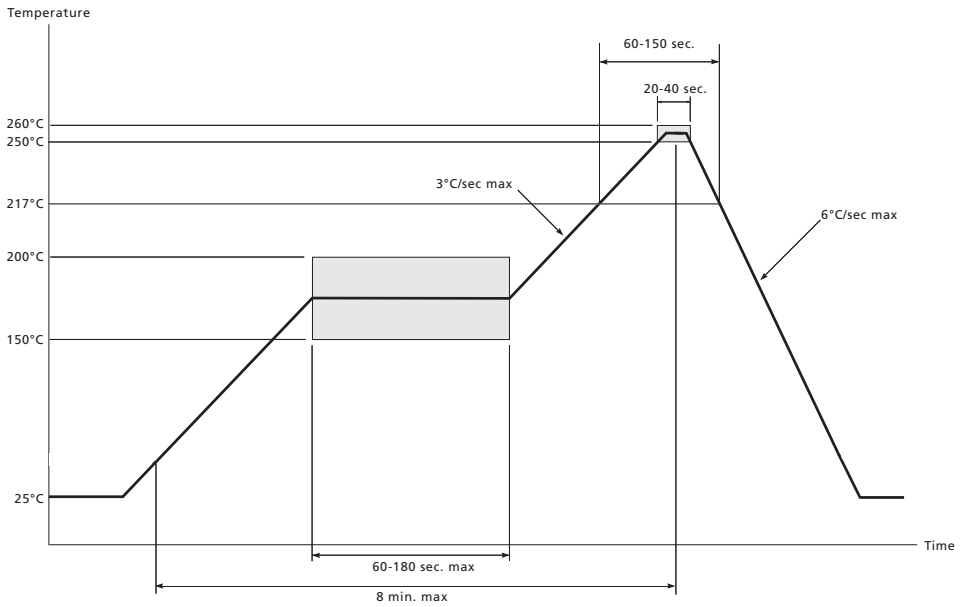


Figure 7-1: Pb-free Solder Reflow Profile

7.5 Ordering Information

Part Number	Package	Pb-free	Temperature Range
GS2961-IBE3	100-ball BGA	Yes	-20°C to 85°C

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

GENNUM CORPORATE HEADQUARTERS
4281 Harvester Road, Burlington, Ontario L7L 5M4 Canada
Phone: +1 (905) 632-2996
E-mail: corporate@gennum.com
Fax: +1 (905) 632-2055
www.gennum.com

OTTAWA
232 Herzberg Road, Suite 101
Kanata, Ontario K2K 2A1
Canada
Phone: +1 (613) 270-0458
Fax: +1 (613) 270-0429

CALGARY
3553 - 31st St. N.W., Suite 210
Calgary, Alberta T2L 2K7
Canada
Phone: +1 (403) 284-2672

UNITED KINGDOM
North Building, Walden Court
Parsonage Lane,
Bishop's Stortford Hertfordshire, CM23 5DB
United Kingdom
Phone: +44 1279 714170
Fax: +44 1279 714171

INDIA
#208(A), Nirmala Plaza,
Airport Road, Forest Park Square
Bhubaneswar 751009
India
Phone: +91 (674) 653-4815
Fax: +91 (674) 259-5733

SNOWBUSH IP - A DIVISION OF GENNUM
439 University Ave. Suite 1700
Toronto, Ontario M5G 1Y8
Canada
Phone: +1 (416) 925-5643
Fax: +1 (416) 925-0581
E-mail: sales@snowbush.com
Web Site: http://www.snowbush.com

MEXICO
288-A Paseo de Maravillas
Jesus Ma., Aguascalientes
Mexico 20900
Phone: +1 (416) 848-0328

JAPAN KK
Shinjuku Green Tower Building 27F
6-14-1, Nishi Shinjuku
Shinjuku-ku, Tokyo, 160-0023
Japan
Phone: +81 (03) 3349-5501
Fax: +81 (03) 3349-5505
E-mail: gennum-japan@gennum.com
Web Site: http://www.gennum.co.jp

TAIWAN
6F-4, No.51, Sec.2, Keelung Rd.
Sinyi District, Taipei City 11502
Taiwan R.O.C.
Phone: (886) 2-8732-8879
Fax: (886) 2-8732-8870
E-mail: gennum-taiwan@gennum.com

GERMANY
Hainbuchenstraße 2
80935 Muenchen (Munich), Germany
Phone: +49-89-35831696
Fax: +49-89-35804653
E-mail: gennum-germany@gennum.com

NORTH AMERICA WESTERN REGION
Bayshore Plaza
2107 N 1st Street, Suite #300
San Jose, CA 95131
United States
Phone: +1 (408) 392-9454
Fax: +1 (408) 392-9427
E-mail: naw_sales@gennum.com

NORTH AMERICA EASTERN REGION
4281 Harvester Road
Burlington, Ontario L7L 5M4
Canada
Phone: +1 (905) 632-2996
Fax: +1 (905) 632-2055
E-mail: nae_sales@gennum.com

KOREA
8F Jinnex Lakeview Bldg.
65-2, Bangidong, Songpagu
Seoul, Korea 138-828
Phone: +82-2-414-2991
Fax: +82-2-414-2998
E-mail: gennum-korea@gennum.com

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331