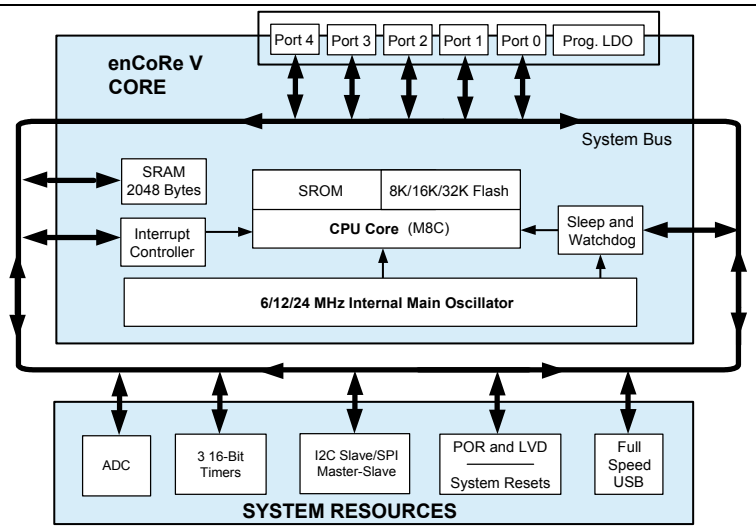
CY7C6431x
CY7C6434x, CY7C6435x
enCoRe™ V Full Speed USB Controller

Features

- Powerful Harvard Architecture Processor
  - M8C processor speeds running up to 24 MHz
  - Low power at high processing speeds
  - Interrupt controller
  - 3.0V to 5.5V operating voltage without USB
  - Operating voltage with USB enabled:
    - 3.15V to 3.45V when supply voltage is around 3.3V
    - 4.35V to 5.25V when supply voltage is around 5.0V
  - Commercial temperature range: 0°C to +70°C
  - Industrial temperature range: -40°C to +85°C
- Flexible On-Chip Memory
  - Up to 32K Flash program storage:
    - 50,000 erase and write cycles
    - Flexible protection modes
  - Up to 2048 bytes SRAM data storage
  - In-System Serial Programming (ISSP)
- Complete Development Tools
  - Free development tool (PSoC Designer™)
  - Full featured, in-circuit emulator and programmer
  - Full speed emulation
  - Complex breakpoint structure
  - 128K trace memory
- Precision, Programmable Clocking
  - Crystal-less oscillator with support for an external crystal or resonator
  - Internal ±5.0% 6, 12, or 24 MHz main oscillator:
    - 0.25% accuracy with Oscillator Lock to USB data, no external components required
    - Internal low speed oscillator at 32 kHz for watchdog and sleep. The frequency range is 19 to 50 kHz with a 32 kHz typical value
- Programmable Pin Configurations
  - Up to 36 GPIO (Depending on Package)
  - 25 mA sink current on all GPIO
  - Pull Up, High Z, Open Drain, CMOS drive modes on all GPIO
  - CMOS Drive Mode (5 mA Source Current) on Ports 0 and 1:
    - 20 mA (at 3.0V) Total Source Current
  - Low dropout voltage regulator for Port 1 pins:
    - Programmable to output 3.0, 2.5, or 1.8V
  - Selectable, regulated digital I/O on Port 1
  - Configurable input threshold for Port 1
  - Hot-swappable Capability on Port 1
- Full-Speed USB (12 Mbps)
  - Eight unidirectional endpoints
  - One bidirectional control endpoint
  - USB 2.0 compliant
  - Dedicated 512 bytes buffer
  - No external crystal required
- Additional System Resources
  - Configurable communication speeds
  - I^2C slave:
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
    - Implementation requires no clock stretching
    - Implementation during sleep modes with less than 100 µA
    - Hardware address detection
  - SPI master and SPI slave:
    - Configurable between 46.9 kHz and 12 MHz
  - Three 16-bit timers
  - 10-bit ADC used to monitor battery voltage or other signals with external components
  - Watchdog and sleep timers
  - Integrated supervisory circuit

enCoRe V Block Diagram



Functional Overview

The enCoRe V family of devices are designed to replace multiple traditional full-speed USB microcontroller system components with one, low cost single-chip programmable component. Communication peripherals (I2C/SPI), a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as illustrated in the "enCoRe V Block Diagram" on page 1, consists of two main areas: the CPU core and the system resources. Depending on the enCoRe V package, up to 36 general purpose I/O (GPIO) are also included.

This product is an enhanced version of Cypress's successful full speed-USB peripheral controllers. Enhancements include faster CPU at lower voltage operation, lower current consumption, twice the RAM and Flash, hot-swappable I/Os, I^2C hardware address recognition, new very low current sleep mode, and new package options.

The enCoRe V Core

The enCoRe V Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

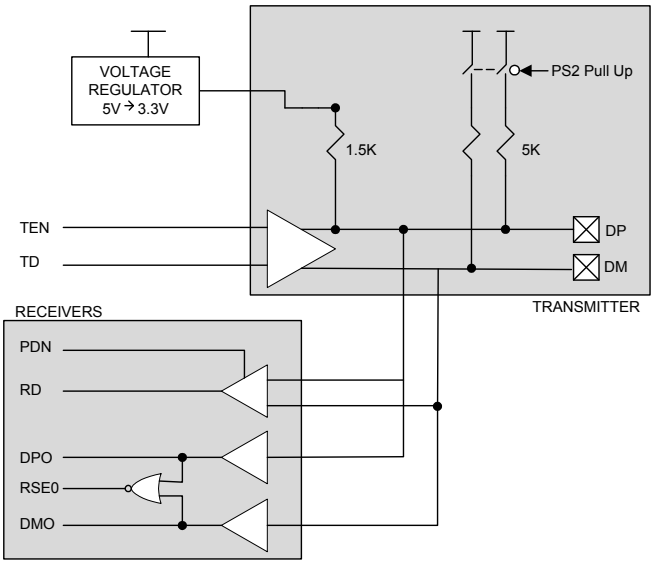
System resources provide additional capability, such as a configurable I^2C slave and SPI master-slave communication interface and various system resets supported by the M8C.

Full-Speed USB

The enCoRe V USB system resource adheres to the USB 2.0 Specification for full speed devices operating at 12 Mb/second with one upstream port and one USB address. enCoRe V USB consists of these components:

- Serial Interface Engine (SIE) block.
- PSoC Memory Arbiter (PMA) block.
- 512 bytes of dedicated SRAM.
- A full-speed USB Transceiver with internal regulator and two dedicated USB pins.

Figure 1. USB Transceiver Regulator



At the enCoRe V system level, the full-speed USB system resource interfaces to the rest of the enCoRe V by way of the M8C's register access instructions and to the outside world by way of the two USB pins. The SIE supports nine endpoints including a bidirectional control endpoint (endpoint 0) and eight unidirectional data endpoints (endpoints 1 to 8). The unidirectional data endpoints are individually configurable as either IN or OUT.

The USB Serial Interface Engine (SIE) allows the enCoRe V device to communicate with the USB host at full speed data rates (12 Mb/s). The SIE simplifies the interface to USB traffic by automatically handling the following USB processing tasks without firmware intervention:

- Translates the encoded received data and formats the data to be transmitted on the bus.
- Generates and checks CRCs. Incoming packets failing checksum verification are ignored.
- Checks addresses. Ignores all transactions not addressed to the device.
- Sends appropriate ACK/NAK/Stall handshakes.
- Identifies token type (SETUP, IN, OUT) and sets the appropriate token bit once a valid token in received.
- Identifies Start-of-Frame (SOF) and saves the frame count.
- Sends data to or retrieves data from the USB SRAM, by way of the PSoC Memory Arbiter (PMA).

[+] Feedback

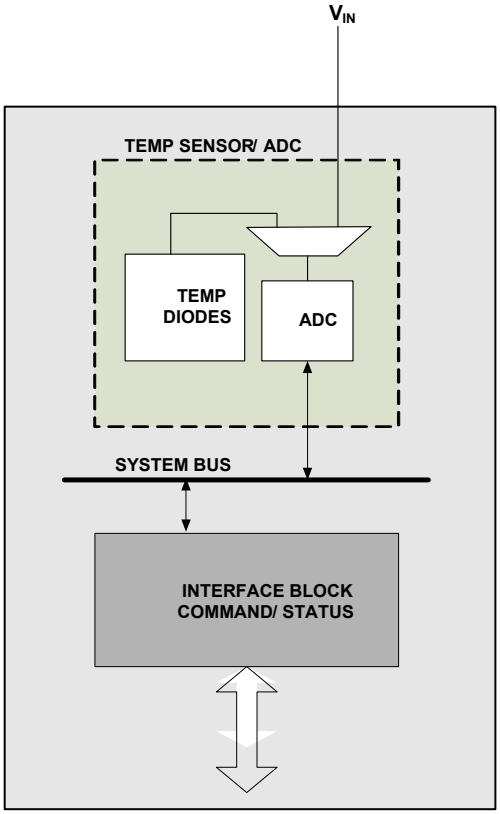
Firmware is required to handle various parts of the USB interface. The SIE issues interrupts after key USB events to direct firmware to appropriate tasks:

- Fill and empty the USB data buffers in USB SRAM.
- Enable PMA channels appropriately.
- Coordinate enumeration by decoding USB device requests.
- Suspend and resume coordination.
- Verify and select data toggle values.

10-bit ADC

The ADC on enCoRe V device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog Mux Bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 2. ADC System Performance Block Diagram



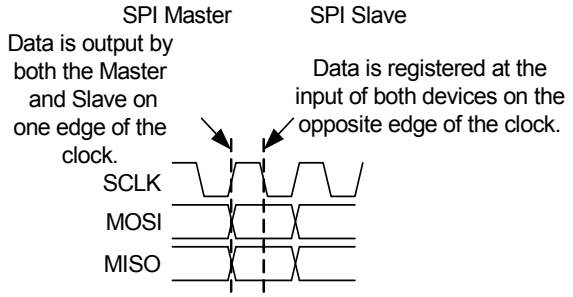
The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the Analog Global Input Mux or the temperature sensor with an input voltage range of 0V to 1.3 V, where 1.3V is 72 percent of full scale.

In the ADC only configuration (the ADC MUX selects the Analog Mux Bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the desired resolution of the ADC. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

SPI

The Serial Peripheral Interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

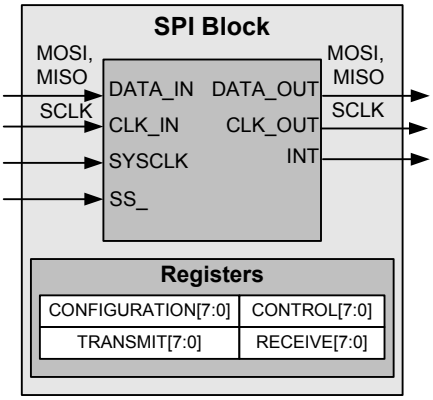
Figure 3. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 4. SPI Block Diagram



[+] Feedback

SPI configuration register (SPI_CFG) sets master/slave functionality, clock speed, and interrupt select. SPI control register (SPI_CR) provides four control bits and four status bits for device interfacing and synchronization.

The SPIM hardware has no support for driving the Slave Select (SS_) signal. The behavior and use of this signal is dependent on the application and enCoRe V device and, if required, must be implemented in firmware.

There is an additional data input in the SPIS, Slave Select (SS_), which is an active low signal. SS_ must be asserted to enable the SPIS to receive and transmit. SS_ has two high level functions:

- To allow for the selection of a given slave in a multi-slave environment.
- To provide additional clocking for TX data queuing in SPI modes 0 and 1.

I²C Slave

The I²C slave enhanced communications block is a serial-to-parallel processor, designed to interface the enCoRe V device to a two-wire I²C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I²C-specific support for status detection and generation of framing bits. By default, the I2C Slave Enhanced module is firmware compatible with the previous generation of I²C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing. The basic I²C features include:

- Slave, transmitter, and receiver operation.
- Byte processing for low CPU overhead.
- Interrupt or polling CPU interface.
- Support for clock rates of up to 400 kHz.
- 7- or 10-bit addressing (through firmware support).
- SMBus operation (through firmware support).

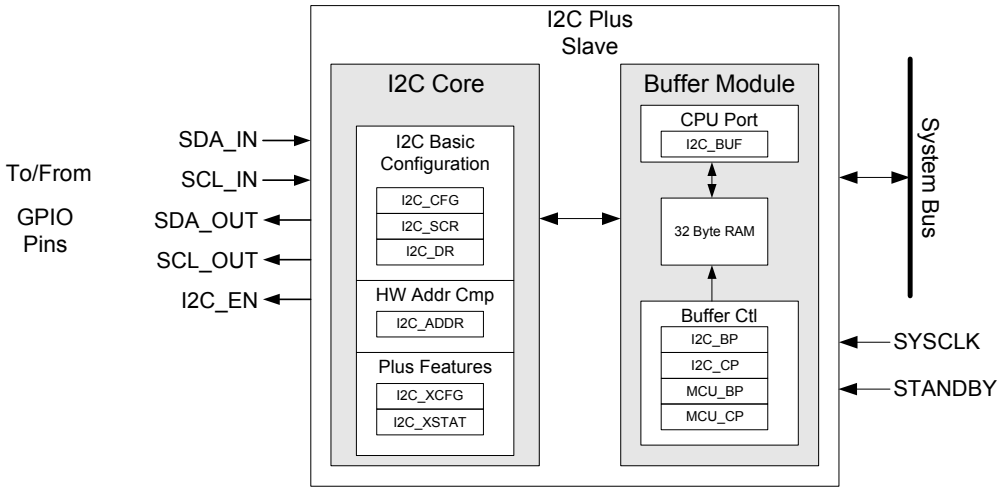
Enhanced features of the I²C Slave Enhanced Module include:

- Support for 7-bit hardware address compare.
- Flexible data buffering schemes.
- A "no bus stalling" operating mode.
- A low power bus monitoring mode.

The I²C block controls the data (SDA) and the clock (SCL) to the external I²C interface through direct connections to two dedicated GPIO pins. When I²C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I²C slave modules, the I²C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I²C bus continues. However, this I²C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI²C buffering mode, the I²C slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Figure 5. I²C Block Diagram



[+] Feedback

Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource.

- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- The 5V maximum input, 1.8, 2.5, or 3V selectable output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V family of parts.

Getting Started

The quickest path to understanding the enCoRe V silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the enCoRe V integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, reference the *PSoC Programmable System-on-Chip Technical Reference Manual*, which can be found on http://www.cypress.com/psoc.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest enCoRe V device data sheets on the web at http://www.cypress.com.

Development Kits

Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. Under Product Categories, click USB (Universal Serial Bus) to view a current list of available items.

Technical Training Modules

Free technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

Consultants

Certified USB consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

[+] Feedback

Development Tools

PSoC Designer™ is a Microsoft® Windows-based, integrated development environment for the enCoRe and PSoC devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the enCoRe and PSoC families.

PSoC Designer Software Subsystems

Chip-Level View

The chip-level view is a traditional integrated development environment (IDE) based on PSoC Designer 4.4. You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time.

System-Level View

The system-level view is a drag-and-drop visual embedded system design environment based on PSoC Designer.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the enCoRe and PSoC families of devices. The products enable you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program flash, read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural help and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all enCoRe and PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

[+] Feedback

Designing with PSoC Designer

The development process for the enCoRe V device differs from that of a traditional fixed function microprocessor. Powerful PSoC Designer tools get the core of your design up and running in minutes instead of hours.

The development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

The chip-level view provides a library of pre-built, pre-tested hardware peripheral components. These components are called “user modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed-signal varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application.

The chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter and contains other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system-level inputs, outputs, and communication interfaces to each other with valuator functions. In the chip-level view, you perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

[+] Feedback

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
API	application programming interface
CPU	central processing unit
GPIO	general purpose IO
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
LSb	least significant bit
LVD	low voltage detect
MSb	most significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
SLIMO	slow IMO
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 7 on page 16 lists all the abbreviations used to measure the enCoRe V devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

[+] Feedback

Pin Configuration

The enCoRe V USB device is available in a variety of packages which are listed and illustrated in the subsequent tables.

16-Pin Part Pinout

Figure 6. CY7C64315/CY7C64316 16-Pin enCoRe V USB Device

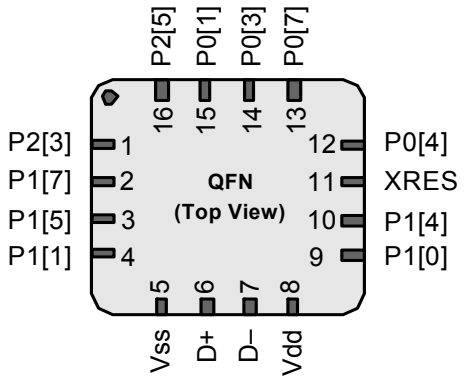


Table 1. 16-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
1	I/O	P2[3]	Digital I/O, Crystal Input (Xin)
2	IOHR	P1[7]	Digital I/O, SPI SS, I2C SCL
3	IOHR	P1[5]	Digital I/O, SPI MISO, I2C SDA
4	IOHR	P1[1][1, 2]	Digital I/O, ISSP CLK, 12C SCL, SPI MOSI
5	Power	Vss	Ground connection
6	USB line	D+	USB PHY
7	USB line	D–	USB PHY
8	Power	Vdd	Supply
9	IOHR	P1[0][1, 2]	Digital I/O, ISSP DATA, I2C SDA, SPI CLK
10	IOHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
11	Input	XRES	Active high external reset with internal pull down
12	IOH	P0[4]	Digital I/O
13	IOH	P0[7]	Digital I/O
14	IOH	P0[3]	Digital I/O
15	IOH	P0[1]	Digital I/O
16	I/O	P2[5]	Digital I/O, Crystal Output (Xout)

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Notes
1. During power up or reset event, device P1[0] and P1[1] may disturb the I2C bus. Use alternate pins if issues are encountered.
2. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

[+] Feedback

32-Pin Part Pinout

Figure 7. CY7C64343/CY7C64345 32-Pin enCoRe V USB Device

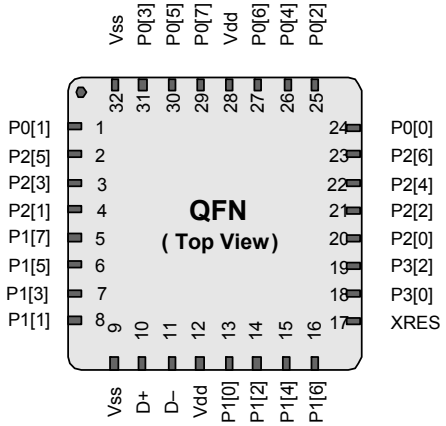


Table 2. 32-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
1	IOH	P0[1]	Digital I/O
2	I/O	P2[5]	Digital I/O, Crystal Output (Xout)
3	I/O	P2[3]	Digital I/O, Crystal Input (Xin)
4	I/O	P2[1]	Digital I/O
5	IOHR	P1[7]	Digital I/O, I2C SCL, SPI SS
6	IOHR	P1[5]	Digital I/O, I2C SDA, SPI MISO
7	IOHR	P1[3]	Digital I/O, SPI CLK
8	IOHR	P1[1][1, 2]	Digital I/O, ISSP CLK, I2C SCL, SPI MOSI
9	Power	Vss	Ground
10	I/O	D+	USB PHY
11	I/O	D–	USB PHY
12	Power	Vdd	Supply voltage
13	IOHR	P1[0][1, 2]	Digital I/O, ISSP DATA, I2C SDA, SPI CLK
14	IOHR	P1[2]	Digital I/O
15	IOHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
16	IOHR	P1[6]	Digital I/O
17	Reset	XRES	Active high external reset with internal pull down
18	I/O	P3[0]	Digital I/O
19	I/O	P3[2]	Digital I/O
20	I/O	P2[0]	Digital I/O
21	I/O	P2[2]	Digital I/O
22	I/O	P2[4]	Digital I/O
23	I/O	P2[6]	Digital I/O
24	IOH	P0[0]	Digital I/O
25	IOH	P0[2]	Digital I/O
26	IOH	P0[4]	Digital I/O
27	IOH	P0[6]	Digital I/O
28	Power	Vdd	Supply voltage
29	IOH	P0[7]	Digital I/O
30	IOH	P0[5]	Digital I/O
31	IOH	P0[3]	Digital I/O
32	Power	Vss	Ground
CP	Power	Vss	Ensure the center pad is connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

[+] Feedback

48-Pin Part Pinout

Figure 8. CY7C64355/CY7C64356 48-Pin enCoRe V USB Device

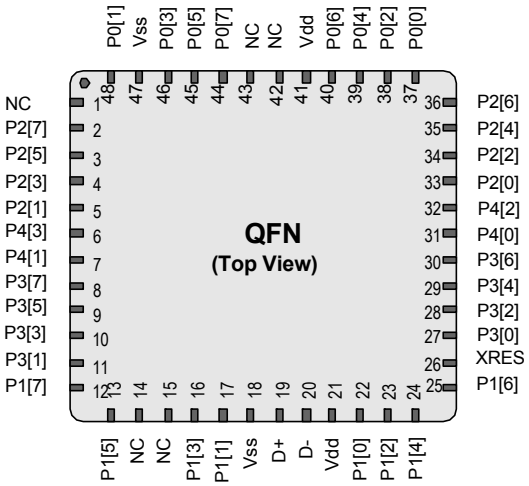


Table 3. 48-Pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
1	NC	NC	No connection
2	I/O	P2[7]	Digital I/O
3	I/O	P2[5]	Digital I/O, Crystal Out (Xout)
4	I/O	P2[3]	Digital I/O, Crystal In (Xin)
5	I/O	P2[1]	Digital I/O
6	I/O	P4[3]	Digital I/O
7	I/O	P4[1]	Digital I/O
8	I/O	P3[7]	Digital I/O
9	I/O	P3[5]	Digital I/O
10	I/O	P3[3]	Digital I/O
11	I/O	P3[1]	Digital I/O
12	IOHR	P1[7]	Digital I/O, I2C SCL, SPI SS
13	IOHR	P1[5]	Digital I/O, I2C SDA, SPI MISO
14	NC	NC	No connection
15	NC	NC	No connection
16	IOHR	P1[3]	Digital I/O, SPI CLK
17	IOHR	P1[1][1, 2]	Digital I/O, ISSP CLK, I2C SCL, SPI MOSI
18	Power	Vss	Supply ground
19	I/O	D+	USB
20	I/O	D–	USB
21	Power	Vdd	Supply voltage
22	IOHR	P1[0][1, 2]	Digital I/O, ISSP DATA, I2C SDA, SPI CLK
23	IOHR	P1[2]	Digital I/O,
24	IOHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
25	IOHR	P1[6]	Digital I/O

[+] Feedback

Table 3. 48-Pin Part Pinout (QFN) (continued)

Pin No.	Type	Pin Name	Description
26	XRES	Ext Reset	Active high external reset with internal pull down
27	I/O	P3[0]	Digital I/O
28	I/O	P3[2]	Digital I/O
29	I/O	P3[4]	Digital I/O
30	I/O	P3[6]	Digital I/O
31	I/O	P4[0]	Digital I/O
32	I/O	P4[2]	Digital I/O
33	I/O	P2[0]	Digital I/O
34	I/O	P2[2]	Digital I/O
35	I/O	P2[4]	Digital I/O
36	I/O	P2[6]	Digital I/O
37	IOH	P0[0]	Digital I/O
38	IOH	P0[2]	Digital I/O
39	IOH	P0[4]	Digital I/O
40	IOH	P0[6]	Digital I/O
41	Power	Vdd	Supply voltage
42	NC	NC	No connection
43	NC	NC	No connection
44	IOH	P0[7]	Digital I/O
45	IOH	P0[5]	Digital I/O
46	IOH	P0[3]	Digital I/O
47	Power	Vss	Supply ground
48	IOH	P0[1]	Digital I/O
CP	Power	Vss	Ensure the center pad is connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Register Reference

The section discusses the registers of the enCoRe V device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 4. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V device has a total register address space of 512 bytes. The register space is also referred to as IO space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

[+] Feedback

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	EP1_CNT0	40	#		80			C0	
PRT0IE	01	RW	EP1_CNT1	41	RW		81			C1	
	02		EP2_CNT0	42	#		82			C2	
	03		EP2_CNT1	43	RW		83			C3	
PRT1DR	04	RW	EP3_CNT0	44	#		84			C4	
PRT1IE	05	RW	EP3_CNT1	45	RW		85			C5	
	06		EP4_CNT0	46	#		86			C6	
	07		EP4_CNT1	47	RW		87			C7	
PRT2DR	08	RW	EP5_CNT0	48	#		88		I2C_XCFG	C8	RW
PRT2IE	09	RW	EP5_CNT1	49	RW		89		I2C_XSTAT	C9	R
	0A		EP6_CNT0	4A	#		8A		I2C_ADDR	CA	RW
	0B		EP6_CNT1	4B	RW		8B		I2C_BP	CB	R
PRT3DR	0C	RW	EP7_CNT0	4C	#		8C		I2C_CP	CC	R
PRT3IE	0D	RW	EP7_CNT1	4D	RW		8D		CPU_BP	CD	RW
	0E		EP8_CNT0	4E	#		8E		CPU_CP	CE	R
	0F		EP8_CNT1	4F	RW		8F		I2C_BUF	CF	RW
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18		PMA0_DR	58	RW		98		I2C_DR	D8	RW
	19		PMA1_DR	59	RW		99			D9	
	1A		PMA2_DR	5A	RW		9A		INT_CLR0	DA	RW
	1B		PMA3_DR	5B	RW		9B		INT_CLR1	DB	RW
	1C		PMA4_DR	5C	RW		9C		INT_CLR2	DC	RW
	1D		PMA5_DR	5D	RW		9D		INT_CLR3	DD	RW
	1E		PMA6_DR	5E	RW		9E		INT_MSK2	DE	RW
	1F		PMA7_DR	5F	RW		9F		INT_MSK1	DF	RW
	20			60			A0		INT_MSK0	E0	RW
	21			61			A1		INT_SW_EN	E1	RW
	22			62			A2		INT_VC	E2	RC
	23			63			A3		RES_WDT	E3	W
	24		PMA8_DR	64	RW		A4		INT_MSK3	E4	RW
	25		PMA9_DR	65	RW		A5			E5	
	26		PMA10_DR	66	RW		A6			E6	
	27		PMA11_DR	67	RW		A7			E7	
	28		PMA12_DR	68	RW		A8			E8	
SPI_TXR	29	W	PMA13_DR	69	RW		A9			E9	
SPI_RXR	2A	R	PMA14_DR	6A	RW		AA			EA	
SPI_CR	2B	#	PMA15_DR	6B	RW		AB			EB	
	2C		TMP_DR0	6C	RW		AC			EC	
	2D		TMP_DR1	6D	RW		AD			ED	
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		PT0_CFG	B0	RW		F0	
USB_SOF0	31	R		71		PT0_DATA1	B1	RW		F1	
USB_SOF1	32	R		72		PT0_DATA0	B2	RW		F2	
USB_CR0	33	RW		73		PT1_CFG	B3	RW		F3	
USBIO_CR0	34	#		74		PT1_DATA1	B4	RW		F4	
USBIO_CR1	35	#		75		PT1_DATA0	B5	RW		F5	
EP0_CR	36	#		76		PT2_CFG	B6	RW		F6	
EP0_CNT0	37	#		77		PT2_DATA1	B7	RW	CPU_F	F7	RL
EP0_DR0	38	RW		78		PT2_DATA0	B8	RW		F8	
EP0_DR1	39	RW		79			B9			F9	
EP0_DR2	3A	RW		7A			BA			FA	
EP0_DR3	3B	RW		7B			BB			FB	
EP0_DR4	3C	RW		7C			BC			FC	
EP0_DR5	3D	RW		7D			BD			FD	
EP0_DR6	3E	RW		7E			BE		CPU_SCR1	FE	#
EP0_DR7	3F	RW		7F			BF		CPU_SCR0	FF	#

Gray fields are reserved; do not access these fields. # Access is bit specific.

[+] Feedback

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	PMA4_RA	40	RW		80			C0	
PRT0DM1	01	RW	PMA5_RA	41	RW		81			C1	
	02		PMA6_RA	42	RW		82			C2	
	03		PMA7_RA	43	RW		83			C3	
PRT1DM0	04	RW	PMA8_WA	44	RW		84			C4	
PRT1DM1	05	RW	PMA9_WA	45	RW		85			C5	
	06		PMA10_WA	46	RW		86			C6	
	07		PMA11_WA	47	RW		87			C7	
PRT2DM0	08	RW	PMA12_WA	48	RW		88			C8	
PRT2DM1	09	RW	PMA13_WA	49	RW		89			C9	
	0A		PMA14_WA	4A	RW		8A			CA	
	0B		PMA15_WA	4B	RW		8B			CB	
PRT3DM0	0C	RW	PMA8_RA	4C	RW		8C			CC	
PRT3DM1	0D	RW	PMA9_RA	4D	RW		8D			CD	
	0E		PMA10_RA	4E	RW		8E			CE	
	0F		PMA11_RA	4F	RW		8F			CF	
PRT4DM0	10	RW	PMA12_RA	50	RW		90			D0	
PRT4DM1	11	RW	PMA13_RA	51	RW		91			D1	
	12		PMA14_RA	52	RW		92			D2	
	13		PMA15_RA	53	RW		93			D3	
	14		EP1_CR0	54	#		94			D4	
	15		EP2_CR0	55	#		95			D5	
	16		EP3_CR0	56	#		96			D6	
	17		EP4_CR0	57	#		97			D7	
	18		EP5_CR0	58	#		98			D8	
	19		EP6_CRO	59	#		99			D9	
	1A		EP7_CR0	5A	#		9A			DA	
	1B		EP8_CR0	5B	#		9B			DB	
	1C			5C			9C		IO_CFG	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E			DE	
	1F			5F			9F			DF	
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
USB_CR1	30	#		70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
USBIO_CR2	33	RW		73			B3			F3	
PMA0_WA	34	RW		74			B4			F4	
PMA1_WA	35	RW		75			B5			F5	
PMA2_WA	36	RW		76			B6			F6	
PMA3_WA	37	RW		77			B7		CPU_F	F7	RL
PMA4_WA	38	RW		78			B8			F8	
PMA5_WA	39	RW		79			B9			F9	
PMA6_WA	3A	RW		7A			BA			FA	
PMA7_WA	3B	RW		7B			BB			FB	
PMA0_RA	3C	RW		7C			BC			FC	
PMA1_RA	3D	RW		7D			BD			FD	
PMA2_RA	3E	RW		7E			BE			FE	
PMA3_RA	3F	RW		7F			BF			FF	

Gray fields are reserved; do not access these fields. # Access is bit specific.

[+] Feedback

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe V USB devices. For the most up to date electrical specifications, verify that you have the most recent data sheet available by visiting the company web site at http://www.cypress.com

Figure 9. Voltage versus CPU Frequency

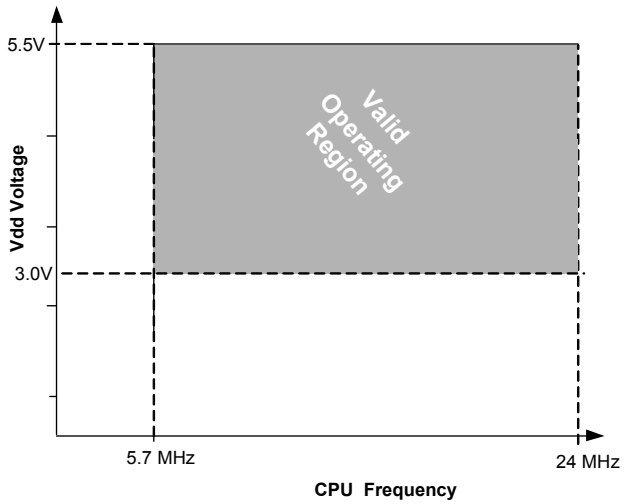
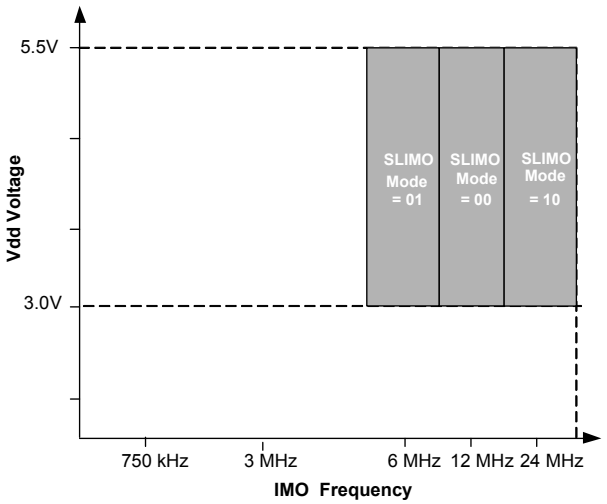


Figure 10. IMO Frequency Trim Options



The following table lists the units of measure that are used in this section.

Table 7. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

[+] Feedback

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 8. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage Temperature[3]	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
Vdd	Supply Voltage Relative to Vss		–0.5	–	+6.0	V
V_{IO}	DC Input Voltage		Vss – 0.5	–	Vdd + 0.5	V
V_{IOZ}	DC Voltage Applied to Tristate		Vss –0.5	–	Vdd + 0.5	V
I_{MIO}	Maximum Current into any Port Pin		–25	–	+50	mA
ESD	Electro Static Discharge Voltage	Human Body Model ESD	2000	–	–	V
LU	Latch up Current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 9. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{AI}	Ambient Industrial Temperature		–40	–	+85	°C
T_{AC}	Ambient Commercial Temperature		0		+70	°C
T_{JI}	Operational Industrial Die Temperature[4]	The temperature rise from ambient to junction is package specific. Refer the table "Thermal Impedances per Package" on page 29. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C
T_{JC}	Operational Commercial Die Temperature	The temperature rise from ambient to junction is package specific. Refer the table "Thermal Impedances per Package" on page 29. The user must limit the power consumption to comply with this requirement.	0		+85	°C

Notes

3. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrade reliability.
4. The temperature rise from ambient to junction is package specific. See Package Handling on page 29. The user must limit the power consumption to comply with this requirement.

[+] Feedback

DC Electrical Characteristics

DC Chip Level Specifications

Table 10 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 10.DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Vdd	Operating Voltage	No USB Activity.	3.0	–	5.5	V
$I_{DD24,3}$	Supply Current, CPU= 24 MHz	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 24 MHz, No USB/I2C/SPI.	–	2.9	4.0	mA
$I_{DD12,3}$	Supply Current, CPU= 12 MHz	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 12 MHz, No USB/I2C/SPI.	–	1.7	2.6	mA
$I_{DD6,3}$	Supply Current, CPU= 6 MHz	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 6 MHz, No USB/I2C/SPI.	–	1.2	1.8	mA
$I_{SB1,3}$	Standby Current with POR, LVD, and Sleep Timer	Vdd = 3.0V, T_A = 25°C, I/O regulator turned off.	–	1.1	1.5	µA
$I_{SB0,3}$	Deep Sleep Current	Vdd = 3.0V, T_A = 25°C, I/O regulator turned off.	–	0.1	–	µA
Vdd_{USB}	Operating Voltage	USB Activity	4.35	–	5.25	V
$I_{DD24,5}$	Supply Current, CPU= 24 MHz	Conditions are Vdd = 5.0V, T_A = 25°C, CPU = 24 MHz, IMO = 24 MHz USB Active, No I2C/SPI.	–	7.1	–	mA
$I_{DD12,5}$	Supply Current, CPU= 12 MHz	Conditions are Vdd = 5.0V, T_A = 25°C, CPU = 12 MHz, IMO = 24 MHz USB Active, No I2C/SPI.	–	6.2	–	mA
$I_{DD6,5}$	Supply Current, CPU= 6 MHz	Conditions are Vdd = 5.0V, T_A = 25°C, CPU = 6 MHz, IMO = 24 MHz USB Active, No I2C/SPI	–	5.8	–	mA
$I_{SB1,5}$	Standby Current with POR, LVD, and Sleep Timer	Vdd = 5.0V, T_A = 25°C, I/O regulator turned off.	–	1.1	–	µA
$I_{SB0,5}$	Deep Sleep Current	Vdd = 5.0V, T_A = 25°C, I/O regulator turned off.	–	0.1	–	µA

Table 11.DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ Pull Up Resistance	With idle bus	0.900	-	1.575	kΩ
Rusba	USB D+ Pull Up Resistance	While receiving traffic	1.425	-	3.090	kΩ
Vohusb	Static Output High		2.8	-	3.6	V
Volusb	Static Output Low			-	0.3	V
Vdi	Differential Input Sensitivity		0.2	-	–	V
Vcm	Differential Input Common Mode Range		0.8	-	2.5	V
Vse	Single Ended Receiver Threshold		0.8	-	2.0	V
Cin	Transceiver Capacitance			-	50	pF
Iio	High Z State Data Line Leakage	On D+ or D- line	-10	-	+10	µA
Rps2	PS/2 Pull Up Resistance		3	5	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

[+] Feedback

ADC Electrical Specifications

Table 12. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input Voltage Range		0		VREFADC	V
C_{IIN}	Input Capacitance				5	pF
R_{IN}	Input Resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF* Data Clock)	1/(400fF* Data Clock)	1/(300fF* Data Clock)	Ω
Reference						
V_{REFADC}	ADC Reference Voltage		1.14		1.26	V
Conversion Rate						
F_{CLK}	Data Clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25		6	MHz
S8	8-bit Sample Rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)		23.4375		ksps
S10	10-bit Sample Rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)		5.859		ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8		10	bits
DNL	Differential Nonlinearity		-1		+2	LSB
INL	Integral Nonlinearity		-2		+2	LSB
E_{Offset}	Offset Error	8-bit resolution	0	3.2	19.2	LSB
		10-bit resolution	0	12.8	76.8	LSB
E_{gain}	Gain Error	For any resolution	-5		+5	%FSR
Power						
I_{ADC}	Operating Current			2.1	2.6	mA
PSRR	Power Supply Rejection Ratio	PSRR (Vdd>3.0V)		24		dB
		PSRR (Vdd<3.0V)		30		dB

[+] Feedback

DC General Purpose IO Specifications

Table 13 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 5.5V and package specific temperature range. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 13. 3.0V and 5.5V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull Up Resistor		4	5.6	8	kΩ
V_{OH1}	High Output Voltage Port 2 or 3 Pins	IOH ≤ 10 µA, maximum of 10 mA source current in all I/Os.	Vdd - 0.2	–	–	V
V_{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 1 mA, maximum of 20 mA source current in all I/Os.	Vdd - 0.9	–	–	V
V_{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled	IOH < 10 µA, maximum of 10 mA source current in all I/Os.	Vdd - 0.2	–	–	V
V_{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled	IOH = 5 mA, maximum of 20 mA source current in all I/Os.	Vdd - 0.9	–	–	V
V_{OH5}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH < 10 µA, Vdd > 3.1V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.3	V
V_{OH6}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH = 5 mA, Vdd > 3.1V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH < 10 µA, Vdd > 3.0V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH = 2 mA, Vdd > 3.0V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH < 10 µA, Vdd > 3.0V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.1	V
V_{OH10}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH = 1 mA, Vdd > 3.0V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low Output Voltage	IOL = 25 mA, Vdd > 3.3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input Low Voltage		–	–	0.8	V
V_{IH}	Input High Voltage		2.0	–		V
V_H	Input Hysteresis Voltage		-	80	-	mV
I_{IL}	Input Leakage (Absolute Value)		–	0.001	1	µA
C_{PIN}	Pin Capacitance	Package and pin dependent. Temp = 25°C.	0.5	1.7	5	pF

[+] Feedback

DC POR and LVD Specifications

Table 14 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{PPOR}	Vdd Value for PPOR Trip[5] PORLEV[1:0] = 10b, HPOR = 1		-	2.82	2.95	V
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b		–	–	–	V
V_{LVD1}	VM[2:0] = 001b		–	–	–	V
V_{LVD2}	VM[2:0] = 010b		2.85	2.92	2.99	V
V_{LVD3}	VM[2:0] = 011b		2.95	3.02	3.09	V
V_{LVD4}	VM[2:0] = 100b		3.06	3.13	3.20	V
V_{LVD5}	VM[2:0] = 101b		–-	–	–	V
V_{LVD6}	VM[2:0] = 110b		–	–	–	V
V_{LVD7}	VM[2:0] = 111b		4.62	4.73	4.83	V

DC Programming Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations		1.71	–	5.25	V
I_{DDP}	Supply Current During Programming or Verify		–	5	25	mA
V_{ILP}	Input Low Voltage During Programming or Verify	See appropriate DC General Purpose IO Specifications table	–	–	V_{IL}	V
V_{IHP}	Input High Voltage During Programming or Verify		$0.65xVdd_{IWRITE}$	–	–	V
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify[6]		–	–	0.2	mA
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify[6]		–	–	1.5	mA
V_{OLP}	Output Low Voltage During Programming or Verify		–	–	Vss + 0.75	V
V_{OHP}	Output High Voltage During Programming or Verify		Vdd_{IWRITE} - 0.9V	–	Vdd_{IWRITE}	V
$Flash_{ENPB}$	Flash Write Endurance[7]		50,000	–	–	Cycles
$Flash_{DR}$	Flash Data Retention[8]		10	20	–	Years

Notes
5. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.
6. Driving internal pull down resistor.
7. Erase/write cycles per block.
8. Following maximum Flash write cycles at Tamb = 55C and Tj = 70C.

[+] Feedback

AC Electrical Characteristics

AC Chip Level Specifications

The following tables list guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	Processing Frequency[9]		5.7	–	25.2	MHz
F_{32K1}	Internal Low Speed Oscillator Frequency	Trimmed[10]	19	32	50	kHz
F_{32K_U}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency)		13	32	82	kHz
F_{32K2}	Internal Low Speed Oscillator Frequency	Untrimmed	13	32	82	kHz
F_{IMO24}	Internal Main Oscillator Stability for 24 MHz ± 5%(12)		22.8	24	25.2	MHz
F_{IMO12}	Internal Main Oscillator Stability for 12 MHz[10]		11.4	12	12.6	MHz
F_{IMO6}	Internal Main Oscillator Stability for 6 MHz[10]		5.7	6.0	6.3	MHz
DC_{IMO}	Duty Cycle of IMO		40	50	60	%
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle		40	50	60	%
SR_{POWER_UP}	Power Supply Slew Rate		–	–	250	V/ms
T_{XRST}	External Reset Pulse Width at Power Up	After supply voltage is valid	1	–	–	ms
T_{XRST2}	External Reset Pulse Width after Power Up[11]	Applies after part has booted	10	–	–	µs

Table 17.AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full speed data rate	Average bit rate	11.97	12	12.03	MHz
Tdjr1	Receiver data jitter tolerance	To next transition	-18.5	–	18.5	ns
Tdjr2	Receiver data jitter tolerance	To pair transition	-9	–	9	ns
Tudj1	Driver differential jitter	To next transition	-3.5	–	3.5	ns
Tudj2	Driver differential jitter	To pair transition	-4.0	–	4.0	ns
Tfdeop	Source jitter for differential transition	To SE0 transition	-2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–		ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns

Table 18.AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	–	20	ns
Tf	Transition fall time	50 pF	4	–	20	ns
TR	Rise/fall time matching		90.00	–	111.1	%
Vcrs	Output signal crossover voltage		1.3	–	2.0	V

Notes
9. Vdd = 3.0V and T_J = 85°C, CPU speed.
10. Trimmed for 3.3V operation using factory trim values.
11. The minimum required XRES pulse length is longer when programming the device (see Table 21 on page 24).

[+] Feedback

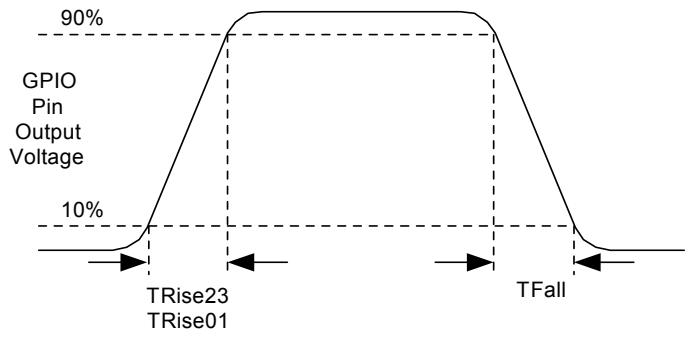
AC General Purpose I/O Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO Operating Frequency	Normal Strong Mode, Ports 0, 1	-	–	12	MHz
TRise23	Rise Time, Strong Mode Ports 2, 3	Vdd = 3.0 to 3.6V, 10% - 90%	15	–	80	ns
TRise01	Rise Time, Strong Mode Ports 0, 1	Vdd = 3.0 to 3.6V, 10% - 90%	10	–	50	ns
TFall	Fall Time, Strong Mode All Ports	Vdd = 3.0 to 3.6V, 10% - 90%	10	–	50	ns

Figure 11. GPIO Timing Diagram



AC External Clock Specifications

Table 20 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High Period		20.6	–	5300	ns
–	Low Period		20.6	–	–	ns
–	Power Up IMO to Switch		150	–	–	µs

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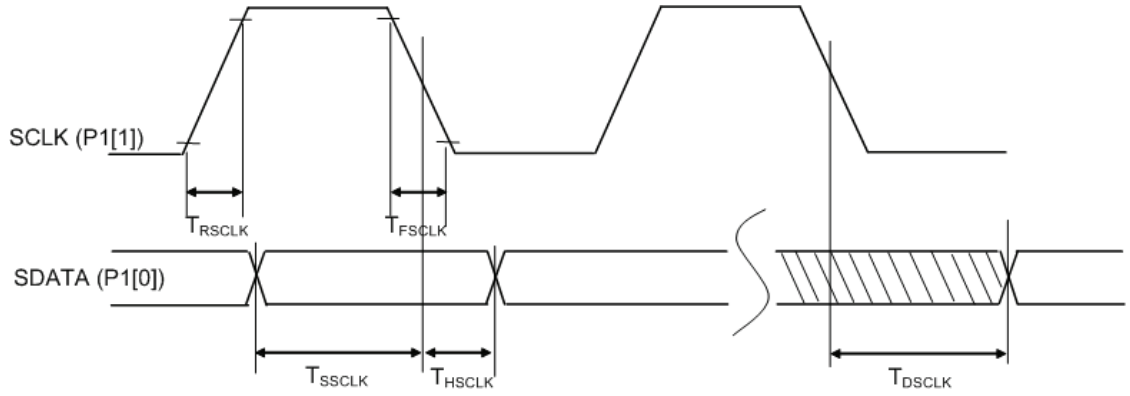
AC Programming Specifications

Table 21 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 21. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK		1	–	20	ns
T_{FSCLK}	Fall Time of SCLK		1	–	20	ns
T_{SSCLK}	Data Setup Time to Falling Edge of SCLK		40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)		–	–	18	ms
T_{WRITE}	Flash Block Write Time		–	–	25	ms
T_{DSCLK1}	Data Out Delay from Falling Edge of SCLK,	Vdd > 3.6V	–	–	60	ns
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	3.0V<Vdd<3.6V	–	–	85	ns
T_{XRST3}	External Reset Pulse Width after Power Up	Required to enter programming mode when coming out of sleep	263	–	–	µs

Figure 12. Timing Diagram - AC Programming Cycle



[+] Feedback

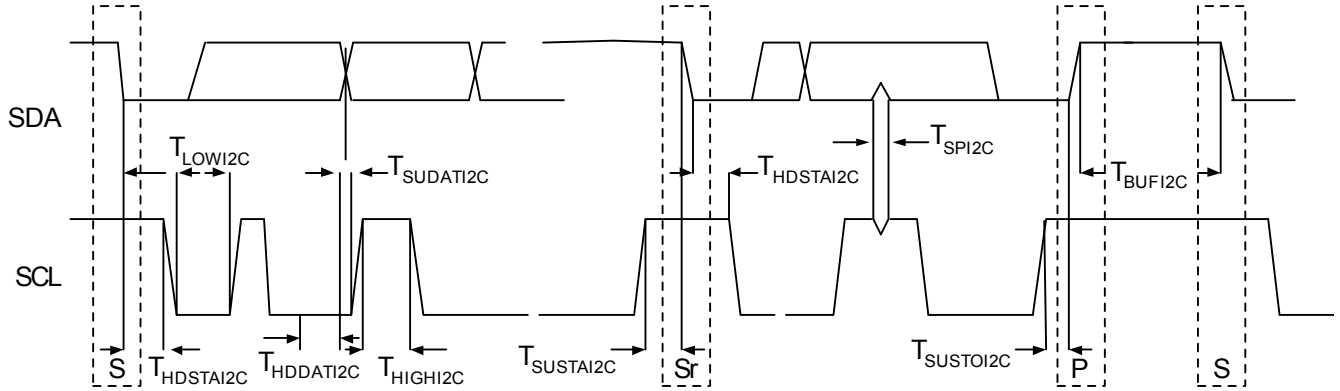
AC I²C Specifications

Table 22 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[12]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 13. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note
12. A Fast mode I2C bus device can be used in a standard mode I2C bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDAT} = 1000 + 250 = 1250$ ns (according to the standard mode I2C bus specification) before the SCL line is released.

[+] Feedback

Table 23. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	6	MHz
DC	SCLK duty cycle			50	–	%
T_{SETUP}	MISO to SCLK setup time		60	–	–	ns
T_{HOLD}	SCLK to MISO hold time		40	–	–	ns
T_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
T_{OUT_HIGH}	MOSI high time		40	–	–	ns

Table 24.SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		0.0469		12	MHz
T_{LOW}	SCLK low time		41.67			ns
T_{HIGH}	SCLK high time		41.67			ns
T_{SETUP}	MOSI to SCLK setup time		30			ns
T_{HOLD}	SCLK to MOSI hold time		50			ns
T_{SS_MISO}	SS high to MISO valid				153	ns
T_{SCLK_MISO}	SCLK to MISO valid				125	ns
T_{SS_HIGH}	SS high time				50	ns
T_{SS_CLK}	Time from SS low to first SCLK		2/SCLK			ns
T_{CLK_SS}	Time from last SCLK to SS high		2/SCLK			ns

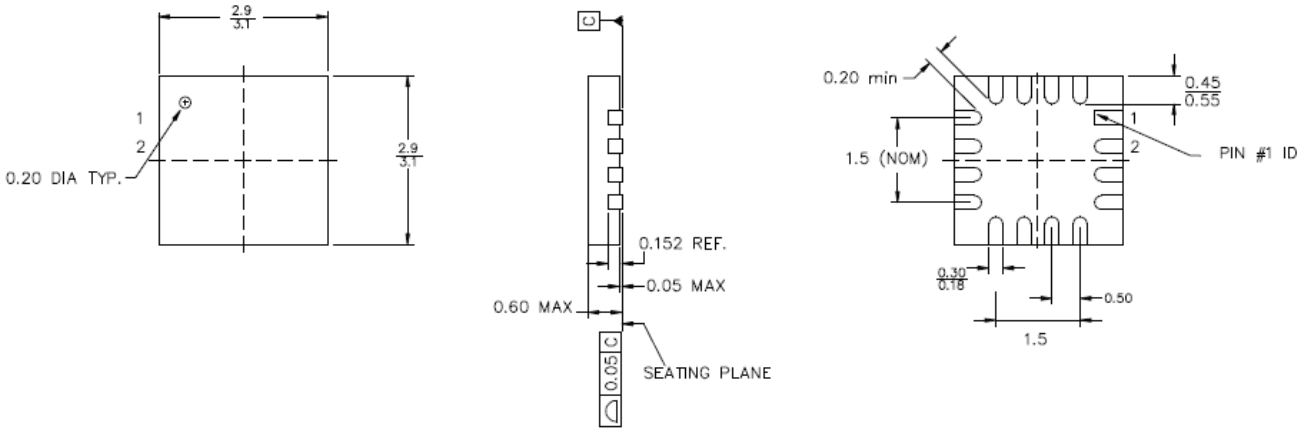
Package Diagram

This section illustrates the packaging specifications for the enCoRe V USB device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the enCoRe V emulation tools and their dimensions, refer to the development kit.

Packaging Dimensions

Figure 14. 16-Pin (3 x 3 mm) QFN (001-09116)



PART NO.	DESCRIPTION
LG16A	LEAD-FREE
LD16A	STANDARD

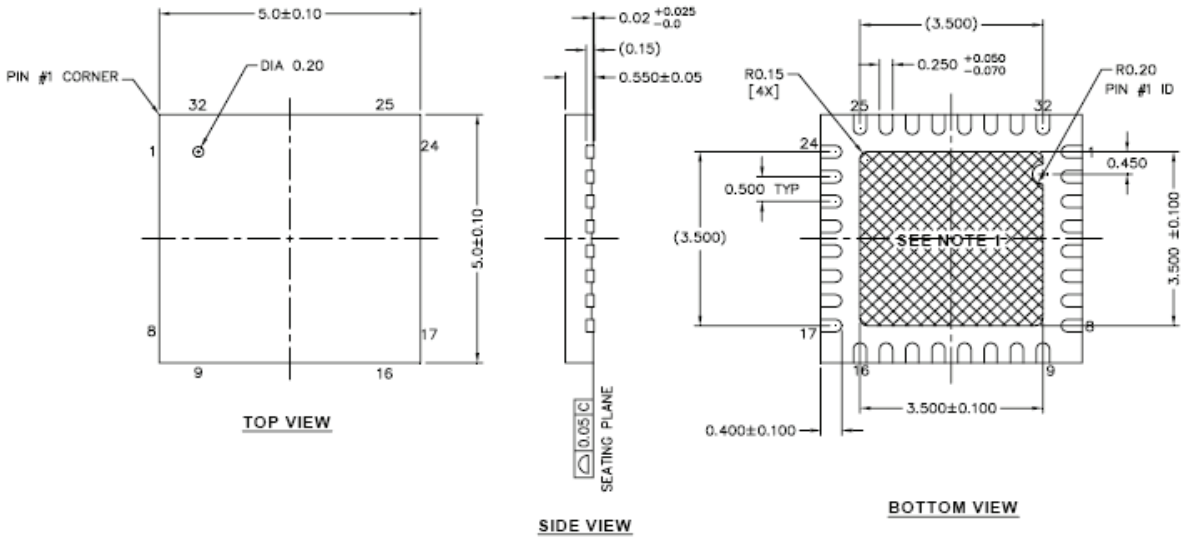
NOTES:

1. JEDEC # MO-220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN MAX

001-09116 *D

[+] Feedback

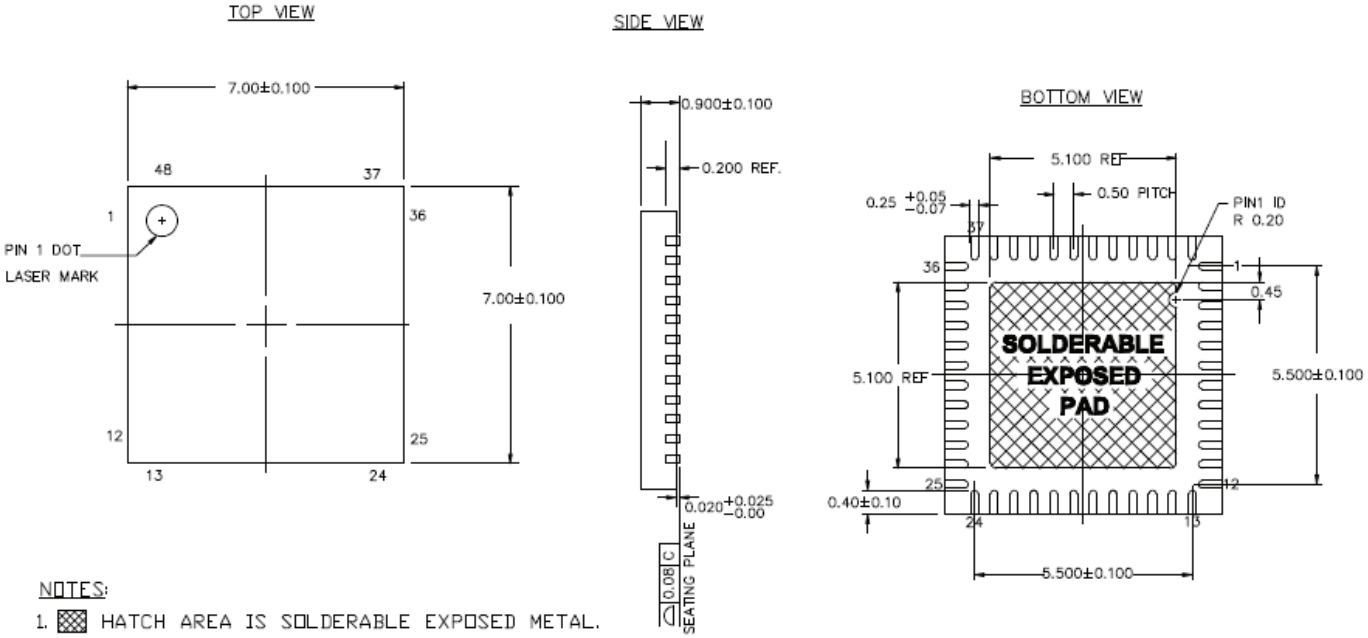
Figure 15. 32-Pin (5 x 5 x 0.55 mm) QFN (001-42168)



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *C

Figure 16. 48-Pin QFN (7 x 7x 0.90 mm) Sawn (001-13191)



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *D

[+] Feedback

Package Handling

Some IC packages require baking before they are soldered onto a PCB to remove moisture that may have been absorbed after leaving the factory. A label on the package has details about the actual bake temperature and the minimum bake time to remove this moisture. The maximum bake time is the aggregate time that the parts exposed to the bake temperature. Exceeding this exposure may degrade device reliability.

Table 25.Package Handling

Parameter	Description	Minimum	Typical	Maximum	Unit
TBAKETEMP	Bake Temperature		125	See package label	°C
TBAKETIME	Bake Time	See package label		72	hours

Thermal Impedances

Table 26. Thermal Impedances per Package

Package	Typical θ_{JA}[13]
16 QFN	32.69 °C/W
32 QFN[14]	19.51 °C/W
48 QFN[14]	17.68°C/W

Capacitance on Crystal Pins

Table 27. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32 QFN	3.2 pF
48 QFN	3.3 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 28.Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[15]	Maximum Peak Temperature
16 QFN	240°C	260°C
32 QFN	240°C	260°C
48 QFN	240°C	260°C

Notes
13. $T_J = T_A$ + Power x θ_{JA}.
14. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.
15. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

[+] Feedback

Ordering Information

Table 29.Ordering Code - Commercial Parts

Ordering Code	Package Information	Flash	SRAM	No. of GPIOs	Target Applications
CY7C64315-16LKXC	16-Pin QFN (3x3 mm)	16K	1K	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64315-16LKXCT	16-Pin QFN (Tape and Reel), (3x3 mm)	16K	1K	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64316-16LKXC	16-Pin QFN (3x3 mm)	32K	2K	11	Feature-rich Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64316-16LKXCT	16-Pin QFN (Tape and Reel), (3x3 mm)	32K	2K	11	Feature-rich Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64343-32LQXC	32-Pin QFN (5x5x0.55 mm)	8K	1K	25	Full-speed USB mouse, Various
CY7C64343-32LQXCT	32-Pin QFN (Tape and Reel), (5X5 mm)	8K	1K	25	Full-speed USB mouse, Various
CY7C64345-32LQXC	32-Pin QFN (5x5x mm)	16K	1K	25	Full-speed USB mouse, Various
CY7C64345-32LQXCT	32-Pin QFN (Tape and Reel), (5x5x mm)	16K	1K	25	Full-speed USB mouse, Various
CY7C64355-48LTXC	48-Pin QFN (7x7 mm)	16K	1K	36	Full-speed USB keyboard, Various
CY7C64355-48LTXCT	48-Pin QFN (Tape and Reel), (7x7 mm)	16K	1K	36	Full-speed USB keyboard, Various
CY7C64356-48LTXC	48-Pin QFN (7x7 mm)	32K	2K	36	Feature-rich Full-Speed USB keyboard, Various
CY7C64356-48LTXCT	48-Pin QFN (Tape and Reel), (7x7 mm)	32K	2K	36	Feature-rich Full-Speed USB keyboard, Various

Table 30.Ordering Code - Industrial Parts

Ordering Code	Package Information	Flash	SRAM	No. of GPIOs	Target Applications
CY7C64315-16LKXI	16-Pin QFN, Industrial (3x3 mm)	16K	1K	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64315-16LKXIT	16-Pin QFN, Industrial (Tape and Reel), (3x3 mm)	16K	1K	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64343-32LQXI	32-Pin QFN, Industrial (5x5x0.55 mm)	8K	1K	25	Full-speed USB mouse, Various
CY7C64343-32LQXIT	32-Pin QFN, Industrial (Tape and Reel), (5X5 mm)	8K	1K	25	Full-speed USB mouse, Various
CY7C64345-32LQXI	32-Pin QFN, Industrial (5x5x mm)	16K	1K	25	Full-speed USB mouse, Various
CY7C64345-32LQXIT	32-Pin QFN, Industrial (Tape and Reel), (5x5x mm)	16K	1K	25	Full-speed USB mouse, Various
CY7C64356-48LTXI	48-Pin QFN, Industrial (7x7 mm)	32K	2K	36	Feature-rich Full-Speed USB keyboard, Various
CY7C64356-48LTXIT	48-Pin QFN, Industrial (Tape and Reel), (7x7 mm)	32K	2K	36	Feature-rich Full-Speed USB keyboard, Various

[+] Feedback

Document History Page

Document Title: CY7C6431x, CY7C6434x, CY7C6435x enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	626256	TYJ	See ECN	New data sheet.
*A	735718	TYJ/ARI	See ECN	Filled in TBDs, added new block diagram, and corrected some values. Part numbers updated as per new specifications.
*B	1120404	ARI	See ECN	Corrected the block diagram and Figure 3, which is the 16-pin enCoRe V device. Corrected the description to pin 29 on Table 2, the Typ/Max values for I_{SB0} on the DC chip-level specifications, the current value for the latch-up current in the Electrical Characteristics section, and corrected the 16 QFN package information in the Thermal Impedance table. Corrected some of the bulleted items on the first page. Added DC Characteristics–USB Interface table. Added AC Characteristics–USB Data Timings table. Added AC Characteristics–USB Driver table. Corrected Flash Write Endurance minimum value in the DC Programming Specifications table. Corrected the Flash Erase Time max value and the Flash Block Write Time max value in the AC Programming Specifications table. Implemented new latest template. Include parameters: Vcrs, Rpu (USB, active), Rpu (USB suspend), Tfdeop, Tfeopr2, Tfeopt, Tfst. Added register map tables. Corrected a value in the DC Chip-Level Specifications table.
*C	1241024	TYJ/ARI	See ECN	Corrected Idd values in Table 6 - DC Chip-Level Specifications.
*D	1639963	AESA	See ECN	Post to www.cypress.com
*E	2138889	TYJ/PYRS	See ECN	Updated Ordering Code table: - Ordering code changed for 32-QFN package: From -32LKXC to -32LTXC - Added a new package type – “LTXC” for 48-QFN - Included Tape and Reel ordering code for 32-QFN and 48-QFN packages Changed active current values at 24, 12 and 6MHz in table “DC Chip-Level Specifications” - IDD24: 2.15 to 3.1mA - IDD12: 1.45 to 2.0mA - IDD6: 1.1 to 1.5mA Added information on using P1[0] and P1[1] as the I2C interface during POR or reset events
*F	2583853	TYJ/PYRS/ HMT	10/10/08	Converted from Preliminary to Final Added operating voltage ranges with USB ADC resolution changed from 10-bit to 8-bit Rephrased battery monitoring clause in page 1 to include “with external components” Included ADC specifications table Included Voh7, Voh8, Voh9, Voh10 specs Flash data retention – condition added to Note [11] Input leakage spec changed to 25 nA max Under AC Char, Frequency accuracy of ILO corrected GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated Spec change for 32-QFN package Input Leakage Current maximum value changed to 1 μA Updated V_{OHV} parameter in Table 13 Updated thermal impedances for the packages Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs.

[+] Feedback

Document Title: CY7C6431x, CY7C6434x, CY7C6435x enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
*G	2653717	DVJA/PYRS	02/04/09	Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections with edits. Removed 'GUI - graphical user interface' from Document Conventions acronym table. Removed 'O - Only a read/write register or bits' in Table 4 Edited Table 8: removed 10-bit resolution information and corrected units column. Added package handling section Added 8K part 'CY7C64343-32LQXC' to Ordering Information.
*H	2714694	DVJA/AESA	06/04/2009	Updated Block Diagram. Added Full Speed USB, 10-bit ADC, SPI, and I2C Slave sections. ADC Resolution changed from 8-bit to 10-bit Updated Table 9 DC Chip Level Specs Updated Table10 DC Char - USB Interface Updated Table 12 DC POR and LDV Specs Changed operating temperature from Commercial to Industrial Changed Temperature Range to Industrial: -40 to 85°C Figure 9: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz Table 14: Removed "Maximum" from the F_{CPU} description Ordering Information: Replaced 'C' with 'I' in all part numbers to denote Industrial Temp Range
*I	2764460	DVJA/AESA	09/16/2009	Changed Table 12: ADC Specs Added F_{32K2} (Untrimmed) spec to Table 16: AC Chip level Specs Changed T_{RAMP} spec to SR_{POWER_UP} in Table 16: AC Chip Level Specs Added Table 27: Typical Package Capacitance on Crystal Pins

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Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331