

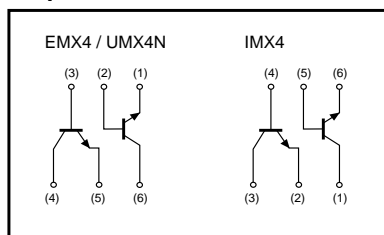
High transition frequency (dual transistors)

EMX4 / UMX4N / IMX4

●Features

- 1) Two 2SC3837K chips in a EMT or UMT or SMT package.
- 2) High transition frequency. ($f_T=1.5\text{GHz}$)
- 3) Low output capacitance. ($C_{ob}=0.9\text{pF}$)

●Equivalent circuits



●Absolute maximum ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	30	V
Collector-emitter voltage	V_{CEO}	20	V
Emitter-base voltage	V_{EBO}	3	V
Collector current	I_C	50	mA
Collector power dissipation	EMX4 / UMX4N	P_C 150(TOTAL)	mW *1
	IMX4	300(TOTAL)	
Junction temperature	T_J	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

*1 120mW per element must not be exceeded.
*2 200mW per element must not be exceeded.

●Package, marking, and packaging specifications

Type	EMX4	UMX4N	IMX4
Package	EMT6	UMT6	SMT6
Marking	X4	X4	X4
Code	T2R	TR	T108
Basic ordering unit (pieces)	8000	3000	3000

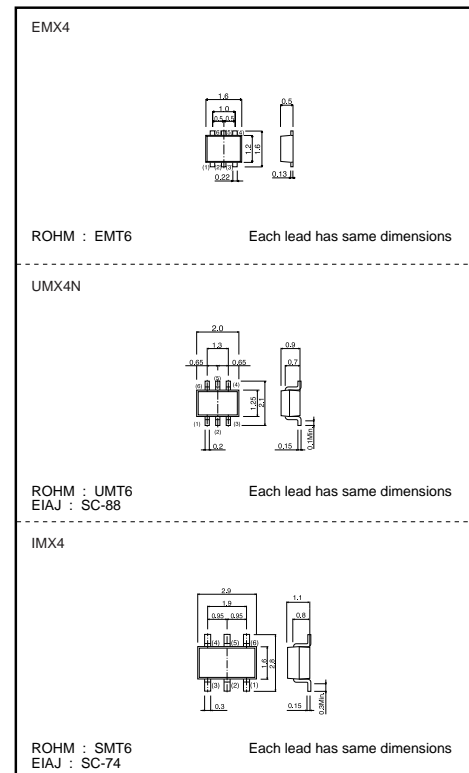
●Electrical characteristics ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	30	-	-	V	$I_C=10\mu\text{A}$
Collector-emitter breakdown voltage	BV_{CEO}	20	-	-	V	$I_C=1\text{mA}$
Emitter-base breakdown voltage	BV_{EBO}	3	-	-	V	$I_E=10\mu\text{A}$
Collector cutoff current	I_{CBO}	-	-	0.5	μA	$V_{CB}=15\text{V}$
Emitter cutoff current	I_{EBO}	-	-	0.5	μA	$V_{EB}=2\text{V}$
DC current transfer ratio	h_{FE}	56	-	180	-	$V_{CE}/I_C=10\text{V}/10\text{mA}$
Collector-emitter saturation voltage	$V_{CE(sat)}$	-	-	0.5	V	$I_C/I_E=20\text{mA}/4\text{mA}$
Transition frequency	f_T	600	1500	-	MHz	$V_{CE}/I_E=10\text{V}/-10\text{mA}$, $f=200\text{MHz}$ *
Output capacitance	C_{ob}	-	0.95	1.6	pF	$V_{CE}/f=10\text{V}/1\text{MHz}$, $I_E=0\text{A}$
Collector-base time constant	$\tau_{bb} \cdot C_c$	-	6	13	ps	$V_{CB}=10\text{V}$, $I_C=10\text{mA}$, $f=31.8\text{MHz}$
Noise factor	NF	-	4.5	-	dB	$V_{CE}=12\text{V}$, $I_C=2\text{mA}$, $f=200\text{MHz}$, $R_g=50\Omega$

*Transition frequency of the device.

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

●Dimensions (Unit : mm)



Transistors

●Electrical characteristic curves

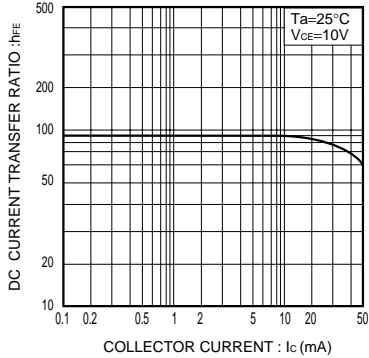


Fig.1 DC current gain vs. collector current

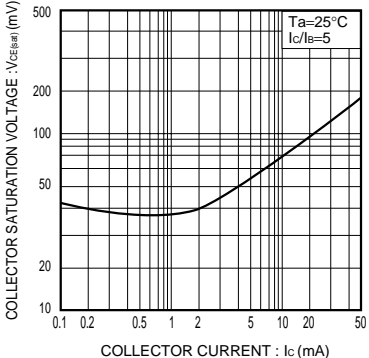


Fig.2 Collector-emitter saturation voltage vs. collector current

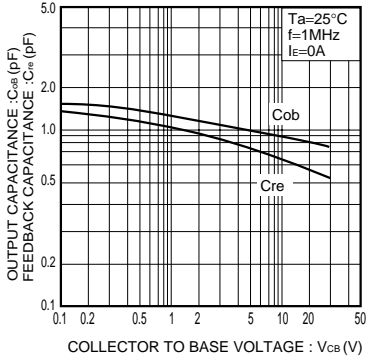


Fig.3 Capacitance vs. reverse bias voltage

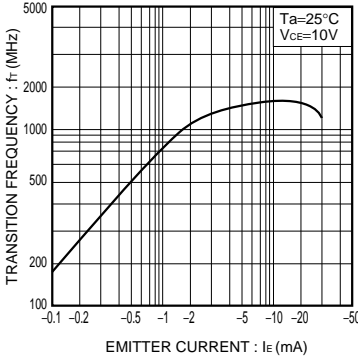


Fig.4 Gain bandwidth product vs. emitter current

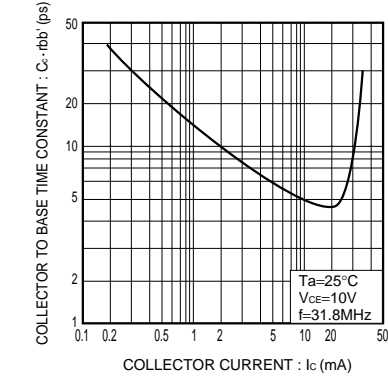


Fig.5 Collector to base time constant vs. collector current

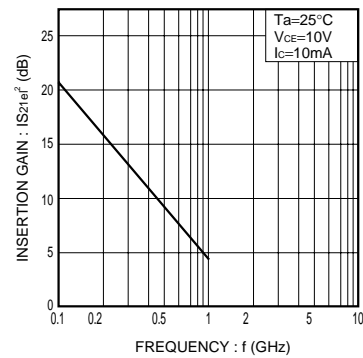


Fig.6 Insertion gain vs. frequency

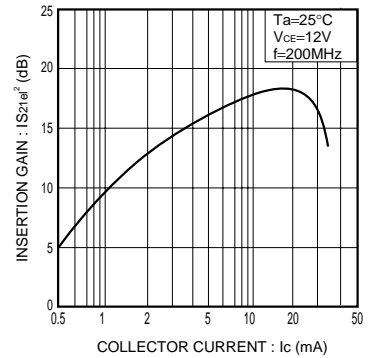


Fig.7 Insertion gain vs. collector current

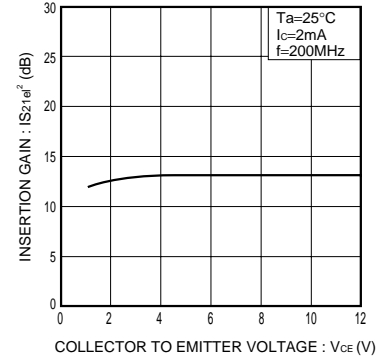


Fig.8 Insertion gain vs. collector voltage

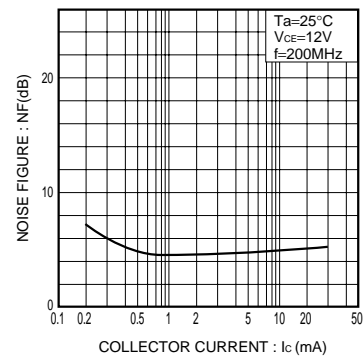


Fig.9 Noise factor vs. collector current

Transistors

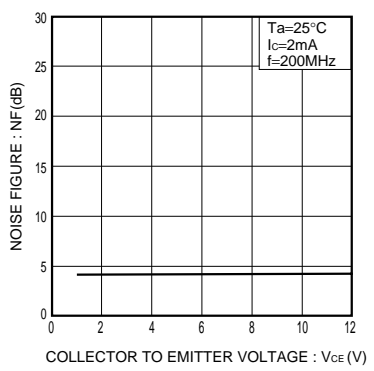


Fig.10 Noise factor vs. collector voltage

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