# 74HC574-Q100; 74HCT574-Q100

## Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 1 — 2 August 2012 Product data sheet

## 1. General description

The 74HC574-Q100; 74HCT574-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL. It is specified in compliance with JEDEC standard no. 7A.

The 74HC574-Q100; 74HCT574-Q100 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops. The 8 flip-flops store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When $\overline{OE}$ is LOW the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- 3-state non-inverting outputs for bus-oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74HC574D-Q100 | −40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74HCT574D-Q100 | | | | |
| 74HC574PW-Q100 | −40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74HCT574PW-Q100 | | | | |

## 4. Functional diagram

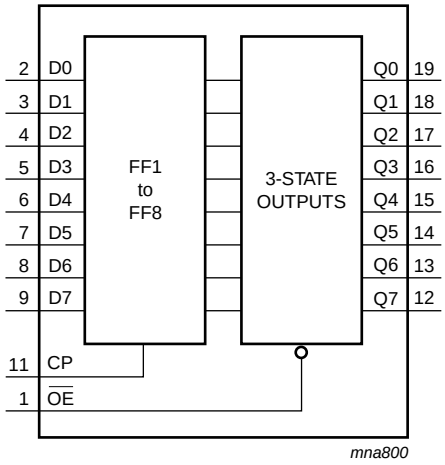



**Fig 1. Functional diagram**

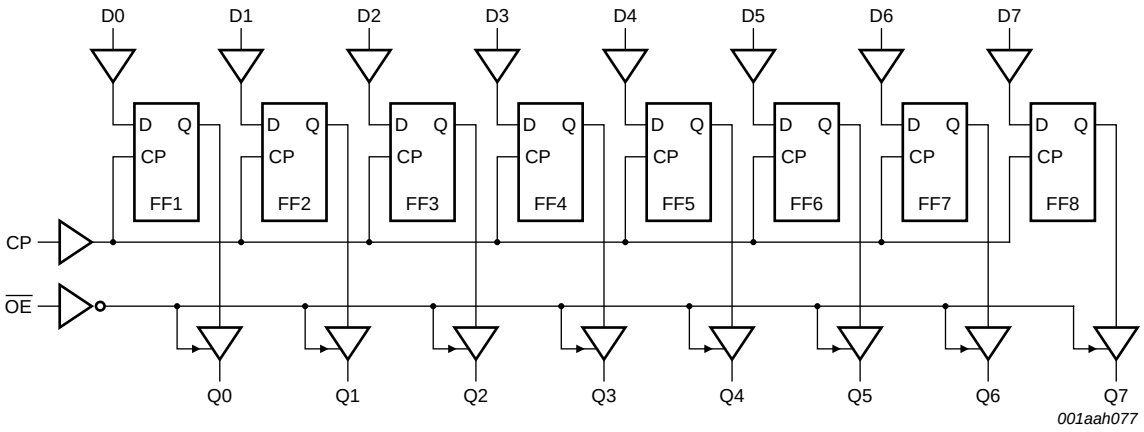



**Fig 2. Logic diagram**


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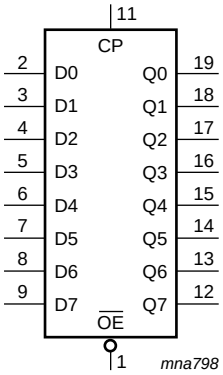



Fig 3. Logic symbol

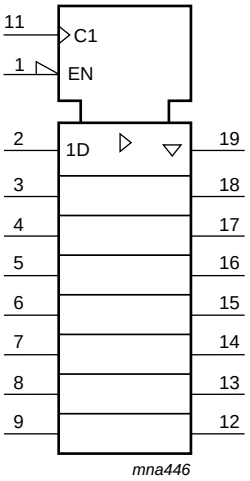



Fig 4. IEC logic symbol

# 5. Pinning information

## 5.1 Pinning

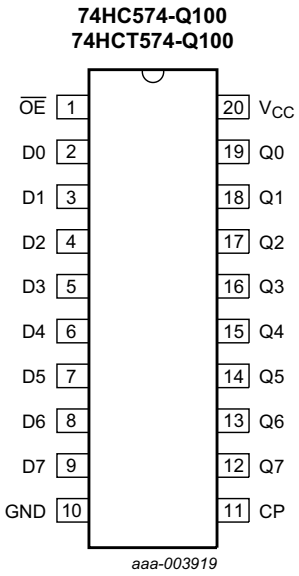



Fig 5. Pin configuration SO20

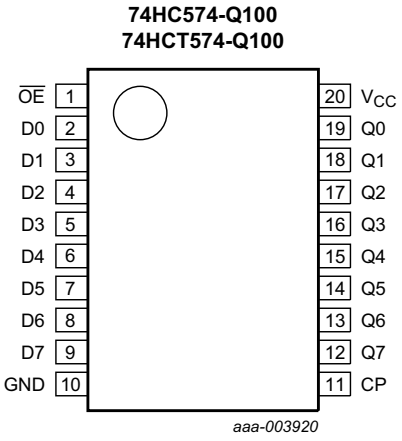



Fig 6. Pin configuration TSSOP20


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### 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{OE}$ | 1 | 3-state output enable input (active LOW) |
| D[0:7] | 2, 3, 4, 5, 6, 7, 8, 9 | data input |
| GND | 10 | ground (0 V) |
| CP | 11 | clock input (LOW-to-HIGH, edge triggered) |
| Q[0:7] | 19, 18, 17, 16, 15, 14, 13, 12 | 3-state flip-flop output |
| $V_{CC}$ | 20 | supply voltage |

## 6. Functional description

**Table 3. Function table[1]**

| Operating mode | Input | | | Internal flip-flop | Output |
|---|---|---|---|---|---|
| | $\overline{OE}$ | CP | Dn | | Qn |
| Load and read register | L | ↑ | l | L | L |
| | L | ↑ | h | H | H |
| Load register and disable output | H | ↑ | l | L | Z |
| | H | ↑ | h | H | Z |

[1] H = HIGH voltage level;
h = HIGH voltage level one setup time prior to the HIGH-to-LOW CP transition;
L = LOW voltage level;
l = LOW voltage level one setup time prior to the HIGH-to-LOW CP transition;
Z = high-impedance OFF-state;
↑ = LOW-to-HIGH clock transition.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +7 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | | - | ±20 | mA |
| $I_O$ | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5$ V) | | - | ±35 | mA |
| $I_{CC}$ | supply current | | | - | +70 | mA |
| $I_{GND}$ | ground current | | | - | −70 | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | | [1] | - | 500 | mW |

[1] For SO20 packages: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.
For TSSOP20 packages: $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.


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## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V)*

| Symbol | Parameter | Conditions | 74HC574-Q100 | | | 74HCT574-Q100 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | $V_{CC}$ = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | $V_{CC}$ = 6.0 V | - | - | 83 | - | - | - | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74HC574-Q100** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | $V_{CC}$ = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | $V_{CC}$ = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = –20 μA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = –20 μA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –20 μA; $V_{CC}$ = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | $I_O$ = –6.0 mA; $V_{CC}$ = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | $I_O$ = –7.8 mA; $V_{CC}$ = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 20 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 μA; $V_{CC}$ = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 6.0 mA; $V_{CC}$ = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O$ = 7.8 mA; $V_{CC}$ = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = $V_{CC}$ or GND; $V_{CC}$ = 6.0 V | - | - | ±0.5 | - | ±5.0 | - | ±10.0 | μA |


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**Table 6. Static characteristics** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V | - | - | 8.0 | - | 80 | - | 160 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | | | | | pF |
| **74HCT574-Q100** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC} = 4.5$ V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC} = 4.5$ V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC} = 4.5$ V | | | | | | | | |
| | | $I_O = -20$ μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O = -6$ mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC} = 4.5$ V | | | | | | | | |
| | | $I_O = 20$ μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 6.0$ mA | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O = 0$ A | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V | - | - | 8.0 | - | 80 | - | 160 | μA |
| $\Delta I_{CC}$ | additional supply current | $V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A | | | | | | | | |
| | | per input pin; Dn inputs | - | 50 | 180 | - | 225 | - | 245 | μA |
| | | per input pin; $\overline{OE}$ input | - | 125 | 450 | - | 563 | - | 613 | μA |
| | | per input pin; CP input | - | 150 | 540 | - | 675 | - | 735 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | | | | | pF |


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## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); $C_L$ = 50 pF unless otherwise specified; for test circuit see Figure 10.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| **For type 74HC574-Q100** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | CP to Qn; see Figure 7 | [1] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | - | 47 | 150 | - | 190 | - | 225 | ns |
| | | $V_{CC}$ = 4.5 V | | - | 17 | 30 | - | 35 | - | 45 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | | - | 14 | - | - | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | | - | 14 | 26 | - | 33 | - | 38 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to Qn; see Figure 9 | [2] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | - | 44 | 140 | - | 175 | - | 210 | ns |
| | | $V_{CC}$ = 4.5 V | | - | 16 | 28 | - | 35 | - | 42 | ns |
| | | $V_{CC}$ = 6.0 V | | - | 13 | 24 | - | 30 | - | 36 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to Qn; see Figure 9 | [3] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | - | 39 | 125 | - | 155 | - | 190 | ns |
| | | $V_{CC}$ = 4.5 V | | - | 14 | 25 | - | 31 | - | 38 | ns |
| | | $V_{CC}$ = 6.0 V | | - | 11 | 21 | - | 26 | - | 32 | ns |
| $t_t$ | transition time | Qn; see Figure 7 | [4] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | - | 14 | 60 | - | 75 | - | 90 | ns |
| | | $V_{CC}$ = 4.5 V | | - | 5 | 12 | - | 15 | - | 18 | ns |
| | | $V_{CC}$ = 6.0 V | | - | 4 | 10 | - | 13 | - | 15 | ns |
| $t_W$ | pulse width | CP HIGH or LOW; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 80 | 14 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V | | 16 | 5 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V | | 14 | 4 | - | 17 | - | 20 | - | ns |
| $t_{su}$ | set-up time | Dn to CP; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 60 | 6 | - | 75 | - | 90 | - | ns |
| | | $V_{CC}$ = 4.5 V | | 12 | 2 | - | 15 | - | 18 | - | ns |
| | | $V_{CC}$ = 6.0 V | | 10 | 2 | - | 13 | - | 15 | - | ns |
| $t_h$ | hold time | Dn to CP; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 5 | 0 | - | 5 | - | 5 | - | ns |
| | | $V_{CC}$ = 4.5 V | | 5 | 0 | - | 5 | - | 5 | - | ns |
| | | $V_{CC}$ = 6.0 V | | 5 | 0 | - | 5 | - | 5 | - | ns |
| $f_{max}$ | maximum frequency | CP; see Figure 7 | | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 6.0 | 37 | - | 4.8 | - | 4.0 | - | MHz |
| | | $V_{CC}$ = 4.5 V | | 30 | 112 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | | - | 123 | - | - | - | - | - | MHz |
| | | $V_{CC}$ = 6.0 V | | 35 | 133 | - | 28 | - | 24 | - | MHz |


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**Table 7. Dynamic characteristics** *...continued*

*Voltages are referenced to GND (ground = 0 V); $C_L$ = 50 pF unless otherwise specified; for test circuit see Figure 10.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $C_{PD}$ | power dissipation capacitance | $C_L$ = 50 pF; f = 1 MHz; $V_I$ = GND to $V_{CC}$ | [5] | - | 22 | - | - | - | - | - | pF |
| **For type 74HCT574-Q100** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | CP to Qn; see Figure 7 | [1] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | | - | 18 | 33 | - | 41 | - | 50 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | | - | 15 | - | - | - | - | - | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to Qn; see Figure 9 | [2] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | | - | 19 | 33 | - | 41 | - | 50 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to Qn; see Figure 9 | [3] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | | - | 16 | 28 | - | 35 | - | 42 | ns |
| $t_t$ | transition time | Qn; see Figure 7 | [4] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | | - | 5 | 12 | - | 15 | - | 18 | ns |
| $t_W$ | pulse width | CP HIGH or LOW; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 16 | 7 | - | 20 | - | 24 | - | ns |
| $t_{su}$ | set-up time | Dn to CP; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 12 | 3 | - | 15 | - | 18 | - | ns |
| $t_h$ | hold time | Dn to CP; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 5 | –1 | - | 5 | - | 5 | - | ns |
| $f_{max}$ | maximum frequency | CP; see Figure 7 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 30 | 69 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | | - | 76 | - | - | - | - | - | MHz |
| $C_{PD}$ | power dissipation capacitance | $C_L$ = 50 pF; f = 1 MHz; $V_I$ = GND to $V_{CC}$ | [5] | - | 25 | - | - | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[2] $t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$.

[3] $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

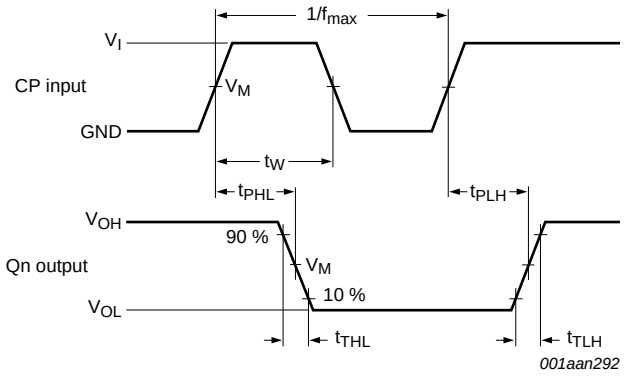
[4] $t_t$ is the same as $t_{THL}$ and $t_{TLH}$.

[5] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.


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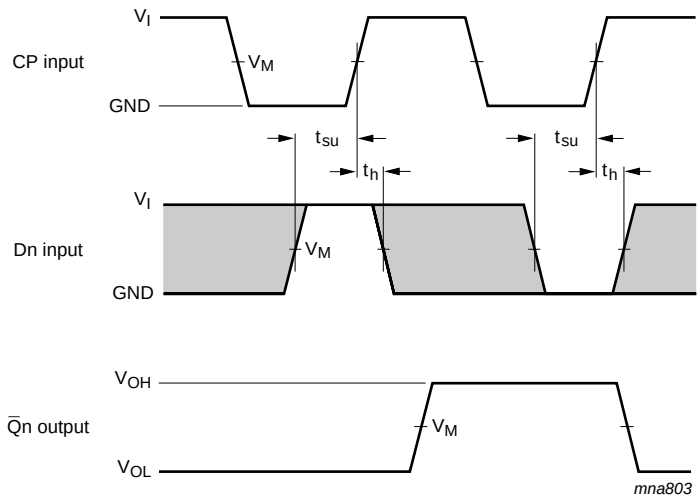
## 11. Waveforms




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 7. Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)**



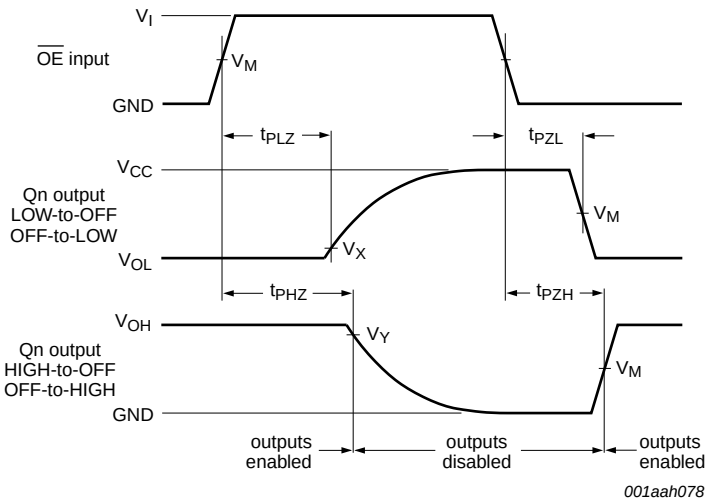

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 8. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times**


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Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

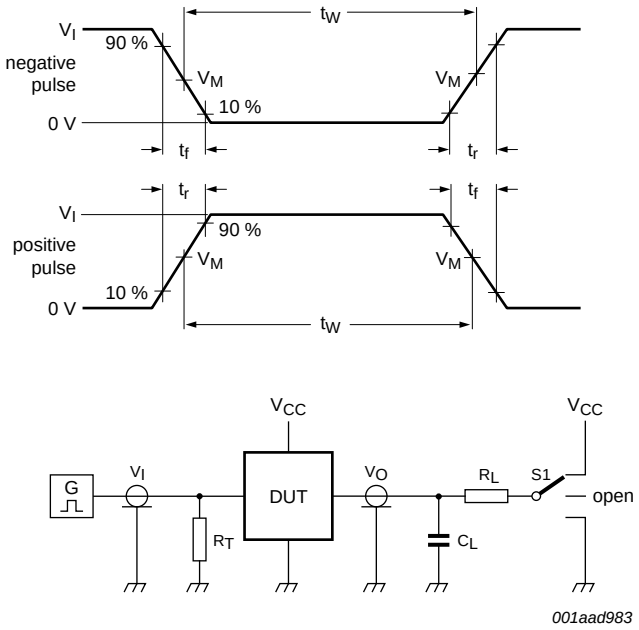
**Fig 9. Enable and disable times**

**Table 8. Measurement points**

| Type | Input | Output | | |
|---|---|---|---|---|
| | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 74HC574-Q100 | $0.5V_{CC}$ | $0.5V_{CC}$ | $0.1V_{CC}$ | $0.9V_{CC}$ |
| 74HCT574-Q100 | 1.3 V | 1.3 V | $0.1V_{CC}$ | $0.9V_{CC}$ |


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Test data is given in Table 9.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistance.

S1 = Test selection switch.

**Fig 10. Test circuit for measuring switching times**

**Table 9. Test data**

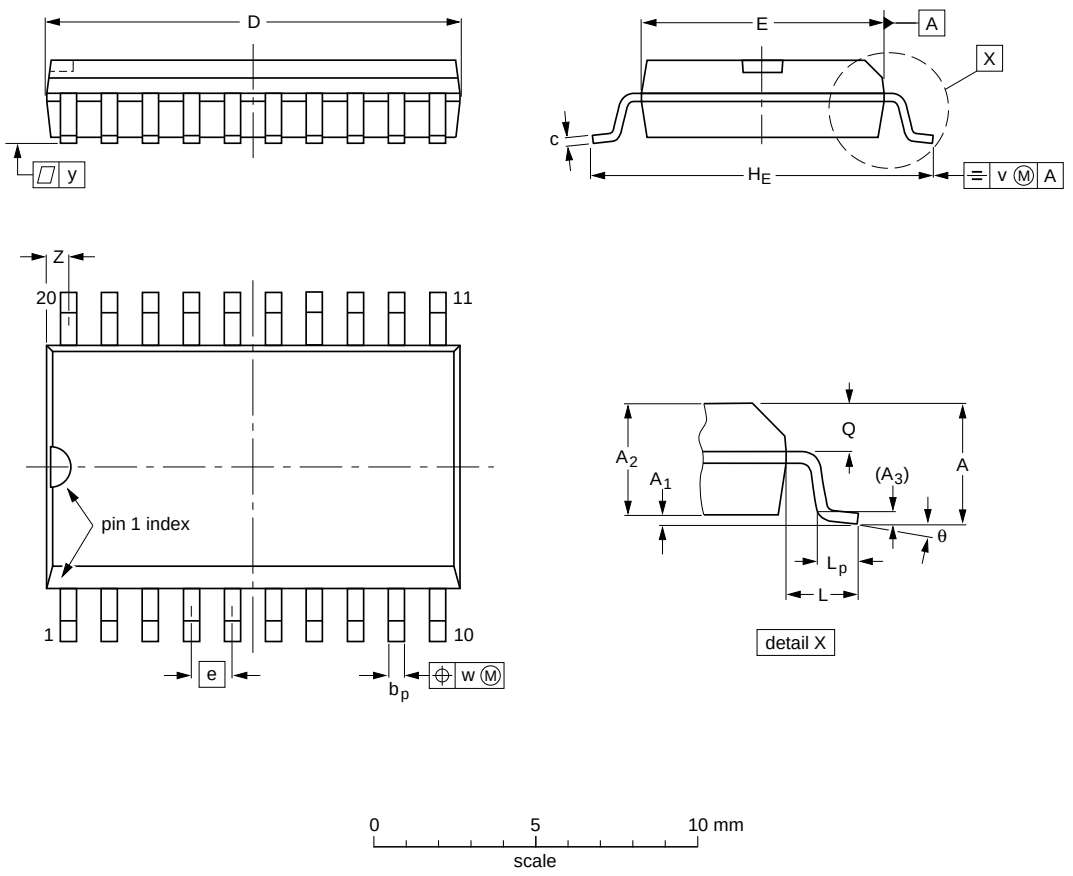
| Type | Input | | Load | | S1 position | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 74HC574-Q100 | $V_{CC}$ | 6 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |
| 74HCT574-Q100 | 3 V | 6 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |


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## 12. Package outline

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

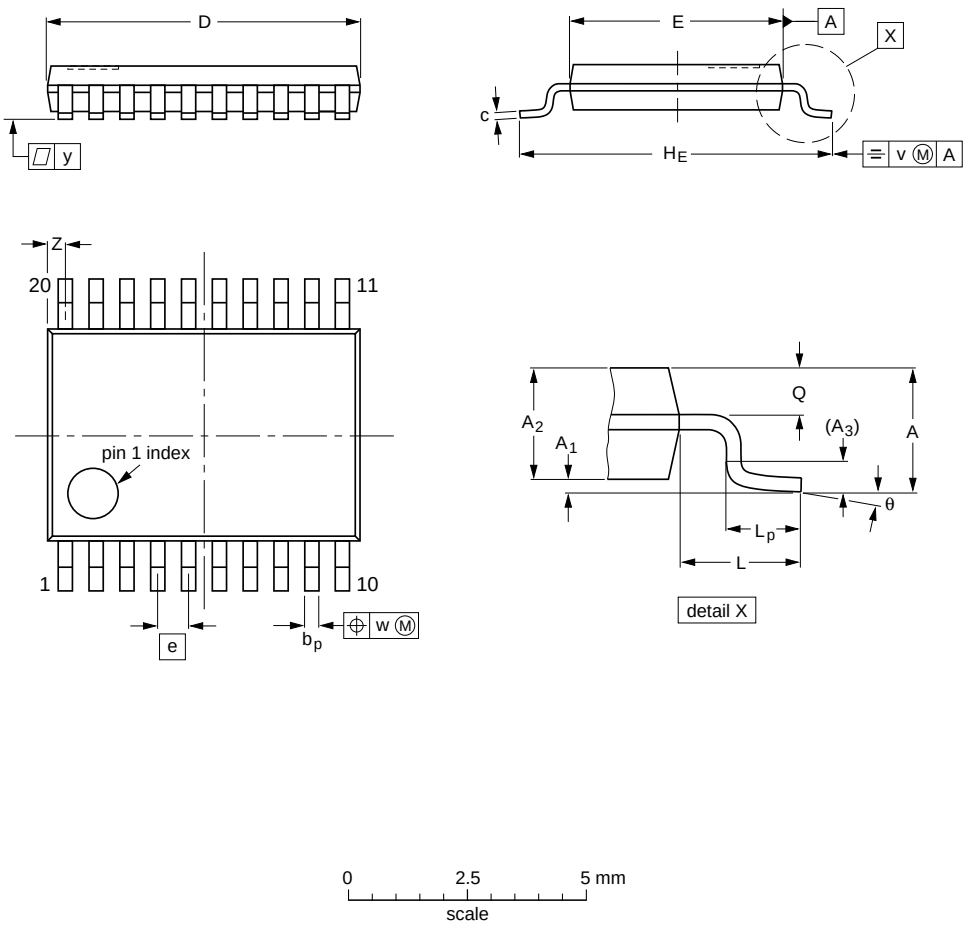
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 11. Package outline SOT163-1 (SO20)**


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**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT360-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 12. Package outline SOT360-1 (TSSOP20)**


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## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |
| MIL | Military |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74HC_HCT574_Q100 v.1 | 20120802 | Product data sheet | - | - |


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# 15. Legal information

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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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