



ALPHA & OMEGA
SEMICONDUCTOR



AO4612

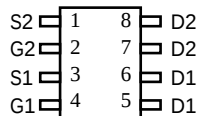
Complementary Enhancement Mode Field Effect Transistor

General Description

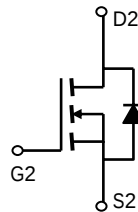
The AO4612 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications. *Standard product AO4612 is Pb-free (meets ROHS & Sony 259 specifications). AO4612L is a Green Product ordering option. AO4612 and AO4612L are electrically identical.*

Features

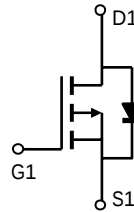
n-channel	p-channel
V_{DS} (V) = 60V	-60V
I_D = 4.5A (V_{GS} =10V)	-3.2A (V_{GS} = -10V)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 56m Ω (V_{GS} =10V)	< 105m Ω (V_{GS} = -10V)
< 77m Ω (V_{GS} =4.5V)	< 135m Ω (V_{GS} = -4.5V)



SOIC-8



n-channel



p-channel

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^A	I_D	4.5	-3.2	A
		3.6	-2.6	
Pulsed Drain Current ^B	I_{DM}	20	-20	
Power Dissipation	P_D	2	2	W
		1.28	1.28	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ\text{C}$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		n-ch	74	110	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	n-ch	35	60	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		p-ch	74	110	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	p-ch	35	40	$^\circ\text{C/W}$

N Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=48\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	2.1	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=4.5\text{A}$ $T_J=125^\circ\text{C}$		46 79	56	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=3\text{A}$		64	77	
						m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=4.5\text{A}$		11		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.74	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=30\text{V}$, $f=1\text{MHz}$		450	540	pF
C_{oss}	Output Capacitance			60		pF
C_{rss}	Reverse Transfer Capacitance			25		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		1.65	2	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$, $I_D=4.5\text{A}$		8.5	10.5	nC
$Q_g(4.5\text{V})$	Total Gate Charge			4.3	5.5	nC
Q_{gs}	Gate Source Charge			1.6		nC
Q_{gd}	Gate Drain Charge			2.2		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$, $R_L=6.7\Omega$, $R_{GEN}=3\Omega$		4.7	7	ns
t_r	Turn-On Rise Time			2.3	4.5	ns
$t_{D(off)}$	Turn-Off DelayTime			15.7	24	ns
t_f	Turn-Off Fall Time			1.9	4	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=4.5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		27.5	35	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=4.5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		32		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

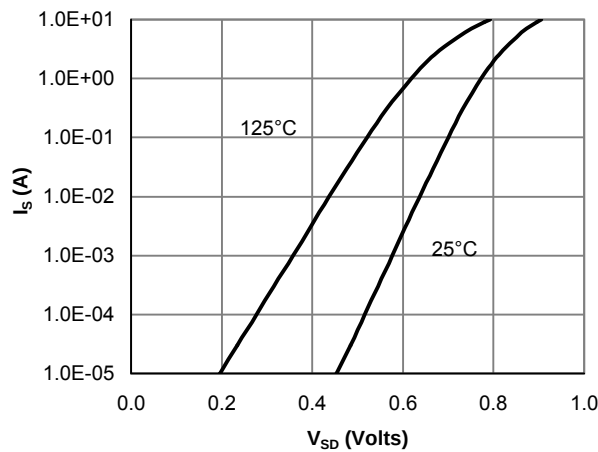
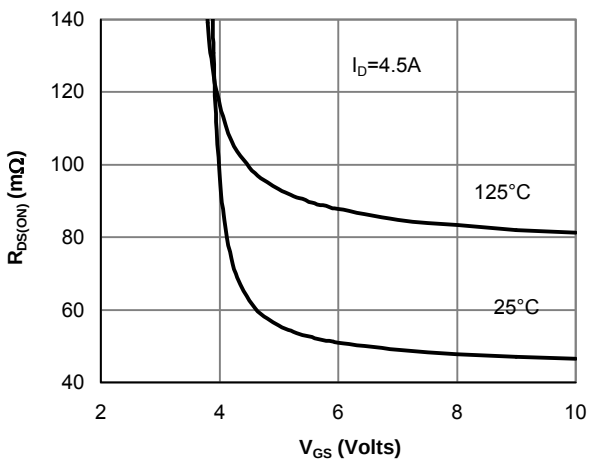
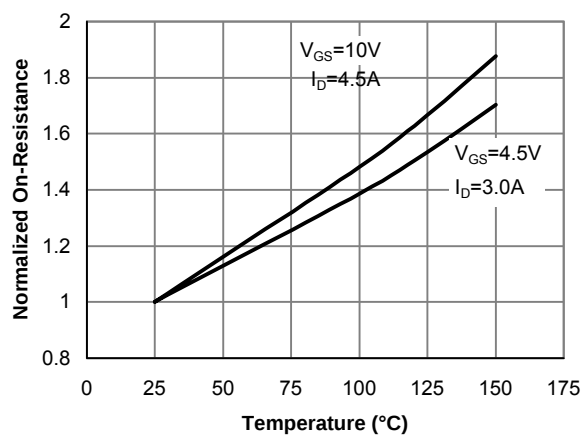
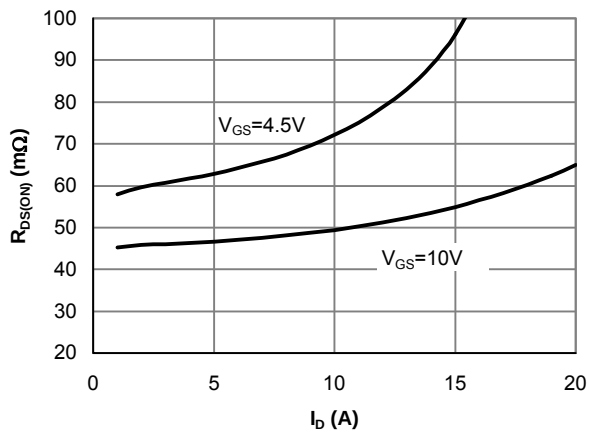
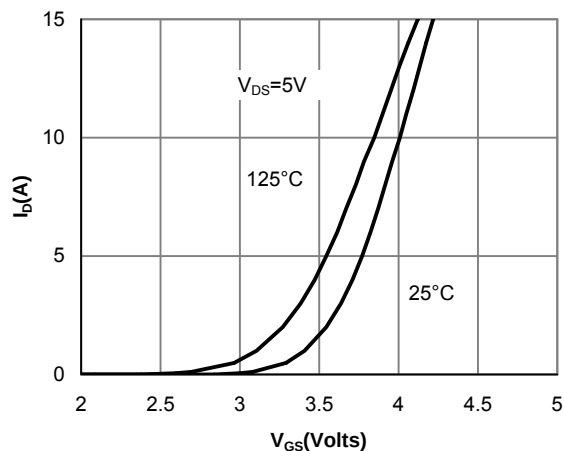
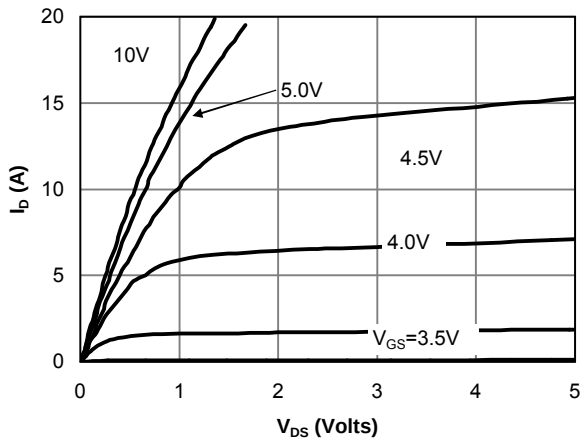
D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

Rev2: August 2005

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL



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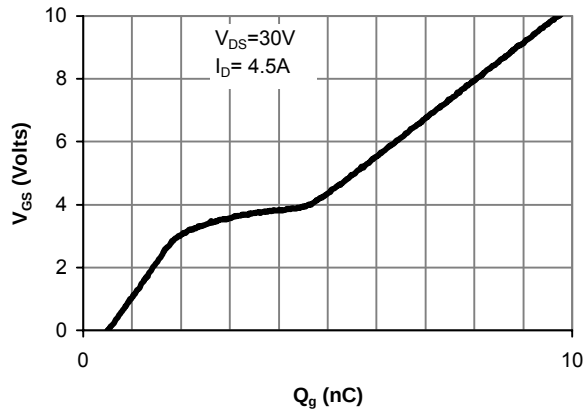


Figure 7: Gate-Charge Characteristics

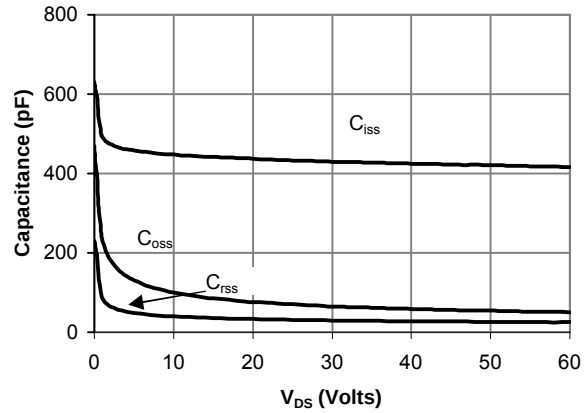


Figure 8: Capacitance Characteristics

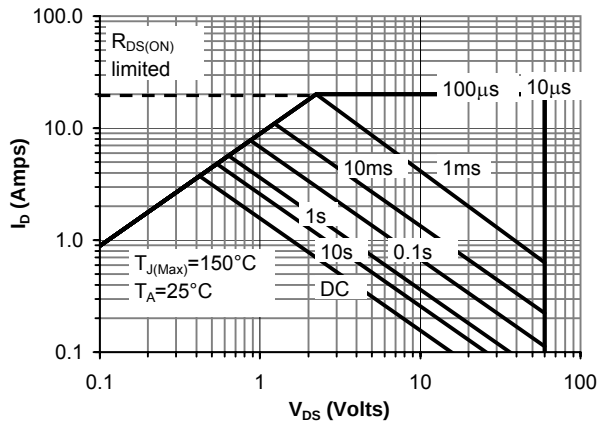


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

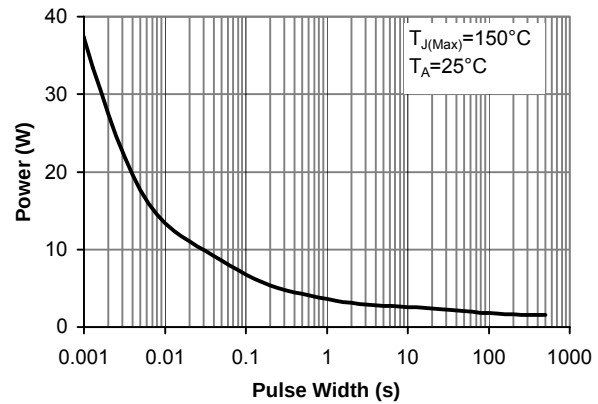


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

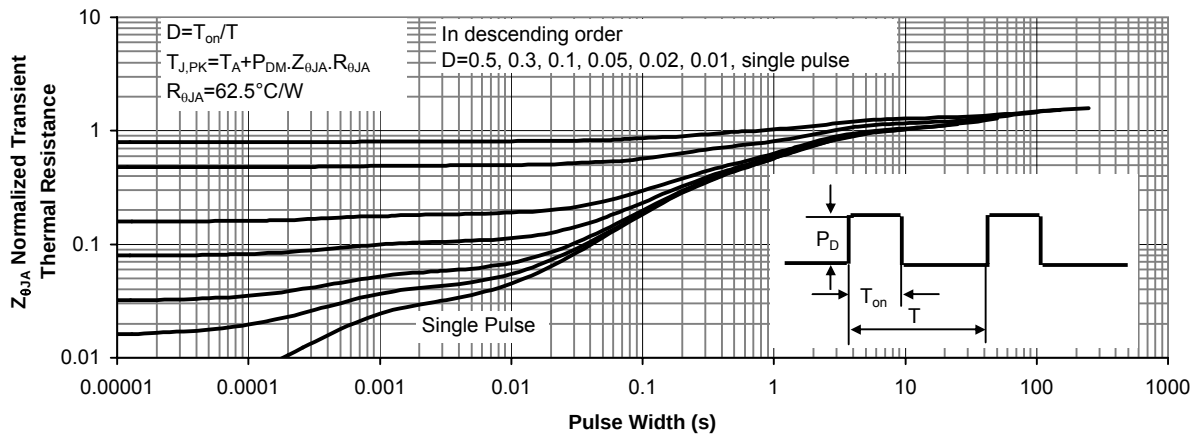


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-48\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1	-2.1	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-3.2\text{A}$ $T_J=125^\circ\text{C}$		84 145	105	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$, $I_D=-2.8\text{A}$		106	135	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-3.2\text{A}$		9		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.73	-1	V
I_S	Maximum Body-Diode Continuous Current				-3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-30\text{V}$, $f=1\text{MHz}$		930	1120	pF
C_{oss}	Output Capacitance			85		pF
C_{rss}	Reverse Transfer Capacitance			35		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		7.2	9	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}$, $V_{DS}=-30\text{V}$, $I_D=-3.2\text{A}$		16	20	nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			8	10	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			3.2		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-30\text{V}$, $R_L=9.4\Omega$, $R_{GEN}=3\Omega$		8	12	ns
t_r	Turn-On Rise Time			3.8	7.5	ns
$t_{D(off)}$	Turn-Off DelayTime			31.5	48	ns
t_f	Turn-Off Fall Time			7.5	15	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-3.2\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		27	35	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-3.2\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		32		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

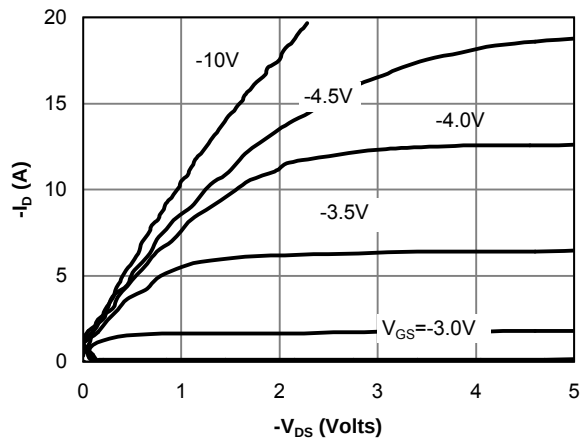


Fig 1: On-Region Characteristics

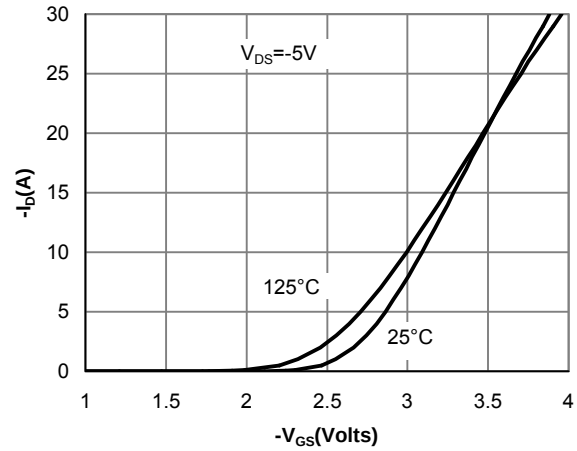


Figure 2: Transfer Characteristics

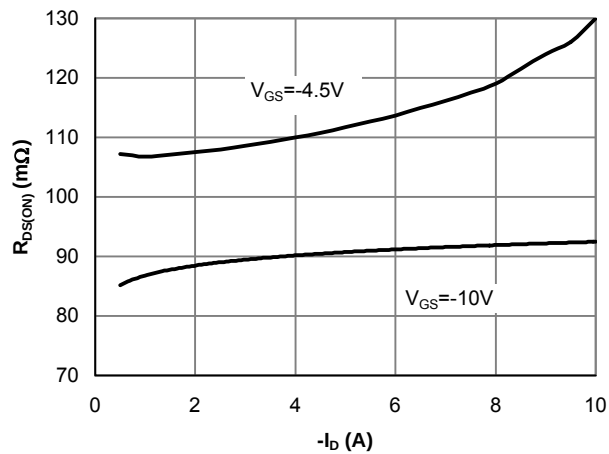


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

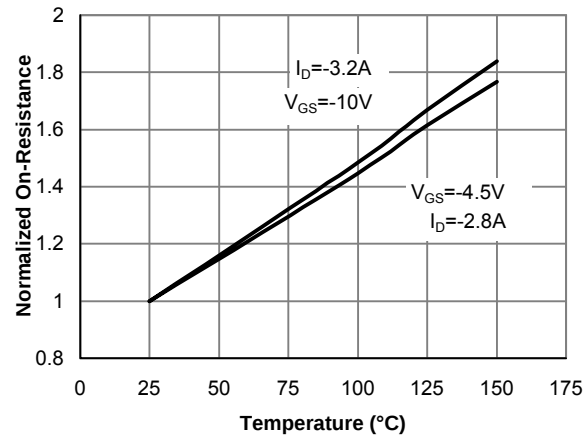


Figure 4: On-Resistance vs. Junction Temperature

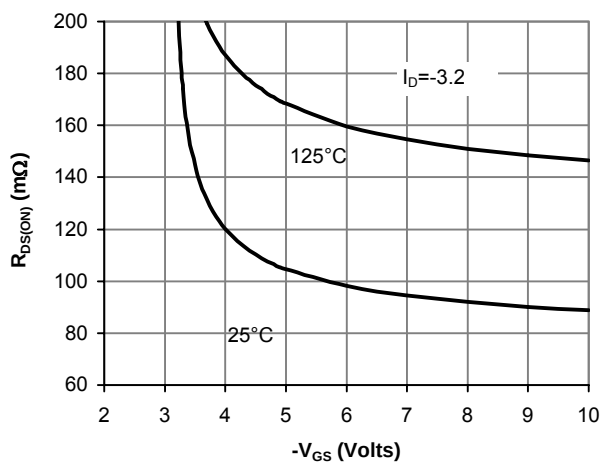


Figure 5: On-Resistance vs. Gate-Source Voltage

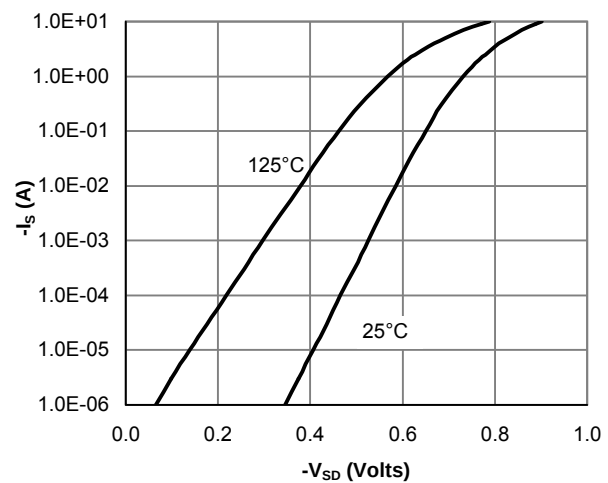


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

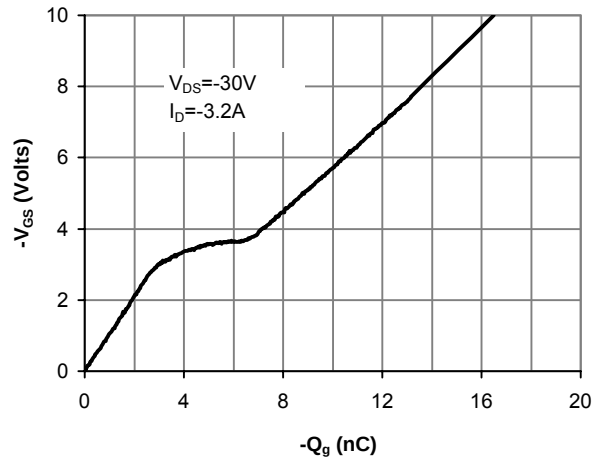


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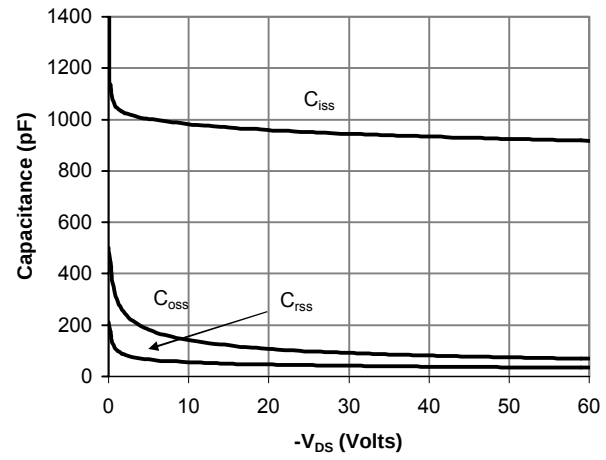


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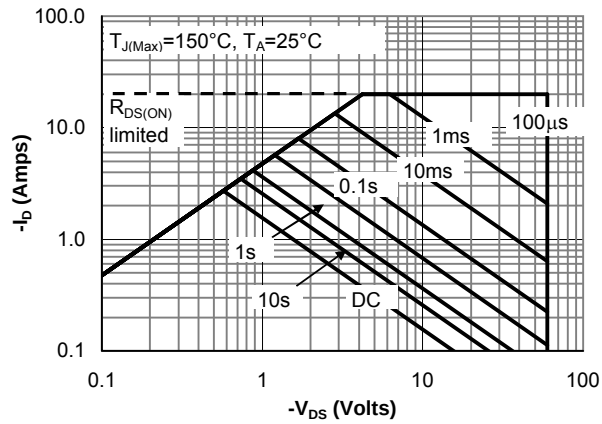


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

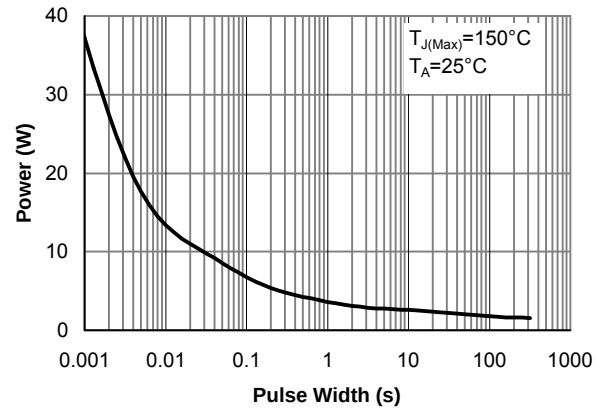


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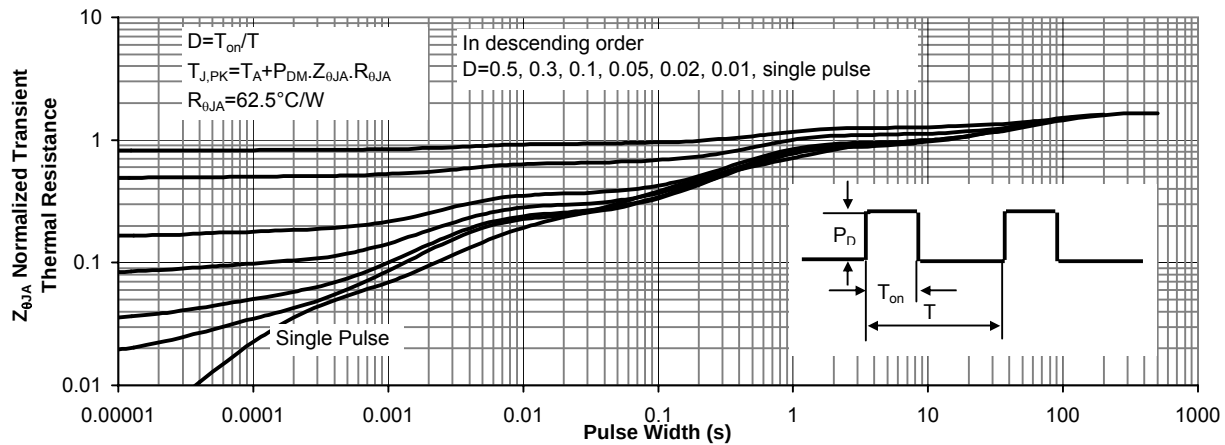


Figure 11: Normalized Maximum Transient Thermal Impedance



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Электрон
Связь**

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