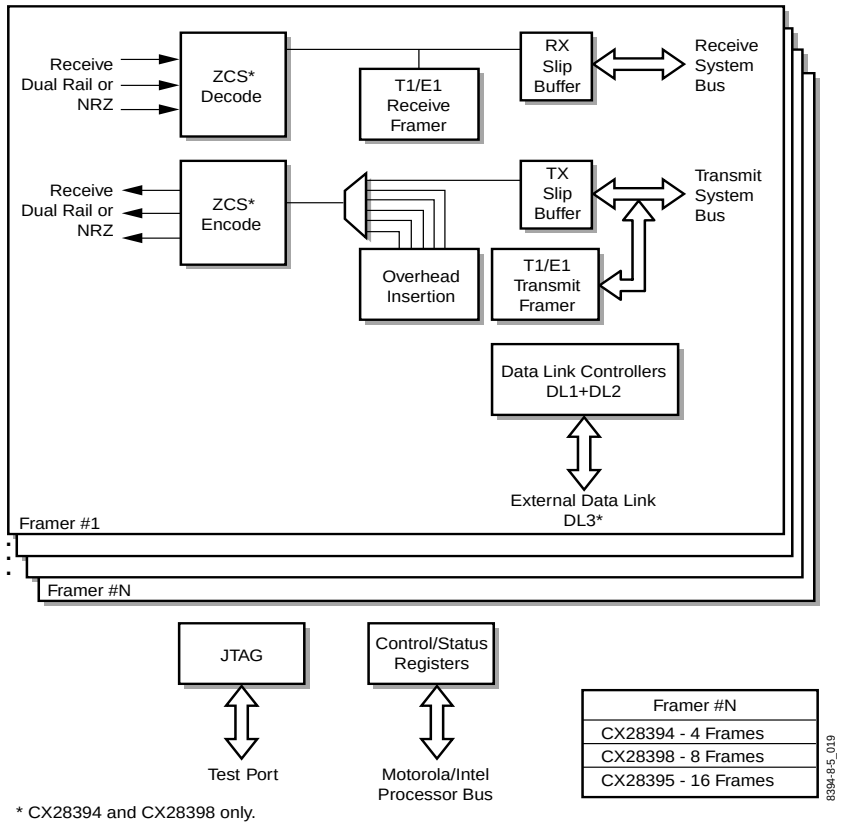
CX28394/28395/28398

Quad/x16/Octal—T1/E1/J1 Framers

The CX28394/28395/28398 is a family of multiple framers for T1/E1/J1 and Integrated Service Digital Network (ISDN) primary rate interfaces operating at 1.544 Mbps or 2.048 Mbps. All framers are totally independent, and each combines a sophisticated framing synchronizer and transmit/receive slip buffers. Operations are controlled through a series of memory-mapped registers accessible via a parallel microprocessor port. Extensive register support is provided for alarm and error monitoring, signaling supervision (including ISDN D-channel/SS7 process), per-channel trunk conditioning, and Facility Data Link (FDL) maintenance. A flexible serial Time Division Multiplexed (TDM) system interface that supports bus rates from 1.536 to 8.192 MHz is featured. Extensive test and diagnostic functions include a full set of loopbacks, Pseudo Random Bit Sequence (PRBS) test pattern generation, Bit Error Rate (BER) meter, and forced error insertion.

Functional Block Diagram



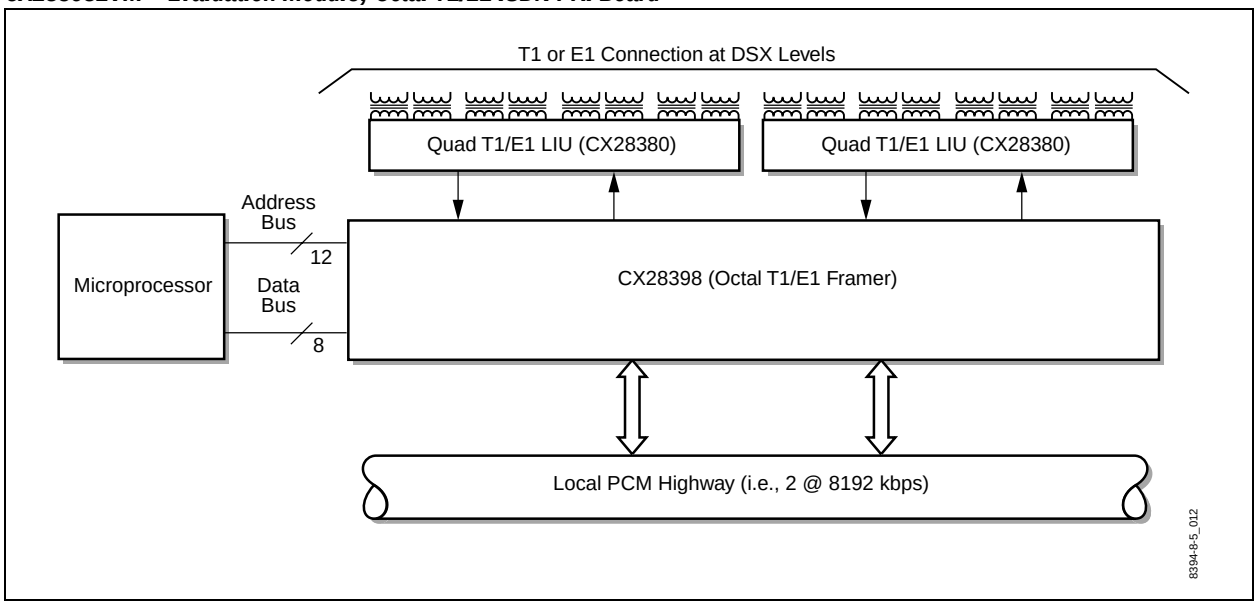
* CX28394 and CX28398 only.

Distinguishing Features

- Up to 16 T1/E1/J1 Framers in one package
- Extensive support of various protocols
- T1: SF, ESF, SLC®96, T1DM, TTC JT(J1)
- E1: PCM-30, G.704, G.706, G.732, ISDN primary rate (ETS300 011, INS 500)
- Extracts and inserts signaling bits
- Dual HDLC controllers per framer for data link and LAPD/SS7 signaling
- Two-frame transmit and receive PCM slip buffers
- Separate or multiplexed system bus interfaces
- Parallel 8-bit microprocessor port supports Intel or Motorola buses
- BERT generation and counting
- B8ZS/HDB3/Bit 7 zero suppression (CX28394 and CX28398 only)
- Operates from a single +3.3 Vdc ± 5% power supply
- Low-power CMOS technology

Applications

- Multiline T1/E1 Channel Service Unit/Data Service Unit (CSU/DSU)
- Digital Access Cross-Connect System (DACS)
- T1/E1 Multiplexer (MUX)
- PBXs and PCM channel bank
- ISDN Primary Rate Access (PRA)
- Frame Relay Switches and Access Devices (FRADS)
- SONET/SDH add/drop multiplexers
- T3/E3 channelized access concentrators



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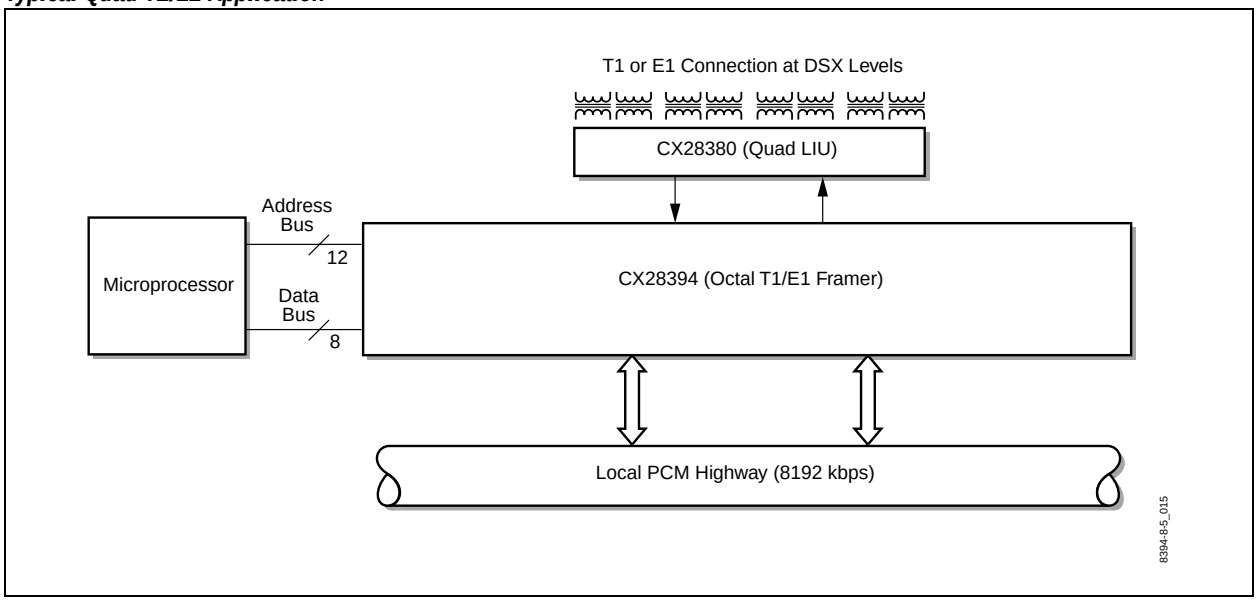
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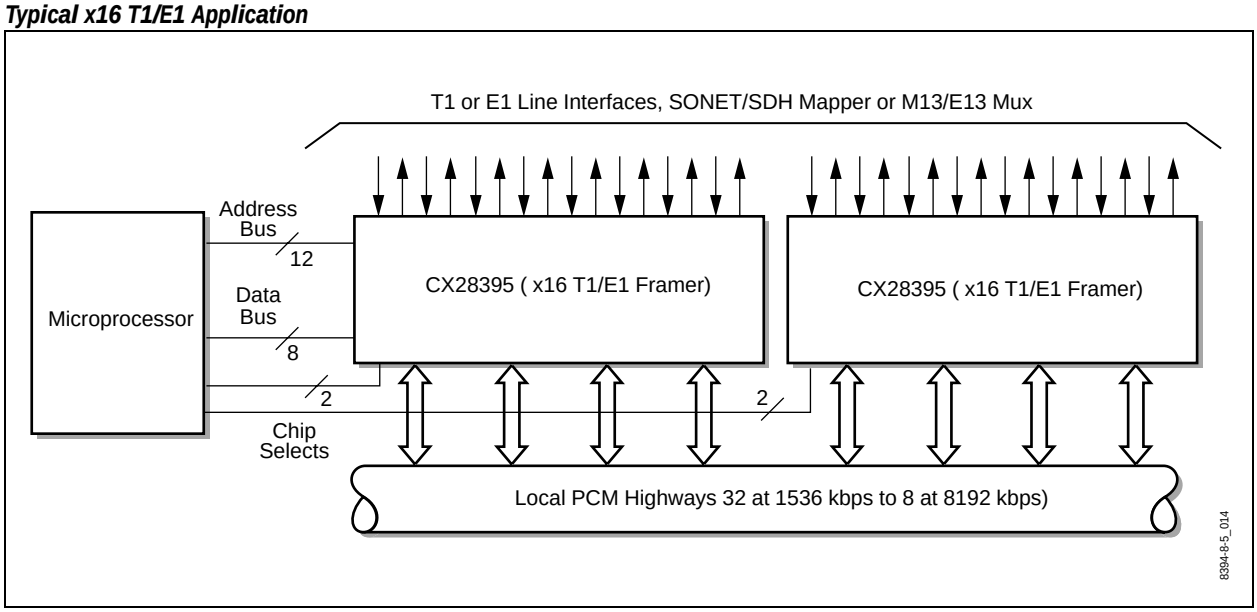
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Typical Quad T1/E1 Application



Typical x16 T1/E1 Application



Ordering Information

Model Number	Number of Framers	Package	Operating Temperature
CX28394-22	4	128-pin TQFP	–40 to 85 °C
CX28398-22	8	208-pin PQFP	–40 to 85 °C
CX28398-23	8	272-pin BGA	–40 to 85 °C
CX28395-19	16	318-pin BGA	–40 to 85 °C
CX28395-18	16	318-pin BGA	0 to 70 °C
CX28398-24	8	208-pin CABGA	–40 to 85 °C
BT00-D660-001	CX28398/CX28380 Evaluation Module		

Detailed Feature Summary

Frame Alignment

- Framed formats:
  - Independent transmit and receive framing modes
  - T1: FT/SF/ESF/SLC/T1DM/TTC-JT(J1)
  - E1: FAS/MFAS/FAS+CAS/MFAS+CAS
- Maximum Average Reframe Time (MART) less than 50 ms
- Transmitter alignment modes:
  - Align to system bus data
  - Align to system bus sync
  - Align to buffer data (embedded framing)
- Unframed mode

Signaling

- T1: 2-, 4-, or 16-state robbed bit ABCD signaling
- E1: Channel Associated Signaling (CAS)
- Common Channel Signaling (CCS) in any time slot
- Per-channel receive signaling stack
- Signaling state change interrupt
- Automatic and manual signaling freeze
- Debounce signaling (2-bit integration)
- UNICODE detection
- Signaling reinsertion on PCM system bus
- Separate I/O for system bus signaling
- Per-channel transparent

Loopbacks

- Remote loopback toward line
  - Retains BPV transparency (CX28394 and CX28398 only)
- Payload loopback
- Per-channel DS0 remote loopback
- Local loopback towards system
  - Framer digital loopback
  - Per-channel DS0 local loopback
- Inband loopback code detection/ generation
- Simultaneous local and remote line loopbacks

Processor Interface

- Parallel 8-bit bus
- Data strobes (Motorola) or address latch enable (Intel)
- Multiplexed or non-multiplexed address/data bus
- Synchronous or asynchronous data transfers
- Open drain interrupt output with maskable sources

Out-of-Service Testing and Maintenance

- Pseudo-Random Bit Sequence (PRBS):
  - Independent transmit and receive
  - 2^{11}; 2^{15}; 2^{20}; 2^{23} patterns
  - Framed or unframed mode
  - Optional 7/14 zero limit
  - Bit Error Counter (BERR)
- Single error insertion:
  - PRBS error
  - Framing error
  - CRC error
  - BPV/LCV error (CX28394 and CX28398 only)
  - COFA error

System Bus Interface (SBI)

- System bus data rates:
  - 1536 kbps (T1 without F-bits)
  - 1544 kbps (T1)
  - 2048 kbps (E1)
  - 4096 kbps (2E1)
  - 8192 kbps (4E1)
- Clock operation at 1x or 2x data rate
- Selectable I/O clock edges
- Master, slave, or mixed bus timing
- Bit and time slot frame sync offsets
- DS0 drop/insert indicators for external mux
- Embedded T1 framing transport per G.802
- Receive and transmit slip buffers
  - Bypass, 2-frame, or 64-bit depth
  - Slip detection with directional status
  - Slip buffer phase status
  - Per-channel idle code insertion
  - Processor accessible data buffers
- Direct connection to upper layer devices:
  - Link layer: Bt8474
  - ATM layer: CN8228
- Direct connection to physical line interface
  - CX28380
- Supported system bus formats:
  - ATT Concentration Highway Interface (CHI)
  - Multi-Vendor Integration Protocol (MVIP)
  - Mitel ST-bus
- Separate or internally multiplexed bus modes

In-Service Performance Monitoring

- One-second timer I/O to synchronize reporting
- Receive error detectors with accumulators:
  - Bipolar/Line Code Violations (LCV) (CX28394 and CX28398 only)
  - Excessive Zeros (EXZ)
  - Loss of Frame (RLOF)
  - Framing Errors (FERR)
  - CRC Errors (CERR)
  - Far End Block Errors (FEBE)
  - Severely Errored Frames (SEF)
  - Change of Frame Alignment (COFA)
- Transmit error detectors:
  - Loss of Frame (TLOF)
  - Framing Errors (TFERR)
  - Multiframe Errors (TMERR)
  - CRC Errors (TCERR)
  - Loss of Transmit Clock (TLOC)
- Receive alarm detectors:
  - Alarm Indication Signal (AIS)
  - Loss of Signal (RLOS)
  - RAI/Yellow Alarm (YEL)
  - Multiframe Yellow (MYEL)
  - Lost Frame Alignment (FRED)
  - Lost Multiframe Alignment (MRED)
  - Carrier Failure Alarm (CFA) with 8:1 dual slope integration
- Controlled Frame Slip (RFSLIP) Uncontrolled Frame Slip (RUSLIP)
- Automatic and on-demand transmit alarms:
  - AIS following RLOS and/or TLOC
  - Automatic AIS clock switching
  - YEL following FRED
  - YEL following 100ms reframe timeout
  - MYEL following MRED
  - FEBE following CERR

Data Links

- Two full-featured data link controllers (DL1 and DL2):
  - 64-octet transmit and receive FIFOs
  - HDLC Message Oriented Protocol (MOP)
  - Unformatted data transfer
  - Unformatted circular buffer
  - End of message/buffer interrupt
  - Near full/empty interrupts at selected depth
- Access any bit combination in any time slot:
  - ISDN D-channels at 16, 32, or 64 kbps
  - National/spare bits (SA-bits) in 4 kbps increments
  - CCS/SS7
  - T1DM R-bits
- Access T1 F-bits in even, odd, or all frames:
  - Automatic Performance Report Message (PRM) generator
  - ESF Facility Data Link (FDL)
  - Unformatted SLC-96 overhead
  - Bit-Oriented Protocol (BOP) priority codeword generation and detection
- Separate I/O for external data link (DL3) on CX28394 and CX28398 devices

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1.0 Product Description

1.1 Overview

The CX2839x devices each contain multiple T1/E1 framers which provide the data access and framing portion of T1 and E1 physical layer interfaces:

Device	Number of Framers
CX28394	4
CX28398	8
CX28395	16

While the framers are identical, there are minor differences among the devices due to the pins provided. These differences are summarized below.

1.1.1 External Datalink

The CX28394 and CX28398 devices include an External Datalink (DL3) which provides signal access to any bit(s) in any time slot of all frames, odd frames, or even frames, including T1 framing bits. Refer to Section 2.2.8, *External Receive Data Link (CX28394 and CX28398 Only)*, and 2.4.1, *External Transmit Data Link (CX28394 and CX28398 Only)*. The DL3 signals are not available on the CX28395 device.

1.1.2 RINDO/TINDO

Receive and Transmit Time Slot Indicator signals are provided by each framer to mark selected (programmable) receive and transmit system bus time slots. On the CX28394 and CX28398 devices, these signals appear on different pins depending on whether Multiplexed System Bus mode or Non-Multiplexed System Bus mode is selected. On the CX28395, they are available only in Multiplexed Bus mode.

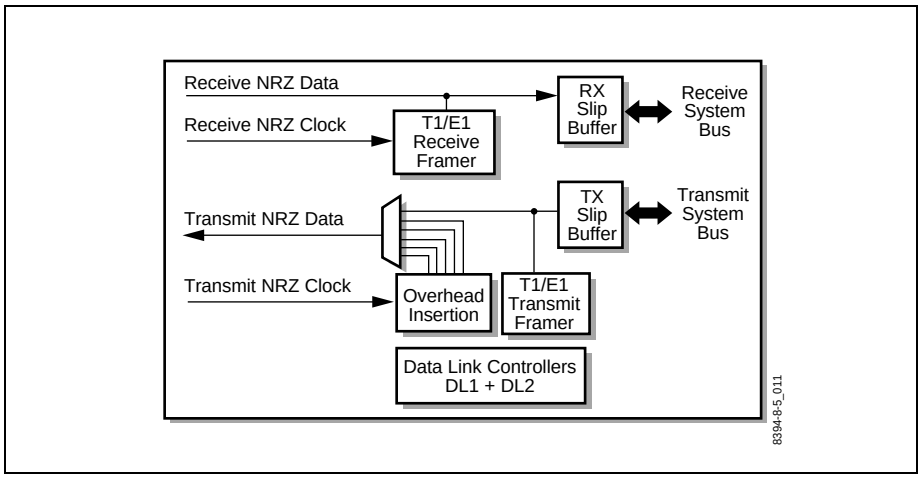
1.1.3 LIU Serial Port

The CX28394 and CX28398 devices include a serial interface which allows a microprocessor to indirectly communicate with a line interface unit such as the CX28380 Quad T1/E1 LIU. This interface allows the microprocessor to control and query the LIU status. This serial interface is not available on the CX28395.

1.1.4 Transmit/Receive Line Interface

The CX28394 and CX28398 devices include line interfaces which can operate in either of two modes: bipolar NRZ or unipolar NRZ. In bipolar NRZ mode, receiver signals RPOSI, RNEGI, and RCKI are used; and transmitter signals TPOSO, TNEGO, and TCKO are used. In unipolar NRZ mode, receiver signals RNRZ and RCKI are used, and transmitter signals TNRZO and TCKO are used. The CX28395 device provides only unipolar NRZ operation and signals. Figure 1-1 illustrates the CX28395 Functional Block Diagram (single framer).

Figure 1-1. CX28395 Functional Block Diagram



1.2 Pin Assignments

The CX28394 is packaged in a 128-pin Quad Flat Pack (TQFP). The CX28395 is packaged in a 318-pin Ball Grid Array (BGA) multi-chip module (MCM). The CX28398 has two package alternatives: a 208-pin Quad Flat Pack (MQFP) and a 272-pin BGA. Pinout diagrams are provided in Figures 1-2 through 1-6 and Tables 1-1 through 1-4 summarize pin assignments for system bus pins. Table 1-5 lists all other pin assignments.

Figures 1-7 through 1-12 illustrate the devices' logic, and Table 1-6 defines the hardware signals.

The following input pins contain an internal pullup resistor (>50 kΩ) and may remain unconnected if the active high input state is desired:

A[7:0]	Address lines unused in INTEL bus mode.
MOTO*	Pullup selects INTEL bus mode if unconnected.
SYNCMD	Pullup selects synchronous processor interface.
TDI (CX28394/28398)	JTAG unused if not connected.
TDI1, TDI2 (CX28395)	JTAG unused if not connected.
TMS	JTAG unused if not connected.
TCK	Disables JTAG if not connected.
TRST*	Disables JTAG reset if not connected.
RST*	Disables hardware reset if not connected.
SERDI	May be left unconnected if not used.

Figure 1-2. CX28394 128-pin TQFP Pinout Diagram

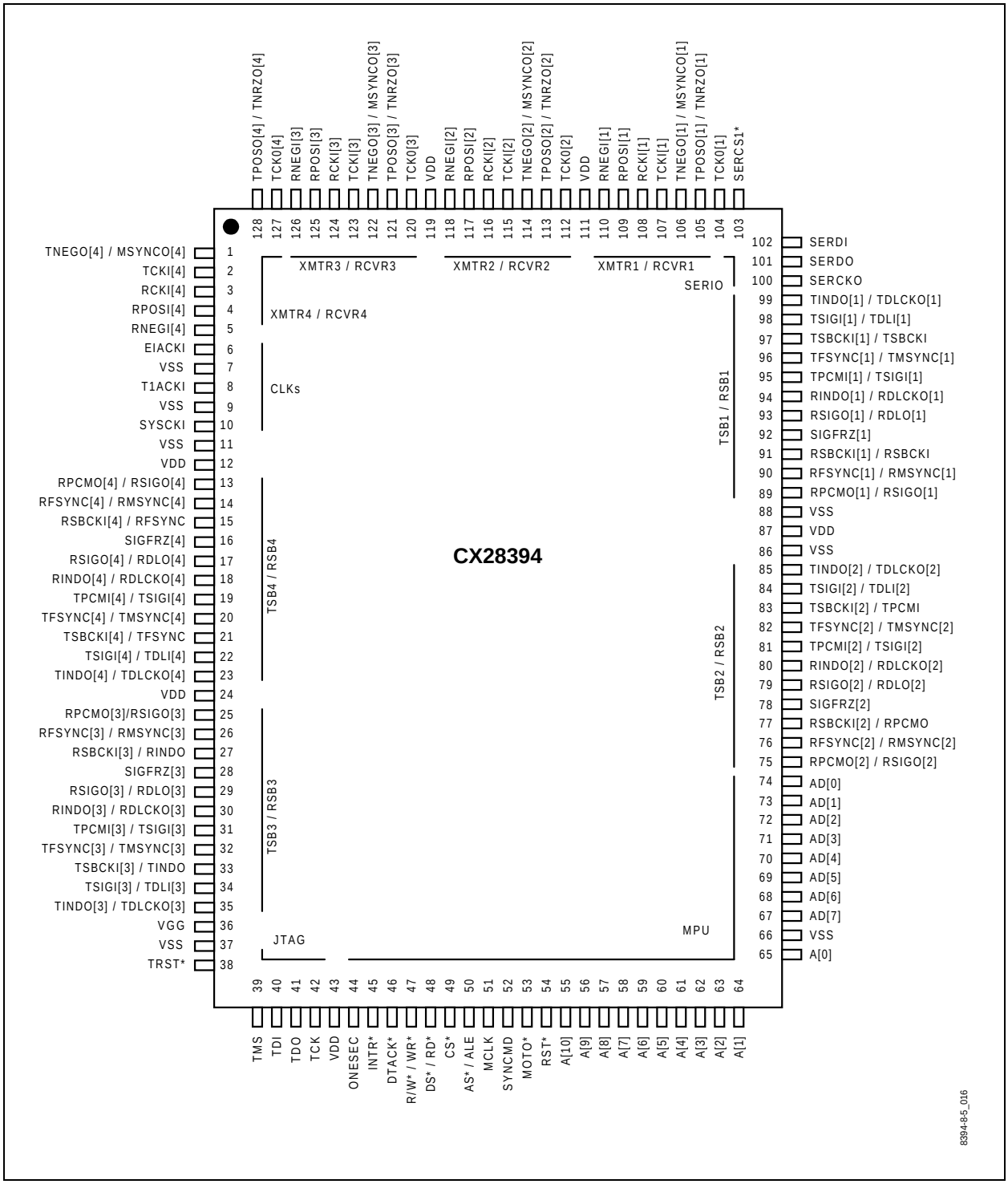


Figure 1-3. CX28395 318-pin BGA Pinout Diagram

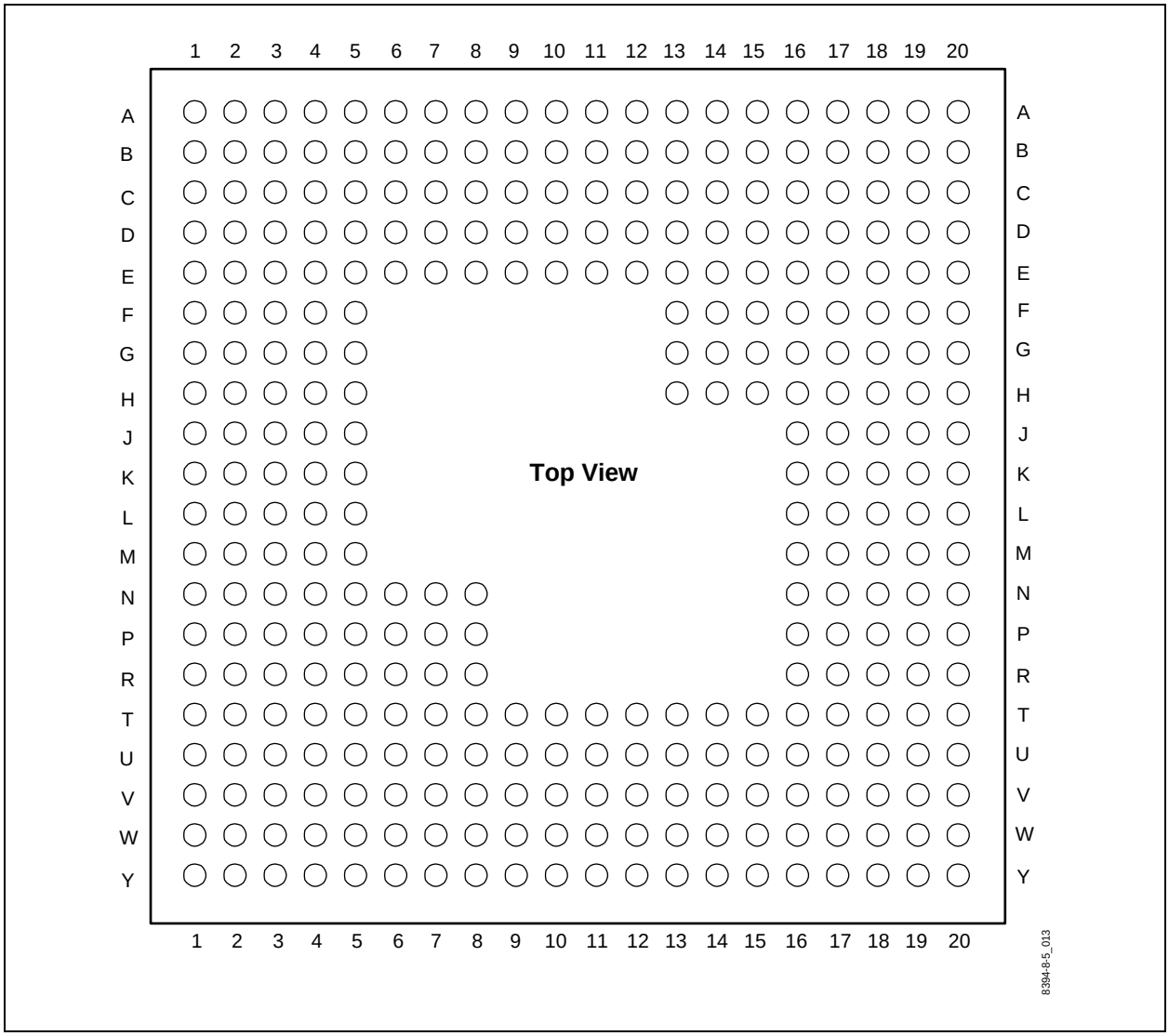


Figure 1-4. CX28398 208-pin PQFP Pinout Diagram

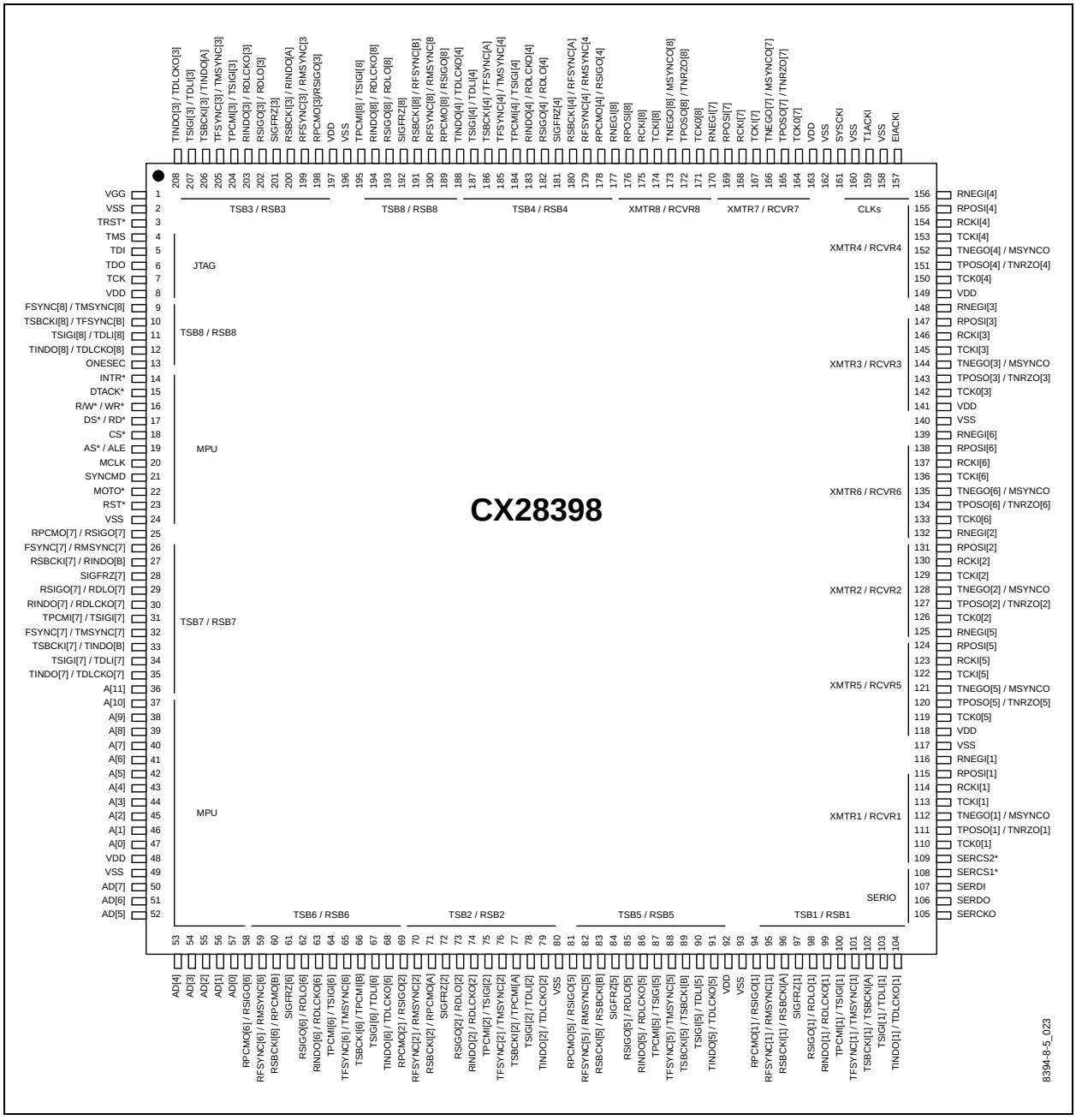


Figure 1-5. CX28398 208-pin CABGA Pinout Diagram

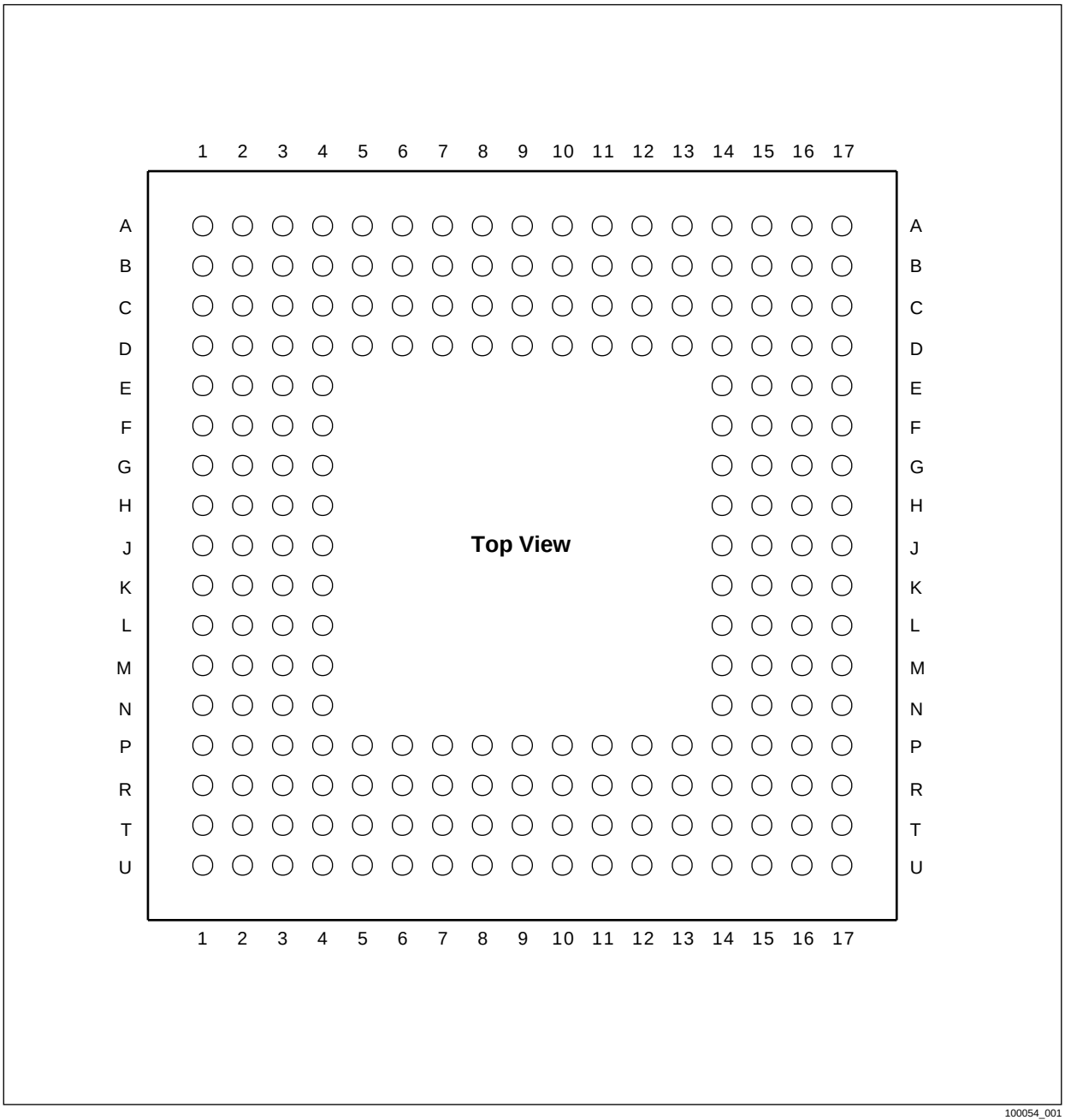


Figure 1-6. CX28398 272-pin BGA Pinout Diagram

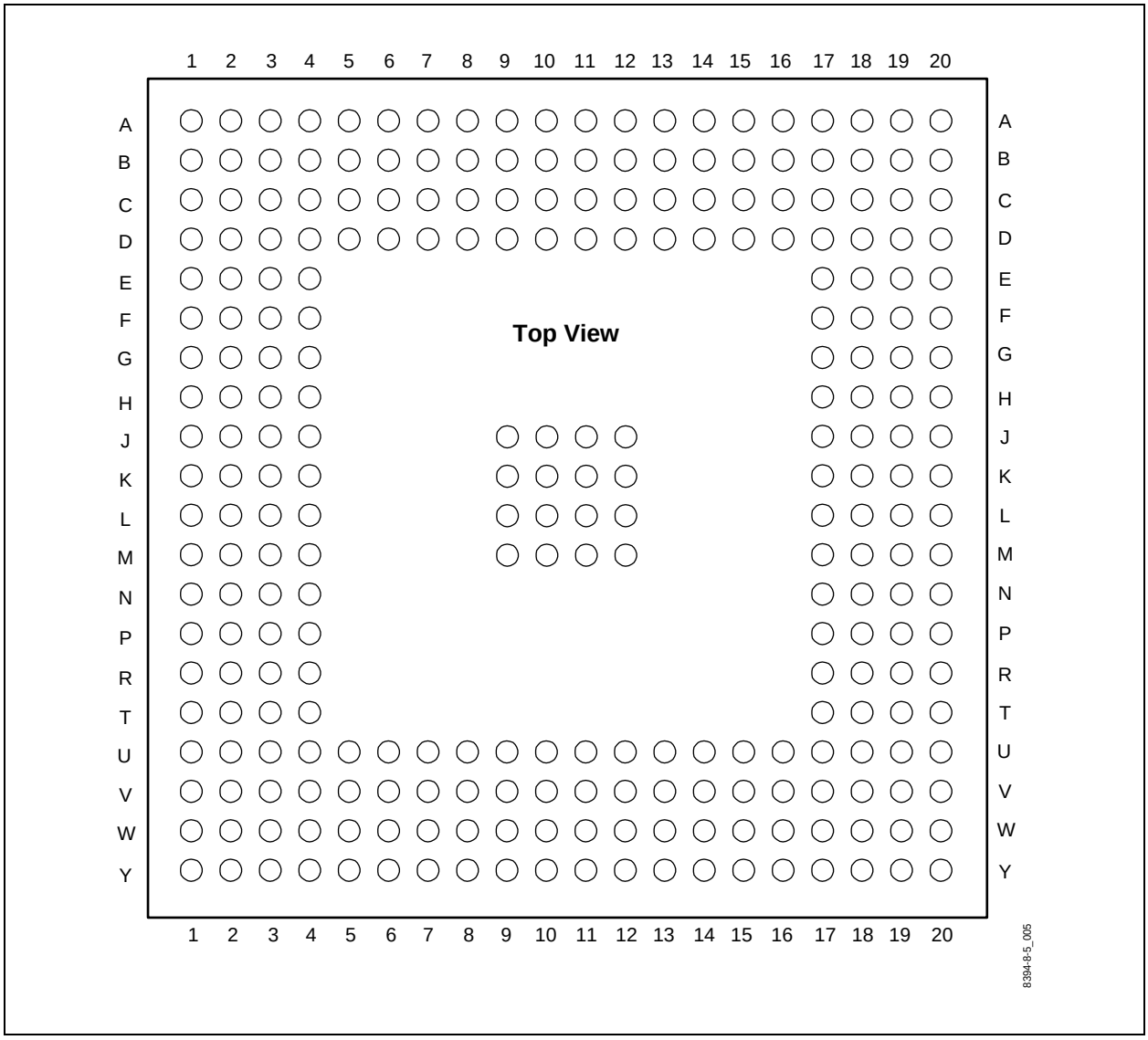


Table 1-1. Pin Assignments (SBI1, SBI2, SBI3, SBI4) *(1 of 2)*

Pin Number					System Bus Interface Pin Functions	
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	Non-Multiplexed Mode SBIMODE[0] = 0 [FCR; addr 080]	Multiplexed Mode SBIMODE[0] = 1 [FCR; addr 080]
89	94	R12	V15	J3	RPCMO[1]	RSIGO[1]
90	95	P11	W16	J4	RFSYNC[1]/RMSYNC[1]	RMSYNC[1]
91	96	U14	Y17	J2	RSBCKI[1]	RSBCKI[A]
92	97	T14	V16	—	SIGFRZ[1]	SIGFRZ[1]
93	98	R13	W17	—	RSIGO[1] / RDLO[1]	RDLO[1]
—	—	—	—	J1	RSIGO[1]	TSTO[1]
94	99	P12	Y18	—	RINDO[1] / RDLCKO[1]	RDLCKO[1]
95	100	U15	V17	K4	TPCMI[1]	TSIGI[1]
96	101	U16	W18	K1	TFSYNC[1]/TMSYNC[1]	TMSYNC[1]
97	102	R14	Y19	K3	TSBCKI[1]	TSBCKI[A]
98	103	P13	V18	—	TSIGI[1] / TDLI[1]	TDLI[1]
—	—	—	—	K2	TSIGI[1]	TSTI[1]
99	104	T15	W19	—	TINDO[1] / TDLCKO[1]	TDLCKO[1]
—	—	—	—	K5	TINDO[1]	—
75	69	R6	W8	E4	RPCMO[2]	RSIGO[2]
76	70	T6	Y8	E3	RFSYNC[2]/RMSYNC[2]	RMSYNC[2]
77	71	U7	V9	E2	RSBCKI[2]	RPCMO[A]
78	72	P7	W9	—	SIGFRZ[2]	SIGFRZ[2]
79	73	R7	Y9	—	RSIGO[2] / RDLO[2]	RDLO[2]
—	—	—	—	F4	RSIGO[2]	TSTO[2]
80	74	T7	W10	—	RINDO[2] / RDLCKO[2]	RDLCKO[2]
81	75	U8	V10	F3	TPCMI[2]	TSIGI[2]
82	76	P8	Y10	F2	TFSYNC[2]/TMSYNC[2]	TMSYNC[2]
83	77	R8	Y11	E1	TSBCKI[2]	TPCMI[A]
84	78	T8	W11	—	TSIGI[2] / TDLI[2]	TDLI[2]
—	—	—	—	F1	TSIGI[2]	TSTI[2]
85	79	U9	V11	—	TINDO[2] / TDLCKO[2]	TDLCKO[2]
—	—	—	—	H5	TINDO[2]	—
25	198	C6	C6	U9	RPCMO[3]	RSIGO[3]
26	199	D6	B5	Y9	RFSYNC[3]/RMSYNC[3]	RMSYNC[3]

Table 1-1. Pin Assignments (SBI1, SBI2, SBI3, SBI4) *(2 of 2)*

Pin Number					System Bus Interface Pin Functions	
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	Non-Multiplexed Mode SBIMODE[0] = 0 [FCR; addr 080]	Multiplexed Mode SBIMODE[0] = 1 [FCR; addr 080]
27	200	C5	A4	U10	RSBCKI[3]	RINDO[A]
28	201	D5	C5	—	SIGFRZ[3]	SIGFRZ[3]
29	202	B5	B4	—	RSIGO[3] / RDLO[3]	RDLO[3]
—	—	—	—	Y10	RSIGO[3]	TSTO[3]
30	203	A4	A3	—	RINDO[3] / RDLCKO[3]	RDLCKO[3]
31	204	A3	C4	V9	TPCMI[3]	TSIGI[3]
32	205	B3	B3	W10	TFSYNC[3]/TMSYNC[3]	TMSYNC[3]
33	206	C4	B2	V10	TSBCKI[3]	TINDO[A]
34	207	A2	A2	—	TSIGI[3] / TDLI[3]	TDLI[3]
—	—	—	—	W9	TSIGI[3]	TSTI[3]
35	208	B4	C3	—	TINDO[3] / TDLCKO[3]	TDLCKO[3]
—	—	—	—	T10	TINDO[3]	—
13	178	A11	B11	U5	RPCMO[4]	RSIGO[4]
14	179	B10	C11	W5	RFSYNC[4]/RMSYNC[4]	RMSYNC[4]
15	180	C10	A11	V6	RSBCKI[4]	RFSYNC[A]
16	181	D10	A10	—	SIGFRZ[4]	SIGFRZ[4]
17	182	A10	B10	—	RSIGO[4] / RDLO[4]	RDLO[4]
—	—	—	—	Y5	RSIGO[4]	TSTO[4]
18	183	A9	C10	—	RINDO[4] / RDLCKO[4]	RDLCKO[4]
19	184	B9	A9	W6	TPCMI[4]	TSIGI[4]
20	185	C9	B9	V5	TFSYNC[4]/TMSYNC[4]	TMSYNC[4]
21	186	D9	C9	U6	TSBCKI[4]	TFSYNC[A]
22	187	A8	A8	—	TSIGI[4] / TDLI[4]	TDLI[4]
—	—	—	—	Y6	TSIGI[4]	TSTI[4]
23	188	C8	B8	—	TINDO[4] / TDLCKO[4]	TDLCKO[4]
—	—	—	—	T8	TINDO[4]	—

Table 1-2. Pin Assignments (SBI5, SBI6, SBI7, SBI8) *(1 of 2)*

Pin Number					System Bus Interface Pin Functions Pin Functions	
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	Non-Multiplexed Mode SBIMODE[0] = 0 [FCR; addr 080]	Multiplexed Mode SBIMODE[0] = 1 [FCR; addr 080]
—	81	U10	Y12	G4	RPCMO[5]	RSIGO[5]
—	82	R9	W12	G2	RFSYNC[5] / RMSYNC[5]	RMSYNC[5]
—	83	P9	V12	G3	RSBCKI[5]	RSBCKI[B]
—	84	T10	Y13	—	SIGFRZ[5]	SIGFRZ[5]
—	85	R10	W13	—	RSIGO[5] / RDLO[5]	RDLO[5]
—	—	—	—	G1	RSIGO[5]	TSTO[5]
—	86	U11	V13	—	RINDO[5] / RDLCKO[5]	RDLCKO[5]
—	87	T11	Y14	H3	TPCMI[5]	TSIGI[5]
—	88	R11	W14	H4	TFSYNC[5] / TMSYNC[5]	TMSYNC[5]
—	89	T12	Y15	H1	TSBCKI[5]	TSBCKI[B]
—	90	U12	V14	—	TSIGI[5] / TDLI[5]	TDLI[5]
—	—	—	—	H2	TSIGI[5]	TSTI[5]
—	91	P10	W15	—	TINDO[5] / TDLCKO[5]	TDLCKO[5]
—	—	—	—	J5	TINDO[5]	—
—	58	P4	Y4	C2	RPCMO[6]	RSIGO[6]
—	59	U3	V5	C4	RFSYNC[6] / RMSYNC[6]	RMSYNC[6]
—	60	U4	W5	C1	RSBCKI[6]	RPCMO[B]
—	61	R4	Y5	—	SIGFRZ[6]	SIGFRZ[6]
—	62	T4	V6	—	RSIGO[6] / RDLO[6]	RDLO[6]
—	—	—	—	D4	RSIGO[6]	TSTO[6]
—	63	U5	W6	—	RINDO[6] / RDLCKO[6]	RDLCKO[6]
—	64	P5	Y6	D2	TPCMI[6]	TSIGI[6]
—	65	R5	V7	D3	TFSYNC[6] / TMSYNC[6]	TMSYNC[6]
—	66	T5	W7	D1	TSBCKI[6]	TPCMI[B]
—	67	U6	Y7	—	TSIGI[6] / TDLI[6]	TDLI[6]
—	—	—	—	C3	TSIGI[6]	TSTI[6]
—	68	P6	V8	—	TINDO[6] / TDLCKO[6]	TDLCKO[6]
—	—	—	—	G5	TINDO[6]	—
—	25	J4	L1	U12	RPCMO[7]	RSIGO[7]
—	26	H2	L2	Y11	RFSYNC[7] / RMSYNC[7]	RMSYNC[7]

Table 1-2. Pin Assignments (SBI5, SBI6, SBI7, SBI8) *(2 of 2)*

Pin Number					System Bus Interface Pin Functions Pin Functions	
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	Non-Multiplexed Mode SBIMODE[0] = 0 [FCR; addr 080]	Multiplexed Mode SBIMODE[0] = 1 [FCR; addr 080]
—	27	H1	L3	Y12	RSBCKI[7]	RINDO[B]
—	28	J1	M1	—	SIGFRZ[7]	SIGFRZ[7]
—	29	J3	M2	—	RSIGO[7] / RDLO[7]	RDLO[7]
—	—	—	—	W11	RSIGO[7]	TSTO[7]
—	30	J2	M3	—	RINDO[7] / RDLCKO[7]	RDLCKO[7]
—	31	K4	N1	W12	TPCMI[7]	TSIGI[7]
—	32	K1	N2	V11	TFSYNC[7] / TMSYNC[7]	TMSYNC[7]
—	33	K2	N3	V12	TSBCKI[7]	TINDO[B]
—	34	L1	P1	—	TSIGI[7] / TDLI[7]	TDLI[7]
—	—	—	—	U11	TSIGI[7]	TSTI[7]
—	35	K3	P2	—	TINDO[7] / TDLCKO[7]	TDLCKO[7]
—	—	—	—	T11	TINDO[7]	—
—	189	D8	C8	W7	RPCMO[8]	RSIGO[8]
—	190	B8	A7	V7	RFSYNC[8] / RMSYNC[8]	RMSYNC[8]
—	191	C7	B7	Y7	RSBCKI[8]	RFSYNC[B]
—	192	A7	A6	—	SIGFRZ[8]	SIGFRZ[8]
—	193	D7	C7	—	RSIGO[8] / RDLO[8]	RDLO[8]
—	—	—	—	V8	RSIGO[8]	TSTO[8]
—	194	B7	B6	—	RINDO[8] / RDLCKO[8]	RDLCKO[8]
—	195	A6	A5	Y8	TPCMI[8]	TSIGI[8]
—	9	E4	E1	W8	TFSYNC[8] / TMSYNC[8]	TMSYNC[8]
—	10	E3	F3	U8	TSBCKI[8]	TFSYNC[B]
—	11	D2	F2	—	TSIGI[8] / TDLI[8]	TDLI[8]
—	—	—	—	U7	TSIGI[8]	TSTI[8]
—	12	D1	F1	—	TINDO[8] / TDLCKO[8]	TDLCKO[8]
—	—	—	—	T9	TINDO[8]	—

Table 1-3. Pin Assignments (SBI9, SBI10, SBI11, SBI12) *(1 of 2)*

Pin Number					System Bus Interface Pin Functions	
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	Non-Multiplexed Mode SBIMODE[0] = [FCR; addr 001]	Multiplexed Mode SBIMODE[0] = 1 [FCR; addr 001]
—	—	—	—	F20	RPCMO[9]	RSIGO[9]
—	—	—	—	F18	RFSYNC[9]/RMSYNC[9]	RMSYNC[9]
—	—	—	—	F19	RSBCKI[9]	RSBCKI[C]
—	—	—	—	F17	RSIGO[9]	TSTO[9]
—	—	—	—	E20	TPCMI[9]	TSIGI[9]
—	—	—	—	E18	TFSYNC[9]/TMSYNC[9]	TMSYNC[9]
—	—	—	—	E19	TSBCKI[9]	TSBCKI[C]
—	—	—	—	E17	TSIGI[9]	TSTI[9]
—	—	—	—	F16	TINDO[9]	—
—	—	—	—	K17	RPCMO[10]	RSIGO[10]
—	—	—	—	K19	RFSYNC[10]/RMSYNC[10]	RMSYNC[10]
—	—	—	—	K18	RSBCKI[10]	RPCMO[C]
—	—	—	—	K20	RSIGO[10]	TSTO[10]
—	—	—	—	J17	TPCMI[10]	TSIGI[10]
—	—	—	—	J20	TFSYNC[10]/TMSYNC[10]	TMSYNC[10]
—	—	—	—	J18	TSBCKI[10]	TPCMI[C]
—	—	—	—	J19	TSIGI[10]	TSTI[10]
—	—	—	—	H16	TINDO[10]	—
—	—	—	—	A4	RPCMO[11]	RSIGO[11]
—	—	—	—	A3	RFSYNC[11]/RMSYNC[11]	RMSYNC[11]
—	—	—	—	B4	RSBCKI[11]	RINDO[C]
—	—	—	—	B3	RSIGO[11]	TSTO[11]
—	—	—	—	A2	TPCMI[11]	TSIGI[11]
—	—	—	—	A1	TFSYNC[11]/TMSYNC[11]	TMSYNC[11]
—	—	—	—	B2	TSBCKI[11]	TINDO[C]
—	—	—	—	B1	TSIGI[11]	TSTI[11]
—	—	—	—	E5	TINDO[11]	—
—	—	—	—	A10	RPCMO[12]	RSIGO[12]
—	—	—	—	D10	RFSYNC[12]/RMSYNC[12]	RMSYNC[12]
—	—	—	—	B10	RSBCKI[12]	RFSYNC[C]

Table 1-3. Pin Assignments (SBI9, SBI10, SBI11, SBI12) *(2 of 2)*

Pin Number					System Bus Interface Pin Functions	
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	Non-Multiplexed Mode SBIMODE[0] = [FCR; addr 001]	Multiplexed Mode SBIMODE[0] = 1 [FCR; addr 001]
—	—	—	—	D9	RSIGO[12]	TSTO[12]
—	—	—	—	A9	TPCMI[12]	TSIGI[12]
—	—	—	—	C9	TFSYNC[12]/TMSYNC[12]	TMSYNC[12]
—	—	—	—	B9	TSBCKI[12]	TFSYNC[C]
—	—	—	—	C10	TSIGI[12]	TSTI[12]
—	—	—	—	E7	TINDO[12]	—

Table 1-4. Pin Assignments (SBI13, SBI14, SBI15, SBI16) *(1 of 2)*

Pin Number					System Bus Interface Pin Functions	
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	Non-Multiplexed Mode SBIMODE[0] = [FCR; addr 001]	Multiplexed Mode SBIMODE[0] = 1 [FCR; addr 001]
—	—	—	—	H18	RPCMO[13]	RSIGO[13]
—	—	—	—	H19	RFSYNC[13]/RMSYNC[13]	RMSYNC[13]
—	—	—	—	H17	RSBCKI[13]	RSBCKI[D]
—	—	—	—	H20	RSIGO[13]	TSTO[13]
—	—	—	—	G17	TPCMI[13]	TSIGI[13]
—	—	—	—	G20	TFSYNC[13]/TMSYNC[13]	TMSYNC[13]
—	—	—	—	G18	TSBCKI[13]	TSBCKI[D]
—	—	—	—	G19	TSIGI[13]	TSTI[13]
—	—	—	—	G16	TINDO[13]	—
—	—	—	—	M18	RPCMO[14]	RSIGO[14]
—	—	—	—	M17	RFSYNC[14]/RMSYNC[14]	RMSYNC[14]
—	—	—	—	M19	RSBCKI[14]	RPCMO[D]
—	—	—	—	L19	RSIGO[14]	TSTO[14]
—	—	—	—	L20	TPCMI[14]	TSIGI[14]
—	—	—	—	L17	TFSYNC[14]/TMSYNC[14]	TMSYNC[14]
—	—	—	—	M20	TSBCKI[14]	TPCMI[D]

Table 1-4. Pin Assignments (SBI13, SBI14, SBI15, SBI16) *(2 of 2)*

Pin Number					System Bus Interface Pin Functions	
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	Non-Multiplexed Mode SBIMODE[0] = [FCR; addr 001]	Multiplexed Mode SBIMODE[0] = 1 [FCR; addr 001]
—	—	—	—	L18	TSIGI[14]	TSTI[14]
—	—	—	—	K16	TINDO[14]	—
—	—	—	—	B7	RPCMO[15]	RSIGO[15]
—	—	—	—	B8	RFSYNC[15]/RMSYNC[15]	RMSYNC[15]
—	—	—	—	D7	RSBCKI[15]	RINDO[D]
—	—	—	—	C8	RSIGO[15]	TSTO[15]
—	—	—	—	A7	TPCMI[15]	TSIGI[15]
—	—	—	—	A8	TFSYNC[15]/TMSYNC[15]	TMSYNC[15]
—	—	—	—	C7	TSBCKI[15]	TINDO[D]
—	—	—	—	D8	TSIGI[15]	TSTI[15]
—	—	—	—	M16	TINDO[15]	—
—	—	—	—	A6	RPCMO[16]	RSIGO[16]
—	—	—	—	A5	RFSYNC[16]/RMSYNC[16]	RMSYNC[16]
—	—	—	—	B6	RSBCKI[16]	RFSYNC[D]
—	—	—	—	D6	RSIGO[16]	TSTO[16]
—	—	—	—	C6	TPCMI[16]	TSIGI[16]
—	—	—	—	B5	TFSYNC[16]/TMSYNC[16]	TMSYNC[16]
—	—	—	—	C5	TSBCKI[16]	TFSYNC[D]
—	—	—	—	D5	TSIGI[16]	TSTI[16]
—	—	—	—	J16	TINDO[16]	—

Table 1-5. Pin Assignments *(1 of 9)*

Pin Number					Pin Functions
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	
7	117	B2	A1	N6	VSS (GND)
9	140	G1	D4	N7	VSS (GND)
11	158	P3	D8	N8	VSS (GND)
37	160	T9	D13	P6	VSS (GND)
66	162	T13	D17	P7	VSS (GND)
86	196	N17	H4	P8	VSS (GND)
—	2	F17	H17	R6	VSS (GND)
—	24	B16	J9	R7	VSS (GND)
—	49	A16	J10	R8	VSS (GND)
—	80	D14	J11	F13	VSS (GND)
—	93	B6	J12	F14	VSS (GND)
—	—	—	K9	F15	VSS (GND)
—	—	—	K10	G13	VSS (GND)
—	—	—	K11	G14	VSS (GND)
—	—	—	K12	G15	VSS (GND)
—	—	—	L9	H13	VSS (GND)
—	—	—	L10	H14	VSS (GND)
—	—	—	L11	H15	VSS (GND)
—	—	—	L12	T13	VSS (GND)
—	—	—	M9	T14	VSS (GND)
—	—	—	M10	—	VSS (GND)
—	—	—	M11	—	VSS (GND)
—	—	—	M12	—	VSS (GND)
—	—	—	N4	—	VSS (GND)
—	—	—	N17	—	VSS (GND)
—	—	—	U4	—	VSS (GND)
—	—	—	U8	—	VSS (GND)
—	—	—	U13	—	VSS (GND)
—	—	—	U17	—	VSS (GND)
111	118	C1	D6	E6	VDD

Table 1-5. Pin Assignments *(2 of 9)*

Pin Number					Pin Functions
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	
119	141	P2	D11	F5	VDD
12	149	U13	D15	N20	VDD
24	163	M15	F4	R16	VDD
43	197	G15	F17	T15	VDD
87	8	F14	K4	Y20	VDD
—	48	C14	L17	—	VDD
—	92	A5	R4	—	VDD
—	—	—	R17	—	VDD
—	—	—	U6	—	VDD
—	—	—	U10	—	VDD
—	—	—	U15	—	VDD
36	1	A1	B1	Y14	VGG
38	3	C3	D2	Y16	TRST*
39	4	B1	D3	W20	TMS
40	5	D4	C1	—	TDI
—	—	—	—	Y15	TDI1
—	—	—	—	T20	TDI2
41	6	D3	D1	—	TD0
—	—	—	—	Y19	TDO1
—	—	—	—	P19	TDO2
42	7	C2	E3	W17	TCK
6	157	A17	A19	P20	E1ACKI
8	159	B15	B17	N19	T1ACKI
10	161	C15	A18	U13	SYSCKI
44	13	F4	G3	—	ONESEC
—	—	—	—	V13	ONESEC1
—	—	—	—	Y13	ONESEC2
45	14	F3	G2	—	INTR*
—	—	—	—	Y18	INTR1*
—	—	—	—	N17	INTR2*

Table 1-5. Pin Assignments *(3 of 9)*

Pin Number					Pin Functions
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	
46	15	E2	G1	—	DTACK*
—	—	—	—	W13	DTACK1*
—	—	—	—	T18	DTACK2*
47	16	E1	H3	Y17	R/W*/WR*
48	17	G4	H2	W14	DS*/RD*
49	18	G3	H1	—	CS*
—	—	—	—	W19	CSI*
—	—	—	—	N18	CS2*
50	19	F2	J3	V14	AS*/ALE
51	20	F1	J2	U14	MCLK
52	21	H4	J1	W15	SYNCMD
53	22	H3	K2	W18	MOTO*
54	23	G2	K3	W16	RST*
—	36	L3	R1	V15	A[11]
55	37	M2	P3	V18	A[10]
56	38	M1	R2	U15	A[9]
57	39	L4	T1	V16	A[8]
58	40	N2	R3	V20	A[7]
59	41	L2	T2	V19	A[6]
60	42	N1	U1	U20	A[5]
61	43	M4	T3	V17	A[4]
62	44	M3	U2	U16	A[3]
63	45	N4	V1	U19	A[2]
64	46	P1	U3	U17	A[1]
65	47	N3	V2	T17	A[0]
67	50	R2	V3	R17	AD[7]
68	51	R1	W2	U18	AD[6]
69	52	T1	Y1	R18	AD[5]
70	53	U1	W3	R20	AD[4]
71	54	T2	Y2	P18	AD[3]

Table 1-5. Pin Assignments *(4 of 9)*

Pin Number					Pin Functions
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	
72	55	U2	W4	R19	AD2]
73	56	T3	V4	P17	AD[1]
74	57	R3	Y3	T19	AD[0]
100	105	U17	W20	—	SERCLKO
101	106	T16	V19	—	SERDO
102	107	T17	U19	—	SERDI
103	108	R16	U18	—	SERCS1* (SERCS*)
—	109	R17	V20	—	SERCS2*
104	110	R15	U20	L3	TCKO[1]
107	113	P16	T20	M3	TCKI[1]
105	111	N15	T18	L4	TPOSO[1]/TNRZO[1]
106	112	P17	T19	L5	TNEGO[1]/MSYNCO[1]
108	114	P15	R18	L1	RCKI[1]
109	115	P14	R19	L2	RPOSI[1]/RNRZI[1]
110	116	N16	R20	—	RNEGI[1]
112	126	K15	L19	N1	TCKO[2]
115	129	K16	K20	P3	TCKI[2]
113	127	K17	L18	N2	TPOSO[2]/TNRZO[2]
114	128	L14	L20	N5	TNEGO[2]/MSYNCO[2]
116	130	J16	K19	P1	RCKI[2]
117	131	J17	K18	P2	RPOSI[2]/RNRZI[2]
118	132	J15	J20	—	RNEGI[2]
120	142	H14	F19	T1	TCKO[3]
123	145	G14	E19	T4	TCKI[3]
121	143	F16	E20	T3	TPOSO[3]/TNRZO[3]
122	144	E17	F18	R5	TNEGO[3]/MSYNCO[3]
124	146	F15	D20	T2	RCKI[3]
125	147	E16	E18	U1	RPOSI[3]/RNRZI[3]
126	148	D17	D19	—	RNEGI[3]
127	150	E15	C20	U2	TCKO[4]

Table 1-5. Pin Assignments *(5 of 9)*

Pin Number					Pin Functions
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	
2	153	E14	B20	U3	TCKI[4]
128	151	D16	D18	U4	TPOSO[4]/TNRZO[4]
1	152	C17	C19	T5	TNEGO[4]/MSYNCO[4]
3	154	D15	C18	V1	RCKI[4]
4	155	C16	B19	V2	RPOSI[4]/RNRZI[4]
5	156	B17	A20	—	RNEGI[4]
—	119	N14	P20	M4	TCKO[5]
—	122	L15	N20	M2	TCKI[5]
—	120	M16	N18	M1	TPOSO[5]/TNRZO[5]
—	121	M17	N19	M5	TNEGO[5]/MSYNCO[5]
—	123	M14	M18	N3	RCKI[5]
—	124	L16	M19	N4	RPOSI[5]/RNRZI[5]
—	125	L17	M20	—	RNEGI[5]
—	133	H17	J19	P4	TCKO[6]
—	136	H15	H19	R2	TCKI[6]
—	134	K14	J18	R1	TPOSO[6]/TNRZO[6]
—	135	H16	H20	P5	TNEGO[6]/MSYNCO[6]
—	137	G17	H18	R3	RCKI[6]
—	138	J14	G20	R4	RPOSI[6] /RNRZI[6]
—	139	G16	G19	—	RNEGI[6]
—	164	B14	B16	V3	TCKO[7]
—	167	C13	B15	Y1	TCKI[7]
—	165	A15	A16	W1	TPOSO[7]/TNRZO[7]
—	166	D13	C15	T6	TNEGO[7]/MSYNCO[7]
—	168	A14	A15	W2	RCKI[7]
—	169	B13	C14	Y2	RPOSI[7] /RNRZI[7]
—	170	D12	B14	—	RNEGI[7]
—	171	C12	A14	Y3	TCKO[8]
—	174	A12	A13	W3	TCKI[8]
—	172	A13	C13	V4	TPOSO[8]/TNRZO[8]

Table 1-5. Pin Assignments *(6 of 9)*

Pin Number					Pin Functions
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	
—	173	B12	B13	T7	TNEGO[8]/MSYNCO[8]
—	175	C11	C12	W4	RCKI[8]
—	176	B11	B12	Y4	RPOSI[8] /RNRZI[8]
—	177	D11	A12	—	RNEGI[8]
—	—	—	—	D20	TCKO[9]
—	—	—	—	B20	TCKI[9]
—	—	—	—	C20	TPOSO[9]/TNRZO[9]
—	—	—	—	E16	TNEGO[9]/MSYNCO[9]
—	—	—	—	D19	RCKI[9]
—	—	—	—	C19	RPOSI[9]/RNRZI[9]
—	—	—	—	B18	TCKO[10]
—	—	—	—	D17	TCKI[10]
—	—	—	—	C17	TPOSO[10]/TNRZO[10]
—	—	—	—	E14	TNEGO[10]/MSYNCO[10]
—	—	—	—	A18	RCKI[10]
—	—	—	—	A17	RPOSI[10]/RNRZI[10]
—	—	—	—	A15	TCKO[11]
—	—	—	—	D15	TCKI[11]
—	—	—	—	C15	TPOSO[11]/TNRZO[11]
—	—	—	—	E12	TNEGO[11]/MSYNCO[11]
—	—	—	—	B15	RCKI[11]
—	—	—	—	A14	RPOSI[11]/RNRZI[11]
—	—	—	—	B14	TCKO[12]
—	—	—	—	D14	TCKI[12]
—	—	—	—	C14	TPOSO[12]/TNRZO[12]
—	—	—	—	E11	TNEGO[12]/MSYNCO[12]
—	—	—	—	A13	RCKI[12]
—	—	—	—	B13	RPOSI[12]/RNRZI[12]
—	—	—	—	B19	TCKO[13]
—	—	—	—	A19	TCKI[13]

Table 1-5. Pin Assignments *(7 of 9)*

Pin Number					Pin Functions
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	
—	—	—	—	A20	TPOSO[13]/TNRZO[13]
—	—	—	—	E15	TNEGO[13]/MSYNCO[13]
—	—	—	—	C18	RCKI[13]
—	—	—	—	D18	RPOSI[13]/RNRZI[13]
—	—	—	—	B17	TCKO[14]
—	—	—	—	B16	TCKI[14]
—	—	—	—	A16	TPOSO[14]/TNRZO[14]
—	—	—	—	E13	TNEGO[14]/MSYNCO[14]
—	—	—	—	C16	RCKI[14]
—	—	—	—	D16	RPOSI[14] /RNRZI[14]
—	—	—	—	C12	TCKO[15]
—	—	—	—	A12	TCKI[15]
—	—	—	—	B12	TPOSO[15]/TNRZO[15]
—	—	—	—	E10	TNEGO[15]/MSYNCO[15]
—	—	—	—	C13	RCKI[15]
—	—	—	—	D13	RPOSI[15] /RNRZI[15]
—	—	—	—	B11	TCKO[16]
—	—	—	—	C11	TCKI[16]
—	—	—	—	D12	TPOSO[16]/TNRZO[16]
—	—	—	—	E8	TNEGO[16]/MSYNCO[16]
—	—	—	—	A11	RCKI[16]
—	—	—	—	D11	RPOSI[16] /RNRZI[16]
—	—	—	E2	E9	NC
—	—	—	G4	T12	NC
—	—	—	E4	L16	NC
—	—	—	J4	N16	NC
—	—	—	C2	P16	NC
—	—	—	K1	T16	NC
—	—	—	L4	—	NC
—	—	—	M4	—	NC

Table 1-5. Pin Assignments *(8 of 9)*

Pin Number					Pin Functions
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	
—	—	—	T4	—	NC
—	—	—	P4	—	NC
—	—	—	W1	—	NC
—	—	—	U5	—	NC
—	—	—	U7	—	NC
—	—	—	U9	—	NC
—	—	—	U11	—	NC
—	—	—	U12	—	NC
—	—	—	Y16	—	NC
—	—	—	U14	—	NC
—	—	—	U16	—	NC
—	—	—	Y20	—	NC
—	—	—	T17	—	NC
—	—	—	P17	—	NC
—	—	—	P18	—	NC
—	—	—	P19	—	NC
—	—	—	M17	—	NC
—	—	—	F20	—	NC
—	—	—	E17	—	NC
—	—	—	G17	—	NC
—	—	—	G18	—	NC
—	—	—	B18	—	NC
—	—	—	C17	—	NC
—	—	—	D16	—	NC
—	—	—	A17	—	NC
—	—	—	C16	—	NC
—	—	—	D14	—	NC
—	—	—	K17	—	NC
—	—	—	J17	—	NC
—	—	—	D12	—	NC

Table 1-5. Pin Assignments *(9 of 9)*

Pin Number					Pin Functions
CX28394 128-pin TQFP	CX28398 208-pin PQFP	CX28398 208-pin CABGA	CX28398 272-pin BGA	CX28395 318-pin BGA	
—	—	—	D10	—	NC
—	—	—	D9	—	NC
—	—	—	D7	—	NC
—	—	—	D5	—	NC

Figure 1-7. CX28394 Logic Diagram (Non-Multiplexed System Bus Mode)

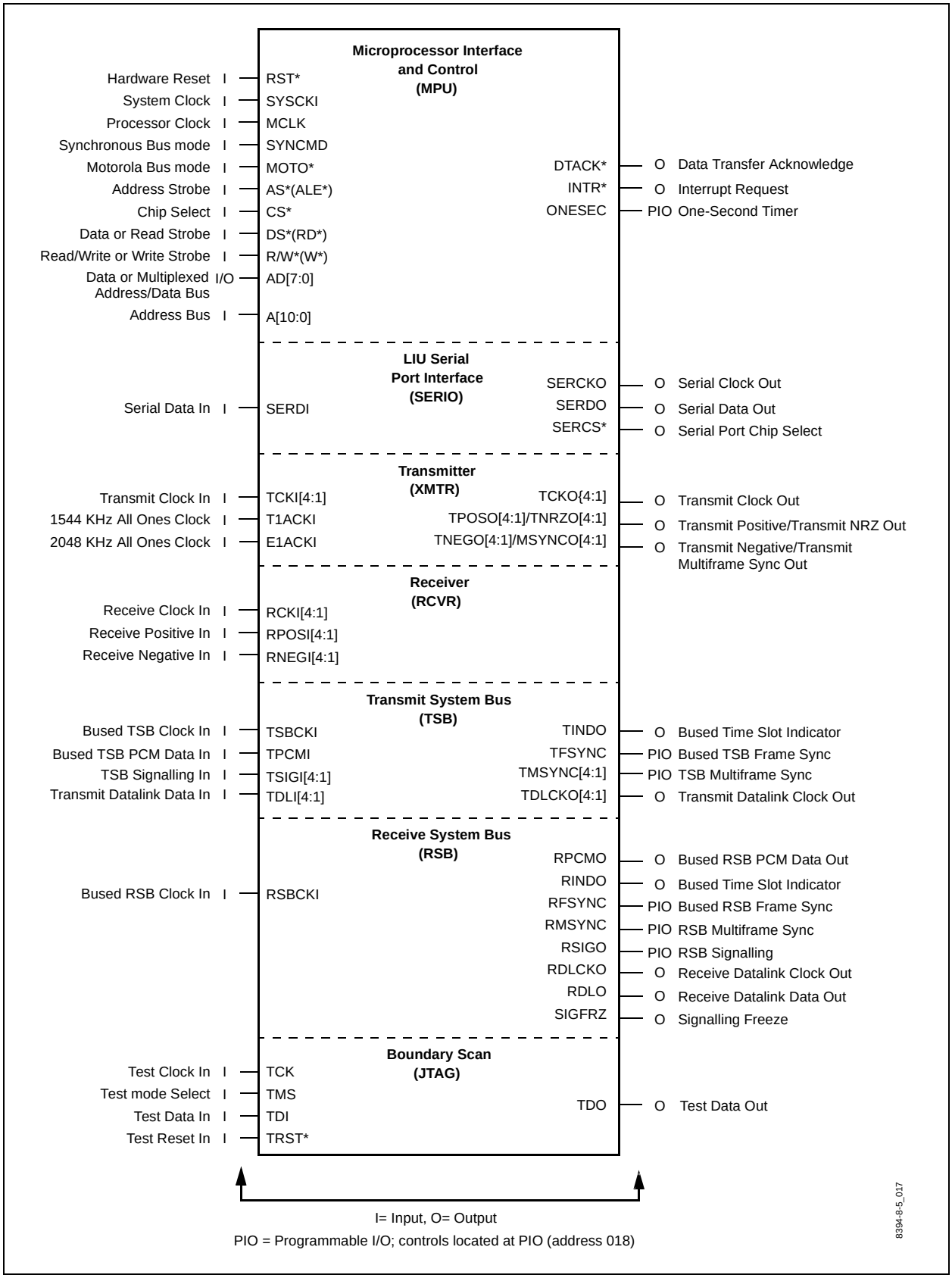


Figure 1-8. CX28394 Logic Diagram (Multiplexed System Bus Mode)

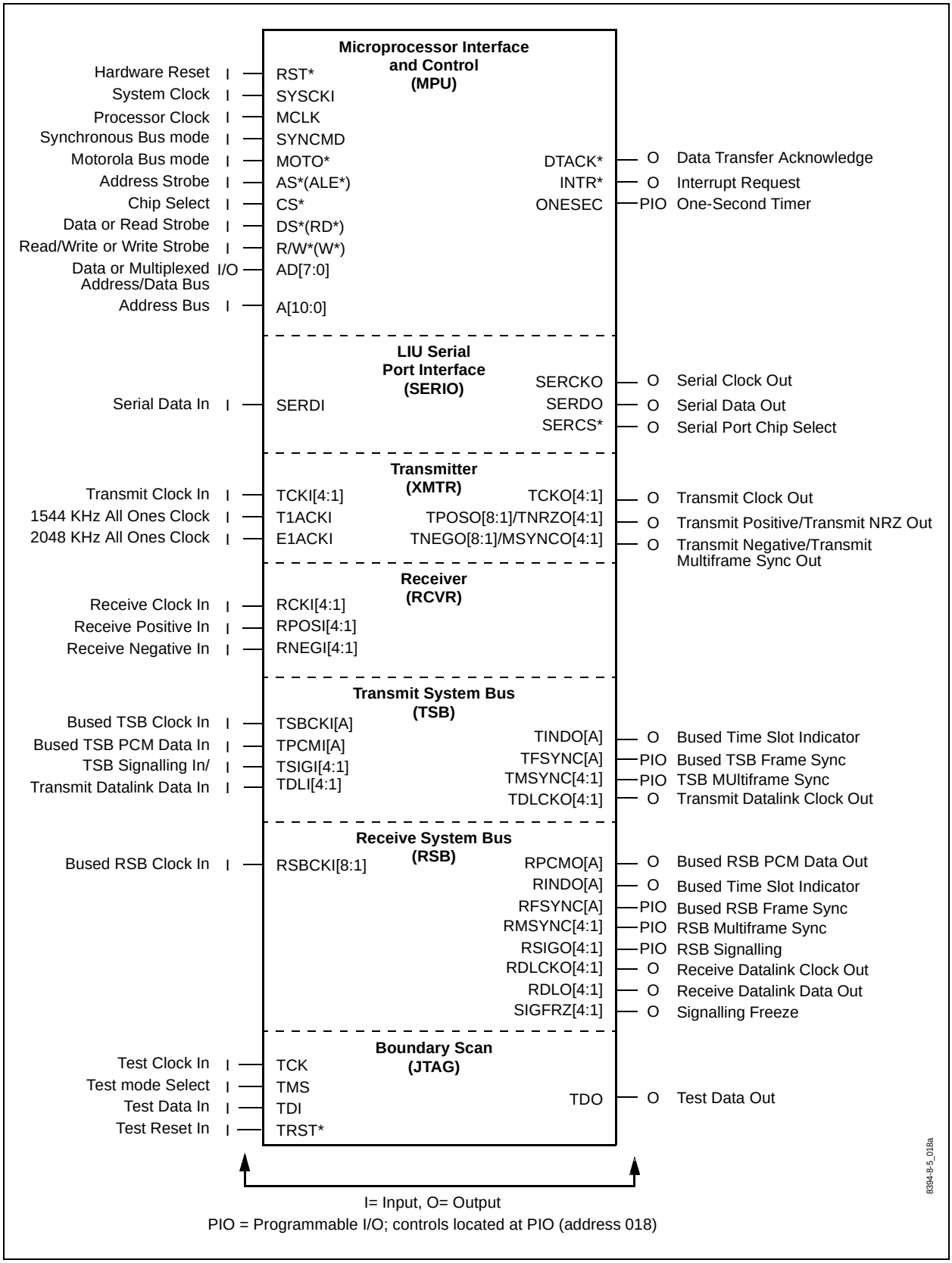


Figure 1-9. CX28398 Logic Diagram (Non-Multiplexed System Bus Mode)

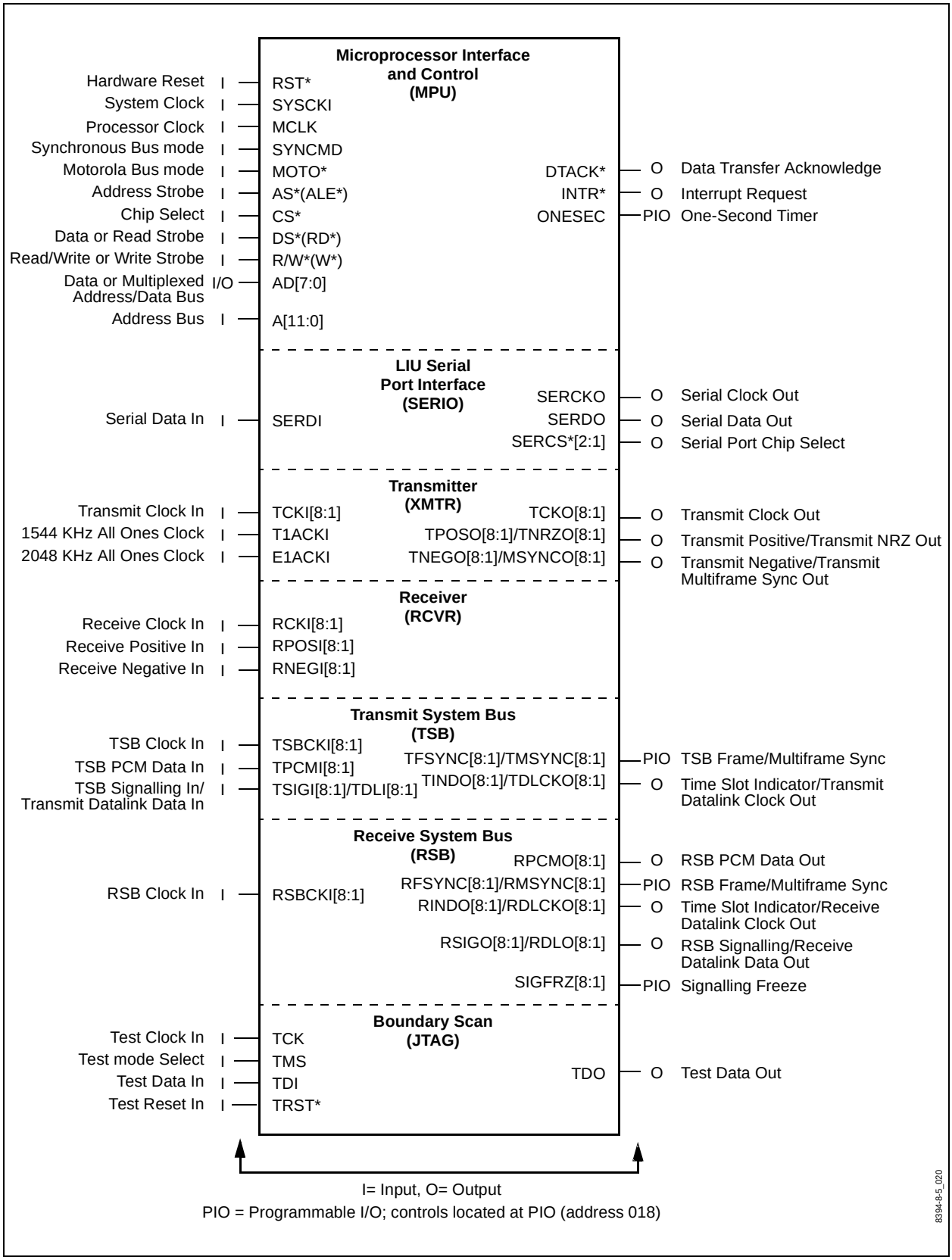


Figure 1-10. CX28398 Logic Diagram (Multiplexed System Bus Mode)

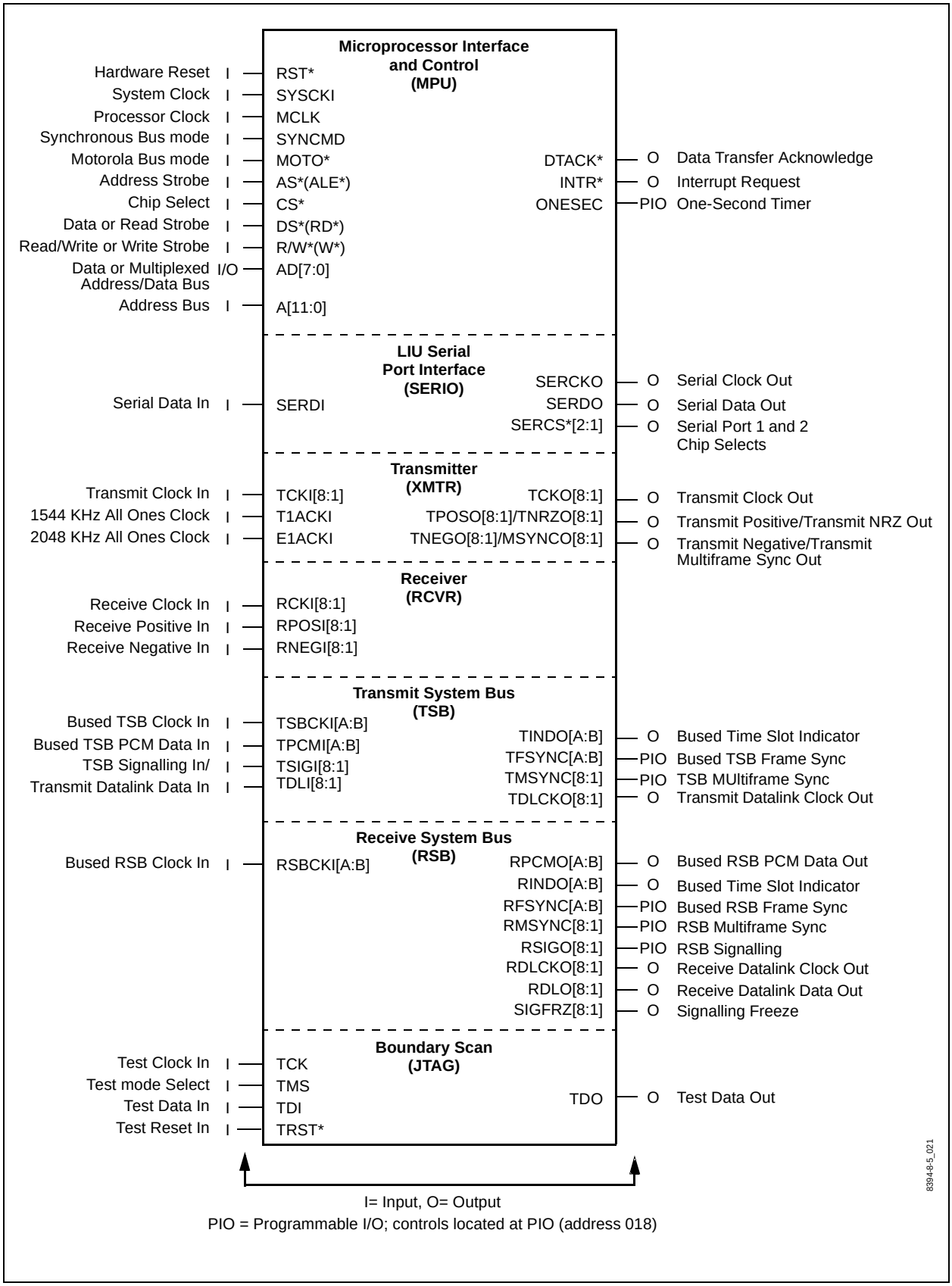


Figure 1-11. CX28395 Logic Diagram (Non-Multiplexed System Bus Mode)

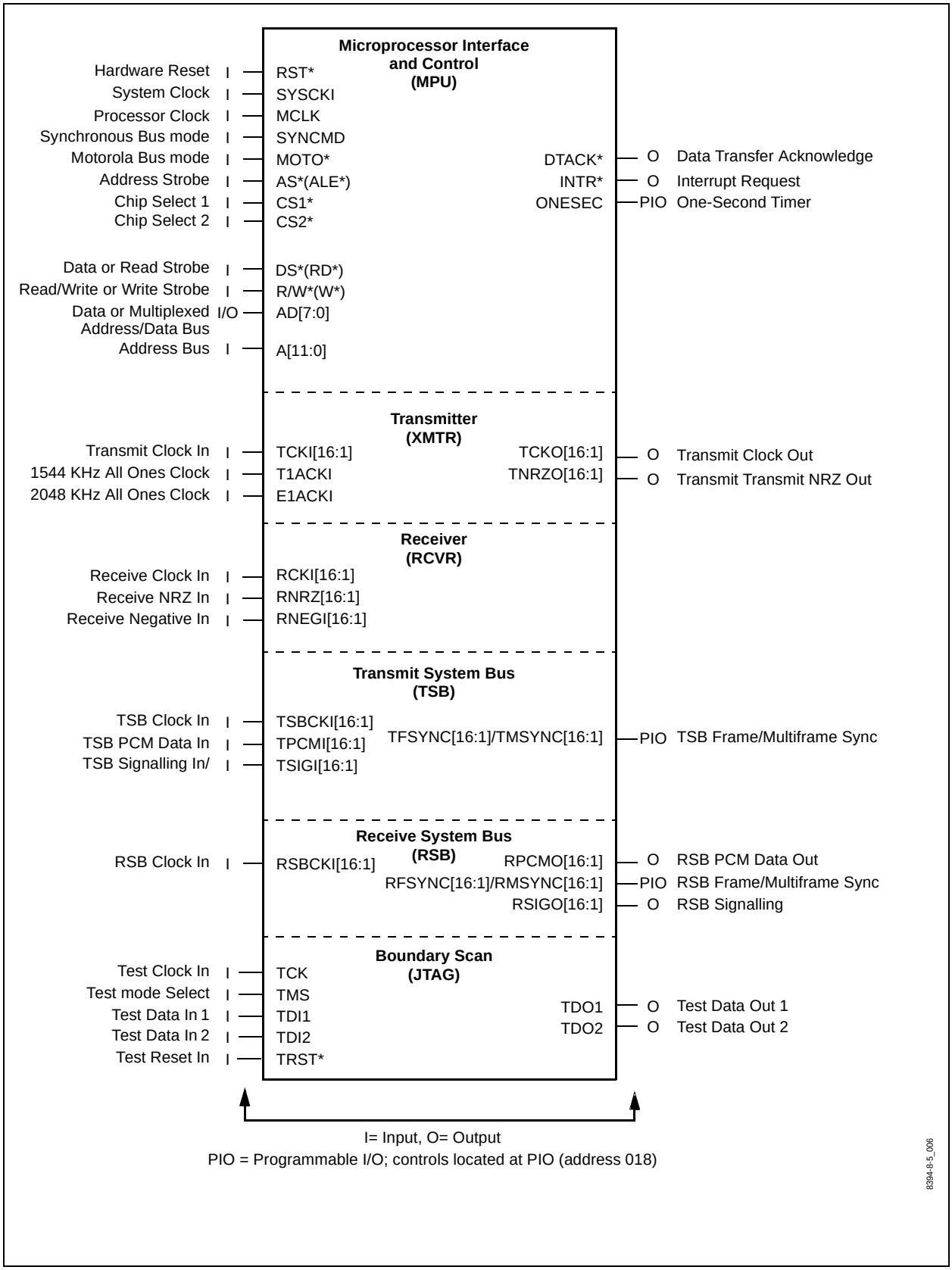


Figure 1-12. CX28395 Logic Diagram (Multiplexed System Bus Mode)

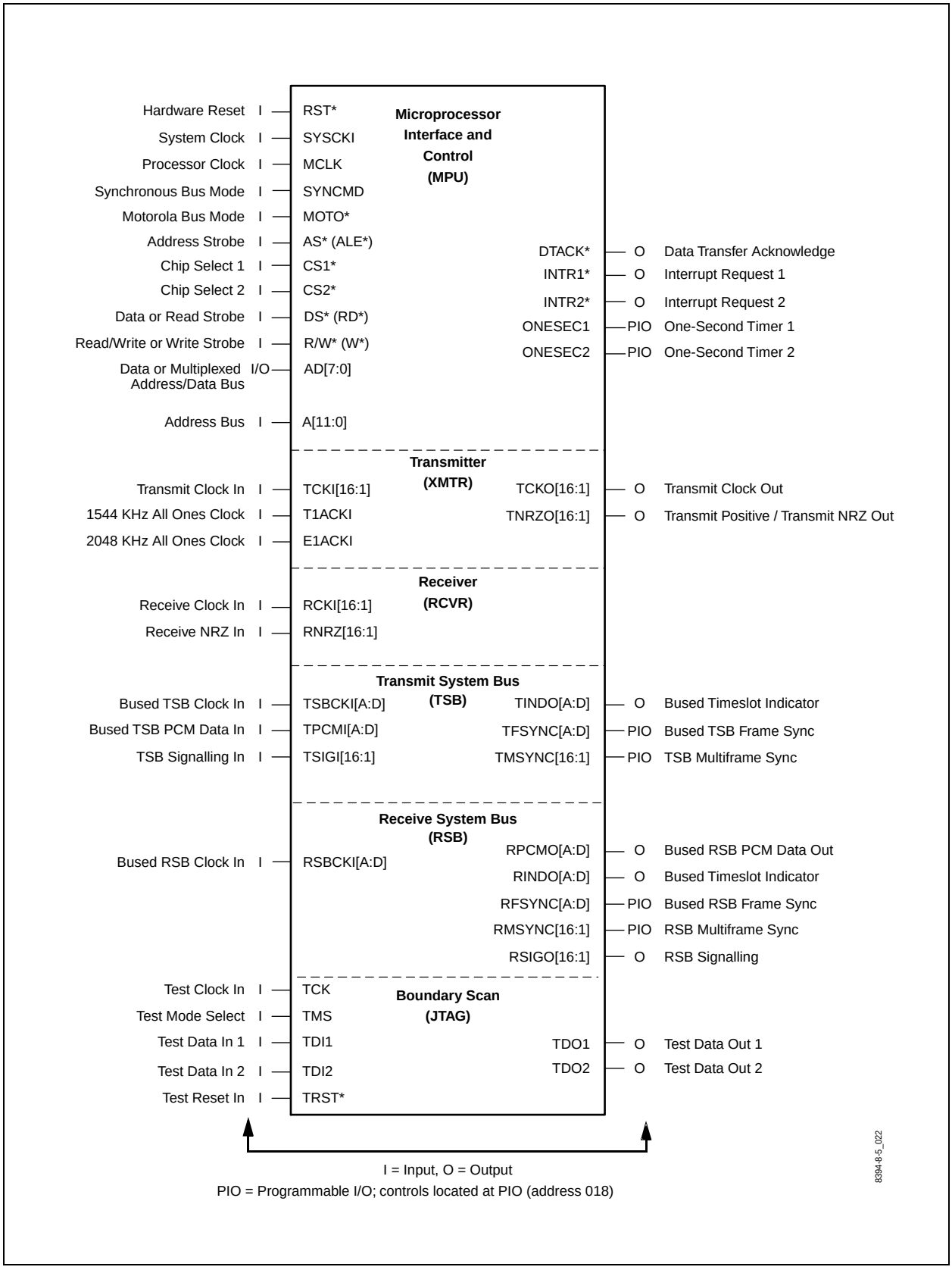


Table 1-6. Hardware Signal Definitions *(1 of 9)*

Pin Label	Signal Name	Device (1)	I/O	Definition
Microprocessor Interface (MPU)				
RST*	Hardware Reset	4, 5, 8	I	High-to-low-to-high cycle forces registers to their power-up state and all PIO pins to the input state. RST* is not mandatory since power-on reset circuit performs an identical function. RST* must remain asserted for a minimum of 2 processor clock cycles (MCLK or SYSCKI, depending on SYNCMD selection).
SYSCKI	System Clock	4, 5, 8	I	Required 32.768 MHz clock for internal use. Supplied from external source.
MCLK	Processor Clock	4, 5, 8	I	System applies MCLK in the range of 8–36 MHz for use with synchronous MPU applications. MCLK is used when SYNCMD = 1 and ignored when SYNCMD = 0.
SYNCMD	Sync mode	4, 5, 8	I	Selects synchronous or asynchronous read/write timing with respect to MCLK. Supports Intel- or Motorola-style buses: 0 = Asynchronous Bus; read and write latches are asynchronously controlled by CS*, DS*, and R/W* signals. 1 = Synchronous Bus; MCLK rising edge samples CS*, DS*, and R/W* to determine valid read/write cycle timing.
MOTO*	Motorola Bus Mode	4, 5, 8	I	Selects Intel- or Motorola-style microprocessor interface. DS*, R/W*, A[11:0], and AD[7:0] functions are affected. 0 = Motorola; AD[7:0] is data, A[11:0] is address, DS* is data strobe, and R/W* indicates read (high) or write (low) data direction. 1 = Intel; AD[7:0] is multiplexed address/data, A[7:0] is ignored, A[11:8] is address, DS* is read strobe (RD*), and R/W* is write strobe (WR*).
A[10:0]	Address Bus	4	I	Address used to identify a register for subsequent read/write data transfer cycle. In Motorola bus mode, all eleven address bits (A[10:0]) are valid. In Intel bus mode, only upper three bits (A[10:8]) are used.
A[11:0]	Address Bus	5, 8	I	Address used to identify a register for subsequent read/write data transfer cycle. In Motorola bus mode, all twelve address bits (A[11:0]) are valid. In Intel bus mode, only upper four bits (A[11:8]) are used.
AD[7:0]	Data Bus or Address Data	4, 5, 8	I/O	Multiplexed address/data (Intel) or data only(Motorola). Refer to MOTO* signal definition.
AS*(ALE)	Address Strobe	4, 5, 8	I	For all processor bus modes, AS* falling edge asynchronously latches address from A[11:0] (Motorola) or A[11:8], AD[7:0] (Intel) to identify one register for subsequent read/write data transfer cycle.
CS1*, CS2*	Chip Select	5	I	Active-low enables read/write decoder. Active high ends current read or write cycle and places data bus output in high impedance. CS1* is the chip select pin for framers 1 to 8, CS2* is the chip select for framers 9 to 16.

Table 1-6. Hardware Signal Definitions *(2 of 9)*

Pin Label	Signal Name	Device (1)	I/O	Definition
Microprocessor Interface (MPU) (Continued)				
CS*	Chip Select	4, 8	I	Active-low enables read/write decoder. Active high ends current read or write cycle and places data bus output in high impedance.
DS*(RD*)	Data Strobe or Read Strobe	4, 5, 8	I	Active-low read data strobe (RD*) for MOTO* = 1, or data strobe (DS*) for MOTO* = 0.
R/W*(WR*)	Read/Write Direction or Write Strobe	4, 5, 8	I	Active-low write data strobe (WR*) for MOTO* = 1, or data select (R/W*) for MOTO* = 0.
ONESEC	One Second Timer	4, 8	PIO	Controls or marks one-second interval used for status reporting. When input, the timer is aligned to ONESEC rising edge. When output, rising edge indicates start of each one-second interval.
ONESEC1 ONESEC2	One Second Timer	5	PIO	Controls or marks one-second interval used for status reporting. When input, the timer is aligned to ONESEC rising edge. When output, rising edge indicates start of each one-second interval. ONESEC1 is the one second timer for framers 1 to 8, ONESEC2 is the one second timer for framers 9 to 16.
INTR*	Interrupt Request	4, 8	O	Open drain active low output signifies one or more pending interrupt requests. INTR* goes to high-impedance state with weak (>50 kΩ) internal pullup resistance after processor has serviced all pending interrupt requests.
INTR1* INTR2*	Interrupt Request	5	O	Open drain active low output signifies one or more pending interrupt requests. INTRn* goes to high-impedance state with weak (>50kΩ) internal pullup resistance after processor has serviced all pending interrupt requests. INTR1* is the interrupt request for framers 1 to 8, INTR2* is the interrupt request for framers 9 to 16.
DTACK*	Data Transfer Acknowledge	4, 8	O	Open drain active low output signifies in-progress data transfer cycle. DTACK* remains asserted (low) for as long as AS* and CS* are both active-low.
DTACK1* DTACK2*	Data Transfer Acknowledge	5	O	Open drain active low output signifies in-progress data transfer cycle. DTACKn* remains asserted (low) for as long as AS* and CSn* are both active-low.

Table 1-6. Hardware Signal Definitions *(3 of 9)*

Pin Label	Signal Name	Device (1)	I/O	Definition
LIU Serial Interface				
SERDI	Serial Data Input	4, 8	I	Serial data input from an LIU is sampled on rising edge of SERCKO and written into Serial Data Register; addr 023.
SERCKO	Serial Clock	4, 8	O	Serial bit clock provided for transmitting and receiving serial LIU data on SERDI and SERDO. SERCKO frequency is 1.024 MHz or 8.192 MHz selectable.
SERDO	Serial Data Output	4, 8	O	Address and data is output to an LIU serially on SERDO. Data changes on falling edge of SERCKO.
SERCS*	Serial Chip Select	4	O	Chip select line used to select an LIU's serial port for communication. SERCS is controlled in Serial Configuration Register; addr 025.
SERCS1* SERCS2*	Serial Chip Selects	8	O	Chip select lines used to select an LIU's serial port for communication. SERCS1* and SERCS2* are independently controlled in Serial Configuration Register; addr 025.
Transmitter (XMTR)				
TCKI[4:1] TCKI[8:1] TCKI[16:1]	TX Clock Input	4 8 5	I	Primary TX line rate clocks for transmitter signals: TPOSO, TNEGO, TNRZO, MSYNCO, TDLI, and TDLCKO. If TSLIP is bypassed, TCKI also clocks TSB signals.
T1ACKI	T1 All Ones Clock	4, 5, 8	I	System optionally applies T1ACKI to use for T1 AIS transmission in case the selected primary transmit clock source fails. T1ACKI is either manually or automatically switched to replace TCKI (see [AISCLK; addr 075]). Systems without a T1 AIS clock should tie T1ACKI to ground.
E1ACKI	E1 All Ones Clock	4, 5, 8	I	System optionally applies E1ACKI to use for E1 AIS transmission in case the selected primary transmit clock source fails. E1ACKI is either manually or automatically switched to replace TCKI (see [AISCLK; addr 075]). Systems without an E1 AIS clock should tie E1ACKI to ground.
TPOSO[4:1] TPOSO[8:1]	TX Positive Rail Output	4 8	O	Line rate data output from ZCS encoder changes on rising edge of TCKO. Active-high marks transmission of a positive AMI pulse.
TNEGO[4:1] TNEGO[8:1]	TX Negative Rail Output	4 8	O	Line-rate data output from ZCS encoder changes on rising edge of TCKO. Active high marks transmission of a negative AMI pulse.
TDLI[4:1] TDLI[8:1]	TX Data Link Input	4 8	I	Selected time slot bits are sampled on TDLCKO falling edge for insertion into the transmit output stream during external data link applications.
TDLCKO[4:1] TDLCKO[8:1]	TX Data Link Clock	4 8	O	Gapped version of TCKI for external data link applications. TDLCKO high clock pulse coincides with low TCKI pulse interval during selected time slot bits, else TDLCKO low (see [DL3_TS; addr 015]).

Table 1-6. Hardware Signal Definitions (4 of 9)

Pin Label	Signal Name	Device (1)	I/O	Definition
Transmitter (XMTR) (Continued)				
TCKO[4:1] TCKO[8:1] TCKO[16:1]	TX Clock Output	4 8 5	O	Line rate clock. TCKO equals selected TCKI or T1ACKI (E1ACKI).
TNRZO[4:1] TNRZO[8:1] TNRZO[16:1]	TX Non Return to Zero Data	4 8 5	O	Line-rate data output from transmitter on rising edge of TCKO. TNRZO does not include ZCS encoded bipolar violations.
MSYNCO[4:1] MSYNCO[8:1] MSYNCO[16:1]	TX Multiframe Sync	4 8 5	O	Active high for one TCKI clock cycle to mark the first bit of TX multiframe coincident with TNRZO. Output on rising edge of TCKO.
Receiver (RCVR)				
RCKI[4:1] RCKI[8:1] RCKI[16:1]	RX Clock Input	4 8 5	I	Line rate clock samples RPOSI and RNEGI or RNRZ.
RNRZI[4:1] RNRZI[8:1] RNRZI[16:1]	RX Positive Rail Input	4 8 5	I	Line rate data input on rising edge of RCKI. Non-return to zero (NRZ) receive data.
RPOSI[4:1] RPOSI[8:1]	RX Positive Rail Input	4 8	I	Line rate data input on rising edge of RCKI. RPOSI and RNEGI levels are interpreted as received AMI pulses, encoded as follows: RPOSI / RNEGI / RX Pulse Polarity 0 / 0 / No pulse 0 / 1 / Negative AMI pulse 1 / 0 / Positive AMI pulse 1 / 1 / Invalid (decoded as a pulse) Unipolar. Non-return to zero (NRZ) data may be connected to RPOSI or RNEGI in which case the other input should be connected to ground. In this configuration RAMI [RCR0; addr 040] should be set to 1 (receive AMI line format) and DIS_LCV [RALM; addr 045] should be set to 1 (disable LCV counting and reporting).
RNEGI[4:1] RNEGI[8:1]	RX Negative Rail Input	4 8	I	Line rate data input on rising edge of RCKI. See RPOSI signal definition.
RDLO[4:1] RDLO[8:1]	RX Data Link Output	4 8	O	Line rate NRZ data output from receiver on falling edge of RCKI. All receive data is represented at the RDLO pin. However, selective RDLO bit positions are also marked by RDLCKO for external data link applications.
RDLCKO[4:1] RDLCKO[8:1]	RX Data Link Clock Output	4 8	O	Gapped version of RCKI for external data link applications. RDLCKO high clock pulse coincides with low RCKO pulse interval during selected time slot bits, otherwise RDLCKO is low (see Figure 2-4, *Receive External Data Link Waveforms*).

Table 1-6. Hardware Signal Definitions *(5 of 9)*

Pin Label	Signal Name	Device (1)	I/O	Definition
Transmit System Bus (TSB)				
TSBCKI[4:1] TSBCKI[8:1] TSBCKI[16:1] TSBCKI[A] TSBCKI[B] TSBCKI[C] TSBCKI[D}	TSB Clock Input Bused TSB Clock Inputs	4 8 5 4,5,8 5,8 5 5	I	Bit clock and I/O signal timing for TSB according to system bus mode (see [SBI_CR; addr 0D0]). System chooses from one of two different clocks to act as TSB clock source (see [CMUX; addr 01A]). Rising or falling edge clocks are independently configurable for data signals TPCMI, TSIGI, TINDO and sync signals TFSYNC and TMSYNC (see [TPCM_NEG and TSYN_NEG; addr 0D4]). When configured to operate at twice the data rate, TSB clock is internally divided by 2 before clocking TSB data signals.
TPCMI[4:1] TPCMI[8:1] TPCMI[16:1] TPCMI[A] TPCMI[B] TPCMI[C] TPCMI[D]	TSB Data Input Bused TSB Data Input	4 8 5 4,5,8 5,8 5 5	I	Serial data formatted into TSB frames consisting of DS0 channel time slots and optional F-bits. One group of 24 T1 time slots or 32 E1 time slots is selected from up to four available groups; data from the group is sampled by TSBCKI, then sent towards transmitter output. Time slots are routed through transmit slip buffer (see [TSLIPn; addr 140–17F]) according to TSLIP mode (see [TSBI; addr 0D4]). F-bits are taken from the start of each TSB frame or from within an embedded time slot (see [EMBED; addr 0D0]) and optionally inserted into the transmitter output (see [TFRM; addr 072] register).
TSIGI[4:1] TSIGI[8:1] TSIGI[16:1]	TSB Signaling Input	4 8 5	I	Serial data formatted into TSB frames containing ABCD signaling bits for each system bus time slot. Four bits of TSIGI time slot carry signaling state for each accompanying TPCMI time slot. Signaling state of every time slot is sampled during first frame of the TSB multiframe and then transferred into transmit signaling buffer [TSIGn; addr 120–13F].
TINDO[4:1] TINDO[8:1] TINDO[16:1] TINDO[A] TINDO[B] TINDO[C] TINDO[D]	TSB Time Slot Indicator Bused TSB Time Slot Indicator	4 8 5 4,5,8 5,8 5 5	O	Active-high output pulse marks selective transmit system bus time slots as programmed by SBCn [addr 0E0-0FF], TINDO occurs on TSBCKI rising or falling edges as selected by TPCM_NEG (see [TSBI; addr 0D4]).
TFSYNC[4:1] TFSYNC[8:1] TFSYNC[16:1] TFSYNC[A] TFSYNC[B] TFSYNC[C] TFSYNC[D]	TSB Frame Sync Bused TSB Frame Sync	4 8 5 4,5,8 5,8 5 5	PIO	Input or output TSB frame sync (see [TFSYNC_IO; addr 018]). TFSYNC output is active high for one TSB clock cycle at programmed offset bit location (see [TSYNC_BIT; addr 0D5]), marking offset bit position within each TSB frame and repeating once every 125 µs. When transmit framer is also enabled, TSB timebase and TFSYNC output frame alignment are established by transmit framer's examination of TPCMI serial data input. When TFSYNC is programmed as an input, the low-to-high signal transition is detected and is used to align TSB timebase to programmed offset bit value. TSB timebase flywheels at 125 µs frame interval after the last TFSYNC is applied.

Table 1-6. Hardware Signal Definitions *(6 of 9)*

Pin Label	Signal Name	Device (1)	I/O	Definition
Transmit System Bus (TSB) (Continued)				
TMSYNC[4:1] TMSYNC[8:1] TMSYNC[16:1]	TSB Multiframe Sync	4 8 5	PIO	Input or output TSB multiframe sync (see [TMSYNC_IO; addr 018]). TMSYNC output is active high for one TSB clock cycle at programmed offset bit location (see [TSYNC_BIT; addr 0D5]), marking offset bit position within each TSB multiframe and repeating once every 6 ms coincident with TFSYNC. When transmit framer is also enabled, TSB timebase and TMSYNC output multiframe alignment are established by transmit framer's examination of TPCMI serial data input. When TMSYNC is programmed as an input, the low-to-high signal transition is detected and is used to align TSB timebase to programmed offset bit value and first frame of the multiframe. TSB timebase flywheels at 6 ms multiframe intervals after the last TMSYNC is applied. If system bus applies TMSYNC input, TFSYNC input is not needed.
Receive Systetm Bus (RSB)				
RSBCKI[4:1] RSBCKI[8:1] RSBCKI[16:1] RSBCKI[A] RSBCKI[B]} RSBCKI[C]} RSBCKI[D]}	RSB Clock Input Bused RSB Data Input	4 8 5 4,5,8 5,8 5 5	I	Bit clock and I/O signal timing for RSB according to system bus mode (see [SBI_CR; addr 0D0]). System chooses from one of two different clocks to act as RSB clock source (see [CMUX; addr 01A]). Rising or falling edge clocks are independently configurable for data signals RPCMO, RSIGO, RINDO and sync signals RFSYNC, RMSYNC (see [RPCM_NEG and RSYN_NEG; addr 0D1]). When configured to operate at twice the data rate, RSB clock is internally divided by 2 before clocking RSB data signals.
RPCMO[4:1] RPCMO[8:1] RPCMO[16:1] RPCMO[A] RPCMO[B] RPCMO[C] RPCMO[D]	RSB Data Output Bused RSB Data Output	4 8 5 4,5,8 5,8 5 5	O	Serial data formatted into RSB frames consisting of DS0 channel time slots, optional F-bits and optional ABCD signaling. Time slots are routed through receive slip buffer (see [RSLIPn; addr 1C0–1FF]) according to RSLIP mode (see [RSBI; addr 0D1]). Data for each output time slot is assigned sequentially from received time slot data according to system bus channel programming (see [ASSIGN; addr 0E0–0FF]). F-bits are output at the start of each RSB frame or at the embedded time slot location (see [EMBED; addr 0D0]). ABCD signaling is optionally inserted on a per-channel basis (see [INSERT; addr 0E0–0FF]) from the local signaling buffer (see [RLOCAL; addr 180–19F]) or from the receive signaling buffer [RSIGn; addr 1A0–1BF]. When enabled, robbed bit signaling or CAS reinsertion is performed according to T1/E1 mode: The eighth time slot bit of every sixth T1 frame is replaced, or the 4-bit signaling value in the E1 time slot 16 is replaced.
RINDO[4:1] RINDO[8:1] RINDO[A] RINDO[B] RINDO[C] RINDO[D]	RSB Time Slot Indicator Bused RSB Time Slot Indicator	4 8 4,5,8 5,8 5 5	O	Active high output pulse marks selective receive system bus time slots as programmed by SBCn [addr 0E0-0FF]. RINDO occurs on RSBCKI rising or falling edges as selected by RPCM_NEG (see [RSBI; addr 0D1]). Only available in Multiplexed System Bus mode on CX28395 (see [FCR; addr 080]).

Table 1-6. Hardware Signal Definitions *(7 of 9)*

Pin Label	Signal Name	Device (1)	I/O	Definition
Receive Systetm Bus (RSB) (Continued)				
RSIGO[4:1] RSIGO[8:1] RSIGO[16:1]	RSB Signaling Output	4 8 5	O	Serial data formatted into RSB frames consisting of ABCD signaling bits for each system bus time slot. Four bits of RSIGO time slot carry signaling state for each accompanying RPCMO time slot. Local or through signaling bits are output in every frame for each time slot and updated once per RSB multiframe, regardless of per-channel RPCMO signaling reinsertion.
RFSYNC[4:1] RFSYNC[8:1] RFSYNC[16:1] RFSYNC[A] RFSYNC[B] RFSYNC[C] RFSYNC[D]	RSB Frame Sync Bused RSB Frame Sync	4 8 5 4,8,5 5,8 5 5	PIO	Input or output RSB frame sync (see [RFSYNC_IO; addr 018]). RFSYNC output is active high for one RSB clock cycle at programmed offset bit location (see [RSYNC_BIT; addr 0D2]), marking offset bit within each RSB frame and repeating once every 125 µs. RSB timebase and RFSYNC output frame alignment begins at an arbitrary position and changes alignment according to RSLIP mode (see [RSBI; addr 0D1]). When RFSYNC is programmed as an input, the low-to-high signal transition is detected and used to align RSB timebase to the programmed offset. RSB timebase flywheels at 125 µs frame interval after the last RFSYNC is applied.
RMSYNC[4:1] RMSYNC[8:1] RMSYNC[16:1]	RSB Multiframe Sync	4 8 5	PIO	Input or output RSB multiframe sync (see [RMSYNC_IO; addr 018]). RMSYNC output is active high for one RSB clock cycle at programmed offset bit location (see [RSYNC_BIT; addr 0D2]), marking offset bit within each RSB multiframe and repeating once every 6 ms coincident with RFSYNC. RSB timebase and RMSYNC output multiframe alignment begins at an arbitrary position and changes alignment according to RSLIP mode (see [RSBI; addr 0D1]). When RMSYNC is programmed as an input, the low-to-high signal transition is detected and is used to align the RSB timebase to programmed offset and first frame of the multiframe. RSB timebase flywheels at 6 ms multiframe interval after the last RMSYNC is applied.
SIGFRZ[4:1] SIGFRZ[8:1]	Signaling Freeze	4 8	O	Active high indicates that signaling bit updates are suspended for both receive signaling buffer [RSIGn; addr 1A0–1BF] and stack [STACK; addr 0DA] register. SIGFRZ is clocked by RSB clock, goes high coincident with receive loss of frame alignment (see RLOF; addr 047) and returns low 6–9 ms after recovery of frame alignment.

Table 1-6. Hardware Signal Definitions (8 of 9)

Pin Label	Signal Name	Device (1)	I/O	Definition
Joint Test Access Group (JTAG)				
TCK	JTAG Clock	4, 5, 8	I	Clock input samples TDI on rising edge and outputs TDO on falling edge.
TDI1, TDI2	JTAG Test Data Input	5	I	Test data input per IEEE Std 1149.1-1990. Used for loading all serial instructions and data into internal test logic. Sampled on the rising edge of TCK. TDI can be left unconnected if it is not being used because it is pulled up internally. TDI1 is the test data input for framers 1 to 8, TDI2 is the test data input for framers 9 to 16.
TDI	JTAG Test Data Input	4, 8	I	Test data input per IEEE Std 1149.1-1990. Used for loading all serial instructions and data into internal test logic. Sampled on the rising edge of TCK. TDI can be left unconnected if it is not being used because it is pulled up internally.
TMS	JTAG Test mode Select	4, 5, 8	I	Active low test mode select input per IEEE Std 1149.1-1990. Internally pulled-up input signal used to control the test-logic state machine. Sampled on the rising edge of TCK. TMS can be left unconnected if it is not being used because it is pulled up internally.
TDO	JTAG Test Data Output	4, 8	O	Test data output per IEEE Std 1149.1-1990. TDO is a three-state output used for reading all serial configuration and test data from internal test logic. Updated on the falling edge of TCK.
TDO1, TDO2	JTAG Test Data Output	5	O	Test data output per IEEE Std, 1149.1-1990. TDO is a three-state output used for reading all serial configuration and test data from internal test logic. Updated on the falling edge of TCK. TDO1 is the test data output for framers1 to 8, TDO2 is the test data output for framers 9 to 16.
TRST*	JTAG Reset	4, 5, 8	I	Active low input to initialize Tap Controller.
Power Supply				
VDD	Power	4, 5, 8	I	+3.3 Vdc ±5%.
VSS	Ground	4, 5, 8	I	0 Vdc.
VGG	High Voltage Power	4, 5, 8	I	+3.3 Vdc ±5%. Connect to +5 Vdc ±5% to ensure 5 V tolerance in applications which include 5 V logic driving signals.

Table 1-6. Hardware Signal Definitions *(9 of 9)*

Pin Label	Signal Name	Device (1)	I/O	Definition
Test				
TSTO[16:1]	Test Output	5	O	Test output. Leave disconnected for normal operation.
TSTI[16:1]	Test Input	5	I	Test input. Connect through 50k ohm pull-up resistor to VDD for normal operation.

NOTE(S):

(1) 4 = CX28394
5 = CX28395
8 = CX28398

1. All RSB and TSB outputs can be placed in high-impedance state (see SBI_OE; addr 0D0).
2. I = Input, O = Output
3. PIO = Programmable I/O; controls located at address 018.
4. Multiple signal names show mutually exclusive pin functions.

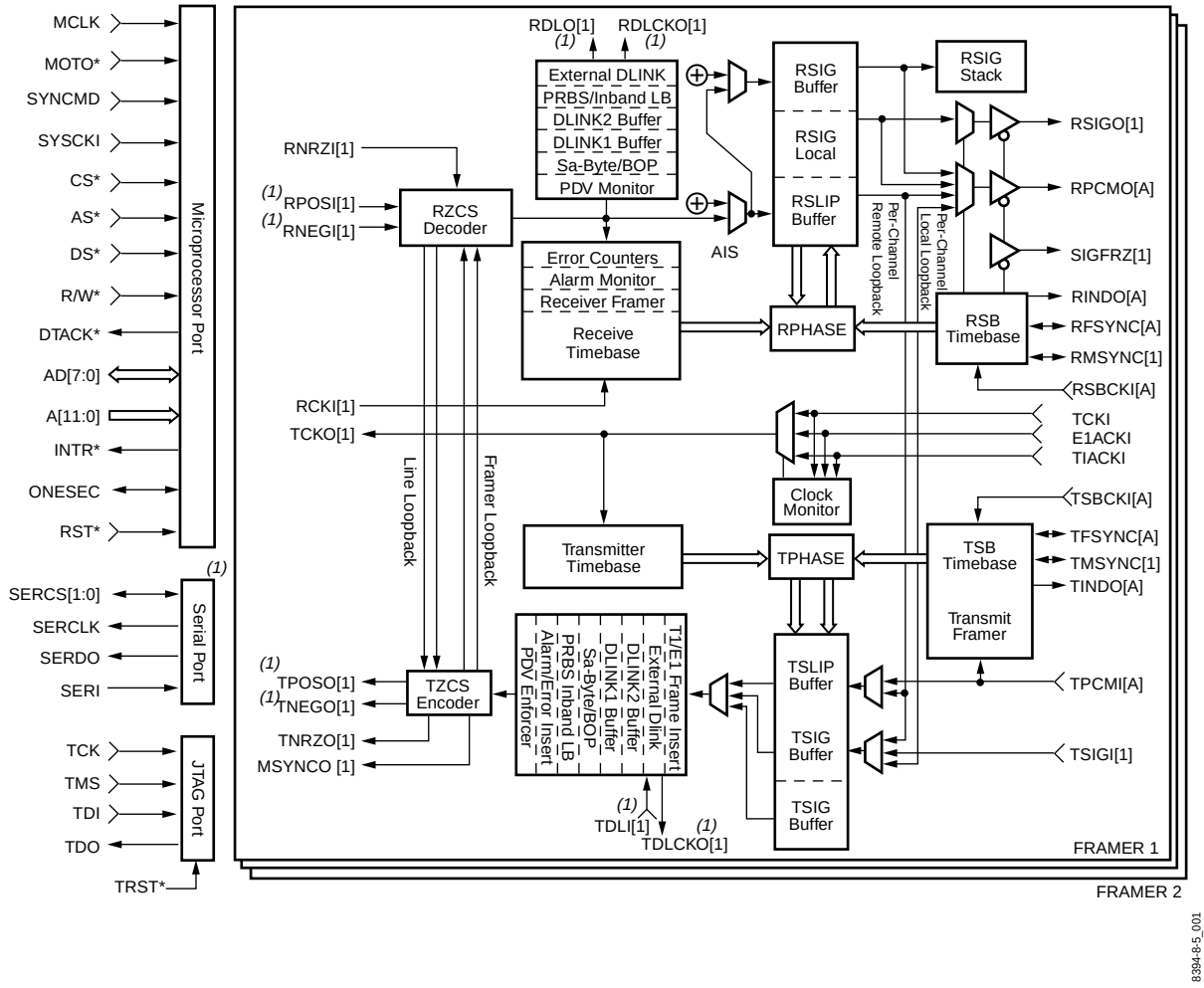
2.0 Circuit Description

2.1 Functional Block Diagram

Figures 2-1 and 2-2 illustrate detailed framer block diagrams for non-multiplexed and multiplexed system bus modes. To show the details of these circuits, individual block diagrams of the functions listed below have been created and are placed, along with descriptions, throughout this section:

- Receiver (RCVR)
- Receive System Bus (RSB)
- Transmit System Bus (TSB)
- Transmitter (XMTR)
- Microprocessor Interface (MPU)
- Joint Test Access Group Port (JTAG)
- Serial Port (SERIO)

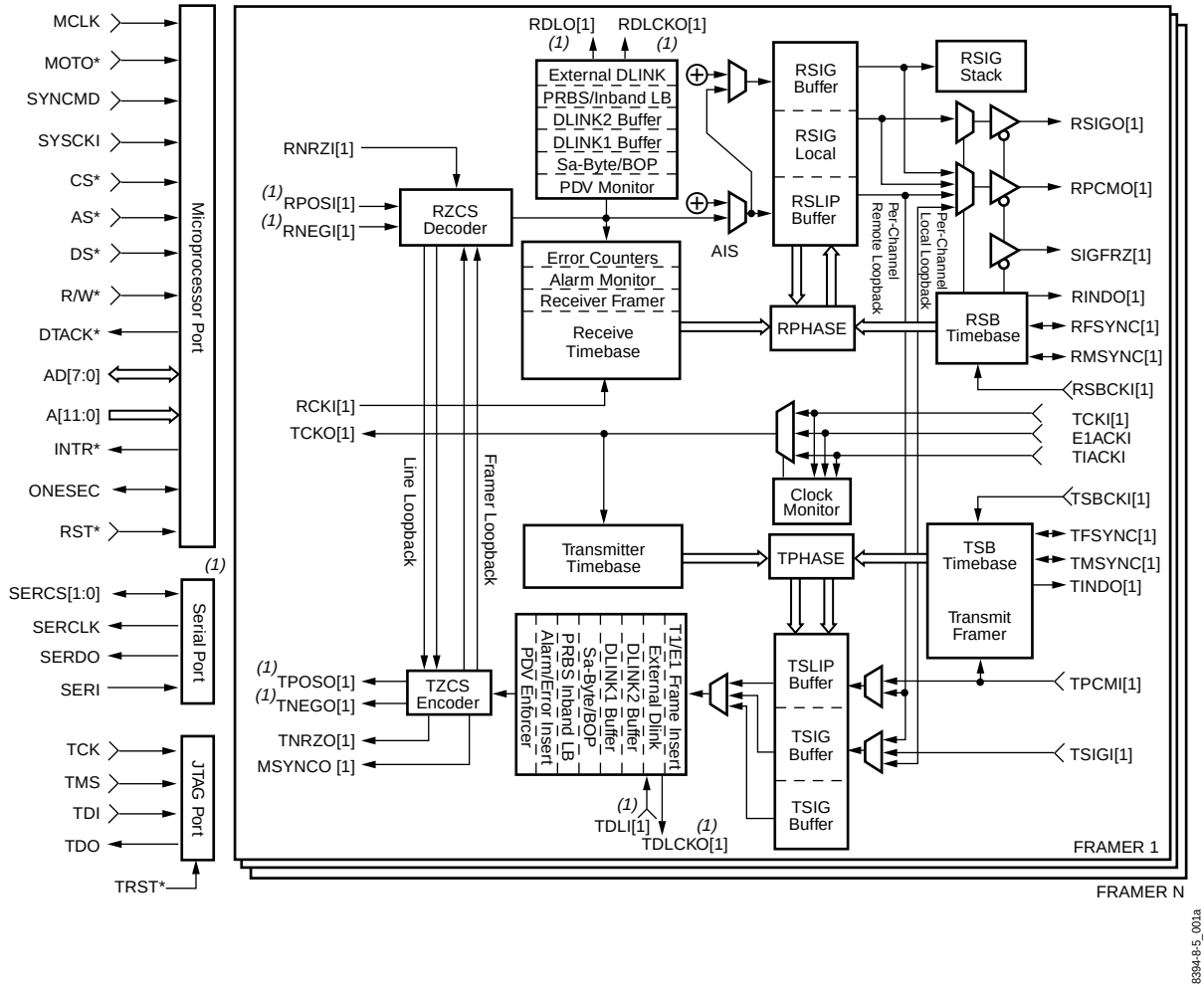
Figure 2-1. Detailed Framer Block Diagram (Multiplexed System Bus Mode)



NOTE(S):

(1) Not available on CX28395.

Figure 2-2. Detailed Framer Block Diagram (Non-multiplexed System Bus Mode)



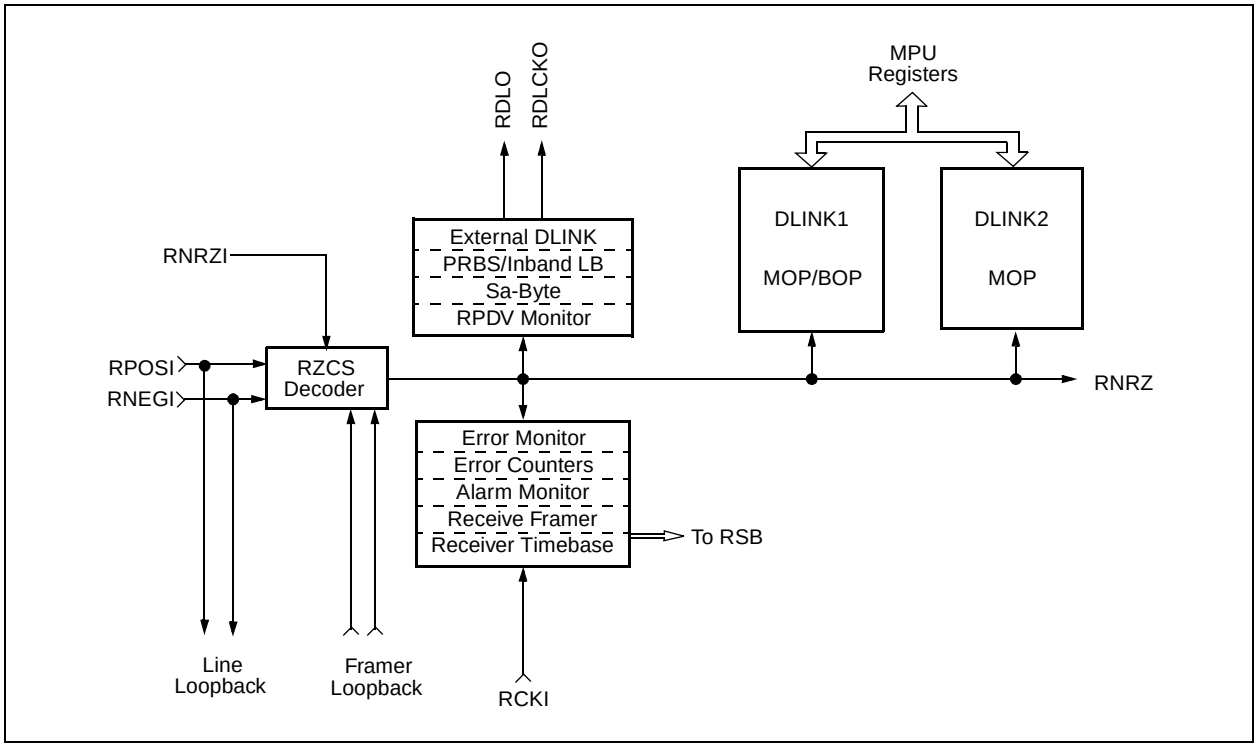
NOTE(S):

(1) Not available on CX28395.

2.2 Receiver

The Receiver (RCVR) inputs single rail NRZ data or decodes positive and negative rail NRZ data into single rail NRZ data. The RCVR, illustrated in Figure 2-3, consists of the following elements: Receive Zero Code Suppression (RZCS) Decoder, In-Band Loopback Code Detector, Error Counters, Error Monitor, Alarm Monitor, Test Pattern Receiver, Receive Framer, External Receive Data Link, and Receive Data Links.

Figure 2-3. RCVR Diagram



2.2.1 ZCS Decoder

The Receive Zero Code Suppression (RZCS) decoder is applicable only to the CX28394 and CX28398. The decoder decodes the dual rail data (bipolar) into single rail data (unipolar). The Receive AMI bit (RAMI) in the Receiver Configuration register [RCR0; addr 040] controls whether the received signal is B8ZS/HDB3 decoded, depending on T1/E1N [addr 001] line rate selection, or if the RZCS decoder is bypassed. If the line code is unknown, the ZCSUB bit in Receive Line Code Status [RSTAT; addr 021] indicates the RPOSI/RNEGI input received one or more B8ZS/HDB3 substitution patterns. If the line code is B8ZS/HDB3-encoded, the RZCS bit in RCR0 should be set to keep the LCV counter from counting BPVs that are part of the B8ZS/HDB3 code.

2.2.2 In-Band Loopback Code Detection

The in-band loopback code detector circuitry detects receive data with in-band codes of configurable value and length. These codes can be used to request loopback of terminal equipment signals or other user specified applications. The two codes are referred to as loopback-activate and loopback-deactivate, although the detectors need not be used only for loopback codes. Generally, any repeating 1–7 bit pattern can be selected. The loopback application is described in Section 9.3.1 of ANSI T1.403-1995. The loopback activate code is set in the Loopback Activate Code Pattern [LBA; addr 043]. The loopback deactivate code is set in the Loopback Deactivate Code Pattern [LBD; addr 044].

The sequence length for the loopback activate and deactivate codes can be programmed for 4, 5, 6, or 7 bits by setting the code length bits of the Receive Loopback Code Detector Configuration register [RLB; addr 042]. Shorter codes can be programmed by repeating the expected pattern (e.g. 3+3 bit code programmed as 6-bit code).

```
T1 In-Band Loopback Codes
     Activate 00001
     Deactivate 001
```

When a loopback code is detected, the LOOPUP or LOOPDN status bit is set in Alarm 2 register [ALM2; addr 048], and the corresponding LOOPUP or LOOPDN bit in Alarm 2 Interrupt Status register (ISR6; addr 005] is set. The loopback detection interrupt can be enabled using the Alarm 2 Interrupt Enable register [IER6; addr 00D]. When enabled, a loop-up or loop-down code detection causes the Alarm 2 Interrupt bit [ALARM2] to be set in the Interrupt Request register [IRR; addr 003] and generates an interrupt. Since loopbacks are not automatically initiated, the processor must intercept and interpret the interrupt status condition to determine when it must enable or disable the loopback control mechanism (e.g., LLOOP; addr 014).

2.2.3 Error Counters

The following Performance Monitoring (PM) counters are available in the RCVR:

- Framing Bit Errors (FERR)
- CRC Errors (CERR)
- Line Code Violations (LCV)
- Far End Block Errors (FEBE)

All PM count registers are reset on read unless LATCH_CNT is set in the Alarm/Error/Counter Latch Configuration register [LATCH; addr 046]. LATCH_CNT enables the one-second latching of counts coincident with the one-second timer interrupt [ISR6; addr 005]. One-second latching of PM counts is required if AUTO_PRM responses are enabled. All PM counters can be disabled during RLOF, RLOS, and RAIS, using the STOP_CNT bit in the LATCH register.

Note that if STOP_CNT is negated, error monitoring during RLOF conditions will detect FERR, CERR, and FEBE according to the last known frame alignment.

2.2.3.1 Frame Bit Error Counter

The 12-bit Framing Bit Error Counter [FERR; addr 050 and 051] increments every time a receive Ft, Fs, T1DM, FPS, or FAS error is detected. Fs (T1) and NFAS (E1) errors can be included in the FERR count by setting FS_NFAS in Receive Alarm Signal Configuration [RALM; addr 045]. An interrupt is available to indicate that the FERR counter overflowed in the Counter Overflow Interrupt Status register [ISR4; addr 007].

2.2.3.2 CRC Error Counter

The 10-bit Cyclic Redundancy Check Error Counter [CERR; addr 052 and 053] increments each time a receive CRC4 (E1) or CRC6 (T1) error is detected. An interrupt is available to indicate that CERR counter overflowed in ISR4.

2.2.3.3 LCV Error Counter

The 16-bit Line Code Violation Error Counter [LCV; addr 054 and 055] increments each time a receive Bipolar Violation (BPV)—not including line coding—is detected. The LCV count can include EXZ if EXZ_LCV in the Receive Alarm Signal Configuration register [RALM; addr 045] is set. EXZ can be configured [RZCS; addr 040] to be 8 or 16 successive zeros, following a one. An interrupt is available to indicate that the LCV counter overflowed in ISR4.

2.2.3.4 FEBE Counter

The 10-bit Far End Block Error (FEBE) counter [FEBE; addr 056 and 057] increments every time the RCVR encounters an E1 far-end block error. An interrupt is available to indicate that the FEBE counter overflowed in ISR4.

2.2.4 Error Monitor

The following signal errors are detected in the RCVR:

- Frame Bit Error (FERR)
- MFAS Error (MERR)
- CAS Error (SERR)
- CRC Error (CERR)
- Pulse Density Violation (PDV)

Each error type has an interrupt enable bit that enables an interrupt to occur marking the event, and an interrupt register bit that is read by the interrupt service routine to determine which event caused the interrupt. All error status registers are reset on read unless the LATCH_ERR bit is set in the Alarm/Error/Counter Latch Configuration register [LATCH; addr 046]. LATCH_ERR enables the one-second latching of alarms coincident with the one-second timer interrupt [ISR6; addr 005]. With LATCH_ERR enabled, any error detected during the one second interval is latched and held during the following one-second interval. LATCH_ERR allows the processor to gather error statistics based on the one-second interval.

2.2.4.1 Frame Bit Error

FERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. FERR indicates that one or more Ft/Fs/FPS frame-bit errors or FAS-pattern errors occurred since the last time the interrupt status was read. The FERR type is determined by the receive framer's configuration [CR0; address 001].

2.2.4.2 MFAS Error

When CRC4 framing is enabled, MERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. MERR is applicable only in E1 mode, and indicates that one or more MFAS pattern errors occurred since the interrupt status was last read.

2.2.4.3 CAS Error

When CAS framing is enabled, SERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. SERR is only applicable in E1 mode, and indicates that one or more errors were received in the TS16 Multiframe Alignment Signal (MAS) since the interrupt status was last read.

2.2.4.4 CRC Error

CERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. CERR is only applicable in T1 ESF and E1 MFAS modes, and indicates that one or more bit errors were found in the CRC4/CRC6 pattern block since the interrupt status was last read.

2.2.4.5 Pulse Density Violation

PDV is reported when the receive signal does not meet the pulse density requirements of ANSI T1.403-1995 (Section 5.6). A PDV is declared when more than 15 consecutive zeros or the average ones density falls below 12.5%. RPDV is reported for the receive direction in the Alarm 1 Interrupt Status register [ISR7; addr 004].

2.2.5 Alarm Monitor

The following signal alarms are detected in the RCVR:

- Loss Of Frame (LOF)
- Loss Of Signal (LOS)
- Receive Analog Loss Of Signal (RALOS)
- Alarm Indication Signal (AIS)
- Remote Alarm Indication (RAI) or Yellow Alarm (YEL)
- Multiframe Yellow Alarm (MYEL)
- Severely Errored Frame (SEF)
- Change Of Frame Alignment (COFA)
- Multiframe AIS (MAIS)

Each alarm has the following: a status register bit that reports the real-time status of the event; an interrupt enable bit that enables an interrupt to mark the event; and an interrupt register bit read by the interrupt service routine to identify the event that caused the interrupt. All alarm status registers are reset on read unless the LATCH_ALM bit is set in the Alarm/Error/Counter Latch Configuration register [LATCH; addr 046]. LATCH_ALM enables the one-second latching of alarms coincident with the one-second timer interrupt [ISR6; addr 005]. With LATCH_ALM enabled, any alarm detected during the one-second interval is latched and held during the following one-second interval.

2.2.5.1 Loss of Frame

Receive Loss Of Frame (RLOF) is declared when the receive data stream does not meet the framing criteria specified in the Receiver Configuration register [RCR0; addr 040].

If the line rate is E1 [T1/E1N; addr 001], RLOF is the logically OR'ed status of FAS, MFAS, and CAS alignment. These alignments, FRED, MRED and SRED, respectively, are available separately in the Alarm 3 Status register [ALM3; addr 049]. Once RLOF is declared the LOF[1:0] bits in ALM3 report the reason for E1 loss of frame alignment. In T1 mode, RLOF is equal to FRED.

The RLOF real-time status is available in Alarm 1 Status register [ALM1; addr 047], and the interrupt status is set in the Alarm 1 Interrupt Status register [ISR7; addr 004]. The RLOF interrupt is enabled by setting RLOF in the Alarm 1 Interrupt Enable register [IER7; addr 00C].

An FRED count [FRED[3:0]; addr 05A] is also available in the SEF/LOF/COFA Alarm Counter [AERR; addr 05A]. An interrupt in Counter Overflow Interrupt Status [ISR4; addr 007] indicates that the FRED counter overflowed.

While T1 framing mode is enabled, the RLOF status and RLOF interrupt status are integrated over 2.0 to 2.5 seconds if the RLOF_INTEG bit is set in the Receive Alarm Signal Configuration register [RALM; addr 045]. The FRED count is unaffected by RLOF_INTEG.

2.2.5.2 Loss of Signal

If the line rate is T1, the criteria for Receive Loss Of Signal (RLOS) is 100 contiguous zeros (consistent with the standard requirement of 175 ±75 zeros). If the line rate is E1, the criteria for RLOS is 32 contiguous zeros. RLOS is cleared upon detecting an average pulse density of at least 12.5% (occurring during a period of 175 ± 75 bits starting with the receipt of a pulse, and where no occurrences of 100/32 contiguous zeros are detected). The RLOS real-time status is available in ALM1, and the interrupt is available in ISR7. The XMTR can be configured to automatically generate an Alarm Indication Signal (AIS) in the transmit direction when RLOS is declared (see AUTO_AIS [TALM; addr 075]).

2.2.5.3 Receive Analog Loss of Signal

RALOS [ALM1; addr 047] can be configured to report loss of receive clock (RCKI) or loss of receive signal [RLOS; addr 047] for 1 msec depending on the RALOS configuration bit [RAL_CON; addr 020]. RALOS status is provided for compatibility with ANSI T1.431 loss of signal detection requirements; and works in conjunction with LIUs which detect loss of signal if the received signal level falls below a certain threshold and which have a signal ‘squelch’ feature. If RAL_CON is set for loss of signal, RALOS indicates that all zeros have been received for at least 1 msec (RLOS is active for 1 msec). If RAL_CON is set for loss of clock, RALOS becomes active (1) if the receive clock on the RCKI pin is not present, and inactive (0) if the clock is present.

2.2.5.4 Alarm Indication Signal

If the line rate is T1 [T1/E1N; addr 001], the criteria for Receive Alarm Indication Signal (RAIS) is the reception of four or fewer zeros in a period of 3 ms (4632 bits) and assertion of RLOF. If the line rate is E1, RAIS is set if two consecutive double frames each contain two or fewer zeros out of 512 bits and FAS alignment is lost [FRED; addr 049]. The RAIS real-time status is available in ALM1. The RAIS interrupt is available in ISR7.

2.2.5.5 Yellow Alarm

The criteria for Yellow Alarm (YEL) is described in Table 3-13, *Receive Yellow Alarm Set/Clear Criteria*. YEL real-time status is available in ALM1; YEL interrupt is available in ISR7.

2.2.5.6 Multiframe YEL

The criteria for Multiframe Yellow Alarm is described in Table 3-13, *Receive Yellow Alarm Set/Clear Criteria*. The MYEL real-time status is available in ALM1, and the interrupt is available in ISR7.

2.2.5.7 Severely Errored Frame

A SEF is reported when the receive signal does not meet the requirements of ANSI T1.231. SEF real-time status is available in ALM3. A 2-bit counter is also available [SEF; addr 05A]. An interrupt is available in ISR4 to indicate that the SEF counter overflowed.

2.2.5.8 Change of Frame Alignment

Each COFA increments a 2-bit counter [COFA; addr 05A]. An interrupt is available in ISR4 to indicate that the COFA counter overflowed.

2.2.5.9 Receive Multiframe AIS

Receive Multiframe AIS (RMAIS) is reported when the receive TS16 signal contains three or fewer zeros out of 128 bits in each multiframe over two consecutive multiframes, according to the requirements of ITU–T Recommendation G.775. RMAIS is only checked in E1 CAS mode. RMAIS real-time status is available in ALM3 [addr 049].

2.2.6 Test Pattern Receiver

The test pattern receiver circuitry can sync on framed or unframed PRBS patterns and count bit errors. This feature is particularly useful for system diagnostics, production testing, and test equipment applications. The PRBS patterns available include 2E11-1, 2E15-1, 2E20-1, and 2E23-1. Each pattern can optionally include Zero Code Suppression (ZCS).

The Receive Test Pattern Configuration register [RPATT; addr 041] controls the test pattern receiver circuit. The BSTART control bit (in RPATT) must be active to enable the test pattern receiver and to begin counting bit errors. RPATT controls the PRBS pattern, ZCS setting (ZLIMIT), and T1/E1 framing (FRAMED). RPATT selects which PRBS pattern the receiver should hunt for pattern sync. ZLIMIT selects the maximum number of consecutive zeros the pattern is allowed to contain. FRAMED mode informs the PRBS pattern receiver not to search for the pattern in the frame bit in T1 mode or search for the pattern in time slot 0 (and time slot 16 if CAS framing is selected) in E1 mode. CAS framing is selected by setting RFRAME[3] to 1 in the Primary Control register [CR0; addr 001]. If FRAMED is disabled, the PRBS pattern receiver searches all time slots for the test pattern.

The RESEED bit in RPATT informs the receive PRBS sync circuit to begin a PRBS pattern search. Once the search begins, any additional writes to RESEED restarts the pattern sync search at a different point in the pattern. The time to sync depends on the pattern and number of bit errors in the pattern.

Pattern sync is reported (when found) in PSYNC status of the Pattern Interrupt Status register [ISR0; addr 00B]. Next, the PRBS Pattern Error counter [BERR; addr 058 and 059] counts bit errors detected on the incoming pattern, provided that BSTART remains active. Error counting stops if the BSTART bit is cleared. The BERR counter is reset to zero after every read, or latched on every ONESEC interrupt as selected by LATCH_CNT [addr 046]. An interrupt is available to indicate the BERR counter overflowed in ISR4.

2.2.7 Receive Framing

Two framers are in the receive data stream: an offline framer and an online frame status monitor. The offline framer recovers receive frame alignment; the online framer monitors frame alignment patterns and recovers multiframe alignment in E1 modes. Table 2-1 lists supported RCVR framing modes. Frame and multiframe synchronization criteria used by the framers, as well as the monitoring criteria of the online framer, are selected in RFRAME[3:0] of the Primary Control register [CR0; addr 001]. Table 2-2 details framing loss/recovery criteria.

Receive frame synchronization is initiated by the online framer's activation of the Receive Loss Of Frame (RLOF) status bit in the Alarm 1 Status register [ALM1; addr 047]. The RLOF criteria is set in the RLOFA, RLOFB, RLOFC, and RLOFD bits of the Receiver Configuration register [RCR01; addr 040]. The online framer supports the following LOF criteria for T1: 2 out of 4, 2 out of 5, and 2 out of 6. For E1, the online framer supports 3 out of 3, with or without 915 out of 1000 CRC errors.

When RLOF is asserted, the offline framer automatically starts searching the receive data stream for a new frame alignment, provided that receive framing is enabled [RABORT; addr 040]. If receive framing is disabled, the offline framer does not automatically search for the frame alignment, but waits for a reframe command [RFORCE; addr 040] to start a frame alignment search. If RLOF integration is enabled [RLOF_INTEG; addr 045] the RLOF status [ALM1; addr 047] and RLOF interrupt status [ISR7; addr 004] is integrated for 2.0 to 2.5 seconds.

The online framer continuously monitors for loss of frame (RLOF) condition [ALM1; addr 047] and searches for E1 multiframe alignment after basic frame alignment is recovered by the offline framer. Receive multiframe alignment is declared when multiframe alignment criteria are met. The receive online framer reports multiframe errors, as well as frame errors and CRC errors in the Error Interrupt Status [ISR5; addr 006].

The offline framer is shared between the RCVR and XMTR and can search only in one direction at any time. Consequently, the processor arbitrates which direction is searched by enabling the reframe request (RLOF and TLOF) for that direction.

Table 2-1. Receive Framer Modes

T1/E1N	RFRAME[3:0]	Receive Framer Mode
0	000X	FAS Only
0	001X	FAS Only + BSLIP
0	010X	FAS + CRC
0	011X	FAS + CRC + BSLIP
0	100X	FAS + CAS
0	101X	FAS + CAS + BSLIP
0	110X	FAS + CRC + CAS
0	111X	FAS + CRC + CAS + BSLIP
1	0000	FT Only
1	0001	ESF + No CRC (FPS only)
1	0100	SF
1	0101	SF + JYEL
1	0110	SF + T1DM
1	1000	SLC + FSLOF
1	1001	SLC
1	1100	ESF + Mimic CRC
1	1101	ESF + Force CRC

Table 2-2. Criteria for Loss/Recovery of Receive Framer Alignment

Mode	Description
FAS	Basic Frame Alignment (BFA) is recovered when the following search criteria are satisfied: • FAS pattern (0011011) is found in frame N. • Frame N+1 contains bit 2 equal to 1. • Frame N+2 also contains FAS pattern (0011011). During FAS-only modes, BFA is recovered when the following search criteria are satisfied: • FAS pattern (0011011) is found in frame N. • No mimics of the FAS pattern are present in frame N+1. • FAS pattern (0011011) is found in frame N+2. ***NOTE(S):*** If FAS pattern is not found in frame N+2, or if FAS mimic is found in frame N+1, the search restarts in frame N+2. Loss of FAS frame alignment (FRED) is declared when one of the following criteria is met: • Three consecutive FAS pattern errors are detected when the FAS pattern consists of a 7-bit (x0011011) pattern in FAS frames and—if FS_NFAS is also active [addr 045]—the FAS pattern includes bit 2 of NFAS frames. • Loss of MFAS (MRED) is due to 915 or more CRC errors out of 1000. • Failure to locate two valid MFAS patterns within 8 ms after BFA. ***NOTE(S):*** In all cases, FRED causes next search for FAS alignment to begin 1 bit after the current FAS location.
BSLIP	FAS Bit Slip Enable. Applicable only for Dutch PTT national applications. If BSLIP is enabled, the online framer is allowed to change RX timebase by ±1 bit when a 1-bit FAS pattern slip is detected. BSLIP does not affect the offline framer's search criteria.
MFAS	CRC4 Multiframe Alignment is recovered when the following search criteria are satisfied: • BFA is recovered, identifying FAS and NFAS frames. • Within 8 ms after BFA, bit 1 of NFAS frames contains two MFAS patterns (001011xx). The second MFAS must be aligned with respect to first MFAS, but the second MFAS pattern is not necessarily received in consecutive frames. • Within 8 ms after BFA, bit 1 of NFAS frames contains the second MFAS pattern (001011xx), aligned to first MFAS. Loss of MFAS alignment (MRED) declared when one of the following criteria is met: • 915 or more CRC4 errors out of 1000 (submultiframe) blocks. • Loss of FAS (FRED). ***NOTE(S):*** If Disable 915 CRC Reframe is set [RLOFD; addr 040], then MRED is activated only by FRED.
CAS	CAS Multiframe Alignment is recovered when the following search criteria are satisfied: • BFA is recovered, identifying TS0 through TS31. • MAS (0000xxxx) multiframe alignment signal pattern is found in the first 4 bits of TS16, and 8 bits of TS16 in preceding frame contains nonzero value. Loss of CAS alignment (SRED) is declared when one of the following criteria is met: • Two consecutive MAS pattern errors are detected. • TS16 contains all zeros in two multiframes (32 consecutive frames). • Loss of FAS (FRED).
FT Only	Terminal frame alignment is recovered when: The first valid Ft pattern (1010) is found in 12 alternate F-bit locations (3 ms), where F-bits are separated by 193 bits. During Ft-only mode, loss of frame alignment (FRED) is declared when: Number of Ft bit errors detected meets selected loss of frame criteria [RLOFA–RLOFC; addr 040].

Table 2-2. Criteria for Loss/Recovery of Receive Framer Alignment

Mode	Description
SF	Superframe alignment is recovered when: • Terminal frame alignment is recovered, identifying Ft bits. • Depends on SF submode: If JYEL, only Ft bits are used, Fs bits are ignored. If no JYEL, SF pattern (001110) found in Fs bits. During any SF mode, loss of frame alignment (FRED) is declared when: Number of frame errors detected—either Ft or Fs bit errors—meets selected loss of frame criteria [RLOFA–RLOFC; addr 040]. FS_NFAS [addr 045] determines whether Fs bits are included in error count.
SLC	Superframe alignment is recovered when: Terminal frame alignment is recovered, identifying Ft bits. SLC pattern (refer to Table A-3, *SLC-96 Fs Bit Contents*) is found in 16 of 36 Fs bits, according to Bellcore TR-TSY-000008. During SLC modes without FSLOF, loss of frame alignment (FRED) is declared when: Number of Ft bit errors detected meets selected reframe criteria [RLOFA–RLOFC; addr 040].
FSLOF	FSLOF instructs the online framer to monitor 16 of 36 Fs bits (SLC multiframe pattern) for loss of frame alignment criteria. FS_NFAS [addr 045] must also be set to include Fs bits in loss of frame. FSLOF does not affect the offline framer's search criteria.
ESF	Extended Superframe alignment is recovered when: A valid FPS candidate is located (001011). Candidate bits are each separated by 772 digits and are received without pattern errors. If there is only one valid FPS candidate and the mode is one of the following: No CRC mode—align to FPS, regardless of CRC6 comparison. Mimic CRC mode—align to FPS, regardless of CRC6 comparison. Force CRC mode—align to FPS, only if CRC6 is correct. If there are two or more valid FPS candidates and the mode is one of the following: No CRC mode—do not align (INVALID status). Mimic CRC mode—align to first FPS with correct CRC6. Force CRC mode—align to first FPS with correct CRC6. During any ESF mode, loss of frame alignment (FRED) is declared when: Number of FPS pattern errors detected meets selected loss of frame criteria [RLOFA–RLOFC; addr 040].
T1DM	During T1DM mode, frame alignment is recovered in two steps: 1. A 6-bit T1DM pattern (10111xx0) is found. 2. A valid F-bit pattern (Ft, Fs, or FPS) is found in the first six consecutive frames of the 12-frame cycle aligned to the T1DM pattern. During T1DM mode, loss of frame alignment (FRED) is declared when: Number of frame errors detected, either Ft, Fs, or T1DM errors, meets selected loss of frame criteria [RLOFA–RLOFC; addr 040]. FS_NFAS [addr 046] does not affect T1DM mode. ***NOTE(S):*** To be compatible with Bellcore TA-TSY-000278, the processor must select SF + T1DM framer mode and reframe criteria = 2 out of 6 F-bit errors [RLOFA–RLOFC; addr 040].

The offline framer waits until the current search is complete (see [FSTAT; addr 017]) before checking for pending LOF reframe requests. If both online framers have pending reframe requests, the offline framer aligns to the direction opposite from that which was most recently searched. For example, if TLOF is pending at the conclusion of a receive search which timed out without finding alignment, the offline framer switches to search in the transmit direction. The TLOF switchover is prevented in the preceding example if the processor asserts TABORT to mask the transmit reframe request. TABORT does not affect TLOF status reporting. For applications that frame in only one direction, the opposite direction should be masked. If, at the conclusion of a receive search, TLOF status is asserted but masked by TABORT, the offline framer continues to search in the receive direction. For applications that frame in both directions, the processor can allow the offline framer to automatically arbitrate among pending reframe requests, or may elect to manually control reframe precedence. An example of manual control follows:

1 Initialize RABORT = 1 and TABORT = 1

2 Enable RLOF and TLOF interrupts

3 Read clear pending ISR interrupts

4 Release RABORT = 0

5 Call LOF Service Routine if either RLOF or TLOF interrupt;
{
(check current LOF status [ALM1, 2; addr 047, 048]
If RLOF recovered and TLOF lost
—Assert RABORT = 1
—Release TABORT = 0
If RLOF lost or TLOF recovered
—Assert TABORT = 1
—Release RABORT = 0
}

The status of the offline framer can be monitored for diagnostic purposes using the Offline Framer Status register [FSTAT; addr 017]. The register reports the following: whether the offline framer is looking at the receive or transmit data streams (RX/TXN); whether the framer is actively searching for a frame alignment (ACTIVE); whether the framer found multiple framing candidates (TIMEOUT); whether the framer found frame sync (FOUND); and whether the framer found no frame alignment candidates (INVALID). Note that these status bits are updated in real time and might be active for only very short (1-bit) periods of time. Table 2-1 lists the receive framer modes.

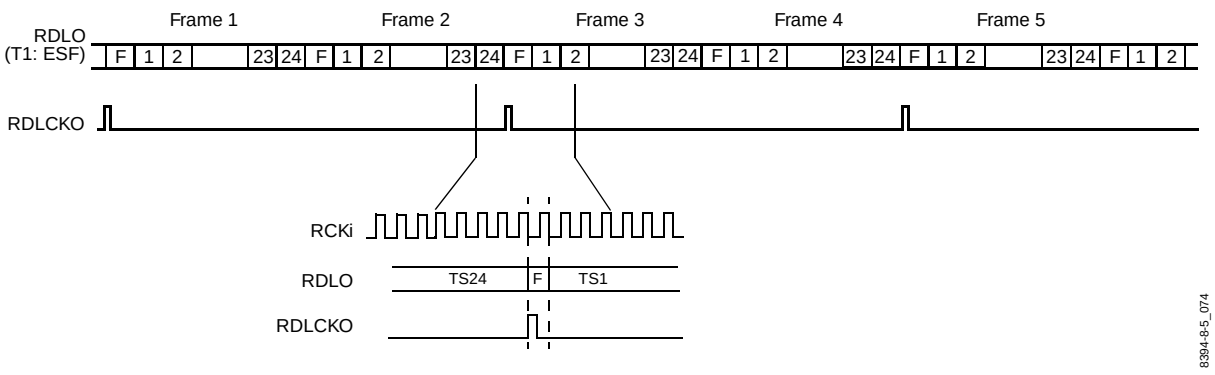
2.2.8 External Receive Data Link (CX28394 and CX28398 Only)

The External Data Link (DL3) provides signal access to any bit(s) in any time slot of all frames, odd frames, or even frames, including T1 framing bits. Pin access to the DL3 receiver is provided through RDLCKO and RDLO. These two pins serve as the DL3 clock output (RDLCKO) and data output (RDLO). The data link mode of the pins is selected using the RDL_IO bit in the Programmable Input/Output register [PIO; addr 018].

Control of DL3 is provided in two registers: External Data Link Channel [DL3_TS; add 015] and External Data Link Bit [DL3_BIT; addr 016]. RDL3 is set up by selecting the bit(s) (DL3_BIT) and time slot [TS[4:0]; addr 015] to be monitored, and then enabling the data link [DL3EN; addr 015], which starts the RDLCKO and TDLCKO gapped clock outputs that mark the selected bits, as shown in Figure 2-4.

NOTE: DL3 signals are not provided on the CX28395. Therefore, DL3_TS must be written to 00 to disable the DL3 transmitter and prevent transmit data corruption.

Figure 2-4. Receive External Data Link Waveforms



NOTE(S): This waveform represents ESF FDL extraction; any combination of bits can alternatively be selected.

2.2.9 Sa-Byte Receive Buffers

The Sa-Byte buffers give read access to the odd frame Sa bits in E1 mode. Five receive Sa-Byte buffers [RSA4 to RSA8; addr 05B to 05F] are available. As a group, the buffers are updated every multiframe from Sa-bits received in TS0. This gives the processor up to 2 ms after the receive multiframe interrupt [RMF; addr 008] occurs to read any Sa-Byte buffer before the buffer content changes.

2.2.10 Receive Data Link

The RCVR contains two independent data link controllers (DL1 and DL2) and a Bit-Oriented Protocol (BOP) transceiver. DL1 and DL2 can be programmed to send and receive HDLC formatted messages in the Message-Oriented Protocol (MOP) mode. Alternatively, unformatted serial data can be sent and received over any combination of bits within a selected time slot or F-bit channel. The BOP transceiver can preemptively receive and transmit BOP messages, such as ESF Yellow Alarm.

2.2.10.1 Data Link Controllers

DL1 and DL2 control two serial data channels operating at multiples of 4 kbps up to the full 64 kbps time slot rate by selecting a combination of bits from odd, even, or all frames. Both DL1 and DL2 support ESF Facilities Data Link (FDL), SLC-96 Data Link, Sa Data Link, Common Channel Signaling (CCS), Signaling System #7 (SS7), ISDN LAPD channels, Digital Multiplexed Interface (DMI) Signaling in TS24, as well as the latest ETSI V.51 and V.52 signaling channels. DL1 and DL2 each contain a 64-byte receive FIFO buffer.

Both data link controllers are configured identically, except for their offset in the register map. The DL1 address range is 0A4 to 0AE, and the DL2 address range is 0AF to 0B9. From this point on, DL1 is used to describe the operation of both data link controllers.

DL1 is enabled using the DL1 Control register [DL1_CTL; addr 0A6]. DL1 will not function until it is enabled. DL1_CTL also controls the format of the data. The following data formats [DL1[1:0]; addr 0A6] are supported on the data link: Frame Check Sequence (FCS), non-FCS, Pack8, or Pack6. FCS and non-FCS are HDLC formatted messages. Pack8 and Pack6 are unformatted messages with 8 bits per FIFO access, or 6 bits per FIFO access, respectively (see Table 2-3).

Table 2-3. Commonly Used Data Link Settings

Data Link	Frame	Time Slot	Time Slot Bits	Mode
ESF FDL	Odd	0 (F-bits)	Don't Care	FCS
T1DM R Bit	All	24	00000010	FCS
SLC-96	Even	0 (F-bits)	Don't Care	Pack6
ISDN LAPD	All	N	11111111	FCS
Sa4	Odd	1	00001000	FCS
NOTE(S): N represents any T1/E1 time slot.				

The time slot and bit selection are performed through the DL1 Time Slot Enable register [DL1_TS; addr 0A4] and the DL1 Bit Enable register [DL1_BIT; addr 0A5]. The DL1 Time Slot Enable register selects the frames and time slot to extract the data link. The frame select tells the receiver to extract the time slot in all frames, odd frames, or even frames. The time slot enable is a value between 0 and 31 that selects which time slot to extract. The DL1 Bit Enable register selects which bits will be extracted in the selected time slot. Refer to Table 2-3 for the common frame, time slot, time slot bits, and modes used.

The Receive Data Link FIFO #1 [RDL1; addr 0A8] is 64 bytes. The Receive FIFO buffer is formatted differently than the transmit FIFO buffer. The Receive buffer contains not only received messages, but also a status byte preceding each message that specifies the size of the received message and the status of that message. The message status reports if the message was aborted, received with a correct or incorrect FCS, or continued. A continued message means the byte count represents a partial message. When all message bytes are read, the buffer contains another status byte. Message bytes can be differentiated from status bytes in the buffer by reading the RSTAT1 bit in the RDL #1 Status register [RDL1_STAT; addr 0A9]. RSTAT1 reports whether the next byte read from the buffer will be a status byte or some number of message bytes.

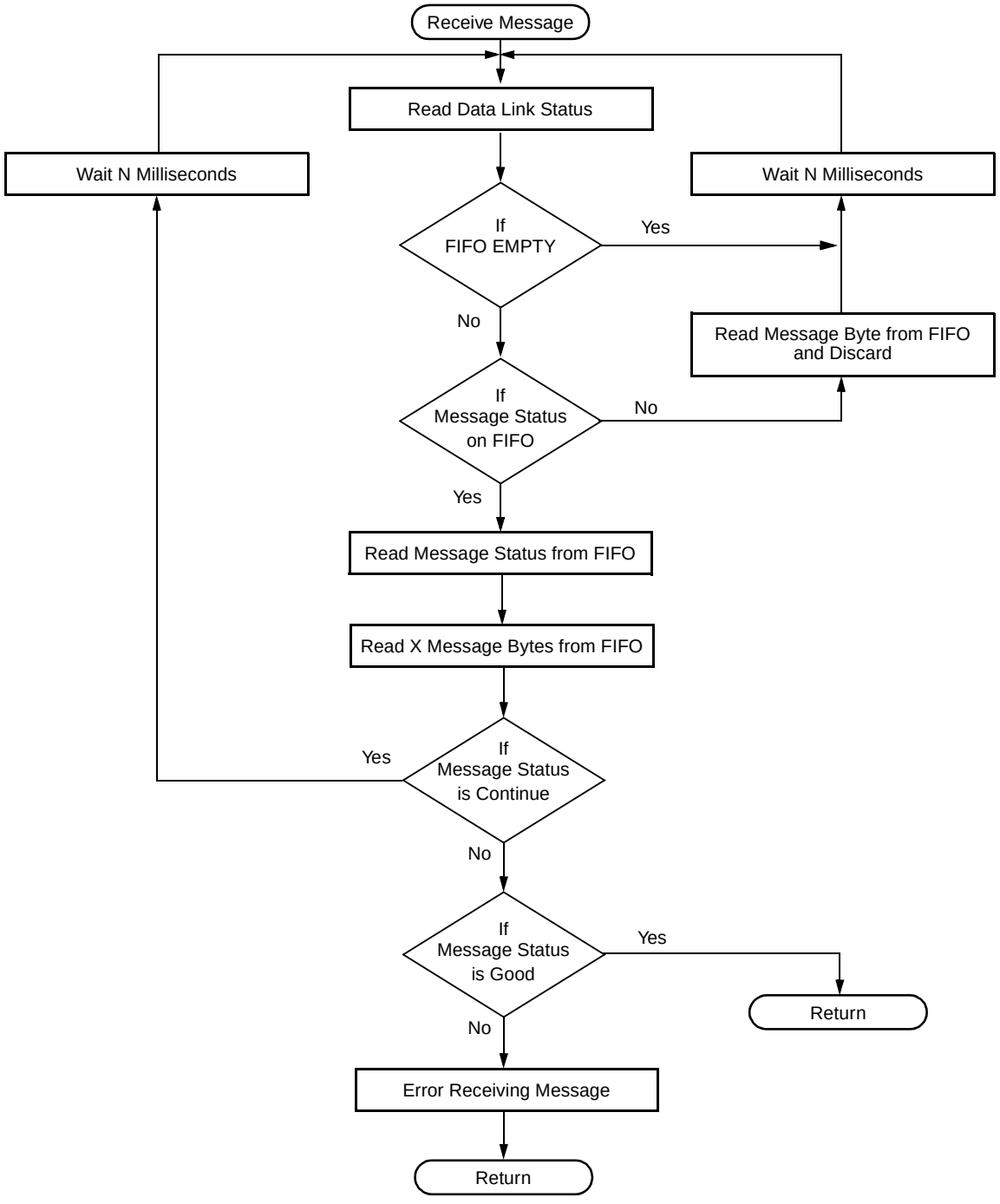
The receive data link controller has a versatile microprocessor interface that can be tuned to the system's CPU bandwidth. For systems with one dedicated CPU, the data link status can be polled. For systems where a single CPU controls multiple devices, the data link can be interrupt-driven. See Figures 2-5 and 2-6 for a high-level description of polling and interrupt driven Receive Data Link Controller software.

Using the Receive FIFO buffer, an entire block of data can be received with very little microprocessor interrupt overhead. Block transfers from the buffer can be controlled by the Near Full Threshold in the FIFO Fill Control register [RDL1_FFC; addr 0A7]. The Near Full Threshold is a user programmable value between 0 and 63. This value represents the maximum number of bytes that can be placed in the Receive buffer without the near full being declared. Once the threshold is set, the Near Full Status (RNEAR1) in RDL #1 Status [RDL1_STAT; addr 0A9] is asserted when the Near Full Threshold is reached. An interrupt, RNEAR, in Data Link 1 Interrupt Status [ISR2; addr 009], is also available to mark this event.

The device uses a hierarchical interrupt structure, with one top-level interrupt request register directing software to the lower levels (see Master Interrupt Request register; addr 081 and Interrupt Request register; addr 003). Of all the interrupt sources, the two most significant bandwidth requirements are signaling and data link interrupts. Each data link controller has a top-level interrupt status register that reports data link operations (see Data Link 1 and 2 Interrupt Status registers [ISR2, ISR1; addr 009 and 00A). The processor uses a three-step interrupt scheme for the data link:

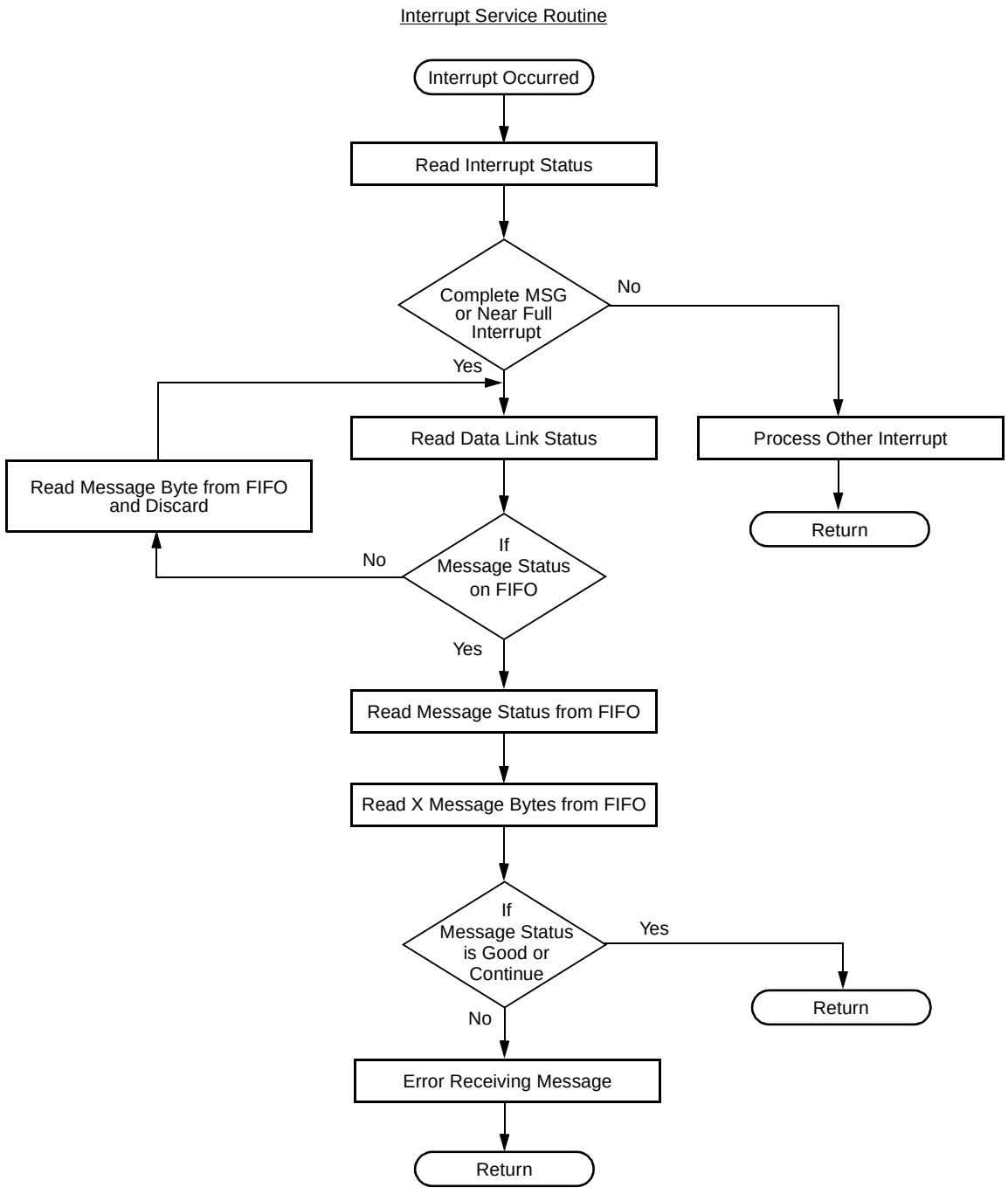
1. Read the Master Interrupt Request register to determine which framer interrupted.
2. Read the Interrupt Request register for that framer.
3. Use that register value to read the corresponding Data Link Interrupt Status register.

Figure 2-5. Polled Receive Data Link Processing



NOTE(S): Message status contains number of message bytes (X) in FIFO.

Figure 2-6. Interrupt-Driven Receive Data Link Processing



NOTE(S): Message status contains number of message bytes (X) in FIFO.

2.2.10.2 RBOP Receiver

The Receive Bit-Oriented Protocol (RBOP) receiver receives BOP messages, including the ESF Yellow Alarm, which consists of repeated 16-bit patterns with an embedded 6-bit codeword as shown in this example:

```
0xxxxxx0 11111111 (received right to left)

[543210] RBOP = 6-bit codeword
```

The BOP message channel is configured to operate over the same channel selected by Data Link #1 [DL1_TS; addr 0A4]. It must be configured to operate over the FDL channel so RBOP can detect priority, command, and response codeword messages according to ANSI T1.403, Section 9.4.1.

RBOP is enabled using the RBOP_START bit in Bit Oriented Protocol Transceiver register [BOP; address 0A0]. BOP codewords are received in the Receive BOP Codeword register [RBOP; addr 0A2], which contains the 6-bit codeword, a valid flag (RBOP_VALID), and a lost flag (RBOP_LOST). The valid flag is set each time a new codeword is put in RBOP, and is cleared on reading the codeword. The lost flag indicates a new codeword overwrote a valid codeword before being read by the processor.

The BOP receiver can be configured to update RBOP using a message length filter and integration filter. The receive BOP message length filter [RBOP_LEN; addr 0A40] sets the number of successive identical messages required before RBOP is updated. RBOP_LEN can be set to 1, 10, or 25 messages. When enabled, the RBOP integration filter [RBOP_INTEG; add 0A0] requires receipt of two identical consecutive 16-bit patterns, without gaps or errors between patterns, to validate the first codeword. RBOP integration is needed to meet the codeword detection criteria while receiving 1/1000 bit error ratio.

The real-time status of the codeword reception can be monitored using the RBOP_ACTIVE bit in the BOP Status register [BOP_STAT; addr 0A3]. Each time a message is put in RBOP register, an interrupt is generated, and the RBOP bit is set in the Data Link 2 Interrupt Status register [ISR1; addr 00A].

2.3 System Bus

Each framer provides high-speed, transmit and receive serial TDM interfaces. These interfaces can be configured as non-multiplexed, individual system buses, or they can be multiplexed internally or externally to provide 2xE1 (4096 Mbps) and 4xE1 (8192 Mbps) buses. The system bus is compatible with the Mitel ST-Bus, the Siemens PEB Bus, and the AT&T CHI Bus and directly connects to other Conexant serial TDM bus devices without the need for any external circuitry. The following five bus rates are supported:

- 1.536 MHz—T1 rate, 24 time slots, without framing bit
- 1.544 MHz—T1 rate with framing bit
- 2.048 MHz—E1 rate, 32 time slots
- 4.096 MHz—twice the E1 rate, 64 time slots
- 8.192 MHz—four times the E1 rate, 128 time slots

2.3.1 Non-Multiplexed Mode

In Non-Multiplexed mode, each framer has a separate system bus interface consisting of the following pin functions:

Receive System Bus (RSB)	Transmit System Bus (TSB)
RSBCKI	TSBCKI
RPCMO	TPCMI
RFSYNC/RMSYNC	TFSYNC/TMSYNC
RINDO/RDLCKO	TINDO/TDLCKO
RSIGO/RDLO	TSIGI/TDLI
SIGFRZ	—

The signal available on dual function pins is controlled using register PIO [addr 018].

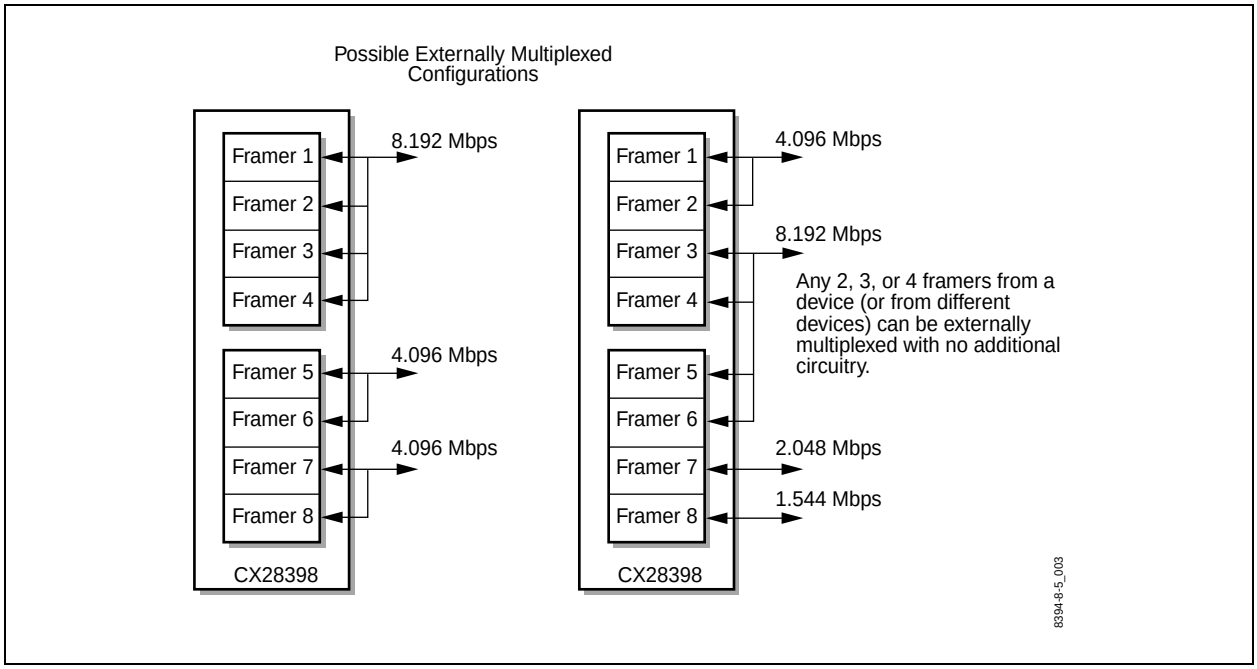
To use Non-Multiplexed mode, SBIMODE[0] and/or SBIMODE[1] in the Framer Control register [FCR; addr 080] must be zero to disable Internally Multiplexed mode. The system bus rate is independent of the line rate and must be selected using SBI[3:0] in the System Bus Interface Configuration register [SBI_CR; addr 0D0]. Register bit SBI_OE [SBI_CR; addr 0D0] must also be set to 1 to enable system bus outputs.

2.3.2 Externally Multiplexed Mode

Externally Multiplexed mode allows any two, three, or four framers (in the same or different devices) to share a common high speed system bus (see Figure 2-7). The 4.096 and 8.192 MHz bus modes contain multiple bus members (bus groups A, B, C, D) which allow multiple T1/E1 signals to share the same system bus. This is done by interleaving the time slots from up to four framers (see Figures 2-10 and 2-11).

To use Externally Multiplexed mode, SBIMODE[0] and/or SBIMODE[1] in the Framer Control register [FCR; addr 080] must be zero to disable Internally Multiplexed mode. The system bus rate is independent of the line rate and must be selected using SBI[3:0] in the System Bus Interface Configuration register [SBI_CR; addr 0D0]. SBI[3:0] is also used to assign each framer to a different bus group. Register bits SBI_OE [SBI_CR; addr 0D0], BUS_RSB [RSB_CR; addr 0D1], and BUS_TSB [TSB_CR; addr 0D4] must be set to 1 to allow system bus outputs to share common connections.

Figure 2-7. Externally Multiplexed Configuration Examples



2.3.3 Internally Multiplexed Mode

Internally Multiplexed mode operation is very similar to Externally Multiplexed mode. The framers in each device are internally grouped into four-framer groups to allow an internally multiplexed mode (see Figure 2-8). In the CX28398, framers 1 through 4 form a group (lower group or group A) and framers 5 through 8 form another (upper group or group B). The CX28395 supports four groups: A, B, C, and D. The CX28394's four framers are also grouped in the same manner. In this mode, system bus signals from all four framers are internally connected and the interface pin functions are redefined. The advantage of this mode is that all system bus signals which are normally available on dual function pins, are now available on separate pins. In Internally Multiplexed mode, the following signals are available for each four-framer group (lower group shown):

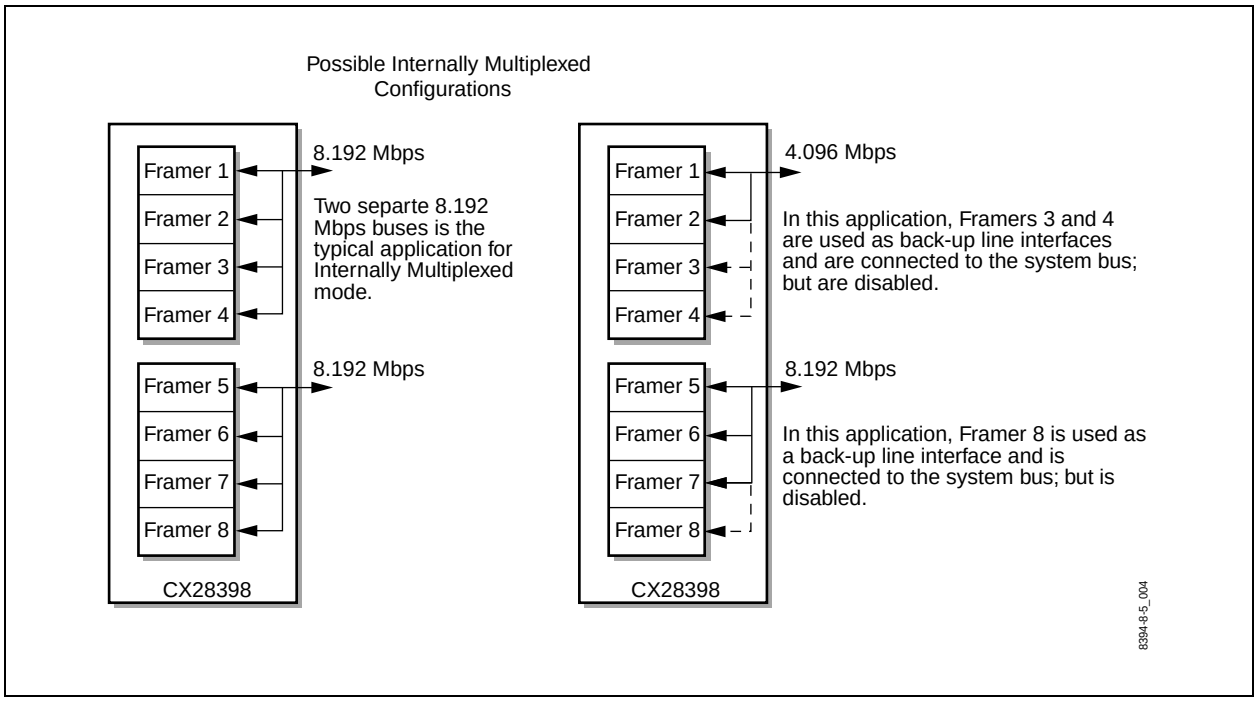
Receive System Bus (RSB)	Transmit System Bus (TSB)	
RSBCKI[A]	TSBCKI[A]	Common, internally connected to all four framers.
RPCMO[A]	TPCMI[A]	
RFSYNC[A]	TFSYNC[A]	
RINDO[A]	TINDO[A]	
RSIGO[1:4]	TSIGI[1:4]	Separate signals.
RMSYNC[1:4]	TMSYNC[1:4]	
RDLCKO[1:4](1)	TDLCKO[1:4](1)	
RDLO[1:4](1)	TDLI[1:4](1)	
SIGFRZ[1:4]	—	

NOTE(S):

(1) These signals are not provided on the CX28395.

To use Internally Multiplexed mode, SBIMODE[0] and/or SBIMODE[1] in the Framer Control register [FCR; addr 080] must be set to 1. The system bus rate is independent of the line rate and must be selected using SBI[3:0] in the System Bus Interface Configuration register [SBI_CR; addr 0D0]. SBI[3:0] is also used to assign each framer to a different bus group. Register bits SBI_OE [SBI_CR; addr 0D0], BUS_RSB [RSB_CR; addr 0D1], and BUS_TSB [TSB_CR; addr 0D4] must be set to 1 to allow system bus outputs to share common connections. Because RFSYNC (and TFSYNC) signals are bused, all four framers' RFSYNC (and TFSYNC) signals must be configured as inputs and driven externally or, alternatively, three framers' sync signals can be configured as inputs and one as an output [PIO; addr 018].

Figure 2-8. Internally Multiplexed Configuration Examples



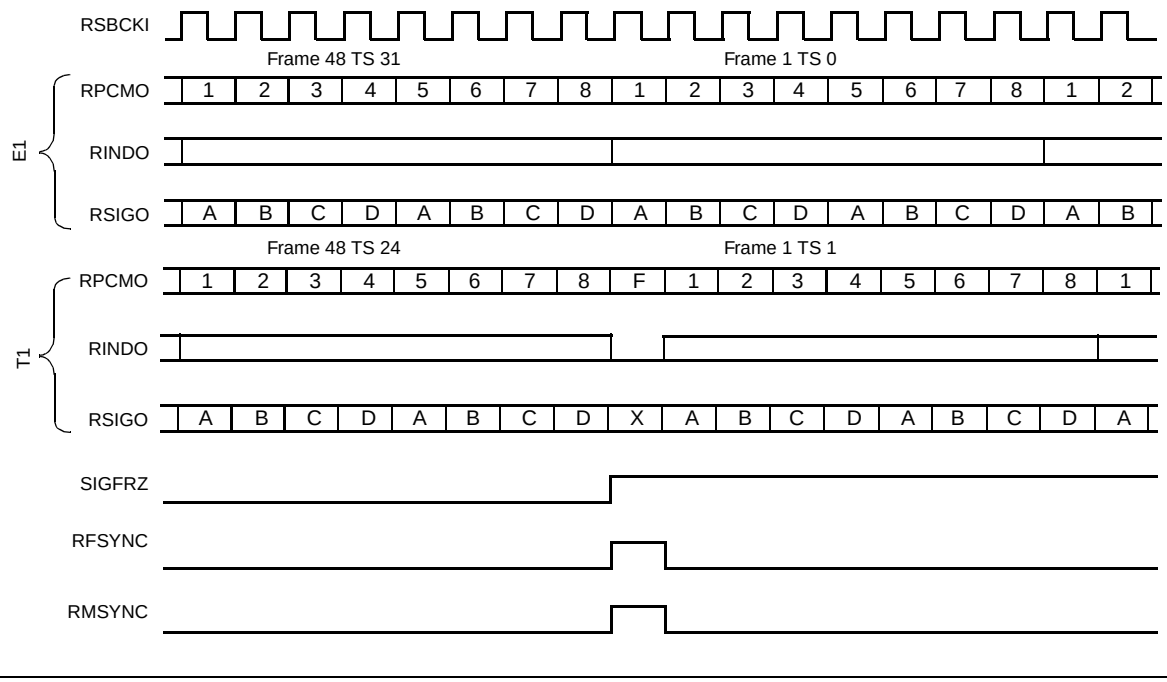
2.3.4 Receive System Bus

The Receive System Bus (RSB) provides a high-speed, serial interface between the RCVR and the system bus. The RSB has the following pins:

Pin Name	Function
RSBCKI	Receive System Bus Clock
RPCMO	Receive PCM Data
RFSYNC/RMSYNC	Receive Frame Sync or Receive Multiframe Sync
RINDO/RDLCKO	Receive Time Slot Indicator or Receive Datalink Clock
RSIGO/RDLO	Receive Signaling Data or Receive Datalink Data
SIGFRZ	Signaling Freeze

Figure 2-9 illustrates the relationship between these signals. Signal definitions are provided in Table 1-6, *Hardware Signal Definitions*. RSB data outputs can be configured to output on the rising or falling edge of RSBCKI (see the Receive System Bus Configuration register [RSB_CR; addr 0D1]).

Figure 2-9. RSB Waveforms



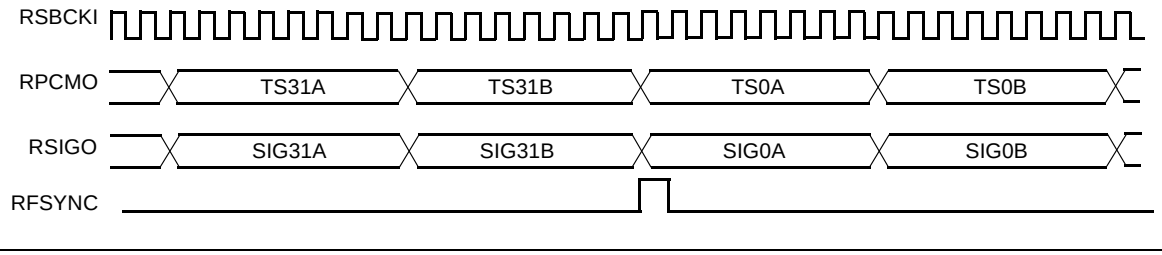
NOTE(S): The Receive Multiframe Sync (RMSYNC) occurs every 6 ms, 48 T1 or 48 E1 frames.

The RSB supports five different system bus rates (MHz):

- 1.536 MHz—T1 rate, 24 time slots, without framing bit
- 1.544 MHz—T1 rate with framing bit
- 2.048 MHz—E1 rate, 32 time slots
- 4.096 MHz—twice the E1 rate, 64 time slots
- 8.192 MHz—four times the E1 rate, 128 time slots

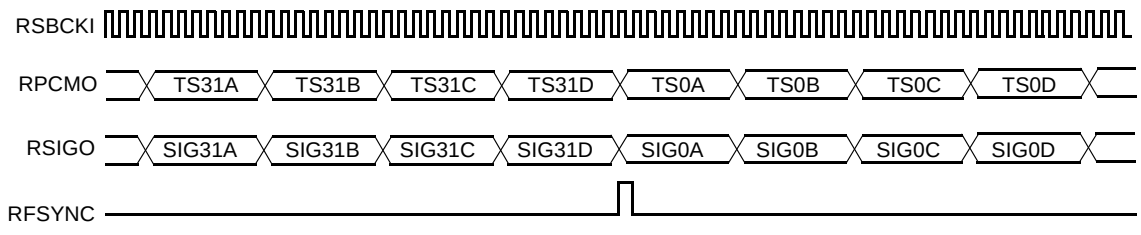
The 4.096 and 8.192 MHz bus modes contain multiple bus members (A, B, C, D) which allow multiple T1/E1 signals to share the same system bus. This is done by interleaving the time slots from up to four framers, without external circuitry (see Figures 2-10 and 2-11). The system bus rate is independent of the line rate and must be selected using the System Bus Interface Configuration register [SBI_CR; addr 0D0].

Figure 2-10. RSB 4096K Bus Mode Time Slot Interleaving



NOTE(S): A and B time slot comes from different framers. Output data on rising edge clock, RCPM_NEG = 0 [addr 0D1]. Output sync on rising edge clock, RSYN_NEG = 0 [addr 0D1]. RSBCKI operates at 1 times the data rate.

Figure 2-11. RSB 8192K Bus Mode Time Slot Interleaving



NOTE(S): A, B, C, and D data comes from different framers. Output data on rising edge clock, RCPM_NEG = 0 [addr 0D1]. Output sync on rising edge clock, RSYN_NEG = 0 [addr 0D1]. RSBCKI operates at 1 times the data rate. RSB.OFFSET equals zero.

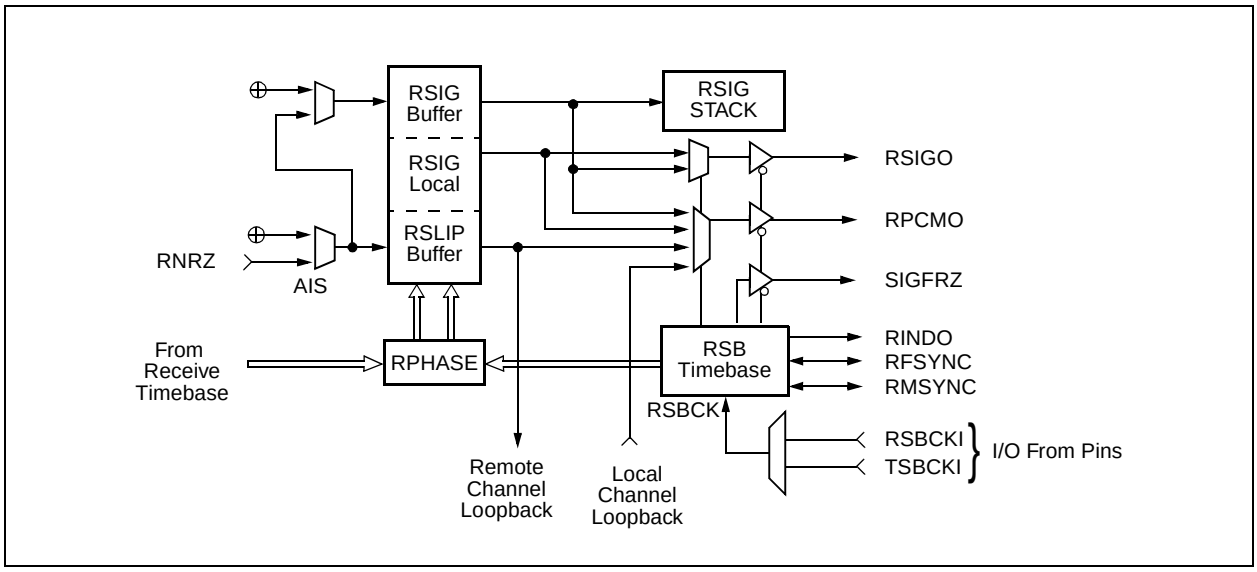
The RSB maps line rate time slots to system bus time slots. The 24 (DS1) or 32 (CEPT) line rate time slots can be mapped to 24, 32, 64, or 128 system bus time slots as listed in Table 2-4. The system bus rate must be greater than or equal to the line rate, except for 1536K bus mode.

Table 2-4. RSB Interface Time Slot Mapping

Line Rate (MHz)	Source Channels	System Bus Rate (MHz)	Destination Time Slots
1.544	24	1.536	24
	24	1.544	24
	24	2.048	32
	24	4.096	64
	24	8.192	128
2.048	32	2.048	32
	32	4.096	64
	32	8.192	128

The RSB, Figure 2-12, consists of a timebase, slip buffer, a signaling buffer, and a signaling stack.

Figure 2-12. RSB Diagram



2.3.4.1 Timebase

The RSB timebase synchronizes RFSYNC, RMSYNC, and RINDO with the Receive System Bus Clock (RSBCKI). The RSBCK can be slaved to two different clock sources: Receive System Bus Clock Input (RSBCKI), or Transmit System Bus Clock Input (TSBCKI). The RSB clock selection is made through the Clock Input Mux register [CMUX; addr 01A]. The system bus clock can also be configured to run at twice the data rate by setting the X2CLK bit in the System Bus Interface Configuration register [SBI_CR; addr 0D0].

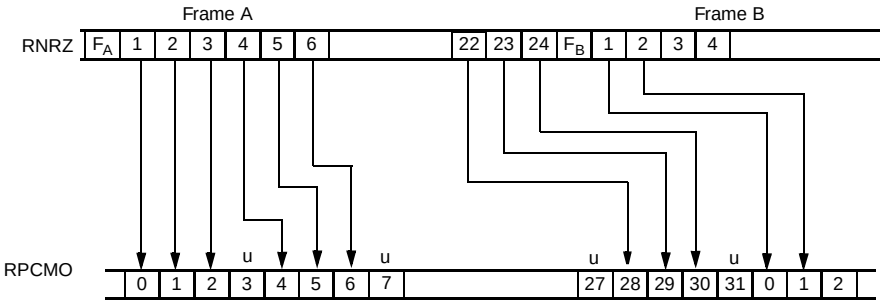
In Non-Multiplexed mode, the RFSYNC/RMSYNC dual function pin is configured for either RFSYNC or RMSYNC using the RMSYNC_EN register bit [PIO; addr 018]. RFSYNC and RMSYNC can be configured as inputs or outputs [PIO; addr 018]. RFSYNC and RMSYNC should be configured as inputs when the RSB timebase is slaved to the system bus [SBI_OE; addr 0D0]. RFSYNC and RMSYNC should be configured as outputs when the RSB timebase is master of the system bus. RFSYNC and RMSYNC can be also configured as rising or falling edge outputs [RSB_CR; addr 0D1]. In addition to having RFSYNC and RMSYNC active on the frame boundary, a programmable offset is available to select the time slot and bit offset in the frame. See the Receive System Bus Sync Time Slot Offset [RSYNC_TS; addr 0D3] and the Receive System Bus Sync Bit Offset [RSYNC_BIT; addr 0D2].

2.3.4.2 Slip Buffer

The 64-byte Receive PCM Slip Buffer [RSLIP; addr 1C0 to 1FF] resynchronizes the Receiver Clock (RCKI) and data (RNRZ), to the Receive System Bus Clock (RSBCK) and data (RPCMO). RSLIP acts like an elastic store by clocking RNRZ data in with RCKI and clocking PCM data out on RPCMO with RSBCK.

If the system bus rate is greater than the line rate (i.e., T1 line rate and E1 system bus rate), there will be a mismatched number of time slots. The mapping of line rate time slots to system bus time slots is done by time slot assignments with the ASSIGN bit in the System Bus Per-Channel Control register [SBC0 to SBC31; addr 0E0 to 0FF]. ASSIGN selects which system bus time slots are used to transport line rate time slots. Time slot mapping is done by mapping the first line rate time slot to the first assigned system bus time slot. For example, T1 to E1 mapping might make every fourth time slot unassigned (i.e., 3, 7, 11, 15, 19, 23, 27, 31); see Figure 2-13. This distribution of unassigned time slots averages out the idle time slots and optimizes the use of the slip buffer.

Figure 2-13. T1 Line to E1 System Bus Time Slot Mapping



NOTE(S):
(1) u = unassigned time slots
(2) F_A = T1 frame bit, frame A
(3) F_B = T1 frame bit, frame B

RSLIP has four modes of operation: Two Frame Normal, 64-bit Elastic, Two-Frame Short, and Bypass. RSLIP mode is set in the Receive System Bus Configuration register [RSB_CR; addr 0D1]. RSLIP is organized as a two-frame buffer. This allows MPU access to frame data, regardless of the RSLIP mode selected. Each byte offset into the frame buffer is a different time slot: offset 0 in RSLIP is always time slot 0 (TS0), offset 1 is always TS1, and so on. The slip buffer has processor read/write access.

Two-Frame Normal

In Normal mode, the slip buffer total depth is two 193-bit frames (T1) or two 256-bit frames (E1). Data is written to the slip buffer using RXCLK, and read from the slip buffer using RSBCK. If a slight rate difference between the clocks occurs, the slip buffer changes from its initial condition—approximately half full—by either adding or removing frames. If RXCLK writes to the slip buffer faster than RSBCK reads the data, the buffer will fill up. When the slip buffer in Normal mode is full, an entire frame of data is deleted. Conversely, if RSBCK reads the slip buffer faster than RXCLK writes the data, the buffer will become empty. When the slip buffer in Normal mode is empty, an entire frame of data is duplicated. When an entire frame is deleted or duplicated it is known as a Frame Slip (FSLIP), which is always one full frame of data. The FSLIP status is reported in the Slip Buffer Status register [SSTAT; addr 0D9]. In T1 mode, the F-bit is treated as part of the frame and can slip accordingly.

64-Bit Elastic In 64-bit Elastic mode, the slip buffer total depth is 64 bits, and the initial throughput delay is 32 bits, one-half of the total depth. Similar to Normal mode, Elastic mode allows the system bus to operate at any of the programmable rates, independent of the line rate. The advantage of this mode over the Normal mode is that throughput delay is reduced from one frame to an average of 32 bits, and the output multiframe always retains its alignment with respect to the output data. The disadvantage of this mode is handling the full and empty buffer conditions. In Elastic mode, an empty or full buffer condition causes an Uncontrolled Slip (USLIP). Unlike an FSLIP, a USLIP is of unknown size within the range of 1 to 256 bits of data. The USLIP status is reported in SSTAT.

Two-Frame Short The Two-Frame Short mode combines the depth of the Normal mode with the throughput delay of the Elastic mode. The Two-Frame Short mode begins in the Elastic mode with a 32-bit initial throughput delay, and switches to the Normal mode when the buffer becomes empty or full; thereafter the Two-Frame Short and normal mode perform identically. If the slip buffer is full (two frames) in the Two-Frame Short mode, an FSLIP is reported, after which the slip buffer and Two-Frame mode perform identically.

Bypass In Bypass mode, data is immediately clocked through RSLIP from the RCVR to RSB, and RCKI internally replaces the system bus clock.

2.3.4.3 Signaling Buffer

The 32-byte Receive Signaling Buffer [RSIG; addr 1A0 to 1BF] stores a single multiframe of signaling data. Each byte offset into RSIG contains signaling data for a different time slot: offset 0 stores TS0 signaling data, offset 1 stores TS1 signaling data and so on. The signaling data is stored in the least significant 4 bits of RSIG. The output signaling data is stored in the most significant 4 bits of RSIG. Similar to RSLIP, the RSIG buffer has read/write processor access to read or overwrite signaling information. RMSYNC extracts robbed-bit signaling from RSIG onto RPCMO; RFSYNC extracts ABCD signaling from RSIG onto RSIGO.

The RSIG buffer has the following configurable features: transparent, robbed-bit signaling; signaling freeze; debounce signaling; and unicode detection. Each feature is available in the Receive Signaling Configuration register [RSIG; addr 0D7]. See the registers section for more details.

2.3.4.4 Signaling Stack

The Receive Signaling Stack (RSTACK) allows the processor to quickly extract signaling changes without polling every channel. RSTACK is activated on a per-channel basis by setting the Received Signaling Stack (SIG_STK) control bit in the Receive Per-Channel Control register [RPC0 to RPC31; addr 180 to 19F]. The signaling stack stores the channel and the A, B, C, and D signaling bits that changed in the last multiframe. The stack has the capacity to store signaling changes for all 24 (T1) or 30 (E1) PCM channels.

At the end of any multiframe where one or more ABCD signaling values have changed, an interrupt occurs with RSIG set in the Timer Interrupt Status register [ISR3; addr 008]. The processor then reads the Receive Signaling Stack [STACK; addr 0DA] twice to retrieve the channel number (WORD = 0) and the new ABCD value (WORD = 1), and continues to read from STACK until the MORE bit in STACK is cleared, indicating the RSIG stack is empty.

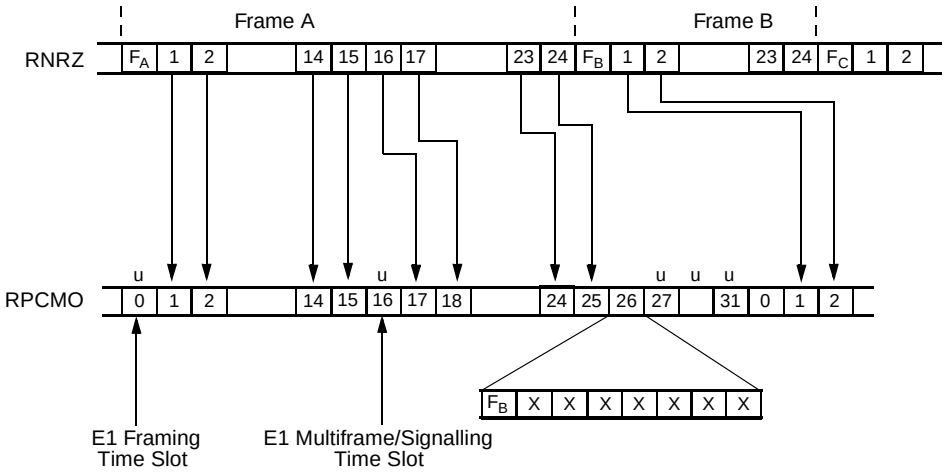
Optionally, the processor can select RSIG interrupt (SET_RSIG; addr 0D7) to occur at each multiframe boundary in T1 modes, regardless of signaling change. This mode provides an interrupt aligned to the multiframe to read the RSIG buffer, rather than to read RSTACK.

2.3.4.5 Embedded Framing

Embedded framing mode bit (EMBED; addr 0D0) instructs the RSB to embed framing bits in RPCMO while in T1 mode.

The Embedded mode supports ITU-T Recommendation G.802, which describes how 24 T1 time slots and one framing bit (193 bits) are mapped to 32 E1 time slots (256 bits). This mapping is done by leaving TS0 and TS16 unassigned; by storing the 24 T1 time slots in TS1 to TS15, and TS17 to TS25; and by storing the frame bit in bit 1 of TS26 (see Figure 2-14). TS26 through TS31 are also unassigned.

Figure 2-14. G.802 Embedded Framing



NOTE(S):

(1) X = unused bits

(2) u = unassigned time slot (see ASSIGN bit [addr 0E0 to 0FF])

(3) F_A = T1 frame bit, frame A

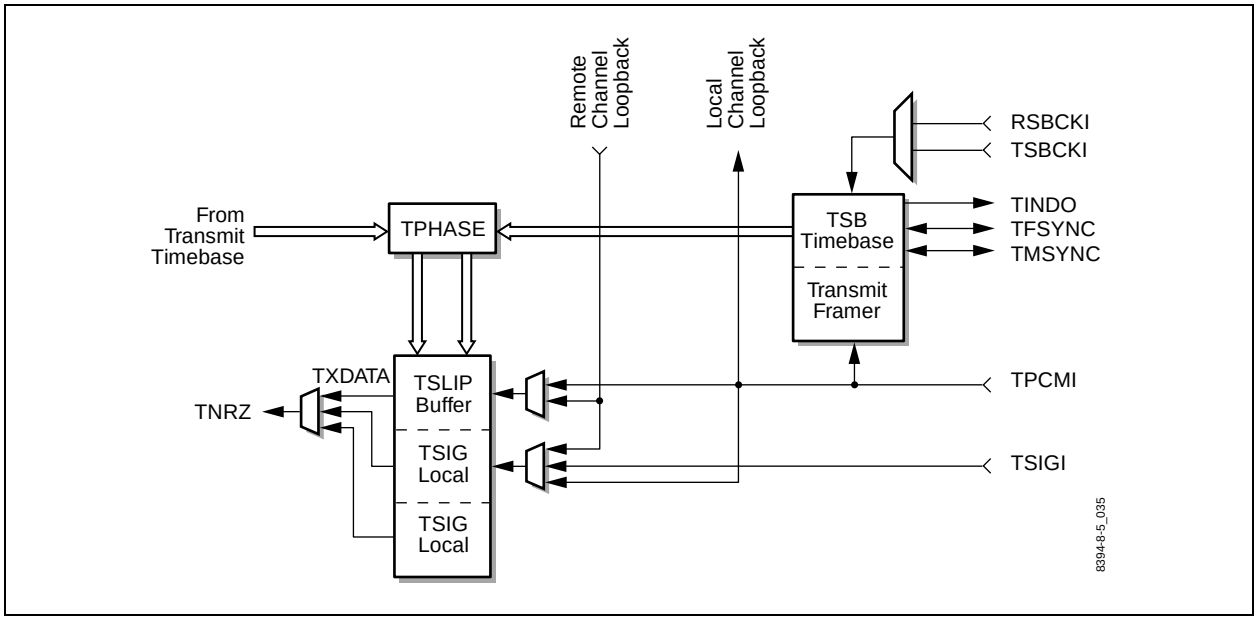
(4) F_B = T1 frame bit, frame B

(5) F_C = T1 frame bit, frame C

2.3.5 Transmit System Bus

The Transmit System Bus (TSB) consists of a timebase, slip buffer, signaling buffer, and transmit framer (Figure 2-15). It provides a high-speed serial interface between the XMTR and the system bus.

Figure 2-15. TSB Interface Block Diagram

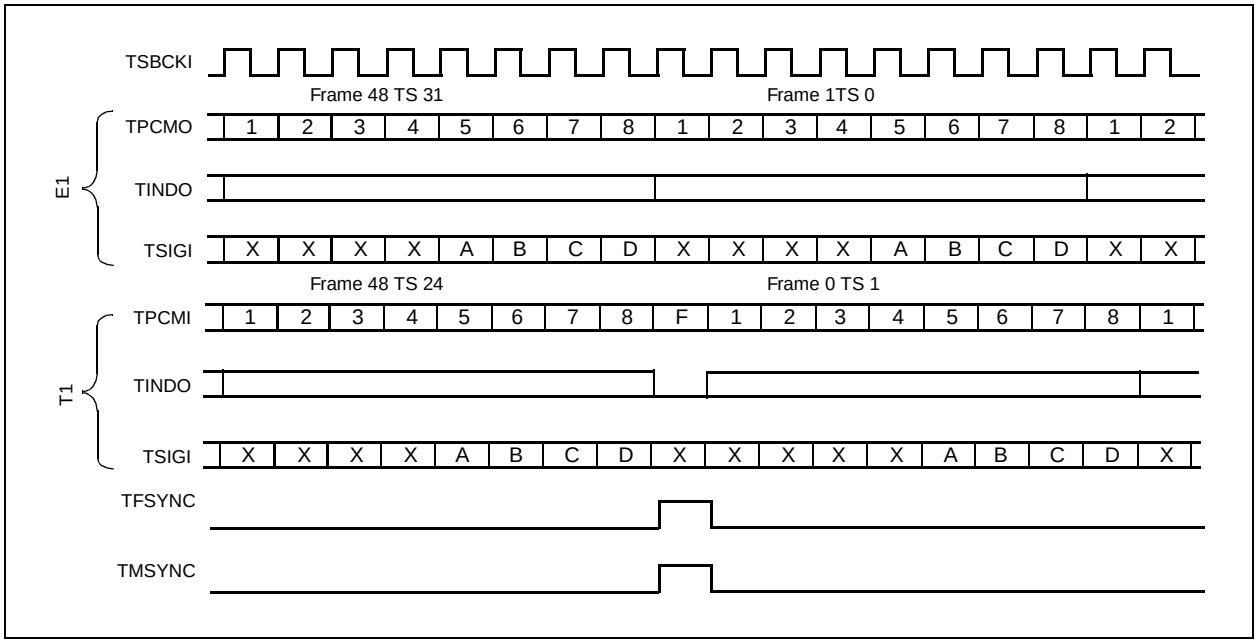


The TSB contains the following five pins:

Pin Name	Function
TSBCKI	Transmit System Bus Clock
TPCMI	Transmit PCM Data
TFSYNC/TMSYNC	Transmit Frame Sync or Transmit Multiframe Sync
TINDO/TDLCKO	Transmit Time Slot Indicator or Transmit Datalink Clock
TSIGI/TDLI	Transmit Signaling Data or Transmit Datalink Data

Refer to Figure 2-16 for the relationship between these signals. Signal definitions are provided in Table 1-6, *Hardware Signal Definitions*. TSB data outputs can be configured to input data on the rising or falling edge of TSBCKI (see the Transmit System Bus Configuration register [TSB_CR; addr 0D4].

Figure 2-16. Transmit System Bus Waveforms

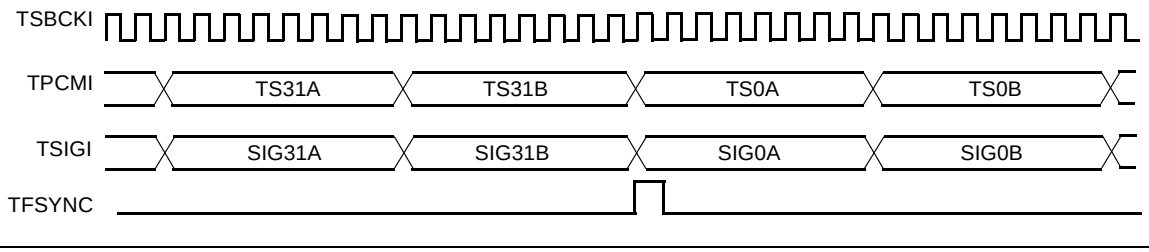


The TSB supports five different system bus rates (MHz):

- 1.536 MHz—T1 rate, 24 time slots, without framing bits
- 1.544 MHz—T1 rate with framing bits
- 2.048 MHz—E1 rate, 32 time slots
- 4.096 MHz—twice the E1 rate, 64 time slots
- 8.192 MHz—four times the E1 rate, 128 time slots.

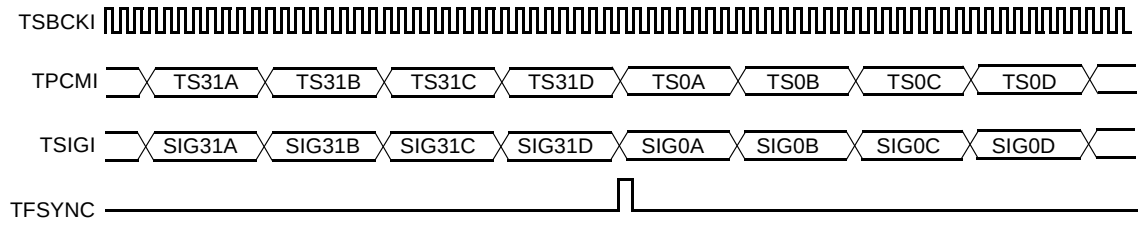
The 4.096 and 8.192 MHz bus modes contain multiple bus members (A, B, C, and D) of which one bus member is selected by the SBI [3:0] bits in the System Bus Interface Configuration register [SBI_CR; 0D0] (see Figures 2-17 and 2-18). The system bus rate is independent of the line rate and must be selected using the System Bus Interface Configuration register.

Figure 2-17. TSB 4096K Bus Mode Time Slot Interleaving



NOTE(S): A and B time slot data comes from different framers. TSBCKI can be operated at 1 or 2 times the data rate.

Figure 2-18. TSB 8192K Bus Mode Time Slot Interleaving



NOTE(S): A, B, C, and D time slot data comes from different framers. TSBCKI can be operated at 1 or 2 times the data rate.

2.3.5.1 Timebase

The TSB timebase synchronizes TPCMI, TFSYNC, TMSYNC, and TINDO with the Transmit System Bus Clock (TSBCK). The TSBCK can be slaved to three different clock sources: Transmit Clock Input (TCKI), Transmit System Bus Clock Input (TSBCKI), and Receive System Bus Clock Input (RSBCKI). The TSB clock selection is made through the Clock Input Mux register [CMUX; addr 01A]. TCKI is automatically selected when the transmit slip buffer is bypassed. The system bus clock can also be configured to run at twice the data rate by setting the X2CLK bit in the System Bus Interface Configuration register [SBI_CR; addr 0D0] when TSLIP is not in Bypass mode.

In Non-Multiplexed mode, the TFSYNC/TMSYNC dual function pin is configured for either TFSYNC or TMSYNC using the TMSYNC_EN register bit [PIO; addr 018]. TFSYNC and TMSYNC can be individually configured as inputs or outputs, [PIO; addr 018]. TFSYNC and TMSYNC should be configured as inputs when the TSB timebase is slaved to the system bus, the transmit framer is disabled [TABORT; addr 071], or TSB carries embedded T1 framing. TFSYNC and TMSYNC should be configured as outputs when the TSB timebase is master of the system bus, or the transmit framer is enabled. TFSYNC and TMSYNC can be also configured as rising or falling edge outputs [TSB_CR; addr 0D4]. In addition to having TFSYNC and TMSYNC active on the frame boundary, a programmable offset is available to select the time slot and bit offset in the frame (see Transmit System Bus Sync Time Slot Offset [TSYNC_TS; addr 0D6] and Transmit System Bus Sync Bit Offset [TSYNC_BIT; addr 0D5]).

2.3.5.2 Slip Buffer

The 64-byte Transmit PCM Slip Buffer [TSLIP; addr 140 to 17F] resynchronizes the Transmit System Bus Clock (TSBCK) and data (TPCMI) to the Transmit Clock (TXCLK) and data (TNRZ). TSLIP acts like an elastic store by clocking PCM data in on TPCMI with TSBCK and clocking TNRZ data out with TXCLK. TPCMI can be configured to sample on the rising or falling edge of TSBCKI (see the Transmit System Bus Configuration register [TSB_CR; addr 0D4]).

TSLIP has four modes of operation: Two Frame Normal, 64-bit Elastic, Two Frame Short, and Bypass. TSLIP mode is set in the Transmit System Bus Configuration register [TSB_CR; addr 0D4]. It is organized as a two-frame buffer, with high frame and low frame buffers. This allows MPU access to frame data, regardless of the TSLIP mode selected. Each byte offset into the frame buffer is a different time slot, offset 0 in TSLIP is always time slot 0 (TS0); offset 1 is always TS1, and so on. The slip buffer has processor read/write access.

Two-Frame Normal

In Normal mode, the slip buffer total depth is two 193-bit frames (T1), or two 256-bit frames (E1). Data is written to the slip buffer using TSBCK and read from the slip buffer using TXCLK. If there is a slight rate difference between the two clocks, the slip buffer changes from its initial condition—approximately half full—by either adding or removing frames. If TSBCK writes to the slip buffer faster than TXCLK reads the data, the buffer becomes full. When the slip buffer in Normal mode is full, an entire frame of data is deleted. Conversely, if TXCLK is reading the slip buffer at a faster rate than TSBCK is writing the data, the buffer will eventually empty, and an entire frame of data is duplicated. When an entire frame is deleted or duplicated, it is known as a Frame Slip (FSLIP). An FSLIP is always one full frame of data. The FSLIP status is reported in the Slip Buffer Status register [SSTAT; addr 0D9].

64-Bit Elastic

In 64-bit Elastic mode, the slip buffer total depth is 64 bits and the initial throughput delay is 32 bits, or one-half of the total depth. Similar to Normal mode, Elastic mode allows the system bus to operate at any of the programmable bus rates, independent of the line rate. The advantage of this mode over the two-frame mode is that throughput delay is reduced from one frame to an average of 32 bits, and the transmit multiframe can retain its alignment with respect to the transmit data. The disadvantage of this mode is handling the full and empty buffer conditions. In 64-bit Elastic mode, an empty or full buffer condition causes an Uncontrolled Slip (USLIP). Unlike an FSLIP, a USLIP is of unknown size, ranging from 1 to 256 bits of data. The USLIP status is reported in SSTAT.

Two-Frame Short

The Two-Frame Short mode combines the depth of the Normal mode with the throughput delay of the Elastic mode. This mode begins in Elastic mode with a 32-bit initial throughput delay, and switches to Normal modes when the buffer is empty or full; thereafter, the Two-Frame Short and Normal modes perform identically. If the slip buffer is full (two frames) in the Two-Frame Short and normal modes, an FSLIP is reported; thereafter, the slip buffer performs exactly like Normal mode.

Bypass

In Bypass mode, data is clocked through TSLIP from the TSB to the XMTR using TXCLK as selected by the TXCLK input clock mux.

2.3.5.3 Signaling Buffer

The 32-byte Transmit Signaling Buffer [TSIG; addr 120–13F] stores a single multiframe of signaling data input from TSIGI pin and is updated as each time slot is received in every TSB frame. Each byte offset into TSIG is a different time slot's signaling data: offset 0 stores TS0 signaling data, offset 1 stores TS1 signaling data, etc. The signaling data is stored in the least significant 4 bits of the signaling buffer. Similar to TSLIP, TSIG has read/write processor access for accessing or overwriting signaling information. TFSYNC is used by the signaling buffer to identify the frame boundaries in the TSIGI data stream.

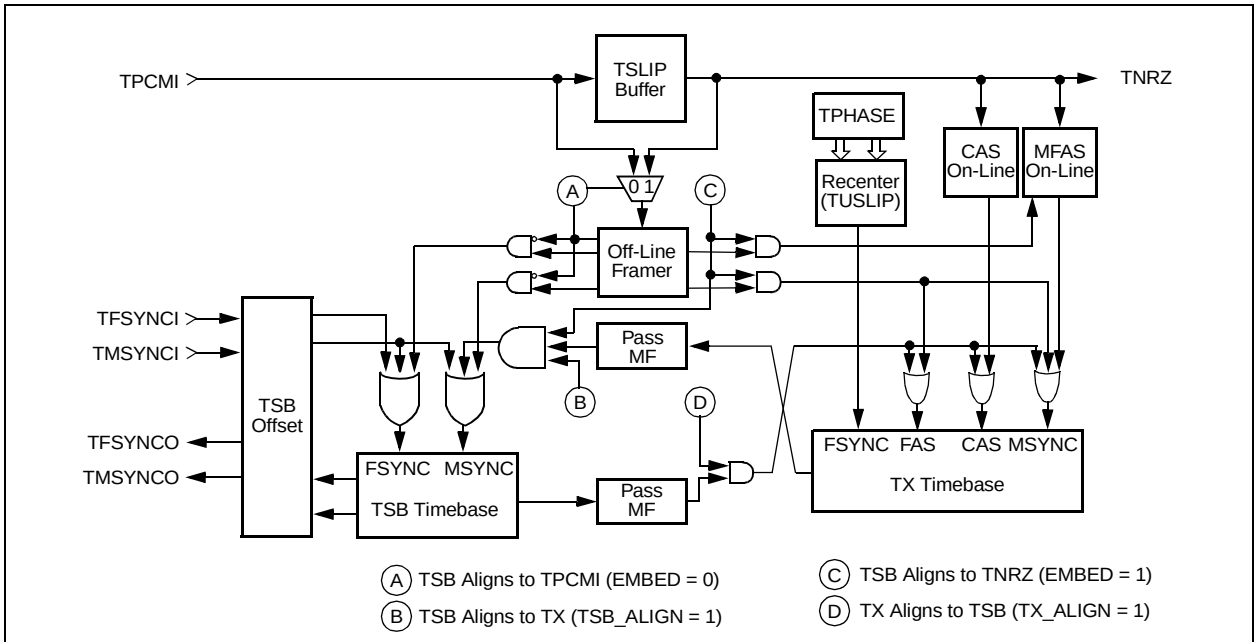
2.3.5.4 Transmit Framing

A transmit framing option is provided to allow the transmitter to automatically align to the transmit PCM data on TPCMI. In this mode, the Transmit Framer searches transmit data for a valid E1 or T1 framing pattern. The transmit data stream has two framing functions: offline framer and an online framer. The offline framer recovers the transmit frame alignment (TFSYNC). The online framer monitors the frame alignment found by the offline framer and recovers multiframe alignment (TMSYNC).

Transmit Frame Alignment

Transmit frame resynchronization is initiated by activating the Transmit Loss Of Frame (TLOF) status bit in the Alarm 2 status [ALM2; addr 048] register by the online framer. The TLOF criteria is set in the TLOFA, TLOFB, and TLOFC bits of the Transmitter Configuration register [TCR1; addr 071]. The online framer supports the following LOF criteria for T1: 2 frame bit errors out of 4, 2 out of 5, or 2 out of 6; for E1, it supports 3 out of 3. Figure 2-19 illustrates transmit framing and timebase alignment options.

Figure 2-19. Transmit Framing and Timebase Alignment Options



NOTE(S):
(1) EMBED located in SBI_CR (addr 0D0).
(2) TSB_ALIGN and TX_ALIGN located in TSB_CR (addr 0D4).

When TLOF is asserted, the offline framer searches the transmit data stream for a new frame alignment, provided that transmit framing is enabled [TABORT; addr 071]. If embedded framing is enabled [EMBED; addr 0D0], the offline framer examines the TSLIP buffer output—TNRZ—for transmit frame alignment. If embedded framing is disabled, the offline framer examines the slip buffer input (TPCMI) for transmit frame alignment. This case (EMBED = 0) is only applicable if TPCMI is configured to operate at the line rate—2,048 kbps E1, or 1,544 kbps T1. If transmit framing is disabled, the offline framer waits for a reframe command [TFORCE; addr 071] before beginning a frame alignment search.

Transmit Multiframe Alignment

After the offline framer recovers frame alignment, the online framer monitors TLOF and searches for multiframe alignment using criteria defined by the Transmit Frame mode [TFRAME; addr 070]. The online framer conducts a multiframe alignment search each time the offline framer recovers transmit frame alignment—as reported by high-to-low transition of transmit loss of frame status [TLOF; addr 048]. After TLOF recovery, the online framer searches continuously for multiframe alignment until the correct pattern sequence is located, or until basic frame alignment is lost (TLOF goes active-high). After multiframe alignment recovery, the online framer checks subsequent multiframes for errored alignment patterns, but does not use those errors as part of the criteria for loss of basic frame alignment.

Note that the online framer's multiframe search status is not directly reported to the processor, but instead is monitored by examination of transmit error status: TMERR, TSERR, and TCERR [addr 00B]. If the system incorporates a certain number of multiframe pattern errors (or a certain error ratio) into the loss of transmit frame alignment criteria, the processor must count multiframe pattern errors to determine when to force a transmit reframe [TFORCE; addr 071].

Transmit Frame Alignment Criteria

The frame synchronization criteria used by the offline framer is set in the TFRAME[3:0] of the Transmit Framer Configuration register [TCR0; addr 070]. (Tables 3-15 and 3-16 illustrate supported transmit framing formats. Also, see Tables 3-17 and 3-18, Criteria for Loss/Recovery of Transmit Frame Alignment.)

Transmit/Receive Framer Arbitration

The offline framer is shared between the RCVR and XMTR and can only search in one direction at a time. Consequently, the host processor can manually arbitrate between RCVR and XMTR reframe requests by manipulating the ABORT and FORCE controls, or by allowing the framer to automatically arbitrate LOF requests.

The offline framer waits until the current search is complete [FSTAT; addr 017] before checking for pending LOF reframe requests. If both online framers have pending reframe requests, the offline framer aligns to the opposite direction of that most recently searched. For example, if TLOF is pending at the conclusion of a receive search which timed out without finding alignment, the offline framer switches to search in the transmit direction. The TLOF switchover is prevented in the preceding example if the processor asserts TABORT to mask the transmit reframe request. TABORT does not affect TLOF status reporting. For applications that frame in only one direction, framing in the opposite direction must be masked. If, at the conclusion of a receive search timeout, TLOF status is asserted but masked by TABORT, the offline framer continues to search in the receive direction.

For applications that frame in both directions, the processor can manually arbitrate among pending reframe requests by controlling the reframe precedence. An example of manual control follows:

1 Initialize RABORT = 1 and TABORT = 1.

2 Enable RLOF and TLOF interrupts.

3 Read clear pending ISR interrupts.

4 Release RABORT = 0.

5 Call LOF Service Routine if either RLOF or TLOF interrupt;
{
(check current LOF status (ALMI, 2; addr 047, 048)
If RLOF recovered and TLOF lost
—Assert RABORT = 1
—Release TABORT = 0
If RLOF lost or TLOF recovered
—Assert TABORT = 1
—Release RABORT = 0
}

The status of the offline framer can be monitored using the Offline Framer Status register [FSTAT; addr 017]. The register reports the following: whether the offline framer is looking at the receive or transmit data streams (RX/TXN); whether the framer is actively searching for frame alignment (ACTIVE); whether the framer found multiple framing candidates (TIMEOUT); whether the framer found frame sync (FOUND); and whether the framer found no frame alignment candidates (INVALID).

2.3.5.5 Embedded Framing

Embedded framing mode [EMBED; addr 0D0] instructs the transmit framer to search TSLIP buffer output (TNRZ) for framing bits while in T1 mode, or for MFAS and CAS in E1 mode. Embedded framing allows the transmit timebase to align with the transmit framer multiframe alignment of the PCM signal transported across the system bus.

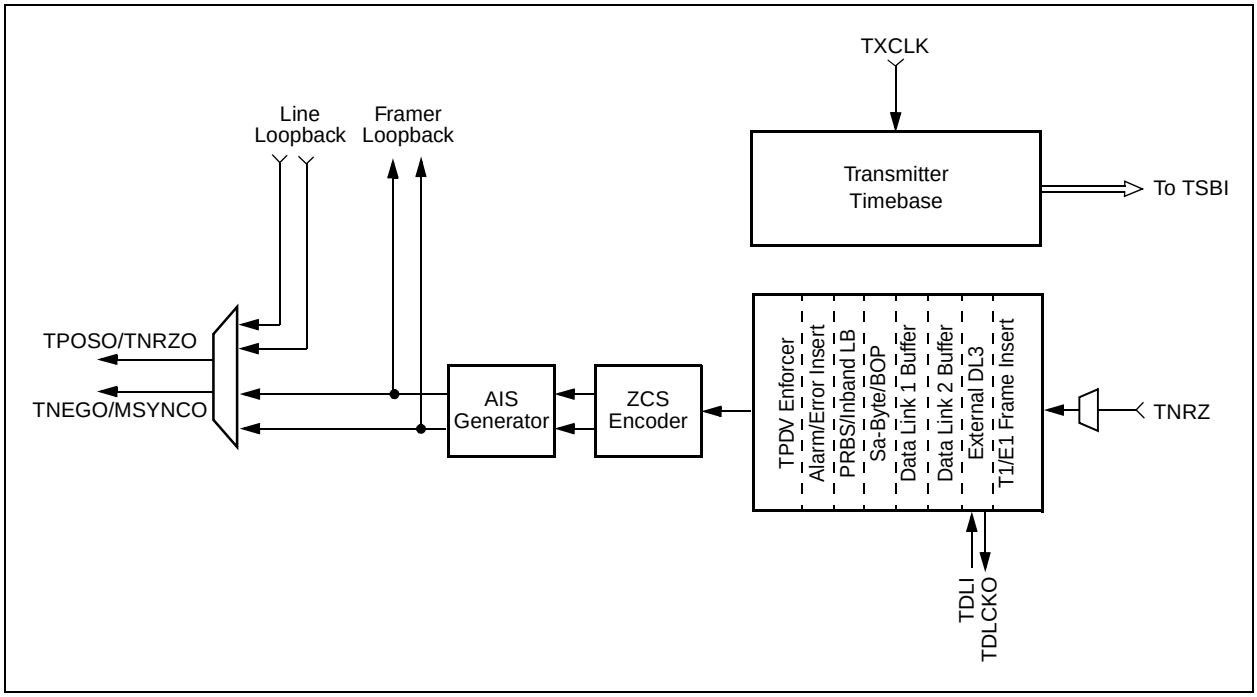
The Embedded mode supports ITU-T Recommendation G.802, which describes how 24 T1 time slots and framing bit (193 bits) are mapped to the 32 E1 time slots (256 bits): by leaving TS0 and TS16 unassigned; by storing the 24 T1 time slots in TS1 to TS15, and in TS17 to TS25; and by storing the frame bit in Bit 1 of TS26 (see Figure 2-14, *G.802 Embedded Framing*).

2.4 Transmitter

The Transmitter (XMTR) inserts T1/E1 overhead data and outputs single rail NRZ data from the TSB or ZCS-encoded P and N rail NRZ data. The CX28395 only provides single rail NRZ transmit signals.

The XMTR, Figure 2-20, consists of the following elements: two Transmit Data Links, Test Pattern Generator, In-Band Loopback Code Generator, Overhead Pattern Generator, Alarm Generator, Zero Code Suppression (ZCS) Encoder, External Transmit Data Link (CX28394 and CX28398 only), CRC Generation, Framing Pattern Insertion, and Far End Block Error Generator.

Figure 2-20. XMTR Diagram



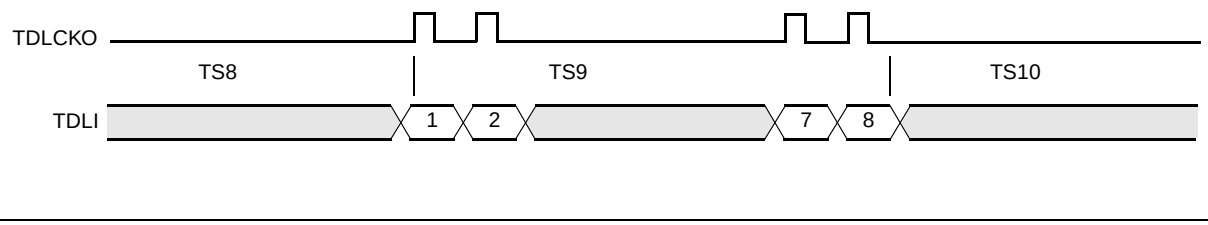
2.4.1 External Transmit Data Link (CX28394 and CX28398 Only)

The External Data Link (DL3) allows the system to externally supply any bit(s) in any time slot in all frames, odd frames or even frames, including T1 framing bits. Pin access to the DL3 transmitter is provided through TDLCKO and TDLI. These two pins serve as the TDL3 clock output (TDLCKO) and data input (TDLI). The mode of the pins is selected using the TDL_IO bit in the Programmable Input/Output register [PIO; addr 018].

Control of DL3 format is provided in two registers: External Data Link Channel [DL3_TS; add 015] and External Data Link Bit [DL3_BIT; addr 016]. Transmit DL3 is set up by selecting the bit(s) [DL3_BIT], time slot [TS[4:0]; addr 015], and frames [EVEN/ODD; addr 015] to be overwritten, then enabling the data link [DL3EN; addr 015]. Enabling the data link will start TDLCKO gating the NRZ data provided on TDLI (see Figure 2-21).

NOTE: DL3 signals are not provided on the CX28395. Therefore, DL3_TS must be written to 00 to disable the DL3 transmitter and prevent transmit data corruption.

Figure 2-21. Transmit External Data Link Waveforms



NOTE(S): This example shows bits 1, 2, 7, and 8 of TS9 selected. Any combination of time slot bits can be selected.

2.4.2 Transmit Data Links

The XMTR contains two independent data link controllers (DL1, DL2), a Performance Report Message (PRM) generator, and a Bit-Oriented Protocol (BOP) transceiver. DL1 and DL2 can be programmed to send and receive HDLC formatted messages in the Message Oriented Protocol (MOP) mode or unformatted serial data over any combination of bits within a selected time slot or F-bit channel. The PRM message generator can immediately or automatically send one-second performance reports. The BOP transceiver can preemptively transmit BOP messages, such as ESF Yellow Alarm.

2.4.2.1 Data Link Controllers

DL1 and DL2 control serial data channels operating at multiples of 4 kbps up to the full 64 kbps time slot rate by selecting a combination of bits from odd, even, or all frames. Both data link controllers support ESF Facilities Data Link (FDL), SLC-96 data link, Sa data link, Common Channel Signaling (CCS), Signaling System #7 (SS7), ISDN LAPD channels, Digital Multiplexed Interface (DMI) signaling in TS24, as well as the latest ETSI V.51 and V.52 signaling channels. DL1 and DL2 each contain a 64-byte transmit buffer which function either as programmable length circular buffers in transparent (unformatted) mode, or as full-length data FIFOs in formatted (HDLC) mode.

DL1 and DL2 are configured identically, except for their offset in the register map. The DL1 address range is 0A4 to 0AE, and the DL2 address range is 0AF to 0B9. From this point on, the DL1 is used to describe the operation of both data link controllers. Transmit Data Link 1 (TDL1) can be viewed as having a higher priority than Transmit Data Link 2 (TDL2) because TDL1 overwrites the primary rate channel after TDL2. Thus, any data that TDL2 writes to the primary rate channel can be overwritten by TDL1, if TDL1 is configured to transmit in the same time slot as TDL2.

The TDL1 is enabled using the DL1 Control register [DL1_CTL; addr 0A6]. TDL1 will not overwrite time slot data until it is enabled. DL1_CTL also controls the data format and the circular buffer/FIFO mode.

The following data formats [DL1[1,0]; addr 0A6] are supported on the data link: Frame Check Sequence (FCS), non-FCS, Pack8, or Pack6. FCS and non-FCS are HDLC-formatted messages. Pack8 and Pack6 are unformatted messages with 8 bits per FIFO access, and 6 bits per FIFO access, respectively.

2.4.2.2 Circular Buffer

The Circular Buffer/FIFO control bit [TDL1_RPT; addr 0A6] allows the FIFO to act as a circular buffer; in this mode, a message can be transmitted repeatedly. This feature is available only for unformatted transmit data link applications. The processor can repeatedly send fixed patterns on the selected channel by writing a 1- to 64-byte message into the circular buffer. The programmed message length repeats until the processor writes a new message. The first byte of each unformatted message is output automatically, aligned to the first frame of a 24-, or 16-frame transmit multiframe (SF/ESF/MFAS). This allows the processor to source overhead or data elements aligned to the TX timebase. In both SF and ESF T1 modes, unformatted messages are aligned on 24-frame boundaries. Therefore, in SF applications the repeating message must be designed to span two SF multiframes.

Each unformatted message written is output-aligned only after the preceding message completes transmission. Therefore, data continuity is retained during the linkage of consecutive messages, provided that the contents of each message consists of a multiple of the multiframe length.

2.4.2.3 Time Slot and Bit Selection

Time slot and bit selection is done through the DL1 Time Slot Enable [DL1_TS; addr 0A4] and DL1 Bit Enable [DL1_BIT; addr 0A5] registers. DL1_TS selects which frames and which time slot will be overwritten. The frame select allows TDL1 to overwrite the time slot in either all frames, odd frames, even frames, or in a special 2 kbps mode. The time slot word enable is a value between 0 and 31 that selects which time slot will be filled with data from the transmit data link buffer. DL1_BIT selects which bits will be overwritten in the time slot selected. Table 2-5 lists commonly used data link settings.

Table 2-5. Commonly Used Data Link Settings

Data Link	Frame	Time Slot	Time Slot Bits	Mode
ESF FDL	Odd	0 (F-bits)	Don't Care	FCS
T1DM R Bit	All	24	00000010	FCS
SLC-96	Even	0 (F-bits)	Don't Care	Pack6
ISDN LAPD	All	N	11111111	FCS
CEPT Sa4	Odd	1	00001000	FCS
NOTE(S): N represents any T1/E1 time slot.				

2.4.2.4 Transmit Data Link FIFO Buffer

The Transmit Data Link FIFO #1 [TDL1; addr 0AD] is a versatile, 64-byte buffer that can be used as a single-byte transmit buffer or for any number of bytes up to 64. As a single-byte FIFO, the Transmit FIFO Empty Status (TMPTY1) in TDL #1 Status [TDL1_STAT; addr 0AE] and Transmit FIFO Empty Interrupt (TEMPTY) in Data Link 1 Interrupt Status (ISR2; addr 009] can be used to do byte-by-byte transmissions.

Using the Transmit Data FIFO, an entire block of data can be transmitted with very little microprocessor interrupt overhead. Block transfers to the FIFO can be controlled by the Near Empty Threshold in the FIFO Empty Control register [TDL1_FEC; addr 0AB]. The Near Empty Threshold is a user-programmable value between 0 and 64 that represents the minimum number of bytes that can be left in the transmit FIFO before near empty is declared. Once the threshold is set, the Near Empty Status (TNEAR1) in TDL #1 Status [TDL1_STAT; addr 0AE] will be asserted whenever the Near Empty Threshold is reached. An interrupt, TNEAR in the Data Link 1 Interrupt Status register [ISR2; addr 009], is also available to mark this event.

2.4.2.5 End of Message

Once an entire message is written to the transmit FIFO or circular buffer, the processor must indicate the end of message by writing any value to the TDL #1 End Of Message (EOM) Control [TDL1_EOM; addr 0AC]. In FCS mode, the EOM indicates that the FCS is to be calculated and transmitted following the last byte in the FIFO. In the circular buffer mode, the EOM indicates the end of the transmit circular buffer.

2.4.2.6 Programming the Data Link Controller

The Transmit Data Link Controller can be programmed according to the system CPU bandwidth. For systems with sufficient CPU bandwidth, the data link status can be polled, and the 64-byte transmit FIFO buffer can be used as a single-byte transmit buffer. For systems with limited CPU bandwidth, the data link can be interrupt-driven, and the entire 64-byte transmit FIFO buffer can be used to store entire messages. See Figures 2-22 and 2-23 for a high level description of polling and interrupt-driven Transmit Data Link Controller software.

The device uses a hierarchical interrupt structure, with one top-level interrupt request register directing software to the lower levels (see Master Interrupt Request register; addr 081 and Interrupt Request register; addr 003). Of all the interrupt sources, the two most significant bandwidth requirements are signaling and data link interrupts. Each data link controller has a top-level interrupt status register that reports data link operations (see Data Link 1 and 2 Interrupt Status registers [ISR2; addr 009, and ISR1; 00A]). The processor uses a three-step interrupt scheme for the data link:

1. Read the Master Interrupt Request register to determine which framer is interrupted.
2. Read the Interrupt Request register for that framer.
3. Use that register value to read the corresponding Data Link Interrupt Status register.

Figure 2-22. Polled Transmit Data Link Processing

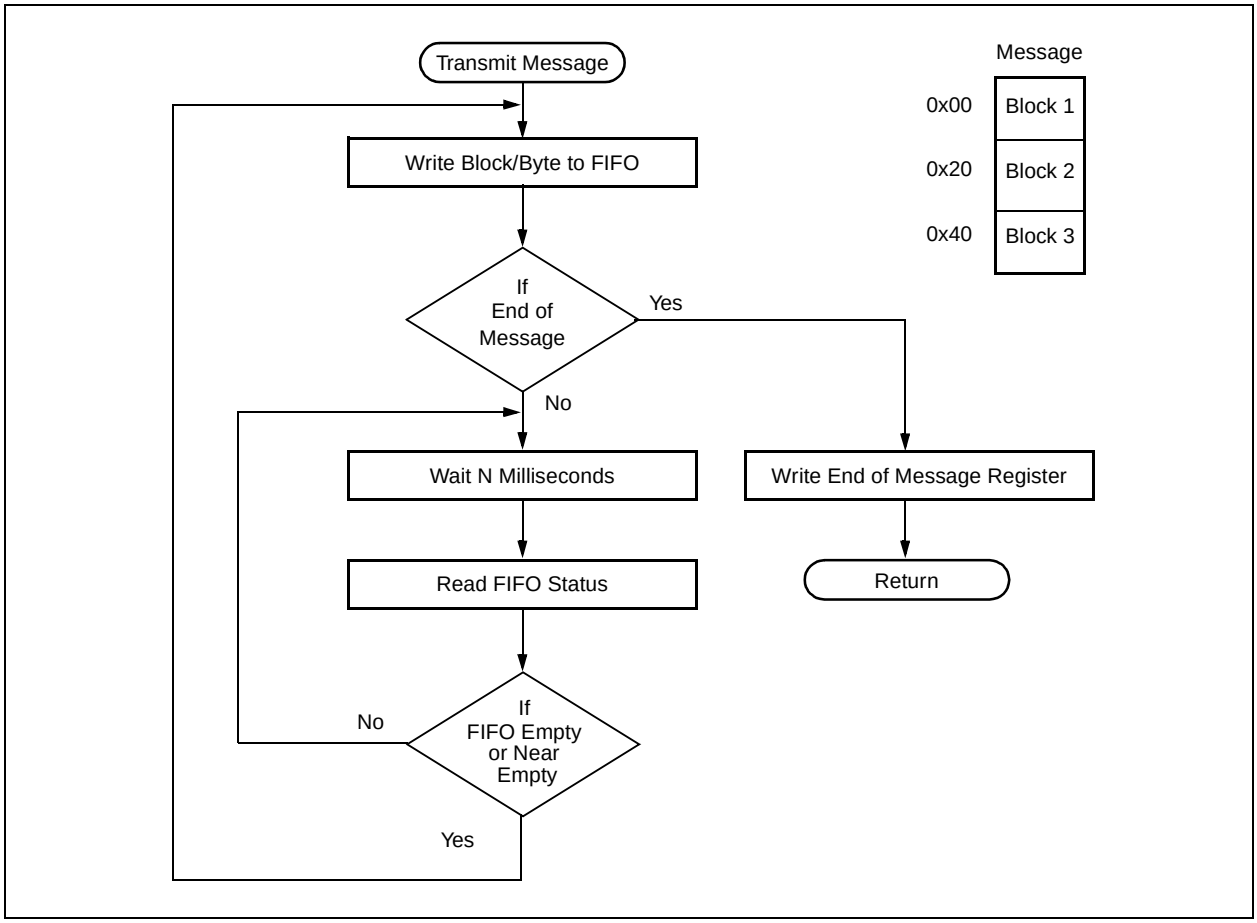
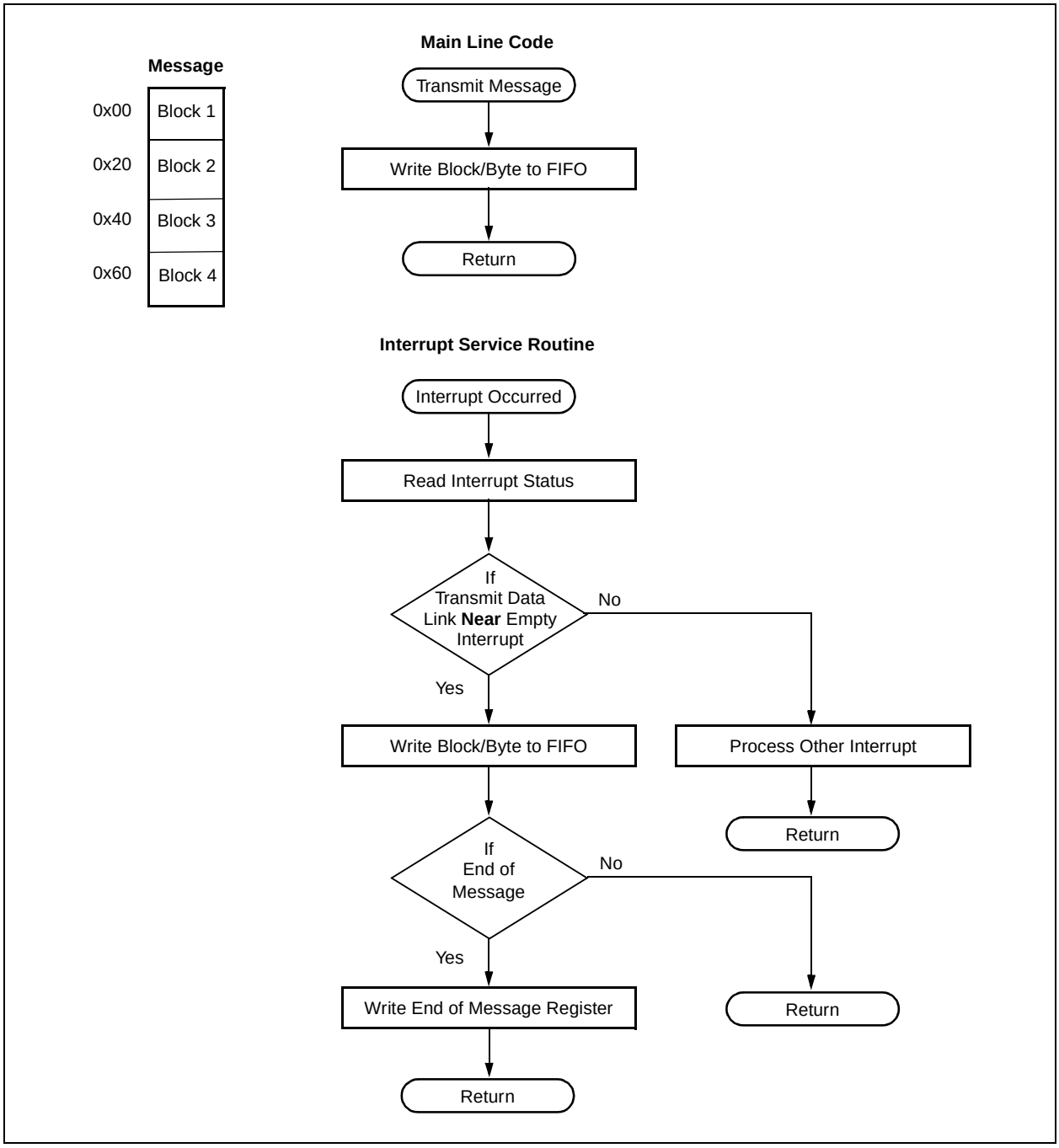


Figure 2-23. Interrupt-Driven Transmit Data Link Processing



2.4.2.7 PRM Generator

In T1 applications, Performance Report Messages (PRMs) are HDLC messages containing path identification and performance monitoring information. If automatic performance report insertion is selected [AUTO_PRM; addr 0AA], a performance report is generated each second and begins transmitting coincident with the one-second timer interrupt [ONESEC; addr 005]. The PRM is sent immediately if the processor sets SEND_PRM bit in the Performance Report Message register [PRM; addr 0AA]. All performance monitoring fields of the message are automatically filled in when a PRM is generated. The remaining PRM bit fields are application-specific and can be configured using the Performance Report Message register.

For limited systems, the automatic PRM generation off-loads a significant portion of CPU bandwidth.

2.4.2.8 TBOP Transceiver

The Transmit Bit-Oriented Protocol (TBOP) transceiver sends BOP messages in T1 applications, including ESF Yellow Alarm. These messages consist of repeated 16-bit patterns with an embedded 6-bit codeword, as shown in this example:

```
0xxxxxx0 11111111 (transmitted right to left)
[543210] TBOP = 6-bit codeword
```

The TBOP is configured to operate over the same channel selected by Data Link #1 [DL1_TS; addr 0A4]. The TBOP channel must be configured to operate over the FDL channel in order for TBOP to convey Priority, Command, and Response codeword messages according to ANSI T1.403, Section 9.4.1. The precedence of transmitted BOP messages with respect to current DL1 transmit activity is configurable using the Transmit BOP mode bits [TBOP_MODE[1,0]; addr 0A0]. BOP messages can also be transmitted during E1 mode, although the 16-bit codeword pattern has not currently been adopted as an E1 standard. The length of the BOP message [TBOP_LEN[1,0]; addr 0A0] can be set to a single pattern, 10 patterns, 25 patterns, or continuous.

BOP codewords are transmitted by writing to the Transmit BOP Codeword [TBOP; addr 0A1]. The real-time status of the codeword transmission can be monitored using TBOP_ACTIVE in the BOP Status register [BOP_STAT; addr 0A3]. A TBOP Transmit interrupt is available in the Data Link 1 Interrupt Status register [ISR2; addr 009] to indicate that a codeword has begun transmission and the next codeword may be written to TBOP.

2.4.3 Sa-Byte Overwrite Buffer

There are five transmit Sa-Byte buffers [TSA4 to TSA8; addr 07B to 07F]. The Sa-Byte buffers insert Sa-bits into the odd frames of TS0. The entire group of 40 bits is sampled every 16 frames coincident with the Transmit Multiframe bit interrupt boundary [TMF; addr 008]. Bit 0 from each TSA register is then inserted during frame 1, bit 1 is inserted during frame 3, bit 2 during frame 5, and so on, which gives the processor up to 2 ms after TMF interrupt to write new Sa-Byte buffer values. Transmit Sa-bits maintain a fixed relationship to the transmit CRC multiframe. Each of the 5 Sa-Byte transmit buffers can be individually enabled using the Manual Sa-Byte Transmit Enable in Transmit Manual Sa-Byte/FEBE Configuration register [TMAN; addr 074].

2.4.4 Overhead Pattern Generation

The transmit overhead generation circuitry provides the ability to insert all of the overhead associated with the Primary Rate Channel. The following types of overhead pattern generation are supported: Framing patterns, Alarm patterns, Cyclic Redundancy Check (CRC), and Far-End Block Error (FEBE).

2.4.4.1 Framing Pattern Generation

The framing pattern generation circuitry inserts the 2-bit terminal framing (Ft) pattern, the 6-bit signaling frame (Fs) pattern, the 6-bit FPS pattern, the 8-bit FAS/NFAS pattern, and the 6-bit MFAS pattern into the transmit data stream.

The Ft pattern in SF, SLC-96, and T1DM is inserted into the transmit data stream by enabling the INS_FBIT in the Transmit Frame Format register [TFRM; addr 072]. The Fs pattern in SF is inserted by enabling the INS_MF bit. The FPS pattern in T1-ESF and the FAS/NFAS pattern in E1 mode are inserted by enabling the INS_FBIT bit. The MFAS pattern is inserted by enabling the INS_MF bit.

2.4.4.2 Alarm Generation

The Transmit Alarm Generation circuitry generates Alarm Indication Signal (AIS) and Remote Alarm Indication (RAI/Yellow Alarm).

AIS Generation

AIS is an unframed all-ones pattern and is normally transmitted when the data source is lost. AIS transmission can be enabled:

1. manually,
2. automatically upon detection of transmit loss of clock, and
3. automatically upon loss of received signal.

Typical applications require transmission of AIS toward the line when DTE transmit data or clock is not present. In most applications, DTE data and clock are isolated from the transmitter requiring manual AIS transmission under software control. Manual insertion of AIS is controlled by the TAIS bit in Transmit Alarm Signal Configuration register [TALM; addr 075]. Setting this bit overwrites the currently transmitted data with the AIS pattern. If AISCLK [TLIU_CR; addr 068] is also set, AIS is transmitted using an alternate transmit line rate clock supplied on E1ACKI (for E1) or T1ACKI (for T1) pins.

Automatic transmission of AIS can be controlled by detection of transmit loss of clock [TLOC; addr 048]. This mode is enabled by setting AISCLK and providing an alternate transmit line rate clock on the E1ACKI or T1ACKI pin. If no transitions are detected on the TCKI pin for eight cycles of E1ACKI or T1ACKI, TLOC is set and AIS is transmitted. AIS is terminated and TLOC cleared when TCKI returns.

By setting AUTO_AIS in the TALM register, automatic transmission of AIS can also be controlled by detection of Receiver Loss Of Signal [RLOS; addr 047]. This mode is typically used to transmit AIS (keep-alive) during line loopback if the received signal is lost. Setting AUTO_AIS simultaneously with setting LLOOP [LOOP; addr 014] enables this operation.

Yellow Alarm Generation

Yellow Alarm, also referred to as RAI (Remote Alarm Indication), is a bit pattern inserted into the transmit stream to alert far-end equipment that the local receiver cannot recover data. Yellow Alarm/RAI is typically transmitted during receive loss of frame and is defined differently depending upon the transmit frame format configured [TFRAME; addr 070]. Table 2-6 describes the Yellow Alarm/RAI transmitted for each frame format.

Table 2-6. Yellow Alarm Generation

Frame Format	Yellow Alarm Transmitted	Mode
SF	Bit 2 of every time slot set to zero	YB2
ESF(1)	Bit 2 of every time slot set to zero	YB2
SLC-96	Bit 2 of every time slot set to zero	YB2
SF/JYEL	F-bit 12 of every superframe set to one	YJ
T1DM	Y bit of the sync byte set to zero	Y24
E1	The A bit of TS0 set to one	Y0

NOTE(S):
(1) Yellow Alarm/RAI for T1-ESF framing is defined as a BOP priority codeword in the FDL channel. T1-ESF Yellow Alarm/RAI is not transmitted using the procedure described below. Instead, T1- ESF Yellow Alarm/RAI is generated by configuring DL1 to continuously transmit an all zeros BOP priority codeword. Refer to Section 2.4.2, *Transmit Data Links*.

Transmission of Yellow Alarm/RAI is controlled by these register bits:

Bit Name	Register
INS_YEL	TFRM; addr 072]
TYEL	TALM; addr 075]
AUTO_YEL	TALM; addr 075]
RLOF	ALM1; addr 047]
RLOF_INTEG	RALM; addr 045]

Insertion of Yellow Alarm/RAI into the transmit stream is controlled by INS_YEL. Yellow Alarm/RAI is inserted only when INS_YEL is set, otherwise these bit positions are supplied by data from TPCMI. Yellow Alarm/RAI generation can be done manually or automatically.

Manual generation of Yellow Alarm/RAI is controlled by TYEL. Setting this bit will immediately and unconditionally overwrite the Yellow Alarm/RAI signal bit(s) in the transmitted data stream with the appropriate pattern.

Automatic generation of Yellow Alarm/RAI is controlled by AUTO_YEL, RLOF, and RLOF_INTEG. If AUTO_YEL is set, Yellow Alarm/RAI is generated during a receive loss of frame alignment (RLOF = 1). Optionally, RLOF integration can be enabled by setting RLOF_INTEG. In this case, both RLOF indication and Yellow Alarm/RAI generation are delayed for approximately 2.5 seconds if a continuous out-of-frame condition exists. Yellow Alarm/RAI generation continues for at least 1 second after RLOF clears.

Multiframe Yellow Alarm Generation

In E1 CAS framing modes, Multiframe Yellow Alarm is inserted into the transmit stream to alert far-end equipment that local received multiframe alignment is not recovered. E1 Multiframe Yellow Alarm is transmitted by setting the Y bit in time slot 16, frame 0.

Transmission of Multiframe Yellow Alarm is controlled by these register bits:

Bit Name	Register
INS_MYEL	[TFRM; addr 072]
TMYEL	[TALM; addr 075]
AUTO_MYEL	[TALM; addr 075]
SRED	[ALM3; addr 049]

Insertion of E1 Multiframe Yellow Alarm is controlled by INS_MYEL and inserted only when INS_MYEL is set. Multiframe Yellow Alarm generation can be initiated manually or automatically.

Manual insertion of Multiframe Yellow Alarm is controlled by TMYEL. Setting this bit will unconditionally overwrite the Multiframe Yellow Alarm signal bit in the transmitted data stream.

Automatic insertion of Multiframe Yellow Alarm is controlled by AUTO_MYEL in the TALM register. When set, the AUTO_MYEL mode will send yellow alarm for the duration of a receive loss of CAS multiframe alignment [SRED; addr 049]

2.4.4.3 CRC Generation

The CRC generation circuitry computes the value of the CRC6 code in T1 mode or the CRC4 code in E1 mode. Once computed, it is inserted into the appropriate position of the transmitted data stream. CRC overwrite is enabled by INS_CRC [TFRM; addr 072]. In T1 mode, CRC6 may be computed on only the payload data or on all data including the F-bit. Setting TINCF [TCR0; addr 070] selects CRC6 computation on all data.

If the transmit frame format is configured as ESF and INS_CRC is active, the 2 kbps CRC sequence is inserted. The position of the CRC-6 bits is shown in Table A-4, *Extended Superframe Format*.

If the transmit frame format is configured as E1, and INS_CRC is active, the 4 kbps CRC sequence is inserted. The position of the CRC-4 bits is shown in Table A-6, *ITU–T CEPT Frame Format Time Slot 0 Bit Allocations*.

2.4.4.4 Far-End Block Error Generation

The register bits that control FEBE are INS_FE [TFRM; addr 072], TFEBE [TMAN; addr 074], FEBE_I [TMAN; addr 074], and FEBE_II [TMAN; addr 074]. The Far-End Block Error (FEBE) generation circuitry inserts FEBE bits automatically or manually. Automatic FEBE generation is enabled by INS_FE. If the transmit frame format is configured as E1 and INS_FE bit is set, a FEBE is generated in response to an incoming CRC-4 error by setting an E-bit of TS0 to zero. Refer to Table A-6, *ITU–T CEPT Frame Format Time Slot 0 Bit Allocations*, for the location of the E-bits within the E1 frame.

Manual FEBE generation is enabled by TFEBE. If the transmit frame format is configured as E1 and TFEBE is set, the FEBE bits are supplied by the processor in FEBE_I and FEBE_II.

2.4.5 Test Pattern Generation

The transmit test pattern generation circuitry overwrites the transmit data with various test patterns and permits logical and frame-bit error insertion. This feature is particularly useful for system diagnostics, production testing, and test equipment applications. The test pattern can be a framed or unframed PRBS pattern. The PRBS patterns available include 2E11-1, 2E15-1, 2E20-1, and 2E23-1. Each pattern can optionally include Zero Code Suppression (ZCS). Error insertion includes LCV, BPV, Ft, CRC4, CRC6, COFA, PRBS, Fs, MFAS, and CAS.

The Transmit Test Pattern Configuration register [TPATT; addr 076] controls the test pattern insertion circuit. TPATT controls the PRBS pattern (TPATT[1:0]) bits), ZCS setting (ZLIMIT bit), T1/E1 framing (FRAMED bit), and starting and stopping transmission (TPSTART bit).

Patterns are generated in accordance with ITU–T O.150 (10/92), O.151 (10/92), and O.152 (10/92). Enabling ZLIMIT modifies the inserted pattern by limiting the number of consecutive zeros. For the 2E11-1 or 2E15-1 PRBS patterns, eight or more zeros will not occur with ZLIMIT enabled. For the 2E20-1 or 2E23-1 PRBS patterns, 15 or more zeros will not occur with ZLIMIT enabled.

Note that the QRSS pattern is a 2E20-1 PRBS with ZLIMIT enabled. This function is performed according to ANSI T1.403 and ITU–T O.151 (10/92).

Frame bit positions can be preserved in the output pattern by enabling FRAMED. In T1 mode, this prevents the test pattern from overwriting the frame bit which occurs every 193 bits. In E1 mode with FRAMED enabled, the test pattern does not overwrite time slot 0 data (FAS and NFAS words) and time slot 16 (CAS signalling word) if CAS framing is also selected. CAS framing is selected by setting TFRAME[3] to 1 in the Transmit Configuration register [TCR0; addr 070]. The test pattern is stopped during these bit periods according to ITU-T O.151, (10/92). If FRAMED is disabled, the test pattern is transmitted in all time slots.

2.4.6 Transmit Error Insertion

The Transmit Error Insert register [TERROR; addr 073] controls error insertion during pattern generation. Writing one to a TERROR bit injects a single occurrence of the respective error on TPOSO/TNEGO and XTIP/XRING outputs; writing a zero has no effect. Multiple transmit errors can be generated simultaneously. Periodic or random bit error rates can also be emulated by software control of the error control bit. Note that injected errors affect the data sent during a Framer or Analog Loopback [FLOOP or ALOOP; addr 014].

Line Code Violations (LCV) are inserted via the TVERR bit of the TERROR register. In T1 mode, if TVERR is set, a BPV is inserted between two consecutive ones. TVERR is latched until the BPV is inserted into the transmit data stream, and then cleared. In E1 mode with HDB3 selected, two consecutive BPVs of the same polarity are inserted. This is registered as a single LCV for the receiving E1 equipment.

Ft, FPS, and FAS bit errors are inserted using the TFERR bit in the TERROR register. TFERR commands a logical inversion of the next frame bit transmitted.

CRC4 (E1) and CRC6 (T1) bit errors are inserted using the TCERR bit in the TERROR register. TCERR commands a logical inversion of the next CRC bit transmitted.

Change Of Frame Alignments (COFAs) are controlled by the TCOFA and BSLIP bits in the TERROR register. TCOFA commands a 1-bit shift in the location of the transmit frame alignment by deleting (or inserting) a 1-bit position from the transmit frame. During E1 modes, BSLIP determines which direction the bit slip occurs. In T1 modes, only 1-bit deletion is provided. Note that TCOFA alters extraction rate of data from transmit slip buffer; thus, repeated TCOFAs eventually cause a controlled frame slip where one frame of data is repeated (T1/BSLIP = 0), or where one frame of data is deleted (BSLIP = 1).

PRBS test pattern errors are inserted by TBERR in the TERROR register. TBERR commands a single PRBS error by logically inverting the next PRBS generator output bit.

Fs and MFAS errors are controlled by the TMERR bit in the TERROR register. TMERR commands a single Fs bit error in T1, or MFAS bit error in E1 by logically inverting the next multiframe bit transmitted.

CAS Multiframe (MAS) errors are controlled by the TSERR bit in the TERROR register. TSERR commands a single MAS pattern error by logically inverting the first MAS bit transmitted.

2.4.7 In-Band Loopback Code Generation

The in-band loopback code generator circuitry overwrites the transmit data with in-band codes of configurable value and length. These codes are sequences with periods of 1 to 7 bits and may, in some applications, overwrite the framing bit. The Transmit Inband Loopback Code Configuration register [TLB; addr 077] controls the functions required for this operation.

A loopback code is generated in the transmit data stream by writing the loopback code to the Transmit Inband Loopback Code Pattern register [LBP; addr 078], and then setting the Start Inband Loopback (LBSTART) and Loopback Length (LB_LEN) bits in the Transmit Inband Loopback Code Configuration register [TLB; addr 077]. The TLB register optionally allows the loopback code to overwrite framing bits using the UNFRAMED bit. The LB_LEN provides loopback code pattern lengths of 4 to 7 bits. Patterns of 2 or 3 bits can be achieved by repeating the pattern in 4- or 6-bit modes, respectively. Framed or unframed all ones or all zeros can also be achieved by setting the pattern to all zeros or all ones.

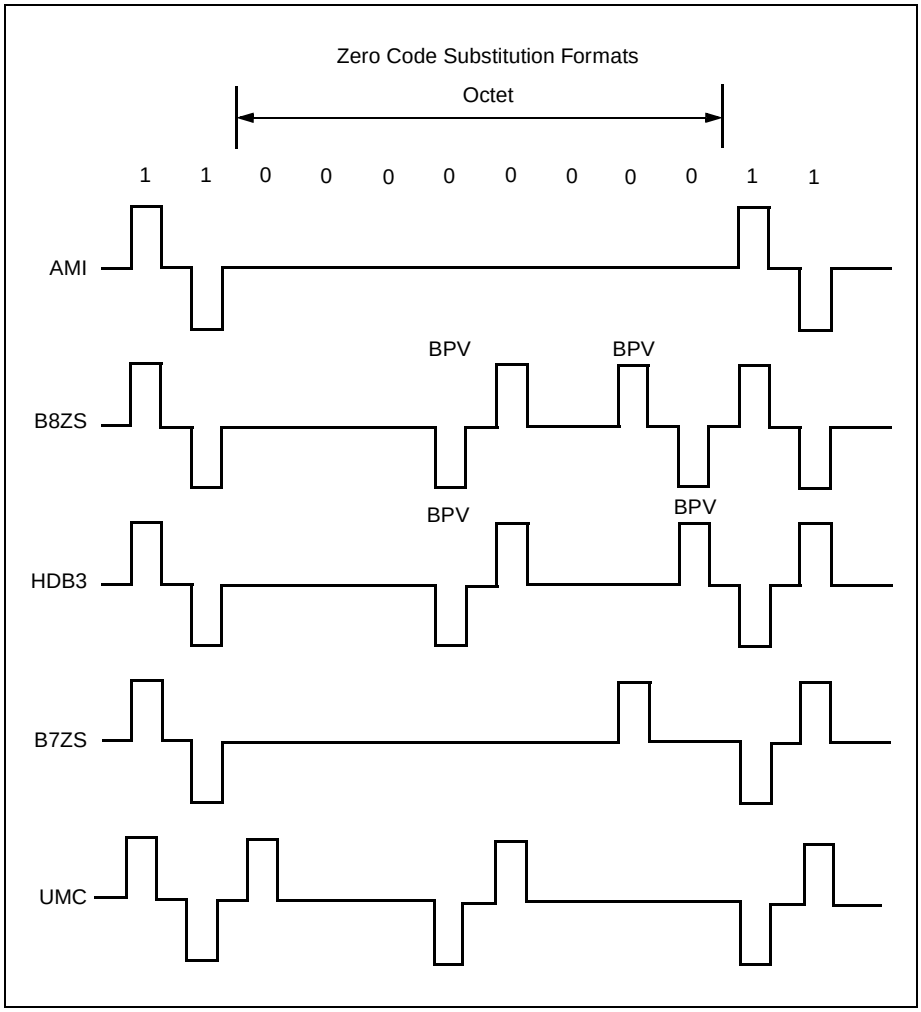
2.4.8 ZCS Encoder

The ZCS encoder encodes the single rail clock and data (unipolar) into dual rail data (bipolar). The Transmit Zero Code Suppression Bits (TZCS[1,0]) in the Transmitter Configuration register [TCR1; addr 071] selects ZCS and Pulse Density Violation (PDV) enforcement options for TPOSO/TNEGO output pins. TZCS supports the following: Alternate Mark Inversion (AMI); High Density Bipolar of order 3 (HDB3); Bipolar with 8 Zero Suppression (B8ZS); Pulse Density Violation (PDV); Unassigned Mux Code (UMC); and Bipolar with 7 Zero Suppression (B7ZS). Note that ZCS encoding, which alters data content, is performed prior to the CRC calculation so the outgoing CRC is always correct.

The AMI line code requires at least 12.5 percent average ones density and no more than 15 consecutive zeros. A one is encoded as either a positive or negative pulse; a zero is the absence of a pulse. Two consecutive pulses of the same polarity are referred to as a Bipolar Violation (BPV).

The HDB3 line code replaces four consecutive zeros by 000V or B00V code, where B is an AMI pulse and V is a bipolar violation (see Figure 2-24). ZCS encoder selects the code that will force the BPV output polarity opposite to the prior BPV.

Figure 2-24. Zero Code Substitution Formats



UMC forces DS0 channels containing 8 zeros to be replaced with the 10011000 code, per Bellcore TA-TSY-000278. Note that RCVR's ZCS decoder cannot recover original data content from a UMC or B7ZS encoded signal, or from a PDV-enforced one.

The output on TPOSO/TNEGO can be changed from dual rail bipolar to NRZ unipolar data (TNRZO) and to multiframe sync clock (MSYNCO), using the Transmit NRZ Data (TNRZ) bit in TCR1[addr 071]. Figures 2-25 and 2-26 illustrate transmit signal timing for both bipolar and unipolar operation.

Figure 2-25. Transmit Signals

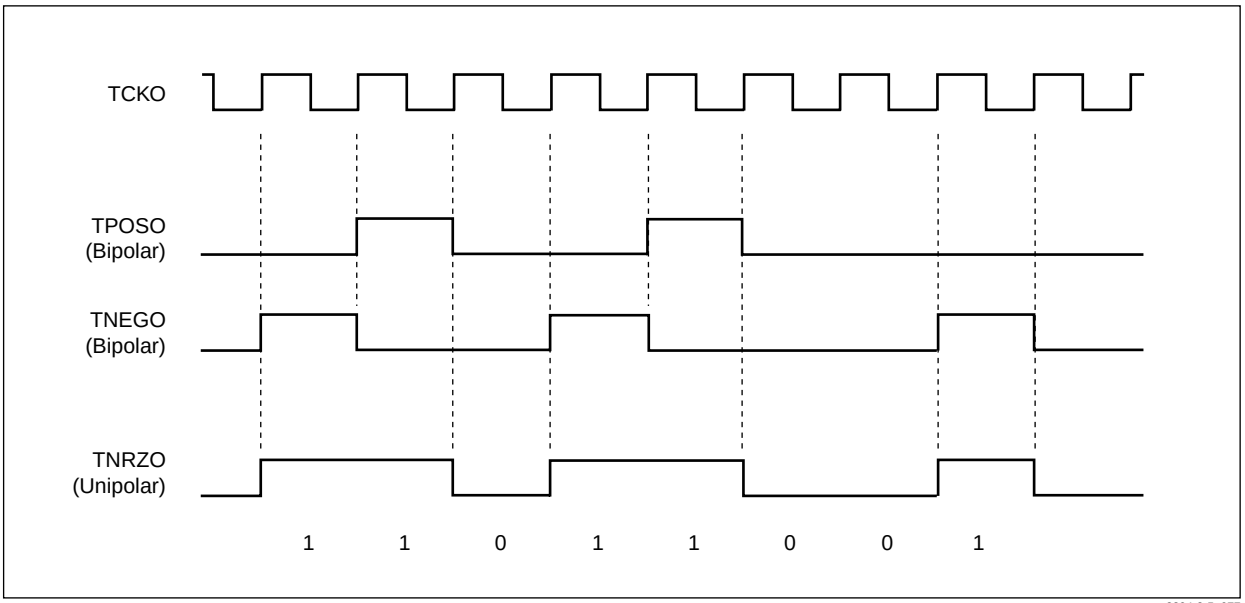
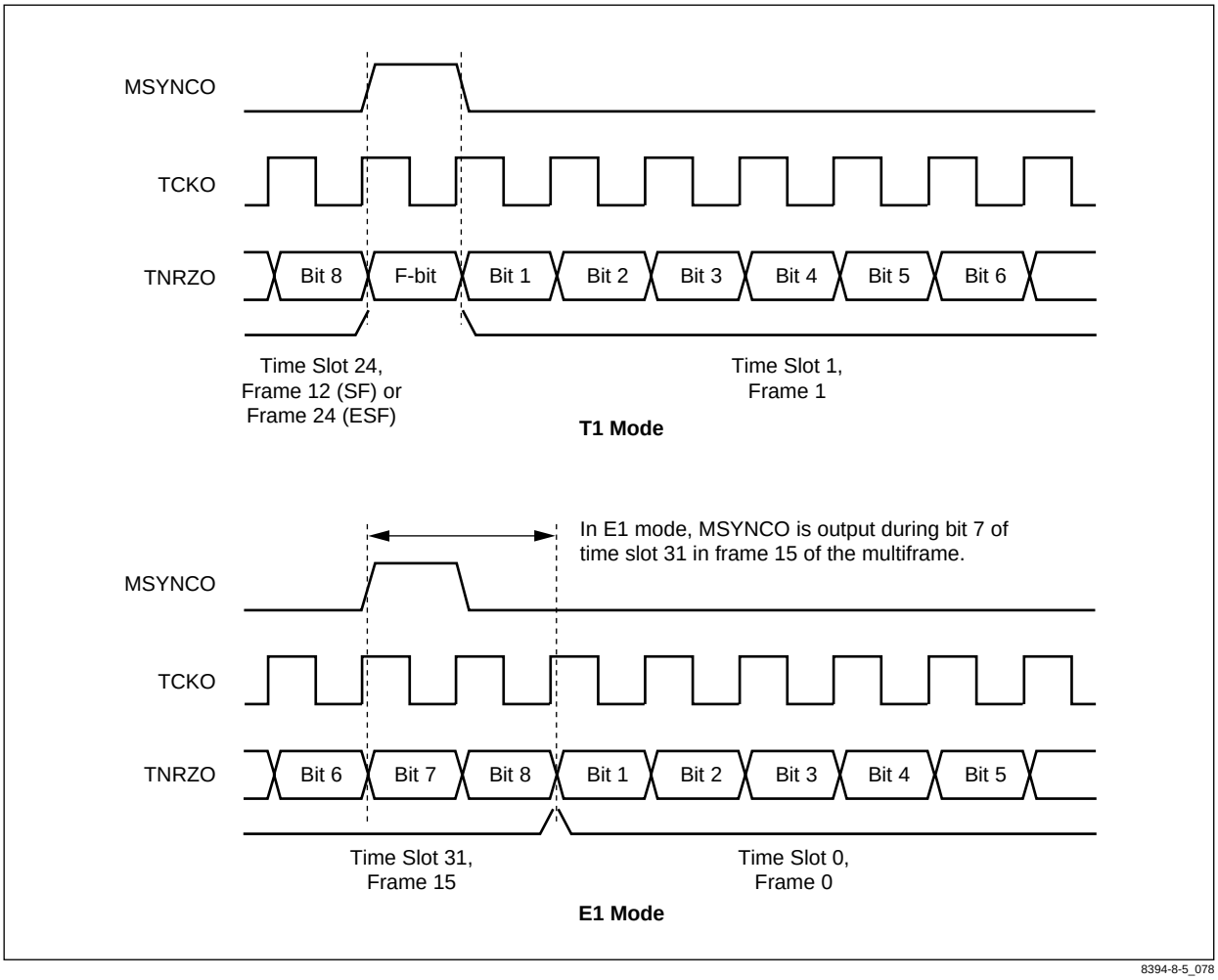


Figure 2-26. NRZ Mode Transmit Signals

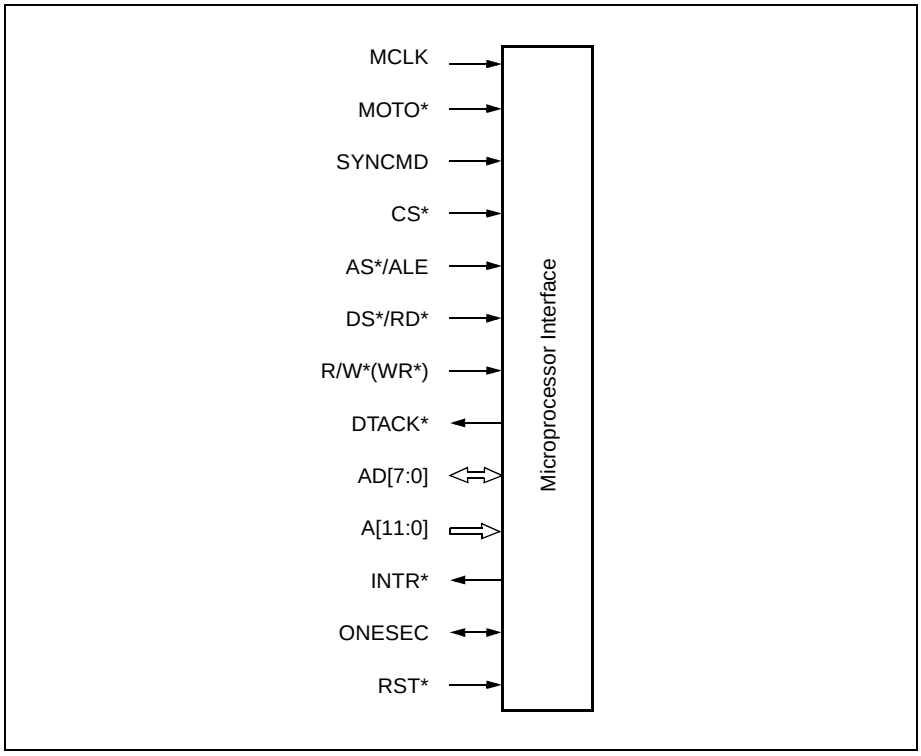


2.5 Microprocessor Interface

The Microprocessor Interface (MPU) provides the capability to configure the device, read status registers and counters, and respond to interrupts (see Figure 2-27). The interface supports both the Intel 8051 and Motorola 68000-type processors. In the Intel mode, the address and data are multiplexed; in the Motorola mode, the address and data are separate pins. Both synchronous and asynchronous Read and Write modes are supported. The synchronous mode is optimized for Motorola 68000-type processors with a maximum clock rate of 36 MHz. The asynchronous mode runs internally at 32 MHz, which limits the processor speed to 30 MHz for 68302 processors, and 16 MHz for 8051 processors.

The microprocessor interface is made up of the following pins: MCLK, MOTO*, SYNCMD, CS*, AS*/ALE, DS*/RD*, R/W*/WR*, DTACK*, AD[7:0], A[11:0], INTR*, ONESEC, RST*. A detailed description of the MPU signals is provided in Table 1-6, *Hardware Signal Definitions*.

Figure 2-27. Microprocessor Interface Block Diagram



2.5.1 Address/Data Bus

In Non-Multiplexed Address Mode, A[11:0] (A[10:0] for CX28394) provides the address for the register access. In Multiplexed Address Mode, A[11:8] (A[10:8] for CX28394) and AD[7:0] provide the address. In both modes, the data bytes flow over the shared bidirectional, byte-wide bus, AD[7:0].

2.5.2 Bus Control Signals

Four signals control operation of the interface port. The control signals are AS*/ALE, CS*, DS*/RD*, and R/W*(WR*). An additional pin, MOTO*, selects whether the interface signals are of a Motorola or Intel style.

When MOTO* is low, indicating a Motorola-style interface, CS*, AS*, R/W*, and DS* signals are expected. When MOTO* is high, indicating an Intel-style interface, CS*, ALE, RD*, and WR* signals are expected.

When MOTO* is high, the address lines are multiplexed with the data. This pin should usually be tied high for Intel devices and tied low for Motorola devices. SYNCMD puts the interface into the Synchronous Processor Interface Mode. Motorola 68000 processors typically have SYNCMD tied high if MCLK is connected to the MPU clock source; Intel 8051 processors have SYNCMD tied low (see Table 2-7).

Table 2-7. Microprocessor Interface Operating Modes

MOTO*	SYNCMD	Description
0	0	Asynchronous Motorola, internal clock
0	1	Synchronous Motorola, external clock
1	0	Asynchronous Intel, internal clock
1	1	Synchronous Intel, external clock

2.5.3 Interrupt Requests

Figure 2-28, Interrupt Generation Block Diagram, details the interrupt generation process. The INTR* output pin is an active low, open-drain type output which provides a common interrupt request for all eight framers and the LIU serial interface.

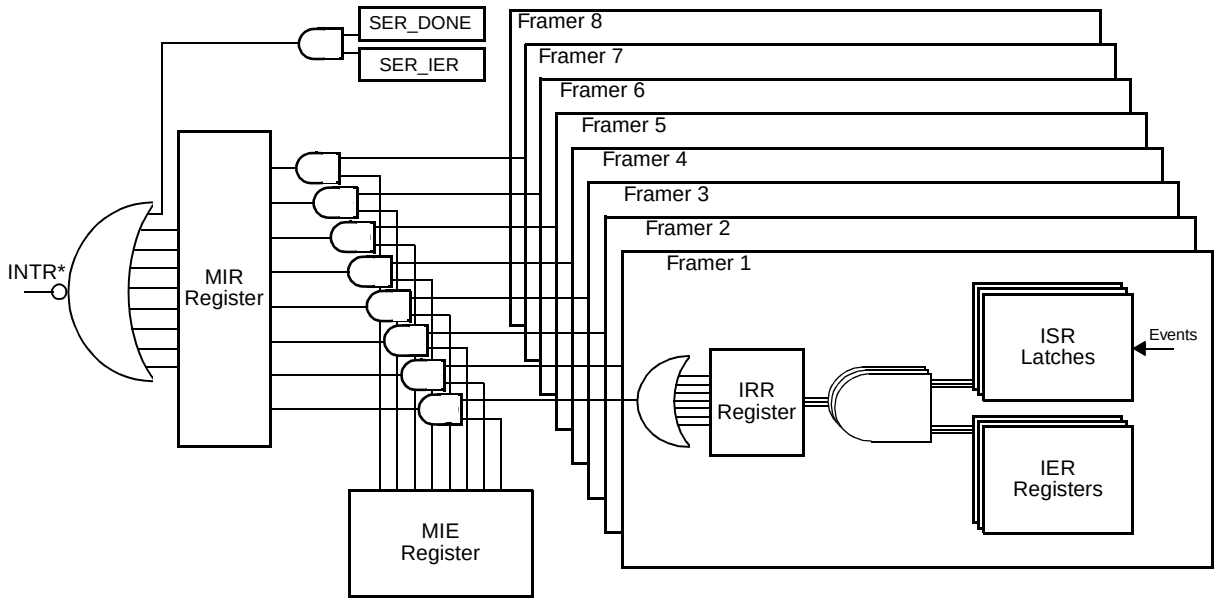
Each framer includes interrupt status registers (ISR[7:0]), interrupt enable registers (IER[7:0]), and an interrupt request register (IRR). Events such as alarm status changes and sync signals are latched in ISR registers until read by the microprocessor. Each ISR bit has a corresponding IER bit used to enable or disable interrupt generation. If enabled, an ISR event is reported in the appropriate IRR bit.

The IRR bits from each framer are gated with the corresponding enable bit in the master interrupt enable register [MIE; addr 01E] and are routed to the master interrupt register [MIR; addr 01D]. MIE provides a convenient location to enable or disable interrupts for an entire framer. The serial done bit [SER_STAT; addr 024] is gated with the serial interrupt enable bit [SER_CONFIG; addr 025] to produce an additional interrupt request. Finally, MIR bits and the LIU serial interface interrupt request are combined to generate a single interrupt request signal on the INTR* pin.

Using these registers, the microprocessor can process interrupts as follows:
Interrupt service routine

1. Read MIR and SER_STAT registers to determine which framer or framers caused the interrupt or whether LIU serial operation occurred.
2. For each interrupting framer, read IRR to determine which ISR contains the interrupt event or events.
3. Read the ISR and mask the interrupt event bit using the corresponding IER to determine which event or events caused the interrupt.
4. Enter the appropriate service routine.

Figure 2-28. Interrupt Generation Block Diagram



NOTE(S):
(1) In CX28395, INTR1* is provided for Framers 1-8, and INTR2* is provided for Framers 9-16.

2.5.4 Device Reset

The device contains four reset methods:

1. Internal Power-On Reset (POR),
2. Hardware Reset which uses the RST* pin,
3. Global Software Reset which uses the GRESET bit in register FCR [addr 080], and
4. Software Reset which uses the RESET bit in register CR0 [addr 001].

All four methods result in device outputs placed in a high-impedance state and configuration registers set to default values as shown in Table 3-4, *Address Map*. In all reset methods, SYSCKI must be present during the reset process for proper operation. MCLK (internal or external) performs the actual register initialization. Therefore, if the SYNCMD pin is connected high to enable external MCLK, the external MCLK must be applied during reset, and if the SYNCMD pin is low during reset, the internal clock (33 MHz) is used and external MCLK is not required. After hardware reset, software reset, or internal power-on reset, the microprocessor must initialize the configuration registers to the desired state.

An internal POR process is initiated during power-up. When VDD has reached approximately 2.0 V, the internal reset process begins and continues for 100 SYSCKI cycles if SYSCKI is applied. If SYSCKI is not present, the device remains in the reset state and does not terminate until detecting 100 SYSCKI cycles. GRESET or RESET can be monitored to determine when POR is complete. MCLK (internal or external) must be present during the POR concurrent with SYSCKI to allow register initialization.

Hardware reset is initiated by bringing the RST* pin active (low) for a minimum of 4 µs. If SYNCMD is high (using external MCLK), external MCLK must be present while RST* is low to allow register initialization. After RST* is deactivated, the internal reset process continues for 5 µs and register access should be avoided. GRESET can be monitored to determine when the reset process is complete.

2.6 Loopbacks

The device provides a complete set of loopbacks for diagnostics, maintenance, and troubleshooting for each framer. All loopbacks perform clock and data switching, if necessary.

2.6.1 Remote Line Loopback

The line loopback loops the RCVR inputs to the XMTR outputs. The loopback provides BPV transparency and the ability to override the looped data with AIS. The RCVR data path is not affected by the activation of this loopback. Remote line loopback is activated by setting the Remote Line Loopback (LLOOP) bit in the Loopback Configuration register [LOOP; addr 014]. It is possible to operate the remote line loopback simultaneously with the local framer loopback.

2.6.2 Remote Payload Loopback

The payload loopback loops all DS0 channels from the RCVR input to the XMTR output. Payload loopback retains time slot integrity, so that numbered time slots from each receive frame are transferred to the same numbered time slots in the transmit frame. Transmit overhead bits—F-bits in T1 mode or TS0 in E1 mode—are supplied by transmit frame formatter or by TSB according to TFRM [addr 072] settings. Existing transmit frame alignment and clock timing are not altered by [PLOOP; addr 014] activation or deactivation, allowing system operation with independent receive and transmit timing. Controlled frame slips are performed in the payload loopback path if receive and transmit clocks are asynchronous, although these slips are not reported to the processor as slip buffer errors. Multiframe integrity is not maintained during PLOOP; therefore, DS0 and signaling channel loopbacks [TPCn; addr 100–11F] must be used to implement payload loopback if transparent or forced signaling is desired. PLOOP overrides transmit per-channel remote loopback selection (TLOOP bit in TPCn).

2.6.3 Remote Per-Channel Loopback

The remote per-channel loopback loops the RCVR input DS0 channel to the XMTR output DS0 channel. The remote per-channel loopback is activated by setting TLOOP in the Transmit Per-Channel Control register [TPC0 to TPC31; addr 100 to 11F].

2.6.4 Local Framer Loopback

The local framer loopback loops the transmit line encoder outputs to the receive line decoder inputs. Transmitter output is not affected by the activation of this loopback. The local framer loopback is activated by setting the Local Framer Loopback (FLOOP) bit in the Loopback Configuration register [LOOP; addr 014]. It is possible to operate the local framer loopback simultaneously with the remote line loopback.

2.6.5 Local Per-Channel Loopback

The local per-channel loopback loops the TSB PCM and signaling inputs to the RSB PCM and signaling outputs on a per-channel basis. The local per-channel PCM loopback is activated by setting RLOOP in the System Bus Per-Channel Control registers [SBC0 to SBC31; addr 0E0 to 0FF]. The local per-channel signaling loopback is activated by setting SIG_LP in System Bus Per-Channel Control registers.

2.7 Serial Interface

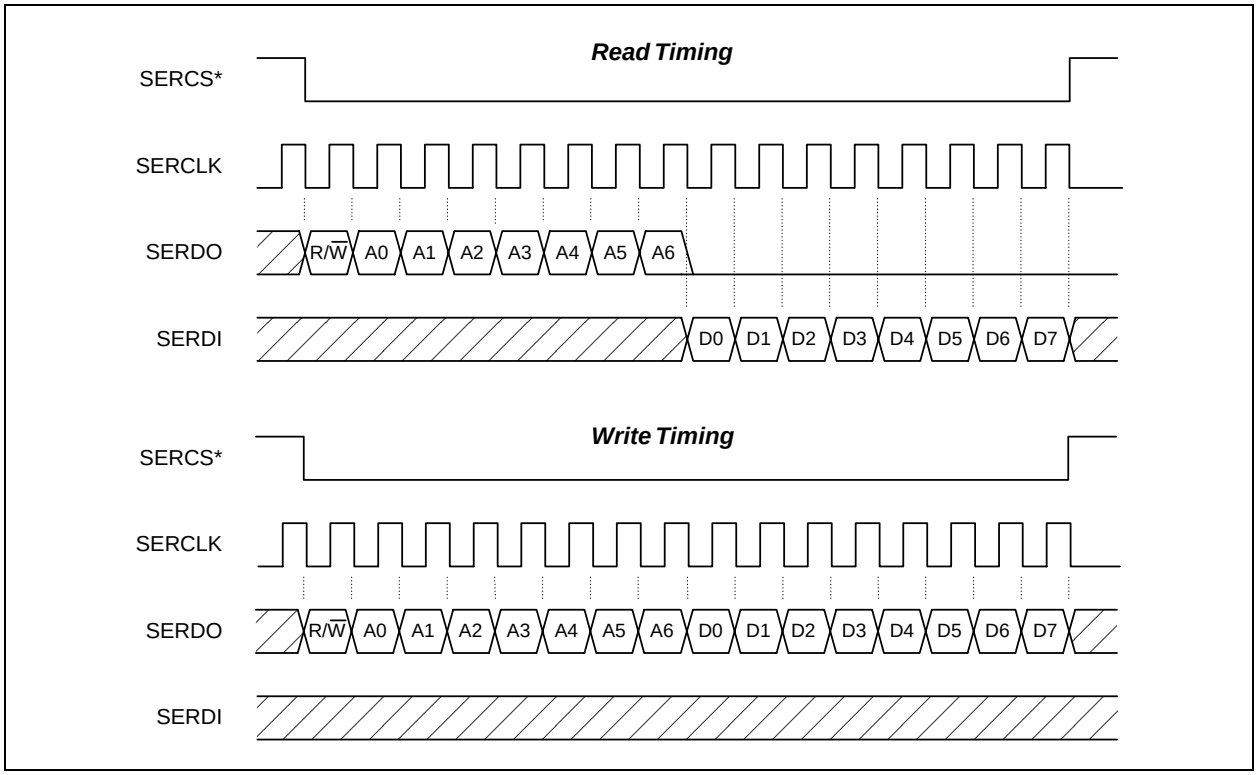
The device provides a serial interface that allows the microprocessor to indirectly communicate with an attached LIU (such as the Conexant CX28380 Quad T1/E1 LIU). This interface allows the microprocessor to control and query the LIU status. One 8-bit register in the LIU can be written via the SERDO pin or read from the SERDI pin at the clock rate determined by the SERCKO clock output. The serial interface supports a glueless interface to two quad LIUs by supplying two independently controlled external chip select lines on the CX28398: SERCS1* and SERCS2*. The CX28394 provides a single SERCS* chip select line. On the CX28395, the serial interface is not accessable.

The serial interface uses a 16-bit process for each write or read operation. During a write operation, a 16-bit word—consisting of [SER_CTRL; addr 022] and [SER_DAT; addr 023]—is transmitted to the LIU. The SER_CTL register contains the LIU register address for the current operation and a read/write control bit. During a read operation, SER_CTL is transmitted and 8-bit data from the LIU is received and placed in SER_DAT register. Writing to SER_CTL initiates a serial interface read or write operation.

The Data register contains either write or read data. For the write operation, its content is written to the SERDO serial port on the eight SERCKO cycles immediately following the Address/Command byte. Likewise, for the read operation, data on the SERDI serial port is input immediately on the eight SERCKO clock cycles following the Address/Command byte.

Figure 2-29 illustrates serial interface timing.

Figure 2-29. Serial Interface Timing Diagram



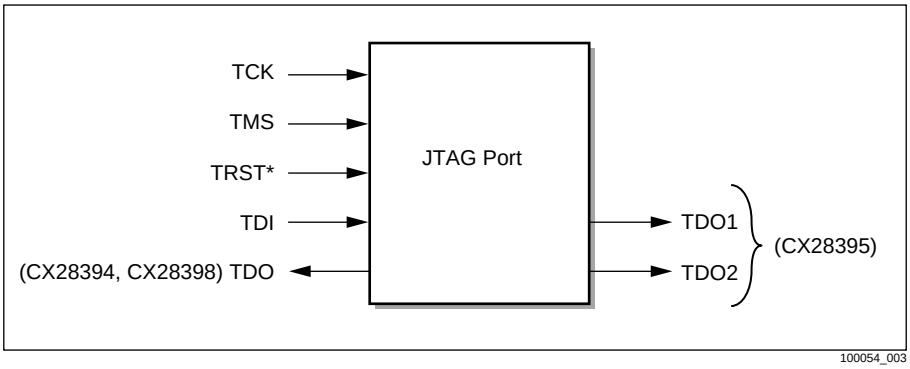
2.8 Joint Test Access Group

The device incorporates printed circuit board testability circuits in compliance with IEEE Std. P1149.1a–1993, *IEEE Standard Test Access Port and Boundary–Scan Architecture*, commonly known as JTAG (Joint Test Action Group).

The JTAG includes a Test Access Port (TAP) and several data registers. The TAP provides a standard interface through which instructions and test data are communicated (see Figure 2-30). A Boundary Scan Description Language (BSDL) file is available from Conexant upon request.

The test access port consists of TDI, TCK, TMS, TDO and TRST* pins.

Figure 2-30. Test Access Port (TAP) Diagram



2.8.1 Instructions

In addition to the required BYPASS, SAMPLE/PRELOAD, and EXTEST instructions, IDCODE instruction is supported. There is also one private instruction. Table 2-8 lists the JTAG instructions along with their codes.

Table 2-8. JTAG Instructions

Instruction	Code
BYPASS	111
SAMPLE/PRELOAD	001
EXTEST	000
IDCODE	010
Private	xxx

2.8.2 Device Identification Register

JTAG ID register consists of a 4-bit version, 16-bit part number, and 11-bit manufacturer number (see Tables 2-11 and 2-9).

Table 2-9. CX28394 Device Identification JTAG Register

Version(1)	Part Number	Manufacturer ID	
0 0 0 0	1 0 0 0 0 0 1 1 1 0 0 1 0 1 0 0	0 0 0 0 0 0 1 0 0 1 1 1	TDO
0x0	0x8394	0X013	
4 bits	16 bits	11 bits	

NOTE(S):
(1) Consult factory for current version number.

Table 2-10. CX28395 Device Identification JTAG Register

Version(1)	Part Number	Manufacturer ID	
0 0 0 0	1 0 0 0 0 0 1 1 1 0 0 1 0 1 0 1	0 0 0 0 0 0 1 0 0 1 1 1	TDO1 TDO2
0x0	0x8395	0X013	
4 bits	16 bits	11 bits	

NOTE(S):
(1) Consult factory for current version number.

Table 2-11. CX28398 Device Identification JTAG Register

Version(1)	Part Number	Manufacturer ID	
0 0 0 0	1 0 0 0 0 0 1 1 1 0 0 1 1 0 0 0	0 0 0 0 0 0 1 0 0 1 1 1	TDO
0x0	0x8398	0X013	
4 bits	16 bits	11 bits	

NOTE(S):
(1) Consult factory for current version number.

3.0 Registers

3.1 Address Map

Registers shown with a default setting are reset to the indicated value following power up, software RESET (CRO; addr 001), GRESET (FCR; addr 080), or hardware reset (RST* pin).

Addresses 000 (hex) to 1FF (hex) are offset by the upper 3 bits of address lines A[11:0] and chip selects as listed in Tables 3-1 through 3-3.

Table 3-1. Address Offset Map (CX28394)

Framer	Chip Select CS*	Offset Address A[10:0] (hex)
1	0	000
2	0	200
3	0	400
4	0	600
NOTE(S): 1. Global registers at 000 and 080–083 may be accessed at any offsets.		

Table 3-2. Address Offset Map (CX28398)

Framer	Chip Select CS*	Offset Address A[11:0] (hex)
1	0	000
2	0	200
3	0	400
4	0	600
5	0	800
6	0	A00
7	0	C00
8	0	E00
NOTE(S): 1. Global registers at 000 and 080–083 may be accessed at any offsets.		

Table 3-3. Address Offset Map (CX28395)

Framer	Chip Select		Offset Address A[11:0] (hex)
	CS1*	CS2*	
1	0	1	000
2	0	1	200
3	0	1	400
4	0	1	600
5	0	1	800
6	0	1	A00
7	0	1	C00
8	0	1	E00
9	1	0	000
10	1	0	200
11	1	0	400
12	1	0	600
13	1	0	800
14	1	0	A00
15	1	0	C00
16	1	0	E00

NOTE(S):
1. Global registers at 000 and 080–083 for framers 1–8 may be accessed at any of the first 8 offsets.
2. Global registers at 000 and 080–083 for framers 9–16 may be accessed at any of the second 8 offsets.

Table 3-4. Address Map *(1 of 5)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting (Hex)
Global	000	DID	R	Device Identification	28
	080	FCR	R/W	Framer Control Register	00
	081	MIR	R	Master Interrupt Request	00
	082	MIE	R/W	Master Interrupt Enable	00
	083	TEST	R/W	Test Configuration	00
Primary Control	001	CR0	R/W	Primary Control Register	00
	003	IRR	R	Interrupt Request Register	—
Interrupt Status	004	ISR7	R	Alarm 1 Interrupt Status	—
	005	ISR6	R	Alarm 2 Interrupt Status	—
	006	ISR5	R	Error Interrupt Status	—
	007	ISR4	R	Counter Overflow Interrupt Status	—
	008	ISR3	R	Timer Interrupt Status	—
	009	ISR2	R	Data Link 1 Interrupt Status	—
	00A	ISR1	R	Data Link 2 Interrupt Status	—
	00B	ISR0	R	Pattern Interrupt Status	00
Interrupt Enable	00C	IER7	R/W	Alarm 1 Interrupt Enable Register	00
	00D	IER6	R/W	Alarm 2 Interrupt Enable Register	00
	00E	IER5	R/W	Error Interrupt Enable Register	00
	00F	IER4	R/W	Count Overflow Interrupt Enable Register	00
	010	IER3	R/W	Timer Interrupt Enable Register	00
	011	IER2	R/W	Data Link 1 Interrupt Enable Register	00
	012	IER1	R/W	Data Link 2 Interrupt Enable Register	00
	013	IER0	R/W	Pattern Interrupt Enable Register	00
Primary	014	LOOP	R/W	Loopback Configuration Register	—
	015	DL3_TS	R/W	External Data Link Channel	—
	016	DL3_BIT	R/W	External Data Link Bit	—
	017	FSTAT	R	Offline Framer Status	—
	018	PIO	R/W	Programmable Input/Output	00
	019	POE	R/W	Programmable Output Enable	3C
	01A	CMUX	R/W	Clock Input Mux	00
	020	RAC	R/W	Receive Alarm Configuration	—
	021	RSTAT	R/W	Receive Line Code Status	—

Table 3-4. Address Map *(2 of 5)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting (Hex)
Serial Interface	022	SER_CTL	R/W	Serial Control	—
	023	SER_DAT	R/W	Serial Data	—
	024	SER_STAT	R/W	Serial Status	—
	025	SER_CONFIG	R/W	Serial Configuration	00
	026	RAM TEST	R/W	Ram Test	—
Digital Receiver (RCVR)	040	RCR0	R/W	Receiver Configuration	—
	041	RPATT	R/W	Receive Test Pattern Configuration	—
	042	RLB	R/W	Receive Loopback Code Detector Configuration	—
	043	LBA	R/W	Loopback Activate Code Pattern	—
	044	LBD	R/W	Loopback Deactivate Code Pattern	—
	045	RALM	R/W	Receive Alarm Signal Configuration	—
	046	LATCH	R/W	Alarm/Error/Counter Latch Configuration	—
	047	ALM1	R	Alarm 1 Status	—
	048	ALM2	R	Alarm 2 Status	—
	049	ALM3	R	Alarm 3 Status	—
Error/Alarm Counters	050	FERR	R	Framing Bit Error Counter LSB	—
	051	FERR	R	Framing Bit Error Counter MSB	—
	052	CERR	R	CRC Error Counter LSB	—
	053	CERR	R	CRC Error Counter MSB	—
	054	LCV	R	Line Code Violation Counter LSB	—
	055	LCV	R	Line Code Violation Counter MSB	—
	056	FEBE	R	Far End Block Error Counter LSB	—
	057	FEBE	R	Far End Block Error Counter MSB	—
	058	BERR	R	PRBS Bit Error Counter LSB	—
	059	BERR	R	PRBS Bit Error Counter MSB	—
	05A	AERR	R	SEF/LOF/COFA Alarm Count	—
Receive Sa-Byte	05B	RSA4	R	Receive Sa4 Byte Buffer	—
	05C	RSA5	R	Receive Sa5 Byte Buffer	—
	05D	RSA6	R	Receive Sa6 Byte Buffer	—
	05E	RSA7	R	Receive Sa7 Byte Buffer	—
	05F	RSA8	R	Receive Sa8 Byte Buffer	—

Table 3-4. Address Map *(3 of 5)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting (Hex)
Digital Transmitter (XMTR)	070	TCR0	R/W	Transmit Framer Configuration	—
	071	TCR1	R/W	Transmitter Configuration	—
	072	TFRM	R/W	Transmit Frame Format	—
	073	TERROR	R/W	Transmit Error Insert	00
	074	TMAN	R/W	Transmit Manual Sa-Byte/FEBE Configuration	—
	075	TALM	R/W	Transmit Alarm Signal Configuration	—
	076	TPATT	R/W	Transmit Test Pattern Configuration	—
	077	TLB	R/W	Transmit Inband Loopback Code Configuration	—
	078	LBP	R/W	Transmit In-Band Loopback Code Pattern	—
Transmit Sa-Byte	07B	TSA4	R/W	Transmit Sa4 Byte Buffer	—
	07C	TSA5	R/W	Transmit Sa5 Byte Buffer	—
	07D	TSA6	R/W	Transmit Sa6 Byte Buffer	—
	07E	TSA7	R/W	Transmit Sa7 Byte Buffer	—
	07F	TSA8	R/W	Transmit Sa8 Byte Buffer	—
BOP	0A0	BOP	R/W	Bit Oriented Protocol Transceiver	00
	0A1	TBOP	R/W	Transmit BOP Code Word	00
	0A2	RBOP	R	Receive BOP Code Word	—
	0A3	BOP_STAT	R	BOP Status	—
Data Link #1	0A4	DL1_TS	R/W	DL1 Time Slot Enable	00
	0A5	DL1_BIT	R/W	DL1 Bit Enable	00
	0A6	DL1_CTL	R/W	DL1 Control	00
	0A7	RDL1_FFC	R/W	RDL #1 FIFO Fill Control	00
	0A8	RDL1	R	Receive Data Link FIFO #1	—
	0A9	RDL1_STAT	R	RDL #1 Status	—
	0AA	PRM	R/W	Performance Report Message	00
	0AB	TDL1_FEC	R/W	TDL #1 FIFO Empty Control	00
	0AC	TDL1_EOM	W	TDL #1 End Of Message Control	—
	0AD	TDL1	R/W	Transmit Data Link FIFO #1	—
	0AE	TDL1_STAT	R	TDL #1 Status	—

Table 3-4. Address Map *(4 of 5)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting (Hex)
Data Link #2	0AF	DL2_TS	R/W	DL2 Time-Slot Enable	00
	0B0	DL2_BIT	R/W	DL2 Bit Enable	00
	0B1	DL2_CTL	R/W	DL2 Control	00
	0B2	RDL2_FFC	R/W	RDL #2 FIFO Fill Control	00
	0B3	RDL2	R	Receive Data Link FIFO #2	—
	0B4	RDL2_STAT	R	RDL #2 Status	—
	0B6	TDL2_FEC	R/W	TDL #2 FIFO Empty Control	00
	0B7	TDL2_EOM	W	TDL #2 End Of Message Control	—
	0B8	TDL2	R/W	Transmit Data Link FIFO #2	—
	0B9	TDL2_STAT	R	TDL #2 Status	—
Test	0BA	DL_TEST1	R/W	DLINK Test Configuration	00
	0BB	DL_TEST2	R/W	DLINK Test Status	00
	0BC	DL_TEST3	R/W	DLINK Test Status	00
	0BD	DL_TEST4	R/W	DLINK Test Control #1 or Configuration #2	00
	0BE	DL_TEST5	R/W	DLINK Test Control #2 or Configuration #2	00
System Bus Interface (SBI)	0D0	SBI_CR	R/W	System Bus Interface Configuration	00
	0D1	RSB_CR	R/W	Receive System Bus Configuration	00
	0D2	RSYNC_BIT	R/W	Receive System Bus Sync Bit Offset	—
	0D3	RSYNC_TS	R/W	Receive System Bus Sync Time Slot Offset	—
	0D4	TSB_CR	R/W	Transmit System Bus Configuration	00
	0D5	TSYNC_BIT	R/W	Transmit System Bus Sync Bit Offset	—
	0D6	TSYNC_TS	R/W	Transmit System Bus Sync Time Slot Offset	—
	0D7	RSIG_CR	R/W	Receive Signaling Configuration	—
	0D8	RSYNC_FRM	R/W	Signaling Reinsertion Frame Offset	—
	0D9	SSTAT	R	Slip Buffer Status	—
	0DA	STACK	R	Receive Signaling Stack	—
	0DB	RPHASE	R	RSLIP Phase Status	—
	0DC	TPHASE	R	TSLIP Phase Status	—
	0DD	PERR	R	RAM Parity Status	—
	0E0–0FF	SBCn: n = 0 to 31	R/W	System Bus Per-Channel Control	—

Table 3-4. Address Map *(5 of 5)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting (Hex)
Buffer Memory	100–11F	TPCn: n = 0 to 31	R/W	Transmit Per-Channel Control	—
	120–13F	TSIGn: n = 0 to 31	R/W	Transmit Signaling Buffer	—
	140–15F	TSLIP_LOn: n = 0 to 31	R/W	Transmit PCM Slip Buffer	—
	160–17F	TSLIP_HIn: n = 0 to 31	R/W	Transmit PCM Slip Buffer	—
	180–19F	RPCn: n = 0 to 31	R/W	Receive Per-Channel Control	—
	1A0–1BF	RSIGn: n = 0 to 31	R/W	Receive Signaling Buffer	—
	1C0–1DF	RSLIP_LOn: n = 0 to 31	R/W	Receive PCM Slip Buffer	—
	1E0–1FF	RSLIP_HIn: n = 0 to 31	R/W	Receive PCM Slip Buffer	—

3.2 Global Control and Status Registers

Global registers are applicable to all framers in the CX28394 and CX28398. There are two sets of global registers for the CX28395, one for each 8-framer group.

000—Device Identification (DID)

Read only value.

7	6	5	4	3	2	1	0
DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]

DID[7:4] Device Revision—A value of 0x4 indicates the current revision.

DID[3:0] Device ID—A value of 0x8 indicates the CX28398 or CX28395. A value of 0x4 indicates the CX28394.

080—Framer Control Register (FCR)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
GRESET	–	–	–	–	ONESEC_IO	SBIMODE[1]	SBIMODE[0]

GRESET Global Reset —When written to 1 by the microprocessor, GRESET initiates an internal global reset process which initializes all global control registers and certain control registers for all framers to their default settings (see Table 3-4). The internal reset process takes a maximum of 15 µsec.

The processor must not write to the control registers until the reset process is complete. GRESET remains active (1) during the reset process to allow the microprocessor to detect reset completion. GRESET also indicates a reset operation triggered by power-up or by an active low RST* pin. After GRESET initialization, the following is true:

- System bus outputs (RSIGO, RPCMO, and SIGFRZ) for all framers are three-stated.
- Programmable I/O pins are configured as inputs.
- Global control and framer control registers are set to their default values.

ONESEC_IO Bidirectional ONESEC Input/Output Mode—Selects input or output mode for ONESEC signal pin and controls the internal timer interval used for one-second status latching [LATCH; addr 046]. When ONESEC is an output, SYSCLK is used to develop the one-second timer interval output with an arbitrarily defined initial starting location. When ONESEC is an input, the timer/latch interval is aligned to rising edge of ONESEC input. The system can apply ONESEC input to define any length timer/latch interval up to 1 second, but not greater than 1 second.

0 = ONESEC input
1 = ONESEC output

SBIMODE[1:0] The processor writes FCR at power-up to configure the system bus interface mode. Each group of four framers can be configured as separate system bus interfaces or as an internally multiplexed group. The group consisting of framers 1 through 4 (9 through 12) can be configured to share a common system bus interface, SBI Bus A. The group consisting of framers 5 through 8 (13 through 16) can also be configured to share a common system bus interface, SBI Bus B.

SBIMODE[1]: 0 = Separate system bus interface mode for framer group 5–8 (13–16).
1 = Common, multiplexed system bus interface mode.

SBIMODE[0]: 0 = Separate system bus interface mode for framer group 1–4 (9–12).
1 = Common, multiplexed system bus interface mode.

081—Master Interrupt Request (MIR)

CX28394

7	6	5	4	3	2	1	0
—	—	—	—	MIR[3]	MIR[2]	MIR[1]	MIR[0]

CX28398 and CX28395

7	6	5	4	3	2	1	0
MIR[7]	MIR[6]	MIR[5]	MIR[4]	MIR[3]	MIR[2]	MIR[1]	MIR[0]

MIR[7:0] An active MIR bit indicates which framer has active interrupts. An MIR bit is latched active (high) whenever any bit in the Interrupt Request Register (IRR[7:0]; addr 003–0B) is set to report an interrupt event.

MIR0: 0 = no interrupt event in framer 0
1 = active interrupt event in framer 0

MIR1: 0 = no interrupt event in framer 1
1 = active interrupt event in framer 1

MIR2: 0 = no interrupt event in framer 2
1 = active interrupt event in framer 2

MIR3: 0 = no interrupt event in framer 3
1 = active interrupt event in framer 3

MIR4: 0 = no interrupt event in framer 4
1 = active interrupt event in framer 4

MIR5: 0 = no interrupt event in framer 5
1 = active interrupt event in framer 5

MIR6: 0 = no interrupt event in framer 6
1 = active interrupt event in framer 6

MIR7: 0 = no interrupt event in framer 7
1 = active interrupt event in framer 7

082—Master Interrupt Enable (MIE)

CX28394

7	6	5	4	3	2	1	0
—	—	—	—	MIE[3]	MIE[2]	MIE[1]	MIE[0]

CX28398 and CX28395

7	6	5	4	3	2	1	0
MIE[7]	MIE[6]	MIE[5]	MIE[4]	MIE[3]	MIE[2]	MIE[1]	MIE[0]

MIE[7:0] MIE is a global interrupt enable for each framer. Writing a one to an MIE bit enables the corresponding framer's IRR bit to be latched in MIR (addr 081) and to activate the INTR* output.

MIE0: 0 = Disable framer 0 IRR interrupt
1 = Enable framer 0 IRR interrupt
MIE1: 0 = Disable framer 1 IRR interrupt
1 = Enable framer 1 IRR interrupt
MIE2: 0 = Disable framer 2 IRR interrupt
1 = Enable framer 2 IRR interrupt
MIE3: 0 = Disable framer 3 IRR interrupt
1 = Enable framer 3 IRR interrupt
MIE4: 0 = Disable framer 4 IRR interrupt
1 = Enable framer 4 IRR interrupt
MIE5: 0 = Disable framer 5 IRR interrupt
1 = Enable framer 5 IRR interrupt
MIE6: 0 = Disable framer 6 IRR interrupt
1 = Enable framer 6 IRR interrupt
MIE7: 0 = Disable framer 7 IRR interrupt
1 = Enable framer 7 IRR interrupt

083—Test Configuration (TEST)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	—	—	—	TEST	—

TEST Global Test Enable—Reserved for Conexant production test.

3.3 Primary Control and Status Register

001—Primary Control Register (CR0)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
RESET	—	RINCF	RFRAME[3]	RFRAME[2]	RFRAME[1]	RFRAME[0]	T1/E1N

RESET Framer Reset—When written to 1 by the microprocessor, RESET initiates an internal reset process which initializes certain control registers to their default settings (see Table 3-4). The internal reset process takes a maximum of 15 µsec.

The processor must not write to the control registers until the reset process is complete. RESET remains active (1) during the reset process to allow the microprocessor to detect reset completion. RESET also indicates a reset operation triggered by power-up, GRESET [FCR; addr 080], or by an active low RST* pin. After RESET initialization, the following is true:

- System bus outputs (RSIGO, RPCMO, and SIGFRZ) are three-stated.
- Programmable I/O pins are configured as inputs.
- Framer control registers are set to their default values.

RINCF Receiver Framer CRC6 include F-bit—Determines if the F-bit is included in the CRC6 remainder calculation in T1 mode (T1/E1N = 1). This bit is ignored in E1 mode (T1/E1N = 0).

0 = T1 ESF CRC6 calculation is performed on the receive data including a 1 in place of the F-bit.
1 = TI ESF CRC6 transmit calculation is performed on receive data including the F-bit.

RFRAME[3:0] Receiver Framer Mode—Establishes the offline framer's search criteria for recovery of frame alignment (reframe). Also works in conjunction with the RLOFA–RLOFD bits [addr 040] to establish the online framer's criteria for loss of frame alignment. Refer to Tables A-1 through A-6 to find which frame bits are monitored and Table 2-2, *Criteria for Loss/Recovery of Receive Framer Alignment*, for frame alignment loss/recovery criteria during the selected mode. Mode descriptions are given in Table 3-5. Online framer's SF, SLC, CAS and MFAS criteria for loss/recovery of multiframe alignment are also selected by RFRAME[3:0].

Table 3-5. Receive Framer Modes

RFRAME[3:0]	T1/E1N	Receive Framer Mode
000X	0	FAS Only
001X	0	FAS Only + BSLIP
010X	0	FAS + CRC
011X	0	FAS + CRC + BSLIP
100X	0	FAS + CAS
101X	0	FAS + CAS + BSLIP
110X	0	FAS + CRC + CAS
111X	0	FAS + CRC + CAS + BSLIP
0000	1	FT Only
0001	1	ESF + No CRC (FPS only)
0100	1	SF
0101	1	SF + JYEL
0110	1	SF + T1DM
1000	1	SLC + FSLOF
1001	1	SLC
1100	1	ESF + Mimic CRC
1101	1	ESF + Force CRC

T1/E1N Global T1/E1 Select—Affects all functions by enabling receive and transmit circuits to operate at either the T1 or E1 line rate. The processor should reinitialize all control register settings after changing the T1/E1N control bit. T1/E1N selects the nominal line rate (shown below) while the exact receive and transmit line rate frequencies are independently determined by their respective input clock or input data references. The actual receive and transmit line frequency can vary within defined tolerances.

0 = 2.048 MHz line rate (E1)
1 = 1.544 MHz line rate (T1)

3.4 Interrupt Control Register

003—Interrupt Request Register (IRR)

An IRR bit is latched active (high) whenever an enabled interrupt source reports an interrupt event in the corresponding Interrupt Status Register [ISR7–ISR0; addr 004–00B]. IRR is latched until the corresponding ISR register is read by the processor. Reading ISR clears the respective IRR bit, independent of clearing ISR bits. Therefore, persistently active ISR bits won't affect INTR* deactivation. All IRR bits are logically OR'ed to activate a corresponding MIR bit and INTR*, so the processor must read IRR = 00 before exiting its interrupt service routine in order to confirm the MIR bit has been deasserted.

7	6	5	4	3	2	1	0
ALARM1	ALARM2	ERROR	COUNT	TIMER	DL1	DL2	PATT

ALARM1 Alarm 1 Interrupt Request—Indicates one or more receiver errors. Processor reads ISR7 [addr 004] to locate specific source.
0 = no event
1 = active interrupt request

ALARM2 Alarm 2 Interrupt Request—Indicates one-second timer expiry, or detection of one or more transmitter errors, or detection of inband loopback codeword. Processor reads ISR6 [addr 005] to locate specific source.
0 = no event
1 = active interrupt request

ERROR Error Interrupt—Indicates one or more errors detected by receive framer, RSLIP, or TSLIP circuits. Processor reads ISR5 [addr 006] to locate specific source.
0 = no event
1 = active interrupt request

COUNT Counter Overflow Interrupt—Indicates one or more error counts [addr 050–05A] have issued an overflow interrupt. Processor reads ISR4 [addr 007] to locate specific source.
0 = no event
1 = active interrupt request

TIMER Timer Interrupt Request—Indicates that the transmit, receive, or system bus timebase has reached a frame count terminus or that the receive signaling stack [STACK; addr 0DA] has been updated with new signaling during the prior multiframe. Processor reads ISR3 [addr 008] to locate specific source.
0 = no event
1 = active interrupt request

DL1 Data Link Controller 1 or BOP Transmit—Indicates that a transmit or receive interrupt issued by DL1 or BOP transceiver has begun transmitting a priority codeword from TBOP [addr 0A1]. Processor reads ISR2 [addr 009] to locate specific source.
0 = no event
1 = active interrupt request

DL2 Data Link Controller 2 or BOP Receive—Indicates that a transmit or receive interrupt issued by DL2 or BOP transceiver has received a valid priority codeword and updated RBOP [addr 0A2]. Processor reads ISR1 [addr 00A] to locate specific source.

0 = no event

1 = active interrupt request

PATT PRBS Pattern or Transmit Framer Error—Indicates detection of PRBS test pattern sync or detection of one or more transmit frame alignment pattern errors. Processor reads ISR0 [addr 00B] to locate specific source.

0 = no event

1 = active interrupt request

3.5 Interrupt Status Registers

An Interrupt Status Register (ISR) bit is latched active (high) whenever its corresponding interrupt source reports an interrupt event. The processor reads ISR to clear all latched ISR bits. If the corresponding interrupt enable is active (high), each interrupt event forces the associated IRR bit active (high). Interrupt sources fall into two categories:

- Rising-edge source reports an interrupt event when status changes from inactive to active state. Unless specifically noted otherwise, all ISR bits are rising-edge sources.
- Dual-edge source reports an interrupt event when status changes from inactive to active (rising edge), or from active to inactive (falling edge). The processor must read the associated real-time status to determine which edge occurred.

Interrupt events are reported in real time in the MIR register and on the INTR* output pin if interrupt enable is active (high). Otherwise, the interrupt status is latched and reported according to the selected latching mode [LATCH; addr 046] without asserting the MIR bit or the INTR* output pin. Table 3-6 summarizes the interrupt status registers.

Table 3-6. Interrupt Status Register Summary

Bit	004 ISR7 ALARM1	005 ISR6 ALARM2	006 ISR5 ERROR	007 ISR4 COUNT	008 ISR3 TIMER	009 ISR2 DL1	00A ISR1 DL2	00B ISR0 PATT
0	SIGFRZ	ONESEC	FERR	FERR[12]	RFRAME	TMSG	TMSG	TFERR
1	RLOF	TLOF	MERR	CRC[10]	RMF	TNEAR	TNEAR	TMERR
2	RLOS	—	SERR	LCV[16]	RMSYNC	TEMPTY	TEMPTY	TSERR
3	RALOS	TLOC	CERR	FEBE[10]	RSIG	TDLERR	TDLERR	TCERR
4	RAIS	—	—	BERR[12]	TFRAME	RMSG	RMSG	PSYNC
5	RPDV	TPDV	—	SEF[2]	TMF	RNEAR	RNEAR	BSLIP
6	RYEL	LOOPUP	RSLIP	COFA[2]	TMSYNC	RFULL	RFULL	—
7	RMYEL	LOOPDN	TSLIP	FRED[4]	TSIG	TBOP	RBOP	—

004—Alarm 1 Interrupt Status (ISR7)

All events reported in ISR7 are from dual-edge sources, except Receive Pulse Density Violation [RPDV]. Any transition of real-time status in Alarm 1 Status Register [ALM1; addr 047] forces the corresponding ISR7 status bit active (high). Active high status is latched and held according to the LATCH_ALM bit [addr 046]. Each event triggers an interrupt if the corresponding IER7 bit is enabled [addr 00C].

7	6	5	4	3	2	1	0
RMYEL	RYEL	RPDV	RAIS	RALOS	RLOS	RLOF	SIGFRZ

RMYEL Loss/Recovery of Multiframe Yellow Alarm—Reports any change in real-time status of Multiframe Yellow (E1) or ESF Yellow (T1) alarm detector.
0 = no event
1 = multiframe yellow alarm transition

RYEL Loss/Recovery of Yellow Alarm—Reports any change in real-time status of Remote Alarm Indication (RAI), also referred to as yellow alarm.
0 = no event
1 = yellow alarm transition

RPDV Receive Pulse Density Violation—Reports each occurrence of a receive pulse density violation according to ANSI T1.403 sliding window criteria. RPDV is latched active upon detection of any window of 8 (N+1) bits which does not contain at least N pulses. For example, RPDV reports each occurrence of 16 consecutive zeros.
0 = no error
1 = receive pulse density violation

RAIS Loss/Recovery of Alarm Indication Signal—Reports any change in real-time status of the AIS detector.
0 = no event
1 = AIS transition

RALOS Loss/Recovery of Receive Signal or Clock—Reports any change in RALOS [ALM1; addr 047] status. RALOS can be configured to report receive loss of clock or a continuous loss of signal for 1 msec.

RLOS Loss/Recovery of Receive Signal—Reports any change in real-time status of digital receive signal detector.
0 = no event
1 = receive signal transition

RLOF Loss/Recovery of Frame Alignment—Reports any change in real-time or integrated status of receive online frame status monitor.
0 = no event
1 = receive frame status transition

SIGFRZ Loss/Recovery of Signaling Freeze—Reports any change in real-time status of the SIGFRZ receiver status, which is also available on the SIGFRZ output pin.
0 = no event
1 = SIGFRZ transition

005—Alarm 2 Interrupt Status (ISR6)

All events reported in ISR6 are from dual-edge sources, except the one-second timer [ONESEC] and Transmit Pulse Density Violation [TPDV]. Any transition of real-time status in the Alarm 2 Status Register [ALM2; addr 048] forces the corresponding ISR6 status bit active (high). Active-high status is latched and held according to the LATCH_ALM bit [addr 046]. Each event triggers an interrupt if the corresponding IER6 bit is enabled [addr 00D].

7	6	5	4	3	2	1	0
LOOPDN	LOOPUP	TPDV	—	TLOC	—	TLOF	ONESEC

LOOPDN Loss/Recovery of Inband Loopback Deactivate Code—Reports any change in real-time status of inband loopback deactivate code detector.
0 = no event
1 = LOOPDN code transition

LOOPUP Loss/Recovery of Inband Loopback Activate Code—Reports any change in real-time status of inband loopback activate code detector.
0 = no event
1 = LOOPUP code transition

TPDV Transmit PDV Monitor/Enforcer—Applicable only if TZCS [addr 071] enables PDV enforcement. When enabled, TPDV is latched active if one or more PDV-enforced ones were output in order to meet ANSI T1.403 minimum pulse density requirements.
0 = no error
1 = PDV-enforced one

TLOC Loss/Recovery of Transmit Clock—Reports any change in real-time status of TCKI clock monitor.
0 = No alarm
1 = clock monitor transition

TLOF Loss/Recovery of Transmit Frame Alignment—Reports any change in real-time status of transmit framer's basic alignment.
0 = no alarm
1 = transmit framer transition

ONESEC One Second Timer Event—ONESEC is derived from the internal 1-second timer or the rising edge of ONESEC input signal according to the selected I/O mode [PIO; addr 018].
0 = no timer event
1 = ONESEC timer expired or rising edge of ONESEC input

006—Error Interrupt Status (ISR5)

All events in ISR5 are from rising edge sources. Each event is latched active high and held according to the LATCH_ERR bit [addr 046] and triggers an interrupt if the corresponding IER5 bit is enabled [addr 00E].

7	6	5	4	3	2	1	0
TSLIP	RSLIP	—	—	CERR	SERR	MERR	FERR

TSLIP Transmit Slip Error—Two types of TSLIP buffer errors are reported: TFSLIP or TUSLIP. Error type is reported separately in slip status [SSTAT; 0D9].
0 = no error
1 = TSLIP error

RSLIP Receive Slip Error—Two types of RSLIP buffer errors are reported: RFSLIP or RUSLIP. Error type is reported separately in slip status [SSTAT; 0D9].
0 = no error
1 = RSLIP error

CERR CRC6/CRC4 Block Error—Applicable to ESF and MFAS modes only, read zero in other modes. CERR indicates one or more bit errors found in received CRC-6 or CRC-4 checksum block pattern.
0 = no error
1 = CRC error

SERR CAS Pattern Error—Applicable only in E1 mode, read zero in T1 mode. SERR indicates one or more bit errors in received TS16 Multiframe Alignment Signal (MAS).
0 = no error
1 = CAS error

MERR MFAS Pattern Error—Applicable only in E1 mode (read zero in T1 mode)—Indicates one or more bit errors in received MFAS alignment pattern.
0 = no error
1 = MFAS error

FERR Frame Error—Ft/Fs/T1DM/FPS/FAS Pattern Error—Indicates one or more Ft/Fs/FPS frame bit errors or FAS pattern errors. Refer to Tables A-1 through A-6 for a description of which frame bits are monitored according to the selected receive framer mode.
0 = no error
1 = frame error

007—Counter Overflow Interrupt Status (ISR4)

All count overflow events in ISR4 are from rising edge sources. Each event is latched active high when the respective error counter [addr 050–05A] reaches its maximum count value, but only while the respective IER4 [addr 00F] interrupt enable bit is active. If the corresponding interrupt is masked, then no overflow status is reported. Active overflow status bits are held until the processor read clears ISR4. Each event triggers an interrupt if the corresponding IER4 bit is enabled.

7	6	5	4	3	2	1	0
FRED[4]	COFA[2]	SEF[2]	BERR[12]	FEBE[10]	LCV[16]	CRC[10]	FERR[12]

FRED[4] Out of Frame Error Count Overflow

COFA[2] Change of Alignment Count Overflow

SEF[2] Severely Errored Frame Count Overflow

BERR[12] Test Pattern Bit Error Count Overflow

FEBE[10] FEBE Error Count Overflow

LCV[16] LCV (BPV+EXZ) Error Count Overflow

CRC[10] CRC6/CRC4 Error Count Overflow

FERR[12] Ft/Fs/FPS/FAS Error Count Overflow

008—Timer Interrupt Status (ISR3)

All events in ISR3 are from rising edge sources. Each event is latched active high and held until the processor read clears ISR3. Each event triggers an interrupt if corresponding IER3 bit is enabled [addr 010].

7	6	5	4	3	2	1	0
TSIG	TMSYNC	TMF	TFRAME	RSIG	RMSYNC	RMF	RFRAME

TSIG Transmit Signaling Multiframe—Activated every 1.5 ms (SF/SLC), 3 ms (ESF), or 2 ms (CAS) coincident with the first bit of a transmit signaling multiframe.
0 = no timer event
1 = transmit signaling multiframe

TMSYNC TX System Bus MF Sync—Activated every 1.5 ms (SF/SLC), 3 ms (ESF), or 2 ms (CAS) coincident with the first bit of transmit system bus multiframe input on TPCMI.
0 = no timer event
1 = TSB multiframe

TMF Transmit Multiframe—TMF is activated every 1.5 ms (SF/SLC), 3 ms (ESF), or 2 ms (MFAS) coincident with the first bit of a transmit multiframe.
0 = no timer event
1 = transmit multiframe

TFRAME Transmit Frame—Activated every 193 bits (T1) or 256 bits (E1) coincident with first bit of a transmit frame. Processor may read TPHASE [addr ODC] to determine which TSLIP buffer half can be accessed.
0 = no timer event
1 = transmit frame

RSIG Receive Signaling Stack—Indicates that one or more signaling bit changes were detected during the prior receive multiframe, and that new ABCD (robbed bit or CAS) signaling is available on the Receive Signaling Stack Register [addr 0DA]. RSIG is cleared by processor read of ISR3, independent of STACK contents.
0 = no stack update
1 = new ABCD signaling

RMSYNC Receive System Bus MF Sync—Activated every 3 ms (SF/SLC/ESF), or 2 ms (CAS) coincident with the first bit of receive system bus multiframe output on RPCMO.
0 = no timer event
1 = RSB multiframe

RMF Receive Multiframe Boundary—RMF is activated every 1.5 ms (SF/SLC), 3 ms (ESF), or 2 ms (MFAS) coincident with the first bit of a received multiframe. If MAS is not included in the receive framer criteria, then RMF is activated at 2 ms interval.
0 = no timer event
1 = receive multiframe

RFRAME Receive Frame Boundary—Activated every 193 bits (T1) or 256 bits (E1) coincident with the first bit of a received frame. Processor may read RPHASE [addr 0DB] to determine which RSLIP buffer half can be accessed.
0 = no timer event
1 = receive frame

009—Data Link 1 Interrupt Status (ISR2)

All events in ISR2 are from rising edge sources. Each event is latched active high and held until the processor read clears ISR2. Each event triggers an interrupt if the corresponding IER2 bit is enabled [addr 011].

7	6	5	4	3	2	1	0
TBOP	RFULL1	RNEAR1	RMSG1	TDLERR1	TEMPTY1	TNEAR1	TMSG1

TBOP BOP Codeword Transmitted—Set when a valid Bit Oriented Codeword has been transmitted and a new TBOP value can be written [TBOP; addr 0A1].

RFULL1 Receive FIFO Full—In HDLC modes, RFULL is set when the data link receiver attempts to write received data to a full FIFO causing the receive data link FIFO to overrun. In unformatted modes (Pack6 and Pack8), RFULL is set when the receive FIFO is filled to the MSG_FILL Limit selected in register RDL1_FFC [addr 0A7].

RNEAR1 Receive FIFO Near Full—Set when the receive FIFO fill level reaches the near full threshold selected in register RDL1_FFC [addr 0A7].

RMSG1 Message Received—Set when a complete message or a partial message is received and available in the receiver FIFO.

TDLERR1 Transmit FIFO Error—Set when the FIFO underruns as a result of the internal logic emptying the FIFO without encountering an end of message [TDL1_EOM; addr 0AC]. The underrun condition also forces transmission of an HDLC abort code.

TEMPTY1 Transmit FIFO Empty—Set when the FIFO overflows as a result of the processor attempting to write to a full FIFO. Overflow data is ignored by the transmit FIFO.

TNEAR1 Transmit FIFO Near Empty —Set when the transmit FIFO level falls below the threshold selected in register TDL1_FEC [addr 0AB].

TMSG1 Message Transmitted—Set when a complete message has been transmitted and the closing flag is just beginning transmission.

00A—Data Link 2 Interrupt Status (ISR1)

All events in ISR1 are from rising edge sources. Each event is latched active high and held until the processor read clears ISR1. Each event triggers an interrupt if the corresponding IER1 bit is enabled [addr 012].

7	6	5	4	3	2	1	0
RBOP	RFULL2	RNEAR2	RMSG2	TDLERR2	TEMPTY2	TNEAR2	TMSG2

RBOP BOP Codeword Received—Set when a valid Bit Oriented Codeword is received and available in the RBOP register [addr 0A2].

RFULL2 Receive FIFO Full—In HDLC modes, RFULL is set when the data link receiver attempts to write received data to a full FIFO causing the receive data link FIFO to overrun. In unformatted modes (Pack6 and Pack8), RFULL is set when the receive FIFO is filled to the MSG_FILL limit selected in register RDL2_FFC [addr 0B2].

RNEAR2 Receive FIFO Near Full—Set when the receive FIFO fill level reaches the near full threshold selected in register RDL2_FFC [addr 0B2].

RMSG2 Message Received—Set when a complete message or a partial message is received and available in the receiver FIFO.

TDLERR2 Transmit FIFO Error—Set when the FIFO underruns as a result of the internal logic emptying the FIFO without encountering an end of message [TDL2_EOM; addr 0B7]. The underrun condition also forces transmission of an HDLC abort code.

TEMPTY2 Transmit FIFO Empty—Set when the FIFO overflows as a result of the processor attempting to write to a full FIFO. Overflow data is ignored by the transmit FIFO.

TNEAR2 Transmit FIFO Near Empty—Set when the transmit FIFO level falls below the threshold selected in register TDL2_FEC [addr 0B6].

TMSG2 Message Transmitted—Set when a complete message has been transmitted and the closing flag is just beginning transmission.

00B—Pattern Interrupt Status (ISR0)

All events in ISR0 are from rising edge sources. Each event is latched active high and held until the processor read clears ISR0. Each event triggers an interrupt if the corresponding IER0 bit is enabled [addr 013].

7	6	5	4	3	2	1	0
—	—	BSLIP	PSYNC	TCERR	TSERR	TMERR	TFERR

BSLIP Online Framer Bit Slip—Active high, indicates receive online framer adjusted receive frame sync by ±1 bit. When BSLIP occurs, the apparent FAS error is not reported elsewhere (not to FERR count, RLOF circuit, or SEF circuit). Applicable only to receive framer modes with BSLIP enabled (see Table 3-5).
0 = no error
1 = frame bit slip

PSYNC Receive PRBS Test Pattern Sync—Forced to inactive (low) status when the processor requests RESEED [addr 041] of the PRBS sync detector and remains low while the detector searches for test pattern sync. PRBS bit errors [BERR; addr 058, 059] are not counted while PSYNC is low. PSYNC remains low for a minimum of 128 bits following RESEED and for as long as the received bit error ratio (BER) exceeds 10E-2. PSYNC is latched active (high) and the PRBS sync detector stops searching when no bit errors are found for a period of 96 bits. The sync detector remains disabled until the processor requests another RESEED. Therefore, any range of BER can be measured after initial pattern sync. The processor must determine criteria for loss of pattern sync based on its accumulation of bit errors over the desired time interval.
0 = no sync
1 = PRBS test pattern sync

TCERR Transmit CRC Error—Reports occurrences of CRC-6 or CRC-4 errors detected on TPCMI data according to the selected T1/E1 mode.
0 = no error
1 = CRC error

TSERR Transmit CAS Error—Reports occurrences of MAS pattern errors detected on TPCMI data if CAS transmit framer mode is selected.
0 = no error
1 = CAS error

TMERR Transmit Multiframe Error—Reports occurrences of Fs or MFAS errors detected on TPCMI data according to the selected transmit framer mode.
0 = no error
1 = transmit multiframe error

TFERR Transmit Frame Error—Reports occurrences of Ft, FPS, or FAS errors detected on TPCMI data according to the selected transmit framer mode.
0 = no error
1 = transmit frame error

3.6 Interrupt Enable Registers

Writing a one to an IER bit allows that specific interrupt source to activate its respective ISR bit, the associated MIR bit. While cleared, each IER bit allows that source to activate its respective ISR bit, but prevents activation of the MIR bit.

00C—Alarm 1 Interrupt Enable Register (IER7)

7	6	5	4	3	2	1	0
RMYEL	RYEL	RPDV	RAIS	RALOS	RLOS	RLOF	SIGFRZ

RMYEL Enable RMYEL Interrupt

RYEL Enable RYEL Interrupt

RPDV Enable RPDV Interrupt

RAIS Enable RAIS Interrupt

RALOS Enable RALOS Interrupt

RLOS Enable RLOS Interrupt

RLOF Enable RLOF Interrupt

SIGFRZ Enable SIGFRZ Interrupt

00D—Alarm 2 Interrupt Enable Register (IER6)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
LOOPDN	LOOPUP	TPDV	—	TLOC	—	TLOF	ONESEC

LOOPDN Enable LOOPDN Interrupt

LOOPUP Enable LOOPUP Interrupt

TPDV Enable TPDV Interrupt

TLOC Enable TLOC Interrupt

TLOF Enable TLOF Interrupt

ONESEC Enable ONESEC Interrupt

00E—Error Interrupt Enable Register (IER5)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
TSLIP	RSLIP	—	—	CERR	SERR	MERR	FERR

TSLIP Enable TSLIP Interrupt

RSLIP Enable RSLIP Interrupt

CERR Enable CERR Interrupt

SERR Enable SERR Interrupt

MERR Enable MERR Interrupt

FERR Enable FERR Interrupt

00F—Count Overflow Interrupt Enable Register (IER4)

7	6	5	4	3	2	1	0
LOF	COFA	SEF	BERR	FEBE	LCV	CRC	FERR

LOF Enable LOF Count Overflow Interrupt

COFA Enable COFA Count Overflow Interrupt

SEF Enable SEF Count Overflow Interrupt

BERR Enable BERR Count Overflow Interrupt

FEBE Enable FEBE Count Overflow Interrupt

LCV Enable LCV Count Overflow Interrupt

CRC Enable CRC Count Overflow Interrupt

FERR Enable FERR Count Overflow Interrupt

Table 3-7. Counter Overflow Behavior

IER4	LATCH_CNT	Count (addr 050–05A)			MIR*
Addr 00F	Addr 046	Saturate	Latch	Clear	Active
0	0	Hold all Ones	hi @rd_LSB	hi @rd_MSB	None
1	0	Rollover	hi @rd_LSB	hi @rd_MSB	@rollover
0	1	Hold all Ones	onesec	None	None
1	1	Rollover	onesec	none	@rollover

010—Timer Interrupt Enable Register (IER3)

7	6	5	4	3	2	1	0
TSIG	TMSYNC	TMF	TFRAME	RSIG	RMSYNC	RMF	RFRAME

TSIG Enable TSIG Interrupt

TMSYNC Enable TMSYNC Interrupt

TMF Enable TMF Interrupt

TFRAME Enable TFRAME Interrupt

RSIG Enable RSIG Interrupt

RMSYNC Enable RMSYNC Interrupt

RMF Enable RMF Interrupt

RFRAME Enable RFRAME Interrupt

011—Data Link 1 Interrupt Enable Register (IER2)

7	6	5	4	3	2	1	0
TBOP	RFULL1	RNEAR1	RMSG1	TDLERR1	TEMPTY1	TNEAR1	TMSG1

TBOP Enable TBOP Interrupt

RFULL1 Enable RFULL Interrupt

RNEAR1 Enable RNEAR Interrupt

RMSG1 Enable RMSG Interrupt

TDLERR1 Enable TDLERR Interrupt

TEMPTY1 Enable TEMPTY Interrupt

TNEAR1 Enable TNEAR Interrupt

TMSG1 Enable TMSG Interrupt

012—Data Link 2 Interrupt Enable Register (IER1)

7	6	5	4	3	2	1	0
RBOP	RFULL2	RNEAR2	RMSG2	TDLERR2	TEMPTY2	TNEAR2	TMSG2

RBOP Enable RBOP Interrupt

RFULL2 Enable RFULL Interrupt

RNEAR2 Enable RNEAR Interrupt

RMSG2 Enable RMSG Interrupt

TDLERR2 Enable TDLERR Interrupt

TEMPTY2 Enable TEMPTY Interrupt

TNEAR2 Enable TNEAR Interrupt

TMSG2 Enable TMSG Interrupt

013—Pattern Interrupt Enable Register (IER0)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	BSLIP	PSYNC	TCERR	TSERR	TMERR	TFERR

BSLIP Enable BSLIP Interrupt

PSYNC Enable PSYNC Interrupt

TCERR Enable TCERR Interrupt

TSERR Enable TSERR Interrupt

TMERR Enable TMERR Interrupt

TFERR Enable TFERR Interrupt

3.7 Primary Control and Status Registers

014—Loopback Configuration Register (LOOP)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	—	PLOOP	LLOOP	FLOOP	—

PLOOP Enable Remote Payload Loopback—Payload from receiver replaces payload on transmitter output. Loopback payload retains time slot and frame integrity, such that numbered time slots from each receive frame are transferred to the same numbered time slots in the transmit frame. Transmit overhead bits, Fbits in T1 mode or TS0 in E1 mode, are supplied by transmit frame formatter or by transmit system bus according to TFRM [addr 072] settings. Existing transmit frame alignment and clock timing is not altered by PLOOP activation or deactivation, thus allowing system operation with independent receive and transmit timing. Controlled frame slips are performed in the payload loopback path if receive and transmit clocks are asynchronous, although these slips are not reported to the processor as slip buffer errors. Multiframe integrity is not maintained during PLOOP. This means that DS0 channel loopbacks [TPCn; addr 100–11F] must be used to implement payload loopbacks when transparent or forced signaling is desired. Note that TIDLE (in TPCn) overrides PLOOP.

0 = no loopback
1 = payload loopback

LLOOP Enable Remote Line Loopback—Received dual-rail unipolar data (RPOSI, RNEGI) is internally connected to transmit dual-rail unipolar data (TPOSO, TNEGO). The receive clock must also be looped when LLOP is selected in CMUX [addr 01A]; TXCLK must be set to 01 to select RCKI as the transmit clock. Loopback data retains BPV transparency. Data input from transmit system bus continues to pass through the transmitter, but is ignored at ZCS encoder outputs. Received data to RSB block is unaffected. LLOOP and FLOOP can be active simultaneously to support both line and network loopbacks at the same time.

0 = no loopback
1 = line loopback

FLOOP Enable Local Framer Loopback—Dual-rail unipolar data from transmit ZCS encoder is internally connected to receive ZCS decoder inputs. Clock switching is automatic during FLOOP loopback mode.

0 = no loopback
1 = framer loopback

015—External Data Link Time Slot (DL3_TS)

DL3_TS works in conjunction with the DL3_BIT Register [addr 016] to determine which transmit time slots are supplied from the TDLI pins and which receive and transmit time slots are accompanied by a gated RDLCKO and TDLCKO output. Refer to Figure 2-21, *Transmit External Data Link Waveforms*. Note that RDLO outputs the entire receive data bit stream, and only selective time slots are marked by RDLCKO. DL3 is not accessible on the CX28395 device, therefore, DL3_TS must be written to 00.

CX28394, CX28398

7	6	5	4	3	2	1	0
DL3EN	ODD	EVEN	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]

CX28395

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

DL3EN Enable External Data Link—Active high enables data insertion from TDLI and clock gating on TDLCKO and RDLCKO outputs according to the selected external data link mode. PIO [addr 018] must select TDL_IO and/or RDL_IO to enable external data link signals.

0 = external data link pins inactive
1 = TDLI/TDLCKO and RDLO/RDLCKO active

ODD/EVEN Odd/Even Frame Select—The external data link is programmed to source and sink data bits during all frames or odd or even frames only. ODD/EVEN also controls gating of RDLCKO and TDLCKO external data link clocks. Frames are counted from 0 through 15 in E1 mode and 1 through 24 in T1 mode, where frames 1, 3, 5 etc., are always considered ODD frames. ODD/EVEN is ignored if T1 Fbits are selected in DL3_TS.

ODD	EVEN	Frame Select
0	0	None. Equivalent to disabling external data link.
0	1	Even frames only. Frame 0, 2, 4, 6, etc.
1	0	Odd frames only. Frame 1, 3, 5, 7, etc.
1	1	All frames

TS[4:0] External Data Link Time Slot Select—Picks one 8-bit time slot for input and output over the external data link pins. Any time slot can be chosen from TS0 to TS31 in E1 mode, or TS1 to TS24 in T1 mode. In T1 mode, TS0 selects Fbits instead of a channel time slot.

00000 T1 Fbits or E1 Time Slot 0
00001 Time Slot 1
| |
11110 Time Slot 30
11111 Time Slot 31

016—External Data Link Bit (DL3_BIT)

7	6	5	4	3	2	1	0
DL3_BIT[7]	DL3_BIT[6]	DL3_BIT[5]	DL3_BIT[4]	DL3_BIT[3]	DL3_BIT[2]	DL3_BIT[1]	DL3_BIT[0]

DL3_BIT[7:0] External Data Link Bit Select—Enables receive (RDLCKO) and transmit (TDLCKO) clock pulse outputs during the selected time slot bits. DL3_BIT and the DL3_TS Register [addr 015] select any combination of bits for input and output on the external data link pins by writing the corresponding DL3_BIT active (high). LSB enables clock pulses coincident with the first bit transmitted or received. Full T1/E1 data stream is output on RDLO as long as the RDL_IO bit [addr 018] is active and regardless of which bits are accompanied by RDLCKO clock pulses. The selected transmit data link bits are sampled from the TDLI pin on the falling edge of TDLCKO to replace normal transmitted data. DL3_BIT has no effect when DL3_TS selects T1 Fbits or when the DL3EN bit is inactive. DL3 is not accessible on the CX28395 device.

0 = disable DL3 bit

1 = enable DL3 bit

017—Offline Framer Status (FSTAT)

Each framer contains a single offline framer that acts as a shared resource for both receive and transmit channels. Current alignment status for receive and transmit channels are reported separately in Alarm Status Registers (ALM1, ALM2; addr 047, 048). FSTAT is thus used primarily for diagnostic purposes to monitor the progress of an alignment search or to verify acknowledgment of a processor-generated forced reframe request. These status bits may only be reported for a very short period of time (i.e., 1 clock cycle) since the RLOF and TLOF reframe requests may immediately request another offline framer search.

7	6	5	4	3	2	1	0
—	—	—	INVALID	FOUND	TIMEOUT	ACTIVE	RX/TXN

INVALID No Candidate—Active high at the conclusion of a search during which no frame alignment candidates were located.

0 = search active, aborted, timed out, or found

1 = alignment not found (no candidate)

FOUND Frame Search Successful—Active high indicates the offline framer located frame alignment according to the selected receive or transmit framer mode. Refer to Table 3-8 for Maximum Average Reframe Time. Upon detection of frame alignment, the following occurs: FOUND goes active high, RLOF or TLOF is cleared by the online framer (depending on RX/TX direction), offline framer goes inactive (if no pending reframe requests), and RX, TX, or TSB timebase is realigned (depending on RX/TX direction and the embedded framing mode). If the reframe pulse causes the receive timebase to align to a position that differs from its existing alignment, the change of frame alignment error counter [COFA; addr 05A] will increment. Changes of the transmit frame alignment are not detected.

0 = no candidate: search active, aborted, or timed out

1 = frame alignment found (one and only one candidate)

NOTE: In E1 receive framer modes, the offline framer also reports intermediate FRED, MRED, and SRED status [ALM3; addr 049] while searching for FAS/MFAS/CAS alignment, respectively.

TIMEOUT Framer Search Timeout—Cleared when the offline framer transitions to its ACTIVE state. If multiple frame candidates exist over the entire mode-dependent timeout interval (refer to Table 3-8), TIMEOUT is latched active high. Processor-generated reframe requests (RFORCE or TFORCE) initiate a single search that extends for up to 24 ms before TIMEOUT. After reporting TIMEOUT, the offline framer starts another search if the reframe request (RLOF or TLOF) is active.

0 = no candidate; search active, aborted, or found
1 = framer search timeout (multiple candidates)

Table 3-8. Maximum Average Reframe Time (MART) and Framer Timeout

Framer Mode	MART	TIMEOUT (addr 017)
Ft	3.5 ms	12 ms ±1 bit
Ft + T1DM	1.0 ms	12 ms ±1 bit
SF	3.5 ms	12 ms ±1 bit
SF + JYEL	4.5 ms	12 ms ±1 bit
SF + TIDM	2.0 ms	12 ms ±1 bit
SLC	15.0 ms	24 ms ±1 bit
ESF	10.0 ms	24 ms ±1 bit
ESF + CRC	15.0 ms	24 ms ±1 bit
ESF + MIMIC	15.0 ms	24 ms ±1 bit
FAS	0.5 ms	8 ms ±125 µs
CAS	2.0 ms	8 ms ±125 µs
MFAS	10.0 ms	8 ms ±125 µs
NOTE(S): MART is defined (per Bellcore TA-0278) as the difference between the time that known good pseudo-random DS1 input is applied and the time that a valid DS0 signal is observed at the output.		

ACTIVE Framer Active—Offline framer transitions to its ACTIVE state in response to RFORCE or TFORCE reframe request from the processor or in response to RLOF or TLOF reframe request from an online framer. Offline framer remains ACTIVE until alignment is found (FOUND), search is aborted [see RABORT, addr 040; or TABORT, addr 071], search reaches its timeout interval (TIMEOUT), or all possible frame candidates are eliminated (INVALID).

0 = offline framer inactive; search completed, aborted or timed out
1 = offline framer actively searching for alignment

NOTE: RFORCE or TFORCE don't change current RLOF or TLOF status. RFORCE or TFORCE is cleared by framer transition to ACTIVE.

RX/TXN RX/TX Reframe Operation—Indicates which direction the offline framer is actively searching or most recently searched for frame alignment. RX/TXN status is updated when offline framer transitions to its ACTIVE state in response to a reframe request.

0 = search data from Transmit System Bus PCM Input (TPCMI)
1 = search data from receive line interface unit

018—Programmable Input/Output (PIO)

7	6	5	4	3	2	1	0
RMSYNC_EN	RDL_IO	TMSYNC_EN	TDL_IO	RFSYNC_IO	RMSYNC_IO	TFSYNC_IO	TMSYNC_IO

RMSYNC_EN Enable RMSYNC—Select which signal is present on bimodal pin, RFSYNC/RMSYNC. When active, receiver multiframe sync (RMSYNC) is enabled. Otherwise, receiver frame sync RFSYNC is enabled.

RDL_IO Enable Receiver Data Link—Select which signals are present on bimodal RDLCKO and RDLO. When active Receiver Data Link Clock Out (RDLCKO) and Receive Data Link Data Out (RDLO) are enabled. Otherwise RINDO and RSIGO are as follows:

0 = select RINDO and RSIGO
1 = select Receive Data Link

TMSYNC_EN Enable TMSYNC—Select which signal is present on bimodal pin, TFSYNC/TMSYNC. When active, transmit multiframe sync (TMSYNC) is enabled. Otherwise, receiver frame sync TFSYNC is enabled.

TDL_IO Enable Transmit Data Link—Select which signals are present on bimodal TDLCKO and TDLI. When active Transmit Data Link Clock Out (TDLCKO) and Transmit Data Link Data Out (TDLO) are enabled. On the CX28395 device, TDL3 is not available and TDL_IO must be written to 0.

0 = select TINDO and TSIGI
1 = select Transmit Data Link

RFSYNC_IO Bidirectional RFSYNC Input/Output Mode—Refer to the system bus sync mode summary in Tables 3-9 and 3-11. When RFSYNC is an input, its low to high transition aligns the RSB timebase to the programmed RSB.OFFSET. Refer to RSYNC_BIT, RSYNC_TS, and RSYNC_FRM offset registers [addr 0D2, 0D3, and 0D8] for a complete description of the RSB Sync Bits Time Slot and Frame Offset. Once aligned, the RSB timebase internally flywheels at a 125 µs interval (8 kHz) until a new RFSYNC pulse is applied. When RFSYNC is programmed as an output, it operates continuously at a 8 kHz frame rate, marking the RSB sync bits and time slot offset position of each frame. Initial RFSYNC alignment and subsequent realignment depends upon RSB Mode [RSBI; addr 0D1] and RSB manual center [RSB_CTR; addr 0D1]. RFSYNC must be programmed as an output when RSLIP is in bypass mode. RFSYNC and RMSYNC are supplied either by the RSB timebase (output) or receive system bus (input) at a programmable RSB sync bit offset, time slot location and frame offset location.

0 = RFSYNC input
1 = RFSYNC output

RMSYNC_IO Bidirectional RMSYNC Input/Output Mode—Refer to the system bus sync mode summary in Table 3-9. When RMSYNC is an input, its low-to-high transition aligns the RSB timebase to the programmed RSB.OFFSET. Once aligned, the RSB timebase internally flywheels at a 3 ms (T1) or 2 ms (E1) interval until a new RMSYNC pulse is applied. Note that RMSYNC input signal must always coincide with RFSYNC. When RMSYNC is an output, it operates continuously at the 6 ms multiframe rate, marking the RSB.OFFSET position of every second multiframe (T1) or every third multiframe (E1). Initial RMSYNC alignment and subsequent realignment depends upon RSB mode [RSBI; addr 0D1] and RSB manual center [RSB_CTR; addr 0D1]. RMSYNC must be programmed as an output when RSLIP is in bypass mode or transparent signaling mode [THRU; addr 0D7].

0 = RMSYNC input
1 = RMSYNC output

TFSYNC_IO Bidirectional TFSYNC Input/Output Mode—TFSYNC_IO programming is dependent on transmit framer and system bus modes as shown in Tables 3-9 and 3-10.
0 = TFSYNC input
1 = TFSYNC output

TMSYNC_IO Bidirectional TMSYNC Input/Output mode—TMSYNC_IO programming is dependent on transmit framer and system bus modes as shown in Tables 3-9 and 3-10.
0 = TMSYNC input
1 = TMSYNC output

Table 3-9. System Bus Sync Mode Summary

FSYNC	MSYNC	SBI Alignment Mode
IN	IN	SBI supplies multiframe and 8 kHz frame alignment. FSYNC must be aligned with MSYNC if both are provided.
IN	IN-GND	SBI supplies 8 kHz frame alignment. Multiframe alignment is arbitrary and MSYNC is unused.
IN	OUT	SBI supplies 8 kHz frame alignment. Multiframe alignment is supplied by the framer.
IN-GND	OUT	Framer supplies multiframe alignment. FSYNC is unused.
OUT	IN	SBI supplies multiframe and frame alignment.
OUT	OUT	Framer supplies frame and multiframe alignment.

Table 3-10. Common TFSYNC and TMSYNC Configurations

Conditions	TFSYNC	TMSYNC	Explanation
Transmit framer disabled. (TABORT = 1)	IN	IN	TSB timebase slaved to system bus TFSYNC or TMSYNC.
	IN-GND	IN	TSB timebase slaved to system bus TMSYNC. TFSYNC is unused.
	IN	IN-GND	TSB timebase slaved to system bus TFSYNC. TMSYNC is unused and multiframe alignment is arbitrary.
	IN	OUT	SB timebase slaved to system bus TFSYNC. TMSYNC alignment is arbitrary.
	OUT	OUT	TSB timebase alignment is arbitrary.
	OUT	IN	TSB timebase slaved to system bus TMSYNC. TFSYNC aligns to TMSYNC input.
Transmit framer enabled to search TPCMI for embedded framing. (EMBED = 0, TABORT = 0)	OUT	OUT	TSB timebase is aligned to embedded framing on TPCMI. TPCMI must be configured to line rate for this case.
Transmit framer enabled to search TNRZ (after TSLIP buffer) for embedded framing. (EMBED = 1, TABORT = 0)	OUT	IN-GND	TSB timebase is aligned to embedded framing on TNRZ data. TMSYNC is unused. TPCMI may be configured for 1,544 kbps or a multiple of 2,048 kbps.

Table 3-11. Common RFSYNC and RMSYNC Configurations

Conditions	RFSYNC	RMSYNC	Explanation
Thru = 0 [RSIG_CR; addr 0D7]	IN	IN	RSB timebase slaved to system bus RFSYNC or RMSYNC.
	IN	OUT	RSB timebase slaved to system bus RFSYNC. RMSYNC alignment is arbitrary.
	OUT	IN	RSB timebase slaved to system bus RMSYNC. RFSYNC aligns to TMSYNC input.
	OUT	OUT	RFSYNC and RMSYNC alignment is arbitrary.
Thru = 1 [RSIG_CR; addr 0D7]	IN	OUT	RSB timebase slaved to system bus RFSYNC. RMSYNC is aligned with the RX timebase and can follow a change of RX multiframe alignment without generating an alarm indication.
	OUT	OUT	RMSYNC is aligned with the RX timebase and can follow a change of RX multiframe alignment without generating an alarm indication. RFSYNC is aligned to RMSYNC.

019—Programmable Output Enable (POE)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	TDL_OE	RDL_OE	INDY_OE	TCKO_OE	—	—

TDL_OE TDLCKO Output Buffer Control—When enabled, TDLCKO is output according to DL3_TS and DL3_BIT [addr 015, 016]. TDL_OE should be written to 1 on the CX28395 device.
0 = TDLCKO output enabled
1 = TDLCKO output three-stated

RDL_OE RDLCKO and RDLO Output Buffer Control—When enabled, both bimodal signals are output by their respective internal circuits. Otherwise, both outputs are placed in high impedance state. RDL_OE should be written to 1 on the CX28395 device.
0 = RDLCKO and RDLO outputs enabled
1 = RDLCKO and RDLO outputs three-stated

INDY_OE RINDO and TINDO Output Buffer Control—When enabled, both bimodal signals are output by their respective internal circuits. Otherwise, both outputs are forced into high impedance state.
0 = RINDO outputs enabled
1 = RINDO outputs three-stated

TCKO_OE TCKO Output Buffer Control—Allows the system to connect multiple devices to a common clock bus by providing programmable three-state control over the TCKO output buffer.
0 = TCKO output enabled
1 = TCKO output three-stated

01A—Clock Input Mux (CMUX)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	RSBCK	—	TSBCK	—	—	TXCLK[1]	TXCLK[0]

RSBCK RSBCK Source Select—Internal clock mux selects from one of two clock signals for application to the RSB timebase. The RSBCKI input pin is ignored if TSBCKI is selected.

RSBCK	RSBCK Source	Notes
0	RSBCKI pin	Normal RSB timebase
1	TSBCKI pin	RSB slaved to TSB

TSBCK TSBCK Source Select—Internal clock mux selects from one of three clock signals for application to the TSB timebase. If TSLIP is bypassed [TSB_CR; addr 0D4], TCKI is selected. The TSBCKI input pin is ignored if TCKI or RSBCKI is selected.

TSBCK	TSBCK Source	Notes
0	TSBCKI pin	Normal TSB timebase
1	RSBCKI pin	TSB slaved to RSB
x	TCKI pin	TSLIP is bypassed

TXCLK[1:0] TXCLK Source Select—Internal transmit clock mux selects from one of three clock signals. The selected clock signal is applied to transmit clock monitor, acts as a timing reference for the transmitter block, and must operate at the T1/E1 line rate. The selected clock signal also appears on TCKO pin. The TCKI input pin is ignored whenever a clock source other than TCKI is selected.

TXCLK[1:0]	TXCLK Source	Notes
00	TCKI	Normal transmit (With TSLIP)
01	RCKI	Transmit slaved to receiver (Loop Timed)
10	RSBCKI	Transmit slaved to RSB

020—Receive Alarm Configuration (RAC)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	RAL_CON	—	—	—	—

RAL_CON RALOS Alarm Configuration – Determines whether RALOS [ALM1; addr 047] reports loss of receive clock (RCKI) or loss of receive signal for 1 msec.

0 = RALOS reports that RLOS [ALM1; addr 047] has been active for 1 msec

1 = RALOS reports loss of clock on RCKI pin

021—Receive Line Code Status (RSTAT)

7	6	5	4	3	2	1	0
—	—	ZCSUB	EXZ	BPV	—	—	—

ZCSUB Zero Code Substitution—Indicates one or more B8ZS/HDB3 substitution patterns have been detected on receiver input data, depending on T1/E1N line rate selection. ZCSUB is reported regardless of whether ZCS decoding is enabled [RAMI; addr 040]. ZCSUB is latched active high upon detection of the first ZCS pattern. The active high hold interval is defined by LATCH_ERR [addr 046].

ZCSUB	T1/E1N	ZCSUB Status
0	X	No ZCS patterns detected
1	0	HDB3 pattern detected
1	1	B8ZS pattern detected

EXZ Excessive Zeros—Reports one or more long strings of zeros detected on the receiver data inputs. Depending on bits RZCS [addr 040] and T1/E1N [addr 001], occurrences of 8, 10, or 16 consecutive zeros are detected. EXZ is latched active high upon detection of the first error. The active high hold interval is defined by LATCH_ERR [addr 046]. If EXZ_LCV [addr 045] is enabled, EXZ errors are also accumulated in LCV count [addr 054, 055].

EXZ	T1/E1N.	RZCS	EXZ Status
0	X	X	No error
1	0	X	10 consecutive zeros
1	1	0	16 consecutive zeros
1	1	1	8 consecutive zeros

BPV Bipolar Violation—Reports one or more bipolar violations detected on the receiver data inputs. Depending on RZCS [addr 040], BPV may or may not include bipolar violations received as part of a B8ZS or HDB3 zero code substitution. Detection of BPV or LCV errors can be selected regardless of whether receive ZCS decoding is enabled [RAMI; addr 040]. BPV is latched active high upon detection of the first error. The active high hold interval is defined by LATCH_ERR [addr 046]. BPV errors are also accumulated in LCV count [addr 054, 055].

BPV	T1/E1N	RZCS	BPV Status
0	X	X	No error
1	0	0	All BPVs, including HDB3 coded BPV
1	0	1	Code violation per ITU 0.162 (two consecutive BPVs of same polarity)
1	1	0	All BPVs, including B8ZS coded BPV
1	1	1	Only BPVs that are not part of B8ZS

3.8 Serial Interface Registers

These registers are not used on the CX28395 device.

022—Serial Control (SER_CTL)

Writing to SER_CTL initiates a serial interface read or write operation. During a write operation, a 16-bit word, consisting of SER_CTL and SER_DAT, is transmitted to the LIU. During a read operation, SER_CTL is transmitted and 8-bit data from the LIU is received and placed in SER_DAT register. SER_RW is transmitted first and SER_DAT[0] is transmitted or received first.

7	6	5	4	3	2	1	0
SER_A[6]	SER_A[5]	SER_A[4]	SER_A[3]	SER_A[2]	SER_A[1]	SER_A[0]	SER_RW

SER_RW Serial Read/Write – Selects the current serial interface operation type.
0 = Write
1 = Read

SER_A[6:0] Serial Interface Register Address – Identifies the LIU register address for the current read or write operation.

023—Serial Data (SER_DAT)

7	6	5	4	3	2	1	0
SER_DAT[7]	SER_DAT[6]	SER_DAT[5]	SER_DAT[4]	SER_DAT[3]	SER_DAT[2]	SER_DAT[1]	SER_DAT[0]

SER_DAT[7:0] Serial Interface Data

024—Serial Status (SER_STAT)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	SER_DONE

SER_DONE Serial Interface Done–During a read or write serial interface operation, SER_DONE is cleared indicating that an operation is in progress. After the operation is complete, this bit is set and an interrupt request is generated if enabled by SER_IER [addr 025]. SER_DONE is also cleared if read by the MPU. When the SER_DONE is cleared, the interrupt request is deactivated to allow the INTR* pin to also be deactivated if all other interrupt sources have been serviced.

025—Serial Configuration (SER_CONFIG)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
SER_CS	SER_CLK	—	—	—	—	—	SER_IER

SER_CS Serial Interface Chip Select 1
0 = sets external SERCS1* signal low
1 = sets external SERCS2* signal low

SER_CLK Serial Interface Clock
0 =1.024 MHz
1 = 8.192 MHz

SER_IER Serial Interface Interrupt Enable
0 = interrupt disabled
1 = interrupt enabled

026—RAM Test

7	6	5	4	3	2	1	0
RT[7]	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]

Reserved for Conexant Production test.

3.9 Receiver Registers

040—Receiver Configuration (RCR0)

7	6	5	4	3	2	1	0
RAMI	RABORT	RFORCE	RLOFD	RLOFC	RLOFB	RLOFA	RZCS

RAMI Receive AMI Encoded Inputs—Disables B8ZS/HDB3 decoding for AMI formatted receive signals. Otherwise, ZCS decoder replaces 000VB0VB code (B8ZS) with 8 zeros in T1 mode or replaces X00V code (HDB3) with 4 zeros in E1 mode: where B is a normal AMI pulse, V is a bipolar violation, and X is a “don't- care.” Regardless of RAMI setting, receipt of a ZCS signature is always detected and reported in ZCSUB status [RSTAT; addr 021].

0 = receive B8ZS/HDB3 line format
1 = receive AMI line format

RABORT Abort/Disable RX Offline Framer—When set, the offline framer ignores reframe requests from the online framer (RLOF) and aborts any in-progress RLOF reframe request. Loss of frame status [RLOF; addr 047] is not affected. While RABORT remains set, offline framer responds only to processor forced reframes (RFORCE). This allows the processor to manually control reframe criteria and prevent changes in the current receive frame alignment. RABORT is typically set only during unframed operation.

0 = normal framer operation
1 = framer disabled

RFORCE Force RX Reframe—Forces the offline framer to perform a single reframe according to selected receive framer mode. RFORCE is automatically cleared when offline framer acknowledges the request [FSTAT; addr 017]. The processor does not typically need to force reframe since the online framer reframe request (RLOF) is active whenever reframe criteria (RLOFD–A) is met. However, the processor may force reframe if frame or CRC error ratios indicate that the framer might have aligned to a duplicated frame alignment pattern.

0 = no effect
1 = force RX reframe

RLOFD–RLOFA RX Reframe Criteria—Determines the number of frame errors that the online framer must detect before declaring loss of frame alignment [ALM1; addr 047]. Refer to receive framer mode [RFRAME; addr 001] Table 2-1, *Receive Framer Modes*, to find which frame bits are monitored.

T1/E1N	RLOFD–A	Reframe Criteria
0	0100	3 consecutive FAS or 915 CRC errors
0	1100	3 consecutive FAS errors
1	0001	2 out of 4 F-bit errors
1	0010	2 out of 5 F-bit errors
1	0100	2 out of 6 F-bit errors

NOTE(S): Other RLOFD–RLOFA combinations are invalid. RAIS and RLOF status is disabled if RLOFD–RLOFA equals all zeros.

RZCS Receive B8ZS/HDB3 Zero Code Substitution (affects only BPV/LCV/EXZ counting)—When set, the ZCS decoder does not include bipolar violations received as part of a B8ZS/HDB3 code in the LCV error count [addr 054, 055]. Otherwise, all bipolar violations are counted. EXZ detection criteria is either 8 or 16 consecutive zeros, depending on RZCS configuration.

0 = ZCS decoder reports all occurrences of BPV; also selects EXZ = 16 zeros

1 = ZCS decoder does not report BPVs received as part of ZCS; also selects EXZ = 8 zeros

041—Receive Test Pattern Configuration (RPATT)

7	6	5	4	3	2	1	0
—	—	RESEED	BSTART	FRAMED	ZLIMIT	RPATT[1]	RPATT[0]

RESEED Reseed PRBS Sync Detector (auto clear)—If BSTART is active high, writing a one to RESEED forces the PRBS sync detector to reseed and search for test pattern sync [PSYNC; addr 00B]. The reseed and search algorithm remains active until test pattern sync is found.

0 = no effect

1 = reseed and search for test pattern sync

BSTART Enable PRBS Detector and Start Counting PRBS Bit Errors—BERR [addr 058, 059] counting is enabled when BSTART is active high, and pattern sync is found [PSYNC=1; addr 00B]. Otherwise, BERR counter holds its present value until cleared by a processor read.

0 = PRBS detector disabled and BERR stops counting

1 = enable PRBS detector and BERR counter

FRAMED PRBS Framed—When set, PRBS test pattern bits are not checked during F-bit locations in T1 mode or TS0 locations in E1 mode. Otherwise, test patterns are checked in all T1/E1 bit locations. FRAMED, ZLIMIT, and RPATT establish the test pattern measurement type as listed in Table 3-12.

Table 3-12. Receive PRBS Test Pattern Measurements *(1 of 2)*

FRAMED	ZLIMIT	RPATT	Test Pattern Measurements	Inversion
0	0	00	Unframed 2^{11}	No
0	0	01	Unframed 2^{15}	Yes
0	0	10	Unframed 2^{20}	No
0	0	11	Unframed 2^{23}	Yes
0	1	00	Unframed 2^{11} with 7 zero limit	No
0	1	01	Unframed 2^{15} with 7 zero limit (non-std)	No
0	1	10	Unframed 2^{20} with 14 zero limit (QRSS/QRS/QRTS)	No
0	1	11	Unframed 2^{23} with 14 zero limit (non-std)	No
1	0	00	Framed 2^{11}	No
1	0	01	Framed 2^{15}	Yes

Table 3-12. Receive PRBS Test Pattern Measurements (2 of 2)

FRAMED	ZLIMIT	RPATT	Test Pattern Measurements	Inversion
1	0	10	Framed 2^{20}	No
1	0	11	Framed 2^{23}	Yes
1	1	00	Framed 2^{11} with 7 zero limit	No
1	1	01	Framed 2^{15} with 7 zero limit (non-std)	No
1	1	10	Framed 2^{20} with 14 zero limit (QRSS/QRS/QRTS)	No
1	1	11	Framed 2^{23} with 14 zero limit (non-std)	No

ZLIMIT PRBS Zero Limit—Determines the number of consecutive zeros allowed within the selected PRBS test pattern. Refer to Table 3-12 for test pattern measurement options.

RPATT[1:0] PRBS Test Pattern—Selects one of four PRBS test pattern lengths used to measure received bit error ratio during out of service testing. Refer to Table 3-12 for test pattern measurement options. PRBS test patterns used by RPATT [addr 041] and TPATT [addr 076] are defined in the ITU standards O.151 and O.152 to use either inverted or non-inverted data. Standard data inversion is used for selected PRBS test patterns unless ZLIMIT is enabled, in which case the test pattern always uses non-inverted data.

042—Receive Loopback Code Detector Configuration (RLB)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	—	DN_LEN[1]	DN_LEN[0]	UP_LEN[1]	UP_LEN[0]

DN_LEN[1:0] Loopback Deactivate Code Length—Selects the number of loopback pattern bits from LBD [addr 044] that are compared to received data. This is done in order to determine whether a Loopback Deactivate Code [LOOPDN; addr 048] has been detected. LOOPDN is recovered if the received data pattern contains fewer than 63 bit errors in a 24 ms period, or lost if 64 or more bit errors are detected in a subsequent 24 ms period. F-bits that overwrite or are inserted into the loopback pattern are not counted as bit errors. Accurate code detection is provided on lines with up to 1E-3 BER.

DN_LEN	LBD Length
00	4 bits
01	5 bits
10	6 bits
11	7 bits

UP_LEN[1:0] Loopback Activate Code Length—Selects the number of loopback pattern bits from LBA [addr 043] that are compared to received data. This is done in order to determine whether a Loopback Activate Code [LOOPUP; addr 048] has been detected. LOOPUP is recovered if the received data pattern contains fewer than 63 bit errors in a 24 ms period, or lost if 64 or more bit errors are detected in a subsequent 24 ms period. F-bits that overwrite or are inserted into the loopback pattern are not counted as bit errors. Accurate code detection is provided on lines with up to 1E-3 BER.

UP_LEN	LBA Length
00	4 bits
01	5 bits
10	6 bits
11	7 bits

043—Loopback Activate Code Pattern (LBA)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
LBA[1]	LBA[2]	LBA[3]	LBA[4]	LBA[5]	LBA[6]	LBA[7]	—

LBA[1] First bit expected of LOOPUP pattern

LBA[2] Second bit expected of LOOPUP pattern

LBA[3] Third bit expected of LOOPUP pattern

LBA[4] Fourth bit expected—Last bit if UP_LEN selects a 4-bit pattern

LBA[5] Fifth bit expected—Last bit if UP_LEN selects a 5-bit pattern

LBA[6] Sixth bit expected—Last bit if UP_LEN selects a 6-bit pattern

LBA[7] Seventh bit expected—Last bit if UP_LEN selects a 7-bit pattern

044—Loopback Deactivate Code Pattern (LBD)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
LBD[1]	LBD[2]	LBD[3]	LBD[4]	LBD[5]	LBD[6]	LBD[7]	—

LBD[1] First bit expected of LOOPDN pattern

LBD[2] Second bit expected of LOOPDN pattern

LBD[3] Third bit expected of LOOPDN pattern

LBD[4] Fourth bit expected—Last bit if DN_LEN selects a 4-bit pattern

LBD[5] Fifth bit expected—Last bit if DN_LEN selects a 5-bit pattern

LBD[6] Sixth bit expected—Last bit if DN_LEN selects a 6-bit pattern

LBD[7] Seventh bit expected—Last bit if DN_LEN selects a 7-bit pattern

045—Receive Alarm Signal Configuration (RALM)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	DIS_LCV	FS_NFAS	EXZ_LCV	YEL_INTEG	RLOF_INTEG	RPCM_YEL	RPCM_AIS

DIS_LCV Disable LCV indication and counting. Primarily used in configurations where receive data is unipolar NRZ. If AUTO_PRM is enabled (PRM; addr 0AA) LV is transmitted with a default value of 0.
0 = LCV counting and indication enabled
1 = LCV counting and indication disabled

FS_NFAS Include FS/NFAS in FERR and FRED—Selects whether Fs bit errors (T1) or NFAS Bit2 errors (E1) are counted as frame errors [FERR; addr 050, 051]. Further selects whether loss of frame alignment [FRED; addr 049] includes Fs or NFAS bit errors as part of the detection criteria. Note that the number of Fs bit locations checked also depends on JYEL framer mode.
0 = FERR and FRED do not include FS/NFAS
1 = FERR and FRED include FS/NFAS

EXZ_LCV Excess Zeros Included in LCV—Whether line code violation error count [LCV; addr 054, 055] includes EXZ errors depends on the EXZ_LCV control setting. Depending on RZCS bit setting [addr 040], each EXZ is equal to either 8 or 16 consecutive zeros.
0 = LCV does not include EXZ
1 = LCV includes EXZ

YEL_INTEG Enable Yellow Alarm Integration—When set, both the receive frame and multiframe yellow alarms [RYEL and RMYEL; addr 047] are integrated, as described in Table 3-13 (per the selected framer mode). RYEL and RMYEL interrupt status [ISR7; addr 004] are similarly affected.
0 = normal RYEL and RMYEL status
1 = integrated RYEL and RMYEL status

Table 3-13. Receive Yellow Alarm Set/Clear Criteria *(1 of 2)*

Mode	Set/Clear Criteria
Y0	Set for 4 frames (500 µs) if 2 consecutive NFAS frames each contain TS0 bit 3 = 1. Cleared for 4 frames if 2 consecutive NFAS frames each contain TS0 bit 3 = 0.
Y0_INT	Set for 16 multiframes (24 ms) if every NFAS frame contains TS0 bit 3 = 1. Cleared for 16 multiframes if 1 or more NFAS frames contain TS0 bit 3 = 0.
Y16	Set for 2 multiframes (4 ms) if frame 0 in 2 consecutive multiframes contains TS16 bit 6 = 1. Cleared for 2 multiframes if frame 0 in 2 consecutive multiframes contains TS16 bit 6 = 0.
Y16_INT	Set for 16 multiframes (24 ms) if every frame 0 contains TS16 bit 6 = 1. Cleared for 16 multiframes if at least 1 frame 0 contains TS16 bit 6 = 0.
YB2	Set for 1 frame (125 µs) if all 24 time slots contain bit 2 = 0. Cleared for 1 frame if 1 or more time slots contain bit 2 = 1.
YB2_INT	Set for 192 frames (24 ms) if less than 15 time slots contain bit 2 = 0. Cleared for 192 frames if 15 or more time slots contain bit 2 = 1.

Table 3-13. Receive Yellow Alarm Set/Clear Criteria *(2 of 2)*

Mode	Set/Clear Criteria
YJ	Set for 1 multiframe (1.5 ms) if frame 12 contains Fs bit = 1. Cleared for 1 multiframe if frame 12 contains Fs bit = 0.
YJ_INT	Set for 16 multiframes (24 ms) if every frame 12 contains Fs bit = 1. Cleared for 16 multiframes (24 ms) if at least 1 frame 12 contains Fs bit = 0.
Y24	Set for 1 frame (125 µs) if TS24 contains bit 6 = 0. Cleared for 1 frame if TS24 contains bit 6 = 1.
Y24_INT	Set for 192 frames (24 ms) if every TS24 bit 6 = 0. Cleared for 192 frames if at least 1 TS24 bit 6 = 1.
YF	Set for 32 frames (4 ms) if 16 FDL bits contain yellow alarm priority codeword pattern (00FFh). Cleared for 32 frames if 16 FDL bits do not contain a yellow alarm priority codeword pattern.
YF_INT	Set upon reception of 16 FDL bits matching yellow alarm priority codeword and remains set as long as the codeword pattern is not interrupted for greater than 100 ms. Cleared when the yellow alarm priority codeword is not present for more than 100 ms (26 missing codewords = 104 ms).

RLOF_INTEG Enable RLOF Integration—When set, the receive loss of frame status [RLOF; addr 047] is integrated for 2.0 to 2.5 seconds during T1 framer modes (not applicable to E1 modes). RLOF interrupt status [ISR7; addr 004] is also integrated. However, receive framer status in ALM3 [addr 049], loss of frame count [FRED[3:0]; addr 05A], and RLOF counter overflow [ISR4; addr 007] are unaffected.

0 = normal RLOF status
1 = integrated RLOF [addr 047] status

RPCM_YEL Send Bit2 Yellow Alarm on RPCMO Output Pin—Similar to RPCM_AIS, except all RPCMO time slot Bit2 locations are replaced by all zeros. Bit2 yellow alarms are applicable only to T1 mode. E1 modes do not require yellow alarm forwarding.

0 = normal RPCMO data
1 = RPCMO includes Bit2 yellow alarm

RPCM_AIS Send AIS on RPCMO Output Pin—Replaces RPCMO data with a continuous series of all ones. RPCM_AIS is useful in CSU or digital section applications, where the local interface must be able to forward an AIS to the opposing interface. RPCM_AIS has a higher priority than RPCM_YEL.

0 = normal RPCMO data
1 = RPCMO replaced with all ones

046—Alarm/Error/Counter Latch Configuration (LATCH)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	—	STOP_CNT	LATCH_CNT	LATCH_ERR	LATCH_ALM

STOP_CNT Stop Error Count during RLOF/RLOS/RAIS—If enabled, error count registers [addr 050–057] are suspended at their present values during any receive loss of frame (RLOF), loss of signal (RLOS), or all ones (RAIS) alarm condition. STOP_CNT does not affect counting of test pattern errors [BERR; addr 058, 059] or alarm events [AERR; addr 05A]. The occurrence of a red or AIS CGA will inhibit further processing of all other performance parameters (i.e., BER, errored seconds, SLIPS, etc.). However, a CGA caused by a yellow alarm will not inhibit further alarm or performance monitoring

0 = continue error count during alarms
1 = stop error count during alarms

LATCH_CNT Enable ONESEC Latching of Counters—Determines interval for which error counts remain held in all count registers [addr 050–057]. LATCH_CNT must be active in T1 mode whenever automatic one-second performance report messaging [AUTO_PRM; addr 0AA] is enabled. Note that LATCH_CNT active during E1 mode prevents the processor from using RLOF counter overflow [addr 007] as a 128 ms MFAS timeout.

When LATCH_CNT is inactive, the processor read of the LSB register reports current LSB error count, it latches current MSB error count to MSB register, and clears LSB. Subsequently, reading MSB register reports current latched MSB error count and then clears MSB.

LATCH_CNT	Count Latched	Count Hold Time
0	Never	Until read clear
1	ONESEC interval	ONESEC interval

LATCH_ERR Enable ONESEC Latching of Errors—Determines the interval for which latched active errors are held in error interrupt [ISR5; addr 006] and pattern interrupt [ISR0; addr 00B] status.

IER	LATCH_ERR	ISR Latched	ISR Hold Time
0	0	Rising edge event	Until read clear
0	1	Rising edge event	ONESEC interval
1	X	Rising edge event	Until read clear

LATCH_ALM Enable ONESEC Latching of Alarms—Determines interval for which latched active alarms remain held in alarm interrupt status [ISR7, ISR6; addr 004, 005].

IER	LATCH_ALM	ISR Latched	ISR Hold Time
0	0	Rising edge or transition	Until read clear
0	1	Rising edge or transition	ONESEC interval
1	X	Rising edge or transition	Until read clear

NOTE(S): Interrupt type determines rising edge or transition event.

047—Alarm 1 Status (ALM1)

ALM1 reports current status of receive alarms. Any change in the current status activates the corresponding interrupt status bit [ISR7; addr 004].

7	6	5	4	3	2	1	0
RMYEL	RYEL	—	RAIS	RALOS	RLOS	RLOF	SIGFRZ

RMYEL Receive Multiframe Yellow Alarm—Real-time or integrated RMYEL status depends on the selected framer mode and the yellow alarm integration mode [YEL_INTEG; addr 045]. Refer to Table 2-1, *Receive Framer Modes*, for mode summary and Table 3-13 for set/clear criteria.

0 = no alarm

1 = receive multiframe yellow alarm

Table 3-14. Receive Yellow Alarm

Receive Framer Mode	YEL_INTEG = 0		YEL_INTEG = 1	
	RYEL	RMYEL	RYEL	RMYEL
FT/SF/SLC	YB2	—	YB2_INT	—
JYEL	YJ	—	YJ_INT	—
T1DM	Y24	—	Y24_INT	—
ESF	YB2	YF	YB2_INT	YF_INT
FAS	Y0	—	Y0_INT	—
CAS	Y0	Y16	Y0_INT	Y16_INT

NOTE(S): Last known frame alignment is used to locate and monitor yellow alarms. Therefore, RYEL and RMYEL will not accurately report alarms during receive loss of frame alignment [RLOF; addr 047].

RYEL Receive Yellow Alarm—Real-time or integrated RYEL status depends on selected receive framer mode and yellow alarm integration mode [YEL_INTEG; addr 045]. Refer to Table 3-14 for mode summary and Table 3-13 for set/clear criteria.

0 = no alarm

1 = receive Yellow Alarm

RAIS Receive Alarm Indication Signal—Criteria for detection and clearance of RAIS per ITU G.775 and ANSI T1.231.

Mode	RAIS	Set/Clear Criteria
E1	0	Cleared if 2 consecutive double frames (500 µs) each contain 3 or more zeros out of 512 bits or FAS alignment is recovered [FRED = 0; addr 049].
E1	1	Set if 2 consecutive double frames each contain 2 or fewer zeros out of 512 bits and FAS alignment is lost [FRED = 1; addr 049].
T1	0	Cleared if data received for a period of 3 ms contains 5 or more zeros out of 4632 bits or frame alignment is recovered [FRED = 0; addr 049].
T1	1	Set if data received for a period of 3 ms contains 4 or fewer zeros out of 4632 bits and frame alignment is lost [FRED = 1; addr 049].

RALOS Receive Loss of Signal or Receive Clock—Reports loss of receive clock (RCKI) or loss of receive signal [RLOS; addr 047] for 1 msec depending on the RALOS configuration bit [RAL_CON; addr 020].

When set for loss of clock, RALOS becomes active (1) if the receive clock on the RCKI pin is not present, and inactive (0) if the clock is present.

When set for loss of signal, RALOS indicates that all zeros have been received for at least 1 msec (RLOS is active for 1 msec). This status is provided for compatibility with ITU-I.431 loss of signal detection requirements; and works in conjunction with LIUs which detect loss of signal if the received signal level falls below a certain threshold and which have a signal 'squelch' feature. Operation is as follows:

- The LIU detects receive loss of signal if the receive level falls below:
  - 30 dB below nominal for T1.
  - 20 dB below nominal for E1
- The LIU squelches (turns off) the signal to the framer so all zeros are received.
- RLOS is reported after 100 continuous zeros are detected.
- RALOS is reported after RLOS is active for 1 msec.

RLOS Receive Loss of Signal—Criteria for detection and clearance of RLOS per ITU G.775 and ANSI T1.231.

Mode	RLOS	Set/Clear Criteria
T1	0	Cleared if received data sustains an average pulse density of 12.5% over a period of 114 bits starting with the receipt of a pulse, and no occurrence of 100 consecutive zeros.
T1	1	Set if 100 consecutive zeros received.
E1	0	Cleared upon reception of 193 bits in which no interval of 32 consecutive zeros appear, where the 193-bit window begins with receipt of a pulse.
E1	1	Set upon reception of 32 consecutive zeros.

RLOF Receive Loss of Frame Alignment—Real-time or integrated RLOF status depends on selected receive framer mode, out of frame criteria [RLOFA–RLOFD; addr 040], and integration mode [RLOF_INTEG; addr 045]. Refer to Tables A-1 through A-6 in Appendix A to find which frame bits are monitored. Refer to Table 2-2, *Criteria for Loss/Recovery of Receive Framer Alignment*, for the loss/recovery criteria. During E1 mode, RLOF indicates logically OR'ed status of FAS/MFAS/CAS alignment machines from which individual alignment status is reported separately in FRED/MRED/SRED [addr 049].

0 = no alarm
1 = receive loss of frame alignment

SIGFRZ Signaling Freeze—Real-time SIGFRZ status indicates when input ABCD signaling bit updates are no longer being written to the receive signaling buffer [RSIGn; addr IA0–IBF]. Consequently, ABCD signaling on RPCMO (if signaling insertion enabled) and RSIGO output pins are fixed to their existing buffered values. SIGFRZ remains active for 6 to 12 ms longer after COFA or RLOF clears. SIGFRZ status is also affected by manual SIGFRZ on/off controls [RSIG_CR; addr 0D7].

0 = no alarm (or FRZ_OFF)
1 = signaling freeze (or FRZ_ON)

048—Alarm 2 Status (ALM2)

Reports real-time status of transmit alarms and inband loopback codeword detectors. Any change in the current status activates the corresponding interrupt status bit [ISR6; addr 005].

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
LOOPDN	LOOPUP	—	—	TLOC	—	TLOF	—

LOOPDN Inband Loopback Deactivate—Reports detection or loss of an inband loopback code which matches the programmed LOOPDN code [LBD; addr 044].

0 = no inband code (or lost)
1 = LOOPDN code detected

LOOPUP Inband Loopback Activate—Reports detection or loss of an inband loopback code which matches the programmed LOOPUP code [LBA; addr 043].

0 = no inband code (or lost)
1 = LOOPUP code detected

TLOC Transmit Loss of Clock—Clock monitor circuit reports TCKI lost if no signal transitions are detected on TCKI pin for eight clock cycles of T1ACKI(T1) or EIACKI(E1). TCKI is reported as present if four or more signal transitions are detected on TCKI pin during eight clock cycles of T1/E1ACKI. When used in conjunction with AISCLK [addr 068], TLOC also identifies which transmit line rate clock (TCKI or T1/E1ACKI) is presently in use and whether AIS data transmission is enforced. Note that TLOC status is indeterminate if the T1/E1ACKI input signal is not present.

0 = TCKI present
1 = TCKI lost

TLOF Transmit Loss of Frame Alignment—Reports transmit framer status per selected mode [TFRAME; addr 070] and loss criteria [TLOFA–TLOFC; addr 071].

0 = recovered
1 = lost

049—Alarm 3 Status (ALM3)

Reports real-time status of the receive framer (not affected by ONESEC latch mode), and miscellaneous latched error status (SEF and RMAIS). Any change of the logical OR of (FRED or MRED or SRED) status activates RLOF interrupt [ISR7; addr 004]. Refer to Table 2-2, *Criteria for Loss/Recovery of Receive Framer Alignment*, [RFRAME; addr 001] to find the criteria for loss/recovery of frame alignment.

7	6	5	4	3	2	1	0
—	RMAIS	SEF	SRED	MRED	FRED	LOF[1]	LOF[0]

RMAIS Receive TS16 Alarm Indication Signal (CAS mode only)—RMAIS is latched active high and cleared by a processor read. Criteria for detection and clearance of RMAIS is per ITU G.775.

Mode	RMAIS Criteria
CAS	Set if TS16 contains three or fewer zeros out of 128 bits in each mutiframe over two consecutive multiframes (4 ms).
Other	Not applicable (read zero).

SEF Severely Errored Frame—SEF is latched active high and cleared by a processor read. Criteria for detection and clearance of SEF is per ANSI T1.231.

Mode	SEF Criteria
E1	Set if two or more (FAS or NFAS) errors detected out of six frames. (FAS + NFAS, or 2 FAS, or 2 NFAS errors, etc.).
FT/SF/SLC	Set if two or more Ft errors are detected out of 3 Ft bits.
ESF	Set if two or more FPS errors detected out of six FPS bits.

SRED Loss of CAS Alignment—Real-time status of CAS alignment machine. SRED is applicable if CAS is enabled, otherwise SRED is zero.
0 = recovery of CAS alignment
1 = loss of CAS alignment

MRED Loss of MFAS Alignment—Real-time status of MFAS alignment machine. MRED is applicable if MFAS is enabled, otherwise MRED is zero.
0 = recovery of MFAS alignment
1 = loss of MFAS alignment

FRED Loss of T1/FAS Alignment—Real-time status of basic frame alignment machine. FRED alarm counter [AERR; addr 05A] increments for each low-to-high FRED transition.
0 = recovery of frame alignment
1 = loss of frame alignment

LOF[1:0] Reason for Loss of Frame Alignment—LOF status is latched whenever FRED reports a loss of frame alignment and remains held at the latched value until the next loss of frame alignment.

LOF[1:0]	LOF Criteria
00	Three consecutive FAS pattern errors
01	Three consecutive NFAS pattern errors
10	915 or more CRC4 errors out of 1000 blocks checked
11	Eight ms timeout while searching for MFAS

3.10 Performance Monitoring Registers

If the counter overflow interrupt [IER4; addr 00F] is enabled for the respective Performance Monitoring counter, the counter is allowed to roll over after reaching its maximum count value. If the overflow interrupt is disabled, the counter will hold its maximum value upon saturation. Refer also to LATCH [addr 046] for a description of one-second latched counter operation. Processor must read LSB before reading MSB of each multi-byte counter.

050—Framing Bit Error Counter LSB (FERR)

7	6	5	4	3	2	1	0
FERR[7]	FERR[6]	FERR[5]	FERR[4]	FERR[3]	FERR[2]	FERR[1]	FERR[0]

FERR[7:0] Ft/Fs/T1DM/FPS/FAS Error Count

051—Framing Bit Error Counter MSB (FERR)

If LATCH_CNT [addr 046] is inactive, reading FERR [addr 051] clears the entire FERR[11:0] count value.

15	14	13	12	11	10	9	8
0	0	0	0	FERR[11]	FERR[10]	FERR[9]	FERR[8]

FERR[11:8] Ft/Fs/T1DM/FPS/FAS Error Count

052—CRC Error Counter LSB (CERR)

7	6	5	4	3	2	1	0
CERR[7]	CERR[6]	CERR[5]	CERR[4]	CERR[3]	CERR[2]	CERR[1]	CERR[0]

CERR[7:0] CRC6/CRC4 Error Count

053—CRC Error Counter MSB (CERR)

If LATCH_CNT [addr 046] is inactive, reading CERR [addr 053] clears the entire CERR[9:0] count value.

15	14	13	12	11	10	9	8
0	0	0	0	0	0	CERR[9]	CERR[8]

CERR[9:8] CRC6/CRC4 Error Count

054—Line Code Violation Counter LSB (LCV)

7	6	5	4	3	2	1	0
LCV[7]	LCV[6]	LCV[5]	LCV[4]	LCV[3]	LCV[2]	LCV[1]	LCV[0]

LCV[7:0] BPV and EXZ (if EXZ_LCV enabled) Error Count

055—Line Code Violation Counter MSB (LCV)

If LATCH_CNT [addr 046] is inactive, reading LCV [addr 055] clears the entire LCV[15:0] count value.

15	14	13	12	11	10	9	8
LCV[15]	LCV[14]	LCV[13]	LCV[12]	LCV[11]	LCV[10]	LCV[9]	LCV[8]

LCV[15:8] BPV and EXZ (if EXZ_LCV enabled) Error Count

056—Far End Block Error Counter LSB (FEBE)

7	6	5	4	3	2	1	0
FEBE[7]	FEBE[6]	FEBE[5]	FEBE[4]	FEBE[3]	FEBE[2]	FEBE[1]	FEBE[0]

FEBE[7:0] FEBE Count (applicable only in E1 mode)

057—Far End Block Error Counter MSB (FEBE)

If LATCH_CNT [addr 046] is inactive, reading FEBE [addr 056, 057] clears the entire FEBE[9:0] count value.

15	14	13	12	11	10	9	8
0	0	0	0	0	0	FEBE[9]	FEBE[8]

FEBE[9:8] FEBE Count (applicable only in E1 mode)

058—PRBS Bit Error Counter LSB (BERR)

Reading BERR transfers the most recent 12-bit count from the internal PRBS error counter to BERR[11:0], then clears the internal error counter without affecting the reported BERR[11:0] value. Subsequent reads of BERR MSB [addr 059] report the BERR [11:8] count value latched when BERR LSB was last read.

7	6	5	4	3	2	1	0
BERR[7]	BERR[6]	BERR[5]	BERR[4]	BERR[3]	BERR[2]	BERR[1]	BERR[0]

BERR[7:0] BERR Count (applicable only for test pattern)

059—PRBS Bit Error Counter MSB (BERR)

15	14	13	12	11	10	9	8
0	0	0	0	BERR[11]	BERR[10]	BERR[9]	BERR[8]

BERR[11:8] BERR Count (suspended if BSTART = 0)

05A—SEF/FRED/COFA Alarm Counter (AERR)

Reading AERR clears the SEF[1:0], COFA[1:0] and FRED[3:0] count values.

7	6	5	4	3	2	1	0
FRED[3]	FRED[2]	FRED[1]	FRED[0]	COFA[1]	COFA[0]	SEF[1]	SEF[0]

FRED[3:0] Receive loss of basic frame alignment count—Increments for each occurrence of FRED [ALM3; addr 049]. The four bit count is large enough to count more than 100 ms worth of MFAS timeout intervals (8 ms each) during E1 modes. Processor may therefore use FRED counter overflow interrupt to indicate that a receive MFAS alignment search has timed out.

COFA[1:0] Change of Frame Alignment Count—Increments each time the offline framer generates a reframe pulse that aligns the receiver timebase to a new bit position.

SEF[1:0] Severely Errored Frame Count—Increments for each occurrence of SEF [ALM3; addr 049].

3.11 Receive Sa-Byte Buffers

Five receive Sa-Byte buffers [RSA4–RSA8] are double-buffered. All five registers are updated with the Sa-bits received in TS0 of odd frames at each receive multiframe interrupt [RMF; addr 008]. Bit 0 of all RSA registers contains data from frame 1, Bit 1 contains data from frame 3, Bit 2 contains data from frame 5, etc. This gives the processor a full 2 ms after RMF interrupt to read any Sa-Byte buffer before the buffer content changes. Processor should ignore RSA buffer contents at all times during T1 mode and also when receiver reports loss of FAS alignment [FRED=1; addr 049] in E1 mode.

05B—Receive Sa4 Byte Buffer (RSA4)

7	6	5	4	3	2	1	0
RSA4[7]	RSA4[6]	RSA4[5]	RSA4[4]	RSA4[3]	RSA4[2]	RSA4[1]	RSA4[0]

RSA4[7] Sa4 bit received in frame 15

RSA4[6] Sa4 bit received in frame 13

RSA4[5] Sa4 bit received in frame 11

RSA4[4] Sa4 bit received in frame 9

RSA4[3] Sa4 bit received in frame 7

RSA4[2] Sa4 bit received in frame 5

RSA4[1] Sa4 bit received in frame 3

RSA4[0] Sa4 bit received in frame 1

05C—Receive Sa5 Byte Buffer (RSA5)

7	6	5	4	3	2	1	0
RSA5[7]	RSA5[6]	RSA5[5]	RSA5[4]	RSA5[3]	RSA5[2]	RSA5[1]	RSA5[0]

RSA5[7] Sa5 bit received in frame 15

RSA5[6] Sa5 bit received in frame 13

RSA5[5] Sa5 bit received in frame 11

RSA5[4] Sa5 bit received in frame 9

RSA5[3] Sa5 bit received in frame 7

RSA5[2] Sa5 bit received in frame 5

RSA5[1] Sa5 bit received in frame 3

RSA5[0] Sa5 bit received in frame 1

05D—Receive Sa6 Byte Buffer (RSA6)

7	6	5	4	3	2	1	0
RSA6[7]	RSA6[6]	RSA6[5]	RSA6[4]	RSA6[3]	RSA6[2]	RSA6[1]	RSA6[0]

RSA6[7] Sa6 bit received in frame 15

RSA6[6] Sa6 bit received in frame 13

RSA6[5] Sa6 bit received in frame 11

RSA6[4] Sa6 bit received in frame 9

RSA6[3] Sa6 bit received in frame 7

RSA6[2] Sa6 bit received in frame 5

RSA6[1] Sa6 bit received in frame 3

RSA6[0] Sa6 bit received in frame 1

05E—Receive Sa7 Byte Buffer (RSA7)

7	6	5	4	3	2	1	0
RSA7[7]	RSA7[6]	RSA7[5]	RSA7[4]	RSA7[3]	RSA7[2]	RSA7[1]	RSA7[0]

RSA7[7] Sa7 bit received in frame 15

RSA7[6] Sa7 bit received in frame 13

RSA7[5] Sa7 bit received in frame 11

RSA7[4] Sa7 bit received in frame 9

RSA7[3] Sa7 bit received in frame 7

RSA7[2] Sa7 bit received in frame 5

RSA7[1] Sa7 bit received in frame 3

RSA7[0] Sa7 bit received in frame

05F—Receive Sa8 Byte Buffer (RSA8)

7	6	5	4	3	2	1	0
RSA8[7]	RSA8[6]	RSA8[5]	RSA8[4]	RSA8[3]	RSA8[2]	RSA8[1]	RSA8[0]

RSA8[7] Sa8 bit received in frame 15

RSA8[6] Sa8 bit received in frame 13

RSA8[5] Sa8 bit received in frame 11

RSA8[4] Sa8 bit received in frame 9

RSA8[3] Sa8 bit received in frame 7

RSA8[2] Sa8 bit received in frame 5

RSA8[1] Sa8 bit received in frame 3

RSA8[0] Sa8 bit received in frame 1

3.12 Transmitter Registers

070—Transmit Framer Configuration (TCR0)

TCR0 selects the offline framer's criteria for recovery of transmit frame alignment and determines the output of transmit frame and alarm formatters overhead bits. In addition, TCR0 works in conjunction with TCR1 [addr 071] and TFRM [addr 072] to select the transmit online frame monitor's criteria for loss of frame alignment and to select which overhead bits are supplied by the transmit frame and alarm formatters.

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	TINCF	TFRAME[3]	TFRAME[2]	TFRAME[1]	TFRAME[0]

TINCF Transmit CRC6 includes F-bit—Determines if the F-bit is included in the CR6 remainder calculation in T1 mode (T1/E1N = 1). This bit is ignored in E1 mode (T1/E1N = 0).

0 = T1 ESF CRC6 calculation is performed on the transmit data including a 1 in place of the F-bit.

1 = T1 ESF CRC6 calculation is performed on transmit data including the F-bit.

TFRAME[3:0] Frame formatter generates Ft, Fs, FPS, FAS, MFAS, and CRC bits. Alarm formatter generates YB2, YJ, Y0, and Y16 bits. Frame and alarm overhead formats are selected by TFRAME[3:0] and T1/E1N settings as given in Tables 3-15 through 3-18. Each yellow alarm is capable of being generated manually, automatically [TALM; addr 075], or bypassed [INS_MYEL; addr 072].

Frame formatter does not generate CAS or Sa-bit overhead. These bits are either supplied by TPCMI in bypass mode [TFRM; addr 072] or by programming TSIGn [addr 120–13F] or TSA4–TSA8 [addr 07B–07F] buffer contents. To insert CAS, the processor selects TLOCAL output signaling for time slot 0 and time slot 16 by programming transmit per-channel control registers TPC0 [addr 100] and TPC16 [addr 110]. The processor then fills ABCD local signaling value for TPC0 with MAS pattern (ABCD = 0000) and TPC16 with XYXX pattern (ABCD = 1011).

Frame formatter does not generate SLC, T1DM, or FDL overhead. These bits are either supplied by TPCMI in bypass mode [TFRM; addr 072] or by programming TSLIP [addr 140–17F], TDL1 [addr 0AD], or TDL2 [addr 0B8] buffer contents.

To insert SLC concentrator, maintenance, alarm, and switch field values, the processor selects any SLC framer format and programs either TDL1 or TDL2. This is done in order to operate in unformatted Pack6 mode over the F-bit channel during even frames, thus overwriting all Fs bits inserted by frame formatter. The data pattern to be sent in 36 Fs bit multiframe is then written as six 6-bit words to TDL1 or TDL2 circular buffer. For real-time overhead manipulation, the processor can rewrite the circular buffer with a new 36-bit pattern as desired.

To insert T1DM, the processor enables TIDLE insertion on time slot 24 by programming the system bus per-channel control [SBC24; addr 0F8], then filling TSLIP buffer locations for TS24 [addr 138, 158] with the T1DM framing pattern (TS24 = 10111YR0). If specific T1DM elements need to be inserted and others bypassed, the processor configures TDL1 or TDL2 to selectively insert only the desired bits. T1DM sync pattern, R-bits, and/or Y-bits. The processor accomplishes this by programming data link bit enables [DL1_BIT; addr 0A5 or DL2_BIT; addr 0B0].

To insert FDL, the processor configures TDL1 to operate over the F-bit channel during odd frames [DL1_TS; addr 0A4] and Automatic Performance Report Messages [AUTO_PRM; addr 0AA] or manually programs TDL1 to send each message.

Table 3-15. E1 Transmit Framer Modes (T1/E1N = 0)

TFRAME	Framer Mode	TS0 Overhead Insertion				Yellow Alarms	
		MFAS	FEBE	CRC4	FAS	YEL	MYEL
00XX	FAS Only	Ones	Ones	Ones	Yes	Y0	–
01XX	FAS + CRC	Yes	Yes	Yes	Yes	Y0	–
10XX	FAS + CAS	Ones	Ones	Ones	Yes	Y0	Y16
11XX	FAS + CRC + CAS	Yes	Yes	Yes	Yes	Y0	Y16

Table 3-16. T1 Transmit Framer Modes (T1/E1N = 1)

TFRAME	Framer Mode	F-bit Overhead Insertion				Yellow Alarms	
		Fs	FPS	CRC6	Ft	YEL	MYEL
0000	FT Only	Ones	–	–	Yes	YB2	–
0100	SF	Yes	–	–	Yes	YB2	–
0101	SF + JYEL	Yes	–	–	Yes	YJ	–
100X	SLC	Yes	–	–	Yes	YB2	–
0001	ESF + No CRC	–	Yes	Ones	–	YB2	YF
1100	ESF + Mimic CRC	–	Yes	Yes	–	YB2	YF
1101	ESF + Force CRC	–	Yes	Yes	–	YB2	YF

Table 3-17. Criteria for E1 Loss/Recovery of Transmit Frame Alignment

Mode	Description
FAS	Basic Frame Alignment (BFA) is recovered when the following search criteria are satisfied: • FAS pattern (0011011) is found in frame N. • Frame N+1 contains bit 2 equal to 1. • Frame N+2 also contains FAS pattern (0011011). During FAS only modes, BFA is recovered when the following search criteria are satisfied: • FAS pattern (0011011) is found in frame N. • No mimics of the FAS pattern present in frame N+1. • FAS pattern (0011011) is found in frame N+2. ***NOTE(S):*** If FAS pattern is not found in frame N+2 or FAS mimic is found in frame N+1, then the search restarts in frame N+2. Transmit Loss of Frame (TLOF) alignment is declared when: • Three consecutive FAS pattern errors are detected, where FAS pattern consists of a 7-bit (x0011011) pattern in FAS frames as well as bit 2 equalling one in NFAS frames.
MFAS	MFAS—CRC Multiframe Alignment is recovered when the following search criteria are satisfied: • BFA is recovered, identifying FAS and NFAS frames. • Within 6 ms after BFA, bit 1 of NFAS frames contains the first MFAS pattern (001011xx). • Within 8ms after BFA, bit 1 of NFAS frames contains the second MFAS pattern (001011xx), aligned to first MFAS. MFAS errors do not cause Transmit Loss of Frame (TLOF) alignment.
CAS	CAS Multiframe Alignment is recovered when the following search criteria are satisfied: • BFA is recovered, identifying TS0 through TS31. • MAS (0000xxxx) Multiframe Alignment Signal pattern is found in the first 4 bits of TS16, and 8 bits of TS16 in preceding frame contains nonzero value. CAS errors do not cause Transmit Loss of Frame (TLOF) alignment.

Table 3-18. Criteria for T1 Loss/Recovery of Transmit Frame Alignment

Mode	Description
FT Only	Terminal Frame Alignment is recovered when: • One and only one valid Ft pattern (1010) is found in 12 alternate F-bit locations (3 ms), where F-bits are separated by 193 bits. Transmit Loss of Frame (TLOF) alignment is declared when: • Number of Ft bit errors detected meets selected loss of frame criteria [TLOFA–TLOFC; addr 071].
SF	Superframe alignment is recovered when: • Terminal frame alignment is recovered, identifying Ft bits. • Depends on SF submode: If JYEL: If SF pattern (00111x) found in Fs bits If no JYEL: SF pattern (001110) found in Fs bits. Fs errors do not cause Transmit Loss of Frame (TLOF) alignment. Transmit loss of frame alignment (TLOF) declared when: • Number of Ft bit errors detected meets selected reframe criteria [TLOFA–TLOFC; addr 071]. Notice that Fs bit multiframe errors are reported in TMERR [ISR0; addr 00B], but do not cause a loss of transmit frame alignment.
SLC	Superframe alignment is recovered when: • Terminal frame alignment is recovered, identifying Ft bits. • SLC pattern (refer to Table A-3, *SLC-96 Fs Bit Contents*) found in 16 of 32 Fs bits according to Bellcore TR-TSY-000008. Fs errors do not cause Transmit Loss of Frame (TLOF) alignment. Transmit loss of frame alignment (TLOF) declared when: • Number of Ft bit errors detected meets selected reframe criteria [TLOFA–TLOFC; addr 071]. Notice that Fs bit multiframe errors are reported in TMERR [ISR0; addr 00B], but do not cause a loss of transmit frame alignment.
ESF	Extended superframe alignment is recovered when: • Valid FPC candidate located (001011). Candidate bits are each separated by 772 digits and received without pattern errors: If only one valid FPS candidate and: No CRC mode: align to FPS regardless of CRC6 comparison. Mimic CRC mode: align to FPS regardless of CRC6 comparison. Force CRC mode: align to FPS only if CRC6 is correct. If two or more valid FPS candidates and: No CRC mode: do not align (INVALID status) Mimic CRC mode: align to first FPS with correct CRC6. Force CRC mode: align to first FPS with correct CRC6. Transmit loss of frame alignment (TLOF) declared when: • Number of FPS pattern errors detected meets selected loss of frame criteria [TLOFA–TLOFC; addr 071].

071—Transmitter Configuration (TCR1)

7	6	5	4	3	2	1	0
TNRZ	TABORT	TFORCE	TLOFC	TLOFB	TLOFA	TZCS[1]	TZCS[0]

TNRZ Transmit NRZ Data—Transmit dual-rail unipolar outputs TPOSO/TNEGO are replaced by non-return to zero unipolar data (TNRZO) and transmit multiframe sync (MSYNCO). Both outputs are clocked on the rising edge of transmitter clock (TCKI). TNRZ must be written to 1 on the CX28395 device.

0 = TPOSO/TNEGO encoded per TZCS[1:0]
1 = TPOSO/TNEGO replaced by TNRZO/MSYNCO

NOTE: MSYNCO active (high) always marks the first bit of transmit multiframe according to the selected transmit framer mode.

TABORT Abort/Disable TX Offline Framer—Offline framer ignores reframe requests from the online framer (TLOF) and aborts any in progress TLOF reframe requests. Loss of frame status [TLOF; addr 048] is not affected. While TABORT remains active, offline framer responds only to the processor force reframe request (TFORCE), which allows the processor to manually control reframe criteria or lock out changes in the current transmit frame alignment.

0 = normal framer operation
1 = framer disabled

TABORT also interacts with EMBED [addr 0D0] to select which data stream is examined by online and offline transmit framer during embedded framing modes. If EMBED is active, TXDATA output from TSLIP is examined and used to align the TX timebase. Otherwise, TPCMI data stream is examined and used to align the TSB timebase as given in Table 3-19.

Table 3-19. Transmit Framer Position

TABORT	EMBED	TSB Alignment	Tx Alignment	Tx Framing Mode	Notes
0	0	TPCMI	Flywheel	Transmit Framing	(1–5)
0	1	TFSYNC/TMSYNC	TXDATA	Embedded Framing	(6–8)
1	X	TFSYNC/TMSYNC	Flywheel	Normal	(5, 6)

NOTE(S):
1. TFSYNC and TMSYNC must be programmed as outputs.
2. Offline framer examines TPCMI to supply TSB frame alignment.
3. Online framer examines TPCMI to supply TSB multiframe alignment.
4. SBI mode must match 2048k or 1544k line rate.
5. TX timebase flywheels at initial alignment until TSB_CTR or TX_ALIGN [addr 0D4].
6. TSB timebase flywheels if TFSYNC/TMSYNC programmed as outputs.
7. Offline framer examines TXDATA to supply TX frame alignment.
8. Online framer examines TXDATA to supply TX multiframe alignment.

TFORCE Force TX Reframe (auto clear)—Forces the offline framer to perform a single reframe according to the selected transmit framer mode. TFORCE is automatically cleared when the framer acknowledges a request [ACTIVE; addr 017]. The processor does not typically need to force reframe since online framer reframe request (TLOF) is active when reframe criteria TLOFC–A is met. However, the processor may wish to force reframe if frame or CRC bit error ratio indicates the framer has aligned to a mimic pattern.

0 = no effect
1 = force TX reframe

TLOFC–TLOFA Transmit Loss Of Frame Criteria—Determines the number of frame errors that the online framer must detect before declaring loss of frame alignment [TLOF; addr 048]. Refer to TFRAME [addr 070] to find which frame bits are monitored during the selected framer mode.

T1/E1N	TLOFC–A	Reframe Criteria
0	100	Three consecutive FAS errors
1	001	Two out of four frame bit errors
1	010	Two out of five frame bit errors
1	100	Two out of six frame bit errors

NOTE(S): All other TLOFC–A combinations are invalid.

TZCS[1:0] Transmit Zero Code Suppression—Selects ZCS and Pulse Density Violation (PDV) enforcement options for TPOSO/TNEGO outputs. B8ZS and HDB3 replace transmitted sequences of 8 zeros or 4 zeros with a recoverable code and are standard T1 and E1 line code options, respectively (see Table 3-20).

Table 3-20. Transmit Zero Code Suppression

TZCS	T1/E1N	T1DM	ZCS	PDV	Zero Code Substitution (Sent left to right)
00	X	X	AMI	None	None
01	0	X	HDB3	None	000V or B00V
01	1	X	B8ZS	None	000VB0VB
10	1	1	UMC	None	10011000
11	1	X	AMI	Enforced	on PDV errors
AMI	Alternate Mark Inversion. Bipolar line code forces successive ones to alternate their output pulse polarity. Analog and digital dual-rail outputs are always AMI encoded, although certain AMI codes are modified to include zero suppression.				
HDB3	Prior to transmission, 4 consecutive zeros are substituted by 000V or B00V code, where B is an AMI pulse and V is a bipolar violation. ZCS encoder selects the code which will force the BPV output polarity opposite that of the prior BPV.				
B8ZS	Prior to transmission, 8 consecutive zeros are substituted by 000VB0VB code, where B is an AMI encoded pulse and V is a bipolar violation.				
PDV	Enforcer overwrites transmit zeros that would otherwise cause output data to fail to meet the minimum required pulse density per ANSI T1.403 sliding window. Note that the enforcer will never overwrite a framing bit and is not applicable during E1 mode. Note that each PDV enforced one causes a nonrecoverable transmitted bit error.				
UMC	Unassigned Mux Code. DS0 channels that contain 8 zeros are substituted with the 10011000 code, per Bellcore TA-TSY-000278. Note that the receiver's ZCS decoder cannot recover original data content from UMC encoded signal.				
NOTE(S): PRBS, inband loopback, and YB2 alarm insertion occur after PDV enforcement. Therefore, output data might violate minimum pulse density requirements while these functions are active.					

072—Transmit Frame Format (TFRM)

TFRM controls the insertion of overhead bits generated by transmit frame and alarm formatters. Bypassed overhead bits flow transparently from TPCMI system bus input through TSLIP buffer.

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	INS_MYEL	INS_YEL	INS_MF	INS_FE	INS_CRC	INS_FBIT

INS_MYEL Insert Multiframe Yellow Alarm—Applicable to E1 modes only. Enables the alarm formatter to output Y16 Multiframe Yellow Alarm. Once enabled, TMYEL and AUTO_MYEL [addr 075] control the alarm output state. This bit must be set to 0 in T1 modes.

0 = bypass

1 = insert multiframe yellow alarm

INS_YEL Insert Yellow Alarm—The alarm formatter outputs yellow alarms YB2 or YJ during T1 modes; or Y0 during E1 modes. In ESF framed T1 mode, the YF Yellow Alarm is transmitted by programming the DL1 data link controller and by transmitting the appropriate bit oriented code message (BOP message). Once enabled, TYEL and AUTO_YEL [addr 075] control the yellow alarm output state. If the system wants to bypass JYEL (Fs bit in frame 12), then it must bypass all Fs bits with INS_MF [addr 072].

0 = bypass

1 = insert yellow alarm.

INS_MF Insert Multiframe Alignment—The frame formatter outputs 6-bit SF alignment pattern in T1 mode, or 6-bit MFAS alignment pattern in E1 mode. INS_MF should be set while TFRAME (addr 070) selects Fs (T1) or MFAS (E1) alignment.

0 = bypass

1 = insert multiframe alignment

INS_FE Insert FEBE— During E1 mode, the alarm formatter automatically outputs TS0 bit 1 of frame 13 (FEBE13) and frame 15 (FEBE15) in response to received CRC4 errors. FEBE13 is active low for each received CRC4 error detected in SMF I. FEBE15 is active low for each received CRC4 error detected in SMF II. INS_FE should be set while TFRAME (addr 070) selects FEBE (E1) alignment.

0 = bypass

1 = insert FEBE

INS_CRC Insert Cyclic Redundancy Check—The frame formatter outputs the calculated CRC6 bits in T1 mode or CRC4 bits in E1 mode.

0 = bypass

1 = insert cyclic redundancy check

INS_FBIT Insert Terminal Framing—The frame formatter outputs a 2-bit Ft alignment pattern in F-bits of odd frames (SF framing) or FPS framing pattern (ESF framing) during T1 modes—or 8-bit FAS/NFAS alignment pattern during E1 modes. INS_FBIT should be set while TFRAME (addr: 070) selects Ft (T1, SF), FPS (T1, ESF), or FAS (E1) alignment.

0 = bypass

1 = insert terminal framing

If F-bits are bypassed while TSLIP is enabled, the system must either use embedded T1 framing or apply at least a double frame (250 µs) multiframe sync pulse (TMSYNC) to provide odd/even frame alignment.

073—Transmit Error Insert (TERROR)

Transmit error insertion capabilities are provided for system diagnostic, production test, and test equipment applications. Writing a one to any TERROR bit injects a single occurrence of the respective error on TPOSO/TNEGO or TNRZO outputs. Writing a zero has no effect. Multiple transmit errors can be generated simultaneously. Injected errors also affect data sent during a Framer Loopback [FLOOP; addr 014].

7	6	5	4	3	2	1	0
TSERR	TMERR	TBERR	BSLIP	TCOFA	TCERR	TFERR	TVERR

TSERR Inject CAS Multiframe (MAS) Error—Injects a single MAS pattern error. TSERR performs a logical inversion of the first MAS bit transmitted.
0 = no effect
1 = inject MAS error

TMERR Inject Multiframe Error—Injects a single Fs bit (T1) or MFAS (E1) bit error. TMERR performs a logical inversion of the next multiframe bit transmitted. Processor can pace writing to TMERR to control which MFAS bit is errored.
0 = no effect
1 = inject multiframe error

TBERR Inject PRBS Test Pattern Error—Injects a single PRBS error by logically inverting the next PRBS generator output bit. Processor can pace writing to TBERR to create the desired bit error ratio (up to 5E-3 if TBERR asserted 1/192 bits at every frame interrupt).
0 = no effect
1 = inject PRBS error

BSLIP/TCOFA Inject Transmit COFA—Forces a 1-bit shift in the location of transmit frame alignment by deleting (or inserting) one bit position from the transmit frame. During E1 modes, BSLIP determines in which direction the bit slip will occur. In T1 modes, only one bit deletion is provided. TCOFA alters the extraction rate of data from the transmit slip buffer; thus, repeated TCOFAs eventually cause a controlled frame slip where one frame of data is repeated (T1/BSLIP = 0) or one frame of data is deleted (BSLIP = 1).

TCOFA	T1/E1N	BSLIP	Transmit COFA
0	X	X	No effect
1	0	0	Inhibit output of TS0 bit 1 for one frame
1	0	1	Insert 1 prior to FAS pattern for one frame
1	1	X	Inhibit output of F-bit for one frame

TCERR Inject CRC Error—Injects a single CRC6 (T1) or CRC4 (E1) bit error. TCERR performs a logical inversion of the next CRC bit transmitted. The processor can pace writing to TCERR to control which CRC bit is errored.
0 = no effect
1 = inject CRC error

TFERR Inject Frame Bit Error—Injects a single Ft, FPS, or FAS bit error depending on the selected transmit framer mode. TFERR performs a logical inversion of the next frame bit transmitted. The processor can pace writing to TFERR, to control which frame bit is errored.
0 = no effect
1 = inject frame error

TVERR Inject Line Code Violation—Injects a single LCV error, depending on line mode and ZCS selected. In T1 mode, the LCV injector waits for transmission of two consecutive pulses on the data output before performing BPV error insertion and clearing the TVERR bit. Therefore, a BPV error cannot be injected into a transmit data stream that does not contain two consecutive ones. TVERR is latched until an opportunity to inject a BPV error is presented. This prevents the receiving end from detecting: frame or multiframe bit errors, CRC errors, multiple BPV errors (due to ZCS pattern corruption), or PRBS test pattern bit errors as a consequence of error insertion. In E1 mode with HDB3 selected, the LCV injector sends two consecutive BPVs of the same polarity, which causes the receiving end to detect a single LCV error.

0 = no effect

1 = inject line code violation

074—Transmit Manual Sa-Byte/FEBE Configuration (TMAN)

7	6	5	4	3	2	1	0
INS_SA[8]	INS_SA[7]	INS_SA[6]	INS_SA[5]	INS_SA[4]	FEBE_II	FEBE_I	TFEBE

INS_SA[8] Manual Sa8-Byte Transmit (0-bypass)

INS_SA[7] Manual Sa7-Byte Transmit (0-bypass)

INS_SA[6] Manual Sa6-Byte Transmit (0-bypass)

INS_SA[5] Manual Sa5-Byte Transmit (0-bypass)

INS_SA[4] Manual Sa4-Byte Transmit (0-bypass)

FEBE_II Transmit FEBE Frame 15.

FEBE_I Transmit FEBE Frame 13.

TFEBE Manual Transmit FEBE (Overrides INS_FE; addr 072)—Provides a manual override for FEBE bits that are normally sent by the alarm formatter [INS_FE; addr 072]. When active, FEBE_I controls the data output in TS0 bit 1 of frame 13 (FEBE13) and, FEBE_II controls the data output in TS0 bit 1 of frame 15 (FEBE15).

INS_FE	TFEBE	FEBE[13]	FEBE[15]	Description
0	X	TPCMI	TPCMI	Bypass FEBE
1	0	SMF I	SMF II	Automatic FEBE
1	1	FEBE_I	FEBE_II	Manual FEBE

NOTE(S): Automatic FEBE insertion uses two separate CRC4 error signals from the receiver to indicate SMF I and SMF II errors. Each error signal is latched and held for one full multiframe to compensate for phase differences between receive and transmit multiframe timing.

075—Transmit Alarm Signal Configuration (TALM)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	AISCLK	AUTO_MYEL	AUTO_YEL	AUTO_AIS	TMYEL	TYEL	TAIS

AISCLK Enable Automatic ACKI Switching—When AISCLK is active and the clock monitor reports a loss of transmit clock [TLOC; addr 048], the transmitter clock is automatically switched to reference TIACKI or EIACKI instead of TCKI. The transmitter is also forced to send AIS (all ones) data. If both AISCLK and TAIS [addr 075] are active, AIS is transmitted using TIACKI or EIACKI clock regardless of the clock monitor status. AISCLK should be set only if the system supplies an alternate line rate clock on TIACKI for TI or EIACKI for EI applications.

Inputs			Status		Transmit	
TAIS	AUTO_AIS	AISCLK	RLOS	TLOC	CLOCK	DATA
0	0	X	X	0	TCKI	Normal
0	0	1	X	0	TCKI	Normal
0	X	1	X	1	TI/EIACKI	AIS
0	1	X	0	0	TCKI	Normal
0	1	0	0	1	TCKI	Normal
0	1	0	1	X	TCKI	AIS
1	X	1	X	X	TI/EIACKI	AIS
1	X	0	X	X	TCKI	AIS
0	0	0	X	1	TCKI	Normal
0	1	1	1	0	TI/E1ACKI	AIS

AUTO_MYEL/TMYEL Manual/Automatic Transmit Multiframe Yellow Alarm—Manual mode sends alarm for as long as TMYEL is active. Automatic mode sends alarm for the duration of a receive loss of multiframe alignment [SRED; addr 049].

INS_MYEL	TMYEL	AUTO_MYEL	Transmit Multiframe Yellow
0	X	X	Supplied by TPCMI
1	0	0	Inactive
1	0	1	Follows SRED status
1	1	X	Active

NOTE(S): To transmit T1DM yellow alarm (Y24), the processor must program TDL1, TDL2, or TSLIP buffer to transmit Y-bit output in time slot 24.

AUTO_YEL /TYEL Manual/Automatic Transmit Yellow Alarm—Manual mode sends the alarm for as long as TYEL is active and yellow alarm insertion [INS_YEL; addr 072] is enabled. Automatic mode sends yellow alarm for the duration of a receive loss of frame alignment [FRED; addr 049].

INS_YEL	TYEL	AUTO_YEL	Transmit Yellow Alarm
0	X	X	Supplied by TPCMI
1	0	0	Inactive
1	0	1	Follows FRED status
1	1	X	Active

NOTE(S): To transmit T1DM yellow alarm (Y24), processor must program TDL1, TDL2 or TSLIP buffer to transmit Y-bit output in time slot 24.

AUTO_AIS /TAIS Manual/Automatic Transmit Alarm Indication Signal—When activated manually (TAIS) or automatically (AUTO_AIS), the alarm formatter replaces all data output on TPOSO/TNEGO/TNRZO with an unframed all ones signal (AIS). This includes replacing data from the receiver during line loopback [LLOOP; addr 014]. Automatic mode sends AIS for the duration of receive loss of signal [RLOS; addr 047]. If AISCLK [addr 075] is enabled, then TAIS also provides manual switch control over ACKI clock input. AUTO_AIS does not affect ACKI switching.

AIS transmission [TAIS, AUTO_AIS; addr 075, or AISCLK; addr 075] does not affect transmit data that is looped back to the receiver during framer loopback [FLOOP; addr 014]. This allows both FLOOP and LLOOP to be active simultaneously, during a loss of signal, without disrupting data in the framer loopback path.

TAIS	AUTO_AIS	AISCLK	Transmit Data	Transmit Clock (TCKO)
0	0	0	Normal, No AIS	TCKI
0	0	1	AIS during TLOC	TI/EIACKI while TLOC
0	1	0	AIS During RLOS	TCKI
0	1	1	AIS During TLOC or RLOS	TI/EIACKI while TLOC
1	X	0	Manual AIS	TCKI
1	X	1	Manual AIS and ACKI	ACKI

NOTE(S): Systems that transmit framed all ones can utilize inband loopback code generator [TLB; addr 077] to send all ones in payload only.

076—Transmit Test Pattern Configuration (TPATT)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	TPSTART	FRAMED	ZLIMIT	TPATT[1]	TPATT[0]

TPSTART Enable Test Pattern Transmission.

FRAMED PRBS Framed—When set, the PRBS pattern does not overwrite framing bit positions and is stopped during these bit periods. In T1 mode, the frame bit (every 193rd bit) is not overwritten. In E1 mode, the PRBS test pattern is not written to time slot 0 (FAS and NFAS words) and time slot 16 (CAS signalling word) if CAS framing is also selected. CAS framing is selected by setting TFRAME[3] to 1 in the Transmit Configuration register [TCR0; addr 070]. If FRAMED is disabled, the test pattern is transmitted in all time slots.

ZLIMIT Enable Zero Limit; 7/14 depending on pattern.

TPATT[1:0] PRBS test patterns used by RPATT [addr 041] and TPATT [addr 076] are defined in the ITU standards O.151 and O.152 to use either inverted or non-inverted data. Standard data inversion is used for the selected PRBS test pattern unless ZLIMIT is enabled, in which case the test pattern uses non-inverted data (see Table 3-12).

Table 3-21. Transmit PRBS Test Pattern Measurements

FRAMED	ZLIMIT	TPATT	Test Pattern Measurements	Inversion
0	0	00	Unframed 2^11	No
0	0	01	Unframed 2^15	Yes
0	0	10	Unframed 2^20	No
0	0	11	Unframed 2^23	Yes
0	1	00	Unframed 2^11 with 7 zero limit	No
0	1	01	Unframed 2^15 with 7 zero limit	No
0	1	10	Unframed 2^20 with 14 zero limit (QRSS/QRS/QRTS)	No
0	1	11	Unframed 2^23 with 14 zero limit (non-std)	No
1	0	00	Framed 2^11	No
1	0	01	Framed 2^15	Yes
1	0	10	Framed 2^20	No
1	0	11	Framed 2^23	Yes
1	1	00	Framed 2^11 with 7 zero limit	No
1	1	01	Framed 2^15 with 7 zero limit (non std)	No
1	1	10	Framed 2^20 with 14 zero limit (QRSS/QRS/QRTS))	No
1	1	11	Framed 2^23 with 14 zero limit (non-std)	No

077—Transmit Inband Loopback Code Configuration (TLB)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	—	LB_LEN[1]	LB_LEN[0]	UNFRAMED	LBSTART

LB_LEN[1:0] Inband Loopback Code Length (from LBP):
00 = 4 bits
01 = 5 bits
10 = 6 bits
11 = 7 bits

UNFRAMED Loopback Code Overwrites Framing.

LBSTART Start Inband Loopback Code Transmission.

078—Transmit Inband Loopback Code Pattern (LBP)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
LBP[1]	LBP[2]	LBP[3]	LBP[4]	LBP[5]	LBP[6]	LBP[7]	—

LBP[1] First bit transmitted

LBP[2] Second bit transmitted

LBP[3] Third bit transmitted

LBP[4] Fourth bit transmitted

LBP[5] Fifth bit transmitted

LBP[6] Sixth bit transmitted

LBP[7] Seventh bit transmitted

3.13 Transmit Sa-Byte Buffers

Five transmit Sa-Byte buffers (TSA4–TSA8) are used to insert Sa-bits in TS0. The entire group of 40 bits is sampled every 16 frames, coincident with the TMF interrupt boundary [addr 008]. Bit 0 from each TSA register is then inserted during frame 1, Bit 1 during frame 3, Bit 2 during frame 5 and so on. This gives the processor up to 2 ms after TMF interrupt to write new Sa-Byte buffer values. Transmit Sa-bits maintain a fixed relationship to the transmit CRC multiframe.

07B—Transmit Sa4 Byte Buffer (TSA4)

7	6	5	4	3	2	1	0
TSA4[7]	TSA4[6]	TSA4[5]	TSA4[4]	TSA4[3]	TSA4[2]	TSA4[1]	TSA4[0]

TSA4[7] Sa4 bit transmitted in frame 15

TSA4[6] Sa4 bit transmitted in frame 13

TSA4[5] Sa4 bit transmitted in frame 11

TSA4[4] Sa4 bit transmitted in frame 9

TSA4[3] Sa4 bit transmitted in frame 7

TSA4[2] Sa4 bit transmitted in frame 5

TSA4[1] Sa4 bit transmitted in frame 3

TSA4[0] Sa4 bit transmitted in frame 1

07C—Transmit Sa5 Byte Buffer (TSA5)

7	6	5	4	3	2	1	0
TSA5[7]	TSA5[6]	TSA5[5]	TSA5[4]	TSA5[3]	TSA5[2]	TSA5[1]	TSA5[0]

TSA5[7] Sa5 bit transmitted in frame 15

TSA5[6] Sa5 bit transmitted in frame 13

TSA5[5] Sa5 bit transmitted in frame 11

TSA5[4] Sa5 bit transmitted in frame 9

TSA5[3] Sa5 bit transmitted in frame 7

TSA5[2] Sa5 bit transmitted in frame 5

TSA5[1] Sa5 bit transmitted in frame 3

TSA5[0] Sa5 bit transmitted in frame 1

07D—Transmit Sa6 Byte Buffer (TSA6)

7	6	5	4	3	2	1	0
TSA6[7]	TSA6[6]	TSA6[5]	TSA6[4]	TSA6[3]	TSA6[2]	TSA6[1]	TSA6[0]

TSA6[7] Sa6 bit transmitted in frame 15

TSA6[6] Sa6 bit transmitted in frame 13

TSA6[5] Sa6 bit transmitted in frame 11

TSA6[4] Sa6 bit transmitted in frame 9

TSA6[3] Sa6 bit transmitted in frame 7

TSA6[2] Sa6 bit transmitted in frame 5

TSA6[1] Sa6 bit transmitted in frame 3

TSA6[0] Sa6 bit transmitted in frame 1

07E—Transmit Sa7 Byte Buffer (TSA7)

7	6	5	4	3	2	1	0
TSA7[7]	TSA7[6]	TSA7[5]	TSA7[4]	TSA7[3]	TSA7[2]	TSA7[1]	TSA7[0]

TSA7[7] Sa7 bit transmitted in frame 15

TSA7[6] Sa7 bit transmitted in frame 13

TSA7[5] Sa7 bit transmitted in frame 11

TSA7[4] Sa7 bit transmitted in frame 9

TSA7[3] Sa7 bit transmitted in frame 7

TSA7[2] Sa7 bit transmitted in frame 5

TSA7[1] Sa7 bit transmitted in frame 3

TSA7[0] Sa7 bit transmitted in frame 1

07F—Transmit Sa8 Byte Buffer (TSA8)

7	6	5	4	3	2	1	0
TSA8[7]	TSA8[6]	TSA8[5]	TSA8[4]	TSA8[3]	TSA8[2]	TSA8[1]	TSA8[0]

TSA8[7] Sa8 bit transmitted in frame 15

TSA8[6] Sa8 bit transmitted in frame 13

TSA8[5] Sa8 bit transmitted in frame 11

TSA8[4] Sa8 bit transmitted in frame 9

TSA8[3] Sa8 bit transmitted in frame 7

TSA8[2] Sa8 bit transmitted in frame 5

TSA8[1] Sa8 bit transmitted in frame 3

TSA8[0] Sa8 bit transmitted in frame 1

3.14 Bit-Oriented Protocol Registers

The Bit Oriented Protocol (BOP) transceiver sends and receives BOP messages, including ESF Yellow Alarm. These messages consist of repeated 16-bit patterns with an embedded 6-bit codeword. The BOP message channel is configured to operate over the same channel selected by the DL1 Time Slot Enable Register [DL1_TS; addr 0A4]. The channel must be configured to operate over the FDL channel in order for BOP messages to convey Priority, Command, and Response codeword messages according to ANSI T1.403, Section 9.4.1. Therefore, DL1 must be configured and enabled to allow BOP operation, as described in Table 3-22.

Table 3-22. DLI Configuration for T1-ESF, FDL

Datalink Configuration Registers	Value	Description
DL1_TS [addr 0A4]	0 × 40	Enabling odd frames, Fbit (T1)
DL1_BIT [addr 0A5]	0 × 00	Select bits to use in time slot.
DL1-CTL [addr 0A6]	0 × 03	Select normal FIFO mode, FCS, Tx enabled, Rx enabled.
RDL1_FFC [addr 0A7]	00######	###### is the threshold for receiver FIFO near full.
TDL1_FEC [addr 0AB]	00######	###### is the threshold FIFO near empty.

The precedence of transmitted BOP messages with respect to current DL1 transmit activity is configurable [TBOP_MODE; addr 0A0]. BOP messages can also be transmitted during E1 mode, although the 16-bit codeword pattern has not currently been adopted as an E1 standard. BOP message format:

```
0xxxxxx0  11111111 (transmitted right to left)
[543210]  6-bit codeword
```

0A0—Bit Oriented Protocol Transceiver (BOP)

7	6	5	4	3	2	1	0
RBOP_START	RBOP_INTEG	RBOP_LEN[1]	RBOP_LEN[0]	TBOP_LEN[1]	TBOP_LEN[0]	TBOP_MODE[1]	TBOP_MODE[0]

RBOP_START BOP Receiver Enable—When active, BOP receiver searches FDL channel for data that matches a 16-bit pattern in the form of 0xxxxxx011111111, where xxxxxx equals a 6-bit codeword. Otherwise, BOP receiver is disabled.
0 = disabled
1 = BOP receiver enable

RBOP_INTEG RBOP Integration—Requires receipt of two identical consecutive 16-bit patterns (without errors or gaps between patterns) to validate a single codeword. In this case, an errored codeword does not increment the pattern count. RBOP integration must be enabled to meet codeword detection criteria while receiving 1E-3 bit error ratio. RBOP_INTEG adds at least one to the number of successive 16-bit patterns needed to qualify receipt of BOP message (2 in a row counts as 1 pattern, 11 in a row counts as 10, and 26 in a row counts as 25).
0 = no integration
1 = RBOP integration

RBOP_LEN[1:0] RBOP Message Length—Selects the number of successive identical 16-bit patterns that are needed to qualify receipt of a single BOP message and to update RBOP [addr 0A2] with the received codeword. At this time RBOP interrupt [ISR1; addr 00A] is also activated. Successive patterns can be separated by any number of bits as long as they do not contain a different valid codeword.

RBOP_LEN	Successive Patterns	Notes
00	1	Single 16-bit pattern updates RBOP
01	10	Minimum command, response length
10	25	Preferred command, response length
11	Change	RBOP updates on receipt of each new pattern

TBOP_LEN[1:0] TBOP Message Length—Selects the number of repeated 16-bit patterns sent as a single message when a TBOP [addr 0A1] codeword is written. Another message, with the same or different codeword value, can be written to TBOP as soon as prior message start is acknowledged via activation of TBOP interrupt [ISR2; addr 009]. If no new message is written, the FDL channel returns to TDL1 output control upon completion of message transmission. Processor changes TBOP_LEN to end transmission of a continuously repeating message.

TBOP_LEN	Repeated Patterns	Message Length (ms)	Notes
00	1	4	Single message sends 16 FDL bits
01	10	40	Minimum command, response length
10	25	100	Preferred command
11	Continuous	Continuous	Required for ESF yellow alarm

TBOP_MODE[1:0] Transmit BOP Mode—Enables BOP transmitter and establishes priority of TBOP [addr 0A1] output in relation to TDL1 [addr 0AD] output. When TBOP messages are given output priority, any write to TBOP aborts TDL1 output within the next eight FDL bit times and then suspends TDL1 data output until TBOP has completed transmission. The processor can check TMSG1 status [addr 0AE] before writing TBOP to determine if TDL1 output is idle. TDL1 buffer can be written while TBOP is granted priority.

When TDL1 messages are given output priority, TBOP output is suspended when the TDL1 buffer becomes non-empty. Furthermore, TBOP is forced to wait until the TDL1 buffer is empty and the TDL1 output is in the idle state. If TBOP_LEN is continuous and TDL1/PRM message output is pending, then TBOP will be suspended at the next 16-bit pattern boundary. TDL1 priority is used to transmit PRM, DS1 Idle (ISID), or optional path maintenance (PID, TSID) messages separated by ESF Yellow Alarm codewords as defined in Annex D of ANSI T1.403.

TBOP_MODE	Mode Description
0X	Disabled: TBOP writes are ignored
10	TBOP output priority
11	TDL1 output priority

0A1—Transmit BOP Codeword (TBOP)

7	6	5	4	3	2	1	0
—	—	TBOP[5]	TBOP[4]	TBOP[3]	TBOP[2]	TBOP[1]	TBOP[0]

TBOP[5] 6th bit transmitted

TBOP[4] 5th bit transmitted

TBOP[3] 4th bit transmitted

TBOP[2] 3rd bit transmitted

TBOP[1] 2nd bit transmitted

TBOP[0] Transmit BOP codeword, 1st bit transmitted

0A2—Receive BOP Codeword (RBOP)

7	6	5	4	3	2	1	0
RBOP_LOST	RBOP_VALID	RBOP[5]	RBOP[4]	RBOP[3]	RBOP[2]	RBOP[1]	RBOP[0]

RBOP_LOST Previous Message Overwritten—Activated when RBOP is updated and RBOP_VALID is already set, indicating that the previous codeword was never read by the processor.
0 = no error
1 = prior codeword lost

RBOP_VALID RBOP Message Valid—Set each time RBOP[5:0] is updated with a codeword value. Reading from RBOP clears RBOP_VALID.
0 = no message or message read
1 = new RBOP message received

RBOP[5] 6th bit received

RBOP[4] 5th bit received

RBOP[3] 4th bit received

RBOP[2] 3rd bit received

RBOP[1] 2nd bit received

RBOP[0] Receive BOP codeword, 1st bit received

0A3—BOP Status (BOP_STAT)

Real-time status of the BOP transmitter and receiver is reported primarily for diagnostic purposes.

7	6	5	4	3	2	1	0
TBOP_ACTIVE	RBOP_ACTIVE	—	—	—	—	—	—

TBOP_ACTIVE TBOP Active—Remains set for the entire length of a message as defined by TBOP_LEN[1:0] [addr 0A0].

RBOP_ACTIVE RBOP Active—Is set as soon as eight ones are detected and remains set if subsequent 1st and 8th bits are zero. For pattern length 1, RBOP_ACTIVE is a short pulse reported at the end of a received 16-bit pattern. For longer lengths, the signal goes high at the end of the first pattern and is held active until the desired number (or change) of patterns is detected. At this point RBOP interrupt is generated. Consequently, this signal is usually high.

3.15 Data Link Registers

Each framer contains two independent Data Link Controllers (DL1, DL2), which are programmed to send and receive HDLC formatted or unformatted serial data over any combination of bits within a selected time slot. The serial data channels operate at a multiple of 4 kbps up to the full 64 kbps time slot rate by selecting a combination of time slot bits from odd, even, or all frames. DL1 and DL2 each contain a 64-byte receive and 64-byte transmit buffer which, function either as programmable length circular buffers or full-length data FIFOs.

0A4—DL1 Time Slot Enable (DL1_TS)

7	6	5	4	3	2	1	0
DL1_TS[7]	DL1_TS[6]	DL1_TS[5]	DL1_TS[4]	DL1_TS[3]	DL1_TS[2]	DL1_TS[1]	DL1_TS[0]

DL1_TS[7] Unchannelized—Test mode only; all time slots selected. Zero for normal operation.

DL1_TS[6, 5] Frame Select—Transmit and receive data link 1 operates on data only during the specified T1/E1 frames. Frame select options give the processor access to different types of data link channels as well as overhead channels. Note that overhead bit insertion is performed after TDL1, so internal transmitter overhead insertion must be bypassed [TFRM; addr 072] before processor supplied overhead can be output from TDL1.

00 = all frames
01 = even frames only
10 = odd frames only
11 = not valid

DL1_TS[4:0] Time Slot Word Enable—Transmit and receive data link 1 operates on data only during the specified time slot. During T1 mode, selecting time slot zero enables data link operation on the F-bit positions.

DL1_TS[4:0]	Time Slot Enable
00000	F-bit (T1) or TS0 (E1)
00001	TS1
|	|
11110	TS30
11111	TS31

0A5—DL1 Bit Enable (DL1_BIT)

7	6	5	4	3	2	1	0
DL1_BIT[7]	DL1_BIT[6]	DL1_BIT[5]	DL1_BIT[4]	DL1_BIT[3]	DL1_BIT[2]	DL1_BIT[1]	DL1_BIT[0]

DL1_BIT[7:0] DL1 Bit Select—Works in conjunction with DL1_TS [addr 0A4] to select one or more time slot bits for data link input and output. Any combination of bits may be enabled by writing the corresponding DL1_BIT active (high). The LSB enables first bit transmitted or received, and MSB enables eighth bit transmitted or received. DL1_BIT has no effect when DL1_TS selects T1 F-bits.

0 = disable data link bit
1 = enable data link bit

0A6—DL1 Control (DL1_CTL)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	TDL1_RPT	DL1[1]	DL1[0]	TDL1_EN	RDL1_EN

TDL1_RPT Circular Transmit Buffer Enable—Processor can fill the transmit FIFO [TDL1; addr 0AD] with up to 64 bytes (Pack6 or Pack8 bits/byte) of unformatted data to be sent repeatedly. While TDL1_RPT is active high, data written to TDL1 is held until the processor writes an end of message [TDL1_EOM; addr 0AC]. After TDL1_EOM is written, the transmitter waits for the beginning of the next output multiframe (based on the selected transmit framing mode) before sending the first byte of the circular buffer. Subsequent bytes are output in the selected time slot/overhead bits and will continue to wrap around (recirculate) from the buffer until the processor writes new buffer data and another TDL1_EOM. This allows the processor to send multiframe aligned data patterns in ESF, SF, SLC, FAS, MFAS or CAS overhead bits.

0 = normal transmit FIFO
1 = enable circular transmit buffer

DL1[1: 0] Data Link 1 Mode—Selects either HDLC-formatted (FCS or Non-FCS) transmit and receive data link message mode or unformatted (Pack8 or Pack6) message mode. During HDLC modes, the transmit/receive circuits perform zero insertion/removal after each occurrence of 5 consecutive ones contained in the message bits, FLAG (0x7E) character insertion/removal during idle channel conditions, and ABORT (0xFF) code insertion/detection upon errored channel conditions. Refer to ITU-T Recommendation Q.921 for complete details of the HDLC link-layer protocol. FCS mode automatically generates, inserts, and checks the 16-bit Frame Check Sequence (FCS) without passing FCS bits through transmit and receive FIFOs.

Non-FCS mode passes all message bits that exist between the opening and closing FLAG characters through the FIFOs, without generating or checking FCS bits. Non-FCS mode allows the processor to generate and check the entire contents of each HDLC frame. Unformatted data link modes provide transparent channel access in which every data link bit transmitted is supplied by the processor through TDL1 and each bit received is passed to the processor through RDL1 [addr 0A8]. Pack8 and Pack6 unformatted mode options select the number of bits per byte that are stored in transmit/receive FIFOs, eight or six bits, respectively. The only data processing performed during unformatted mode is the alignment of transmitted and received data bits with respect to the transmit/receive multiframe.

00 = FCS
01 = No FCS
10 = Pack8
11 = Pack6

TDL1_EN Transmit Data Link 1 Enable—When enabled, transmitter begins to empty and to format the contents of the transmit data link FIFO for output during the selected time slot bits according to the selected DL1[1:0] mode. Also enables generation of transmitter data link interrupt events.

0 = disabled
1 = enable transmit data link

RDL1_EN Receive Data Link 1 Enable—When enabled, receiver begins to format data from the selected time slot bits and to fill the receive data link FIFO according to the selected DL1[1:0] mode. Also enables generation of receiver data link interrupt events.

0 = disabled
1 = enable receive data link

0A7—RDL #1 FIFO Fill Control (RDL1_FFC)

7	6	5	4	3	2	1	0
MSG_FILL[1]	MSG_FILL[0]	FFC[5]	FFC[4]	FFC[3]	FFC[2]	FFC[1]	FFC[0]

MSG_FILL[1:0] Unformatted Message Fill Limit—Applicable only for Pack8 and Pack6 modes, the message fill limit selects how many receive FIFO locations [RDL1; addr 0A8] are filled before the receive data link generates an RFULL interrupt [ISR2; addr 009] and generates a corresponding RDL1 Partial message status word entry. Fill limit thus determines how many bytes constitute an unformatted message. Fill limits give the processor an alternative to using RNEAR interrupts to signal the end of a received unformatted message. Note the number of bits per unformatted message must divide evenly by the number of bits monitored per multiframe.

For example, SLC applications monitor Fs bits during even frames for a total of 36 bits monitored out of 72 frames. Using Pack6 mode, that group of 36 Fs bits from each SLC multiframe can be chosen to constitute one unformatted message by selecting a message fill limit which equals 6 bytes (of 6 bits/byte). In the SLC example, an RFULL interrupt would then be generated every 9 ms on each SLC multiframe boundary. Fill limits provided for T1 cases are multiples of 6 bytes (i.e. 6, 12 or 18 FIFO locations) to hold 1 or more multiframes worth of monitored data. In E1 mode, fill limits are multiples of 8 bytes to correspond with the 16 frame multiframe lengths (i.e. monitoring CRC4 in MFAS framing mode or TS16 in CAS framing mode).

T1/E1N	MSG_FILL[1:0]	Message Fill Limit
X	00	Disabled
0	01	8 bytes
0	10	16 bytes
0	11	24 bytes
1	01	6 bytes
1	10	12 bytes
1	11	18 bytes

FFC[5:0] Near Full FIFO Threshold—Selects FIFO depth of near full interrupt [RNEAR; addr 009] and near full level status [RNEAR1; addr 0A9]. The RNEAR interrupt and RNEAR1 indicator are both activated when the number of empty FIFO locations equals the selected threshold. The threshold controls how many data and/or status bytes (64 minus threshold value) that the processor must read from RDL1 after RNEAR interrupt. This is done to clear the RNEAR1 indicator as well as to determine how much time remains (in bytes) for the processor to read RDL1 before the receive FIFO is full. If a receive message is in progress when the near full threshold is reached, the receiver issues a message interrupt [RMSG; addr 009] and places a Partial message in the receive FIFO.

FFC[5:0]	Empty @ RNEAR	Filled @ RNEAR
00 0000	none	64 = RFULL
00 0001	1 empty FIFO location	63 filled
00 0010	2 empty FIFO locations	62 filled
|	|	|
11 1110	62 empty FIFO locations	1 filled
11 1111	63 empty FIFO locations	0 filled = empty

0A8—Receive Data Link FIFO #1 (RDL1)

Two different read byte values are supplied: WORD0 equals message status, and WORD1 equals message data. The processor determines which byte value is located in the FIFO by first reading the receiver data link status [RDL1_STAT; addr 0A9]. In some cases, multiple consecutive status bytes may be placed in the FIFO, so the processor must always read RDL1_STAT before reading RDL1 to distinguish between WORD0 and WORD1 byte values. However, each time a non-zero byte count [RDL1_CNT] status is read, the processor is guaranteed the next RDL1_CNT reads from RDL1 will equal message data [WORD1] and not message status. Note that a status byte occupies 1 byte of FIFO space, just the same as a message data byte occupies 1 byte of FIFO space.

WORD0: Message Status

7	6	5	4	3	2	1	0
EOM[1]	EOM[0]	RDL1_CNT[5]	RDL1_CNT[4]	RDL1_CNT[3]	RDL1_CNT[2]	RDL1_CNT[1]	RDL1_CNT[0]

EOM[1, 0] End of Message—Receive data link reports an End of Message status for each occurrence of a complete (Good), a continued (Partial), an errored (FCS/Non-integer), or an aborted (Abort) message. Note that properly received unformatted messages are reported with a Partial end of message status. The processor responds to Good or Partial status by reading the indicated number of data bytes [RDL1_CNT] from RDL1. For abort or error cases, RDL1_CNT equals zero to indicate that all received data from that message was discarded. Note that a Good status with RDL1_CNT=0 is reported if the processor reads RDL1 while the receiver is in progress of filling the FIFO (in which case RDL1_STAT contains RSTAT1=1 and RMSG1=1). If an abort or error status with zero byte count is reported after the processor has already buffered a prior HDLC Partial message, that partial buffered processor data should be discarded. Abort status is reported if the receiver detects a string of 7 or more consecutive ones during an HDLC message. FCS error status is reported if FCS mode is enabled, and the checksum calculated over the received HDLC message does not match the received 16-bit FCS. Non-integer error status is reported if the receiver detects a closing FLAG character that yields an HDLC message length which is not an integer number of 8-bit octets.

00 = Good
01 = FCS/Non-integer
10 = Abort
11 = Partial

RDL1_CNT[5:0] Byte Count [5:0]—Indicates the number of Message Data [WORD1] bytes that are stored in subsequent consecutive FIFO locations, constituting one received message. The reported byte count is the actual number of bytes, in the range of 0 to 63 bytes, where 0 indicates zero bytes for the processor to read. The processor can either read the specified number of message data bytes consecutively from RDL1 or can poll RDL1_STAT after reading each data byte until RDL1_STAT reports an end of message (i.e. RMPTY1=1 or RSTAT1=1).

WORD1: Message Data

7	6	5	4	3	2	1	0
RDL1[7]	RDL1[6]	RDL1[5]	RDL1[4]	RDL1[3]	RDL1[2]	RDL1[1]	RDL1[0]

RDL1[7:0] Receive Message Data—Filled by the receiver data link, from LSB to MSB, with bits from the selected channel. Processor reads 8-bit FIFO data during HDLC and Pack8 modes. During Pack6 mode, only the six least significant bits RDL1[5:0] are filled.

0A9—RDL #1 Status (RDL1_STAT)

7	6	5	4	3	2	1	0
—	—	—	RMSG1	RSTAT1	RMPTY1	RNEAR1	RFULL1

RMSG1 In Progress Receive Message—Real time status of receive message sequencer is provided mostly for processor polled applications. During HDLC modes, RMSG1 is high for the interval between opening and closing FLAG characters to indicate the receiver is actively filling FIFO locations (in which case RSTAT1 is also held high). RMSG1 is low while the channel receives FLAG or Abort characters. During unformatted modes, RMSG1 is high continuously.

0 = channel idle
1 = channel actively filling FIFO

RSTAT1 Next FIFO Read Equals Message Status—For non-empty FIFO conditions (RMPTY1=0), RSTAT1 indicates the next byte read from RDL1 returns WORD0 message status or WORD1 message data. Note that RSTAT1 equals zero if the FIFO is empty and there is no message in progress. The processor polls RSTAT1 before reading RDL1 to determine how to interpret RDL1 read byte value or the processor checks RSTAT1 in response to RMSG interrupt [ISR2; addr 009].

0 = RDL1 byte equals Message Data (or empty FIFO, if RMTPY1=1)
1 = RDL1 byte equals Message Status (if RMPTY1=0)

RMPTY1 Receive FIFO Empty—Indicates no data or status bytes are present in the receive data link FIFO.

0 = FIFO contains data or status as indicated by RSTAT1
1 = FIFO empty

RNEAR1 Receive FIFO Near Full—Indicates data link has filled receive FIFO to the near full threshold level specified in FFC[5:0]. Upon reaching the near full level, the receiver updates the message status byte [WORD0] placed on top of the FIFO and reports the current in progress message with a Partial end of message status. The processor must read those filled FIFO locations to clear RNEAR1 status indicator and to enable the next RNEAR interrupt.

0 = FIFO depth is below the near full level
1 = FIFO has been filled to the near full level

RFULL1 Receive FIFO Full—Indicates data link has completely filled 64 byte locations in the receive FIFO. In all cases, RFULL1 is an error, indicating the processor didn't keep pace with the receiver and indicates one or more received messages were discarded after the FIFO became full. The FIFO may still contain one or more Good received messages, and the processor may still process all receive FIFO contents as usual. However, any message that was in progress when FIFO reached full is discarded and is also reported with Partial end of message status and a zero byte count (which distinguishes a full end of message status from a normal abort or error message status).

0 = FIFO is less than full

1 = FIFO has been completely filled

0AA—Performance Report Message (PRM)

7	6	5	4	3	2	1	0
AUTO_PRM	PRM_CR	PRM_R	PRM_U1	PRM_U2	PRM_SL	AUTO_SL	SEND_PRM

AUTO_PRM Automatic PRM Insertion—AUTO_PRM instructs the data link transmitter to format and send a Performance Report Message on the selected transmit channel after each occurrence of the ONESEC interrupt. To meet PRM requirements specified in ANSI T1.403-1995, FCS mode [DL1_CTL; addr 0A6] and one second error count latching [LATCH_CNT; addr 046] must both be enabled. In addition, the data link channel must be selected to output on Facility Data Link (FDL) framing bits [DL1_TS=0x40; addr 0A4]. Octets 1-14 of the transmit PRM message contents are automatically encoded as shown in Table A-5, *Performance Report Message Structure*. The encodings are based on the number of received CRC, FPS, LCV, SEF and FRED errors [addr 050-05A]. RFSLIP errors [SSTAT; addr 0D9] are also automatically encoded if AUTO_SL (described below) is enabled. The remaining PRM message contents typically remain fixed and are supplied by the processor from other bits that follow in the PRM register. Note that BOP priority codeword transmissions are interrupted by AUTO_PRM if TDL1 is granted output priority [TBOP_MODE=11; addr 0A0]. Note also that AUTO_PRM messages take up no space in the transmit data link FIFO, but are inserted on the transmit channel only after the FIFO is empty. Therefore, if the processor needs to transmit another type of FDL message between PRM messages, the processor must write that message after AUTO_PRM has begun sending (i.e. after ONESEC interrupt).

0 = no automatic PRM

1 = send PRM automatically every ONESEC

PRM_CR Transmit CR Message Bit—The processor writes the selected C/R bit value to send in each PRM.

PRM_R Transmit R Message Bit—The processor writes the selected R bit value to send in each PRM.

PRM_U1 Transmit U1 Message Bit—The processor writes the selected U1 bit value to send in each PRM.

PRM_U2 Transmit U2 Message Bit—The processor writes the selected U2 bit value to send in each PRM.

PRM_SL Transmit SL Message Bit—The processor writes the selected SL bit value to send in each PRM.

AUTO_SL Automatic SL Bit Insertion—RFSLIP error status is encoded into the transmit PRM contents. Or, the PRM_SL bit value supplied by the processor is sent.
0 = send PRM_SL value in SL bit
1 = send RFSLIP error status in SL bit

SEND_PRM Immediately Generate and Send PRM—Similar to AUTO_PRM mode, SEND_PRM instructs the data link transmitter to format and send a Performance Report Message according to ANSI T1.403-1995. But SEND_PRM executes immediately rather than waiting for ONESEC interrupt. Thus SEND_PRM gives processor control over PRM transmit timing. This is easier for the processor to manage if other FDL message types must also be transmitted.

0AB—TDL #1 FIFO Empty Control (TDL1_FEC)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	FEC[5]	FEC[4]	FEC[3]	FEC[2]	FEC[1]	FEC[0]

FEC[5:0] Near Empty Transmit FIFO Threshold—Selects FIFO depth of near empty interrupt [TNEAR; addr 009] and near empty level status [TNEAR1; addr 0AE]. The TNEAR interrupt is activated when the number of data bytes remaining to be transmitted from the FIFO falls below the selected threshold. The TNEAR1 indicator is active as long as the number of processor filled FIFO locations is below the selected threshold. Thus TNEAR1 is active high when the transmit FIFO is completely empty and remains active until the processor writes the selected threshold number of bytes to TDL1 [addr 0AD]. Assuming the processor writes 64 bytes to completely fill an empty FIFO, then a TNEAR interrupt occurs after the transmitter has sent the number of bytes required to bring the FIFO level back down below the selected threshold. Hence, the processor can consecutively write 64 - FEC[5:0] number of bytes to the transmit FIFO in response to a TNEAR interrupt. The interrupt also signifies how much time remains (in bytes) for the processor to write TDL1 before transmit FIFO is emptied. Typically, FEC[5:0] is set to a small value (below 10 byte threshold) to minimize the number of TNEAR interrupts and maximize the time between TNEAR interrupts.

FEC[5:0]	Byte threshold @ TNEAR	Empty @ TNEAR
00 0000	Disabled	Disabled
00 0001	1 byte threshold	63 empty
00 0010	2 byte threshold	62 empty
|	|	|
11 1110	62 byte threshold	2 empty
11 1111	63 byte threshold	1 empty

0AC—TDL #1 End Of Message Control (TDL1_EOM)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
EOM[7]	EOM[6]	EOM[5]	EOM[4]	EOM[3]	EOM[2]	EOM[1]	EOM[0]

TDL1_EOM End of Transmit Message. Writing any data value to TDL1_EOM marks the last byte of data written into the transmit FIFO as the end of an HDLC message (FCS or Non-FCS mode) or marks the end of a transmit circular buffer. Processor must write TDL1_EOM after writing a complete message or the last byte of a circular buffer into TDL1 [addr 0AD]. The written data value is ignored and cannot be read back. Multiple HDLC messages are allowed to be queued in the transmit FIFO simultaneously. In addition, the transition from one circular buffer to another occurs only after the end of message byte of the current circular buffer has been sent.

0AD—Transmit Data Link FIFO #1 (TDL1)

7	6	5	4	3	2	1	0
TDL1[7]	TDL1[6]	TDL1[5]	TDL1[4]	TDL1[3]	TDL1[2]	TDL1[1]	TDL1[0]

TDL1[7:0] Transmit Message Data—Output by the transmitter data link, from LSB to MSB, and sent on the selected time slot bits. Processor writes 8-bit FIFO data during HDLC and Pack8 modes. During Pack6 mode, only the six least significant bits TDL1[5:0] are used.

0AE—TDL #1 Status (TDL1_STAT)

7	6	5	4	3	2	1	0
—	—	—	—	TMSG1	TMPTY1	TNEAR1	TFULL1

TMSG1 In Progress Transmit Message—The real time status of the transmit message sequencer is provided mostly for diagnostic purposes. During HDLC modes, TMSG1 is high for the interval between opening and closing FLAG characters. This indicates that transmitter is actively pulling data bytes from transmit FIFO locations. TMSG1 is low while the channel transmits FLAG or Abort characters. During unformatted and circular buffer modes, TMSG1 is high continuously.

0 = channel idle

1 = channel actively emptying FIFO

TMPTY1 Transmit FIFO Empty—Indicates no message data is present in transmit data link FIFO. This is typically checked by the processor in response to a TMSG or TNEAR interrupt. If this is a TMSG interrupt, the processor checks TMPTY1 to determine that all queued messages were sent (TMPTY1=1) or more queued messages remain to be sent (TMPTY1=0). If this is a TNEAR interrupt, the processor confirms TMPTY1=0 to verify the partial transmit message was not aborted by a FIFO underrun.

0 = FIFO contains data to be transmitted
1 = FIFO empty

TNEAR1 Transmit FIFO Near Empty—Indicates data link has emptied transmit FIFO to below the near empty threshold specified in FEC[5:0]. After sending the byte that occupied the near empty FIFO threshold level, TNEAR1 goes active high, which generates a TNEAR interrupt. The processor must write data to TDL1 to fill the transmit FIFO beyond the near empty threshold in order to clear TNEAR1 status and enable the next TNEAR interrupt event.

0 = FIFO depth is below the near empty level
1 = FIFO has been emptied past the near empty level

TFULL1 Transmit FIFO Full—Indicates processor has completely filled 64 byte locations in transmit FIFO. While TFULL1 remains active, any subsequent processor writes to TDL1 are ignored. If the processor should inadvertently write to TDL1 while TFULL1 is active, the processor must allow FIFO to become completely empty without writing to TDL1_EOM in order to force the transmitter to send an Abort character.

0 = FIFO is less than full
1 = FIFO has been completely filled

0AF—DL2 Time Slot Enable (DL2_TS)

7	6	5	4	3	2	1	0
DL2_TS[7]	DL2_TS[6]	DL2_TS[5]	DL2_TS[4]	DL2_TS[3]	DL2_TS[2]	DL2_TS[1]	DL2_TS[0]

DL2_TS[7] Unchannelized—Test mode only; all time slots selected. Zero for normal operation.

DL2_TS[6, 5] Frame Select—Transmit and receive data link 2 operates on data only during the specified T1/E1 frames. Frame select options give the processor access to different types of data link channels, as well as overhead channels. Overhead bit insertion is performed after TDL2, so internal transmitter overhead insertion must be bypassed [TFRM; addr 072] before the processor supplied overhead can be output from TDL2.

00 = all frames
01 = even frames only
10 = odd frames only
11 = Not valid

DL2_TS[4:0] Time Slot Word Enable—Transmit and receive data link 2 operates on data only during the specified time slot. During T1 mode, selecting time slot zero enables data link operation on the F-bit positions.

DL2_TS[4:0]	Time Slot Enable
00000	F-bit (T1) or TS0 (E1)
00001	TS1
|	|
11110	TS30
11111	TS31

0B0—DL2 Bit Enable (DL2_BIT)

7	6	5	4	3	2	1	0
DL2_BIT[7]	DL2_BIT[6]	DL2_BIT[5]	DL2_BIT[4]	DL2_BIT[3]	DL2_BIT[2]	DL2_BIT[1]	DL2_BIT[0]

DL2_BIT[7:0] DL2 Bit Select—Works in conjunction with DL2_TS [addr 0AF] to select one or more time slot bits for data link input and output. Any combination of bits may be enabled by writing the corresponding DL2_BIT active (high). The LSB enables the first bit transmitted or received, and MSB enables eighth bit transmitted or received. DL2_BIT has no effect when DL2_TS selects T1 F-bits.

0 = disable data link bit

1 = enable data link bit

0B1—DL2 Control (DL2_CTL)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	TDL2_RPT	DL2[1]	DL2[0]	TDL2_EN	RDL2_EN

TDL2_RPT Circular Transmit Buffer Enable—Processor can fill transmit FIFO [TDL2; addr 0B8] with up to 64 bytes (Pack6 or Pack8 bits/byte) of unformatted data to be sent repeatedly. While TDL2_RPT is active high, data written to TDL2 is held until the processor writes an end of message [TDL2_EOM; addr 0B7]. After TDL2_EOM is written, the transmitter waits for the beginning of the next output multiframe (based on the selected transmit framing mode) before sending the first byte of the circular buffer. Subsequent bytes are output in the selected time slot/overhead bits and will continue to wrap around (recirculate) from the buffer until the processor writes new buffer data and another TDL2_EOM. This allows the processor to send multiframe aligned data patterns in ESF, SF, SLC, FAS, MFAS, or CAS overhead bits.

0 = normal transmit FIFO

1 = enable circular transmit buffer

DL2[1: 0] Data Link 2 Mode—Selects either HDLC formatted (FCS or Non-FCS) transmit and receive data link message mode or unformatted (Pack8 or Pack6) message mode. During HDLC modes, the transmit/receive circuits perform zero insertion/removal after each occurrence of 5 consecutive ones contained in the message bits. These include FLAG (0x7E) character insertion/removal during idle channel conditions and ABORT (0xFF) code insertion/detection upon errored channel conditions. Refer to ITU-T Recommendation Q.921 for complete details of the HDLC link-layer protocol. FCS mode automatically generates, inserts, and checks the 16-bit Frame Check Sequence (FCS) without passing FCS bits through transmit and receive FIFOs. While Non-FCS mode passes all message bits that exist between the opening and closing FLAG characters through the FIFOs, without generating or checking FCS bits. Non-FCS mode allows the processor to generate and check the entire contents of each HDLC frame. Unformatted data link modes provide transparent channel access in which every data link bit transmitted is supplied by the processor through TDL1, and each bit received is passed to the processor through RDL2 [addr 0B3]. Pack8 and Pack6 unformatted mode options select the number of bits per byte that are stored in transmit/receive FIFOs, eight or six bits, respectively. The only data processing performed during unformatted mode is the alignment of transmitted and received data bits with respect to the transmit/receive multiframe.

00 = FCS
01 = No FCS
10 = Pack8
11 = Pack6

TDL2_EN Transmit Data Link 2 Enable—When enabled, the transmitter begins to empty and to format the contents of the transmit data link FIFO for output during the selected time slot bits according to the selected DL2[1:0] mode. Also enables generation of transmitter data link interrupt events.

0 = disabled
1 = enable transmit data link

RDL2_EN Receive Data Link 2 Enable—When enabled, the receiver begins to format data from the selected time slot bits and to fill the receive data link FIFO according to the selected DL2[1:0] mode. Also enables generation of receiver data link interrupt events.

0 = disabled
1 = enable receive data link

0B2—RDL #2 FIFO Fill Control (RDL2_FFC)

7	6	5	4	3	2	1	0
MSG_FILL[1]	MSG_FILL[0]	FFC[5]	FFC[4]	FFC[3]	FFC[2]	FFC[1]	FFC[0]

MSG_FILL[1:0] Unformatted Message Fill Limit—This is applicable only for Pack8 and Pack6 modes. The message fill limit selects how many receive FIFO locations [RDL2; addr 0B3] are filled before the receive data link generates an RFULL interrupt [ISR1; addr 00A] and a corresponding RDL2 Partial message status word entry. Fill limit thus determines how many bytes constitute an unformatted message. The fill limits give the processor an alternative to using RNEAR interrupts to signal the end of a received unformatted message. The number of bits per unformatted message must divide evenly by the number of bits monitored per multiframe. For example, SLC applications monitor Fs bits during even frames for a total of 36 bits monitored out of 72 frames. Using Pack6 mode, the group of 36 Fs bits from each SLC multiframe can be chosen to constitute one unformatted message. This is accomplished by selecting a message fill limit which equals 6 bytes (of 6 bits/byte). In the SLC example, an RFULL interrupt would then be generated every 9 ms on each SLC multiframe boundary. Fill limits provided for T1 cases are multiples of 6 bytes (i.e. 6, 12 or 18 FIFO locations) to hold one or more multiframes worth of monitored data. In E1 mode, fill limits are multiples of 8 bytes to correspond with the 16-frame multiframe lengths (i.e. monitoring CRC4 in MFAS framing mode or TS16 in CAS framing mode).

T1/E1N	MSG_FILL[1:0]	Message Fill Limit
X	00	Disabled
0	01	8 bytes
0	10	16 bytes
0	11	24 bytes
1	01	6 bytes
1	10	12 bytes
1	11	18 bytes

FFC[5:0] Near Full FIFO Threshold—Selects FIFO depth of near full interrupt [RNEAR; addr 00A] and near full level status [RNEAR2; addr 0B4]. The RNEAR interrupt and RNEAR2 indicator are both activated when the number of empty FIFO locations equals the selected threshold. The threshold controls how many data and/or status bytes (64 minus threshold value) the processor must read from RDL2 after RNEAR interrupt to clear the RNEAR2 indicator as well as how much time remains (in bytes) for the processor to read RDL2 before receive FIFO is full. If a receive message is in progress when the near full threshold is reached, the receiver issues a message interrupt [RMSG; addr 00A] and places a Partial message in the receive FIFO.

FFC[5:0]	Empty @ RNEAR	Filled @ RNEAR
00 0000	None	64 = RFULL
00 0001	1 empty FIFO location	63 filled
00 0010	2 empty FIFO locations	62 filled
|	|	|
11 1110	62 empty FIFO locations	1 filled
11 1111	63 empty FIFO locations	0 filled = empty

0B3—Receive Data Link FIFO #2 (RDL2)

Two different read byte values are supplied: WORD0 equals message status, and WORD1 equals message data. The processor determines which byte value is located in the FIFO by first reading the receiver data link status [RDL2_STAT; addr 0B4]. In some cases, multiple consecutive status bytes may be placed in the FIFO. Thus, the processor must always read RDL2_STAT before reading RDL2 to distinguish between WORD0 and WORD1 byte values. However, each time a non-zero byte count [RDL2_CNT] status is read, the processor is guaranteed the next RDL2_CNT reads from RDL2 will equal message data [WORD1] and not message status. A status byte occupies 1 byte of FIFO space, just the same as a message data byte occupies 1 byte of FIFO space.

WORD0: Message Status

7	6	5	4	3	2	1	0
EOM[1]	EOM[0]	RDL2_CNT[5]	RDL2_CNT[4]	RDL2_CNT[3]	RDL2_CNT[2]	RDL2_CNT[1]	RDL2_CNT[0]

EOM[1, 0] End of Message—The receive data link reports an End of Message status for each occurrence of a complete (Good), a continued (Partial), an errored (FCS/Non-integer), or an aborted (Abort) message. Note that properly received unformatted messages are reported with a Partial end of message status. The processor responds to Good or Partial status by reading the indicated number of data bytes [RDL2_CNT] from RDL2. For abort or error cases, RDL2_CNT equals zero to indicate all received data from that message was discarded. Note that a Good status with RDL2_CNT=0 is reported if the processor reads RDL2 while the receiver is in progress of filling the FIFO (in which case RDL2_STAT contains RSTAT2=1 and RMSG2=1). If an abort or error status with zero byte count is reported after the processor has already buffered a prior HDLC Partial message, that partial buffered processor data should be discarded. Abort status is reported if the receiver detects a string of 7 or more consecutive ones during an HDLC message. FCS error status is reported if FCS mode is enabled, and the checksum calculated over the received HDLC message does not match the received 16-bit FCS. Non-integer error status is reported if the receiver detects a closing FLAG character yielding an HDLC message length which is not an integer number of 8-bit octets.

00 = Good
01 = FCS/Non-integer
10 = Abort
11 = Partial

RDL2_CNT[5:0] Byte Count [5:0]—Indicates the number of Message Data [WORD1] bytes that are stored in subsequent consecutive FIFO locations, constituting one received message. The reported byte count is the actual number of bytes in the range of 0 to 63 bytes, where 0 indicates for the processor to read. The processor can either read the specified number of message data bytes consecutively from RDL2 or can poll RDL2_STAT after reading each data byte until RDL2_STAT reports an end of message (i.e. RMPTY2=1 or RSTAT2=1).

WORD1: Message Data

7	6	5	4	3	2	1	0
RDL2[7]	RDL2[6]	RDL2[5]	RDL2[4]	RDL2[3]	RDL2[2]	RDL2[1]	RDL2[0]

RDL2[7:0] Receive Message Data—Filled by the receiver data link, from LSB to MSB, with bits from the selected channel. The processor reads 8-bit FIFO data during HDLC and Pack8 modes. During Pack6 mode, only the six least significant bits RDL2[5:0] are filled.

0B4—RDL #2 Status (RDL2_STAT)

7	6	5	4	3	2	1	0
—	—	—	RMSG2	RSTAT2	RMPTY2	RNEAR2	RFULL2

RMSG2 In Progress Receive Message—The real-time status of the receive message sequencer is provided mostly for processor polled applications. During HDLC modes, RMSG2 is high for the interval between opening and closing FLAG characters to indicate the receiver is actively filling FIFO locations (in which case RSTAT2 is also held high). RMSG2 is low while the channel receives FLAG or Abort characters. During unformatted modes, RMSG2 is high continuously.

0 = channel idle

1 = channel actively filling FIFO

RSTAT2 Next FIFO Read Equals Message Status—For non-empty FIFO conditions (RMPTY2=0), RSTAT2 indicates that the next byte read from RDL2 will be WORD0 message status or WORD1 message data. Notice that RSTAT2 equals zero if the FIFO is empty, and there is no message in progress. Processor polls RSTAT2 before reading RDL2 to determine how to interpret RDL2 read byte value, or checks RSTAT2 in response to RMSG interrupt [ISR1; addr 00A].

0 = RDL2 byte equals Message Data (or empty FIFO, if RMTPY2=1)

1 = RDL2 byte equals Message Status (if RMPTY2=0)

RMPTY2 Receive FIFO Empty—Indicates no data or status bytes are present in receive data link FIFO.

0 = FIFO contains data or status as indicated by RSTAT2

1 = FIFO empty

RNEAR2 Receive FIFO Near Full—Indicates the data link has filled receive FIFO to the near full threshold level specified in FFC[5:0]. Upon reaching the near full level, the receiver updates the message status byte [WORD0] placed on top of the FIFO and reports the current in progress message with a Partial end of message status. The processor must read those filled FIFO locations to clear RNEAR2 status indicator, and to enable the next RNEAR interrupt.

0 = FIFO depth is below the near full level

1 = FIFO has been filled to the near full level

RFULL2 Receive FIFO Full—Indicates data link has completely filled 64 byte locations in the receive FIFO. In all cases, RFULL2 is an error, indicating the processor didn't keep pace with the receiver and indicates one or more received messages were discarded after the FIFO became full. The FIFO may still contain one or more Good received messages, and the processor may still process all receive FIFO contents as usual. However, any message that was in progress when FIFO reached full is discarded and is also reported with Partial end of message status and a zero byte count (which distinguishes a full end of message status from a normal abort or error message status).

0 = FIFO is less than full

1 = FIFO has been completely filled

0B6—TDL #2 FIFO Empty Control (TDL2_FEC)

7	6	5	4	3	2	1	0
—	—	FEC[5]	FEC[4]	FEC[3]	FEC[2]	FEC[1]	FEC[0]

FEC[5:0] Near Empty Transmit FIFO Threshold—Selects a FIFO depth of near empty interrupt [TNEAR; addr 00A] and near empty level status [TNEAR2; addr 0B9]. The TNEAR interrupt is activated when the number of data bytes remaining to be transmitted from the FIFO falls below the selected threshold. The TNEAR2 indicator is active as long as the number of processor filled FIFO locations is below the selected threshold. Thus, TNEAR2 is active high when the transmit FIFO is completely empty and remains active until the processor writes the selected threshold number of bytes to TDL2 [addr 0B8]. Assuming the processor writes 64 bytes to completely fill an empty FIFO, TNEAR interrupt occurs after the transmitter has sent the number of bytes required to bring the FIFO level back down below the selected threshold. Hence, the processor is guaranteed to be able to consecutively write 64 – FEC[5:0] number of bytes to the transmit FIFO in response to a TNEAR interrupt. The interrupt also signifies how much time remains (in bytes) for the processor to write TDL2 before transmit FIFO is emptied. Typically, FEC[5:0] is set to a small value (approximately 5–10 byte threshold) to minimize the number of TNEAR interrupts and maximize the time between TNEAR interrupts.

FEC[5:0]	Byte Threshold @ TNEAR	Empty @ TNEAR
00 0000	Disabled	Disabled
00 0001	1 byte threshold	63 empty
00 0010	2 byte threshold	62 empty
|	|	|
11 1110	62 byte threshold	2 empty
11 1111	63 byte threshold	1 empty

0B7—TDL #2 End Of Message Control (TDL2_EOM)

7	6	5	4	3	2	1	0
EOM[7]	EOM[6]	EOM[5]	EOM[4]	EOM[3]	EOM[2]	EOM[1]	EOM[0]

TDL2_EOM End of Transmit Message. Writing any data value to TDL2_EOM marks the last byte of data written into the transmit FIFO as the end of an HDLC message (FCS or Non-FCS mode) or the end of a transmit circular buffer. The processor must write TDL2_EOM after writing a complete message or the last byte of a circular buffer into TDL2 [addr 0B8]. The written data value is ignored and cannot be read back. Multiple HDLC messages are allowed to be queued in the transmit FIFO simultaneously. In addition, the transition from one circular buffer to another occurs only after the end of message byte of the current circular buffer has been sent.

0B8—Transmit Data Link FIFO #2 (TDL2)

7	6	5	4	3	2	1	0
TDL2[7]	TDL2[6]	TDL2[5]	TDL2[4]	TDL2[3]	TDL2[2]	TDL2[1]	TDL2[0]

TDL2[7:0] Transmit Message Data—Output by the transmitter data link from LSB to MSB and sent on the selected time slot bits. Processor writes 8-bit FIFO data during HDLC and Pack8 modes. During Pack6 mode, only the six least significant bits, TDL2[5:0], are used.

0B9—TDL #2 Status (TDL2_STAT)

7	6	5	4	3	2	1	0
—	—	—	—	TMSG2	TMPTY2	TNEAR2	TFULL2

TMSG2 In Progress Transmit Message—The real time status of the transmit message sequencer is provided mostly for diagnostic purposes. During HDLC modes, TMSG2 is high for the interval between the opening and closing FLAG characters to indicate the transmitter is actively pulling data bytes from transmit FIFO locations. TMSG2 is low while the channel transmits FLAG or Abort characters. During unformatted and circular buffer modes, TMSG2 is continuously high.

0 = channel idle

1 = channel actively emptying FIFO

TMPTY2 Transmit FIFO Empty—Indicates that no message data is present in the transmit data link FIFO. This is typically checked by processor in response to a TMSG or TNEAR interrupt. If this is a TMSG interrupt, the processor checks TMPTY2 to determine that all queued messages were sent (TMPTY2=1) or more queued messages remain to be sent (TMPTY2=0). If this is a TNEAR interrupt, the processor confirms TMPTY2=0 to verify the partial transmit message was not aborted by a FIFO underrun.

0 = FIFO contains data to be transmitted

1 = FIFO empty

TNEAR2 Transmit FIFO Near Empty—Indicates data link has emptied transmit FIFO to below the near empty threshold specified in FEC[5:0]. After sending the byte that occupied the near empty FIFO threshold level, TNEAR2 goes active high, which generates a TNEAR interrupt. The processor must write data to TDL2 to fill the transmit FIFO beyond the near empty threshold. This is done in order to clear TNEAR2 status and enable the next TNEAR interrupt event.

0 = FIFO depth is below the near empty level

1 = FIFO has been emptied past the near empty level

TFULL2 Transmit FIFO Full—Indicates processor has completely filled 64 byte locations in transmit FIFO. While TFULL2 remains active, any subsequent processor writes to TDL2 are ignored. If the processor should inadvertantly write to TDL2 while TFULL2 is active, the processor must allow FIFO to become completely empty without writing to TDL2_EOM, in order to force the transmitter to send an Abort character.

0 = FIFO is less than full

1 = FIFO has been completely filled

0BA—DLINK Test Configuration (DL_TEST1)

Data link test registers [addr 0BA-0BE] are for Conexant production test. Set to zero for normal operation. Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	—	DL_TEST1[3]	DL_TEST1[2]	DL_TEST1[1]	DL_TEST1[0]

DL_TEST1[3] Clock Test—Zero for normal operation, where clocks controlled by DL1_CTL and DL2_CTL [addr 0A6, 0B1]. When active high, clocks are always enabled.

DL_TEST1[2] Shadow Select—Report shadow pointers instead of normal read/write pointers.

DL_TEST1[1, 0] FIFO Select: 00 = RDL1; 01 = RDL2; 10 = TDL1; 11 = TDL2

0BB—DLINK Test Status (DL_TEST2)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	DL_TEST2[5]	DL_TEST2[4]	DL_TEST2[3]	DL_TEST2[2]	DL_TEST2[1]	DL_TEST2[0]

DL_TEST2[5:0] Read or Shadow Read Pointer—Reports selected FIFO read pointer current address.

0BC—DLINK Test Status (DL_TEST3)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	DL_TEST3[5]	DL_TEST3[4]	DL_TEST3[3]	DL_TEST3[2]	DL_TEST3[1]	DL_TEST3[0]

DL_TEST3[5:0] Write or Shadow Write Pointer—Specifies selected FIFO write pointer address.

0BD—DLINK Test Control #1 or Configuration #2 (DL_TEST4)

7	6	5	4	3	2	1	0
—	DL_TEST4[6]	DL_TEST4[5]	DL_TEST4[4]	DL_TEST4[3]	DL_TEST4[2]	DL_TEST4[1]	DL_TEST4[0]

DL_TEST4[6] TFIFO1 Read Clear—Force transmit FIFO read pointer to empty.

DL_TEST4[5] TFIFO1 Write Clear—Force transmit FIFO write pointer to empty.

DL_TEST4[4] TFIFO1 Write—MPU data goes to specified write pointer address.

DL_TEST4[3] RFIFO1 Read Clear—Force receive FIFO read pointer to empty state (flush).

DL_TEST4[2] RFIFO1 Write Clear—Force receive FIFO write pointer to empty state (flush).

DL_TEST4[1] RFIFO1 Write—MPU data goes to specified write pointer address.

DL_TEST4[0] RFIFO1 Bypass—Pipe receive data.

0BE—DLINK Test Control #2 or Configuration #2 (DL_TEST5)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	DL_TEST5[6]	DL_TEST5[5]	DL_TEST5[4]	DL_TEST5[3]	DL_TEST5[2]	DL_TEST5[1]	DL_TEST5[0]

DL_TEST5[6] TFIFO2 Read Clear—Force transmit FIFO read pointer to empty.

DL_TEST5[5] TFIFO2 Write Clear—Force transmit FIFO write pointer to empty.

DL_TEST5[4] TFIFO2 Write—MPU data goes to specified write pointer address.

DL_TEST5[3] RFIFO2 Read Clear—Force receive FIFO read pointer to empty state (flush).

DL_TEST5[2] RFIFO2 Write Clear—Force receive FIFO write pointer to empty state (flush).

DL_TEST5[1] RFIFO2 Write—MPU data goes to specified write pointer address.

DL_TEST5[0] RFIFO2 Bypass—Pipe receive data.

3.16 System Bus Registers

0D0—System Bus Interface Configuration (SBI_CR)

7	6	5	4	3	2	1	0
X2CLK	SBI_OE	EMF	EMBED	SBI[3]	SBI[2]	SBI[1]	SBI[0]

X2CLK Enable Times 2 Clocks—X2CLK modifies the number of RSB/TSB clock cycles used to clock a single data bit onto RSB and TSB. When X2CLK is active, two RSBCKI/TSBCKI clock cycles occur for each RPCMO, RSIGO, SIGFRZ, TPCMI, and TSIGI bit. But the FSYNC and MSYNC signals remain at the full 1x RSBCKI/TSBCKI clock rate.
0 = RSB/TSB signals at RSBCKI/TSBCKI
1 = Two SBCKI clock cycles per SBI bit (except FSYNC and MSYNC).

SBI_OE Enable System Bus Outputs—Places RPCMO, RSIGO, RINDO, and SIGFRZ output buffers under the control of the RSB timebase. SBI_OE also places the TINDO output buffer under the control of TSB timebase. Inactive (low) forces SBI output buffers to a high-impedance state. Power on and RESET [addr 001] force SBI_OE to an inactive state to avoid bus contention on devices sharing system bus connections.
0 = SBI outputs forced to high-impedance state
1 = SBI outputs controlled by respective RSB or TSB timebase

EMF Embedded Framing—During T1 mode, EMF controls placement of T1 framing bits on RPCMO and sampling of T1 framing bits from TPCMI according to the selected embedded framing format. EMF supports system buses that carry T1 frames but operate above T1 line rate. EMF allows the system bus to transport and maintain 193-bit frame integrity as T1 data is passed through RSLIP and/or TSLIP buffers.
0 = G.802 embedded format
1 = Reserved embedded format

EMBED EMBED instructs the transmit framer (refer to [TABORT; addr 071]) to align the TX timebase with respect to the frame and multiframe alignment embedded in the transmit line rate data output from TSLIP (TXDATA). EMBED is required during applications that bypass frame formatter [TFRM; addr 072] or Sa-bits [TMAN; addr 074]. If TSLIP is enabled, EMBED is inactive, and overhead is bypassed, TX timebase is not guaranteed to align to TXDATA, and bypassed overhead cannot reliably pass through TSLIP. EMBED is applicable to all system bus modes.

EMBED	T1/E1N	Embedded Framing Mode
0	X	Transmit framer searches TPCMI
1	0	TS0 embedded; search TXDATA
1	1	G.802 embedded; search TXDATA

NOTE(S): Embedded F-bits reach TX output only if frame formatter [TFRM; addr 072] is in bypass or transparent mode.

TS0 Embedded — The offline framer examines TXDATA to align TX timebase to the embedded FAS pattern. If MFAS is also enabled [TFRAME; addr 070], transmit online framer examines TXDATA to align TX timebase to the embedded MFAS pattern. While EMBED is active, TXDATA output is monitored, and transmit frame errors are reported in ISR0 [addr 00B]. Embedded TS0 supports E1 overhead bypass options for applications where TSLIP buffer is enabled.

G.802 Embedded — Automatically supports ITU–T Recommendation G.802, which defines frame format conversion between T1 and E1 line rates. This is accomplished by locating T1 F-bits in Bit 1 of Time Slot 26 of each system bus frame. G.802 embedded mode is applicable for system buses that are 1x, 2x, or 4x multiples of E1 line rate. Full implementation of G.802 also requires the processor to program TS0, TS16, and TS26–TS31 as unassigned system bus time slots [SBCn; addr 0E0–0FF].

SBI[3:0] System Bus Interface Mode—Defines transmit and receive system bus data format. System buses operate in one of nine basic formats which differ in the number of total available data time slots and the associated system bus clock rate. If the total time slots are a multiple of 32, SBI also defines which bus group of 32 byte-interleaved time slots are assigned to the respective device.

SBI[3:0]	Mode	Clock (Kbps)	Total Time Slots	Bus Group
0000	128A	8192	128	Group 0
0001	128B	8192	128	Group 1
0010	128C	8192	128	Group 2
0011	128D	8192	128	Group 3
0100	64A	4096	64	Group 0
0101	64B	4096	64	Group 1
0110	32	2048	32	—
0111	24+F	1544	24 + F-bit	—
1000	24	1536	24	—

0D1—Receive System Bus Configuration (RSB_CR)

7	6	5	4	3	2	1	0
BUS_RSB	SIG_OFF	RPCM_NEG	RSYN_NEG	BUS_FRZ	RSB_CTR	RSBI[1]	RSBI[0]

BUS_RSB Enable Bussed RSB Outputs—Applicable only if the system bus outputs are controlled by SBI timebases [SBI_OE = 1; addr 0D0]. When BUS_RSB is active, RPCMO, RSIGO, and RINDO outputs from multiple devices are allowed to share common receive system bus connections. Unused time slots are three-stated during those bus groups that are not selected by SBI mode [addr 0D0]. Otherwise, unused time slots repeat their output data value for all bus groups.
0 = RSB time slot value repeated for all bus groups
1 = three-state RSB outputs during unused bus groups

SIG_OFF Inhibit RPCMO Signaling Reinsertion—Disables insertion of ABCD signaling for all time slots on the receive system bus PCM output (RPCMO). Otherwise, ABCD signaling is reinserted on RPCMO as controlled by System Bus Per-Channel [SBCn; addr 0E0–0FF] and RX Per-Channel [RPCn; addr 180–19F] controls.
0 = enable insertion of signaling onto RPCMO
1 = inhibit RPCMO signaling

RPCM_NEG Output Data on Falling Edge Clock—Selects RSBCKI rising or falling edge clock signal to output RPCMO, RSIGO, RINDO, and SIGFRZ.
0 = RSB rising edge outputs
1 = RSB falling edge outputs

RSYN_NEG Output Sync on Falling Edge Clock—Selects RSBCKI rising or falling edge clock signal for RFSYNC or RMSYNC outputs. Opposite RSBCKI edge is used if RFSYNC or RMSYNC is programmed as an input.
0 = RFSYNC or RMSYNC rising edge output (falling edge input)
1 = RFSYNC or RMSYNC falling edge output (rising edge input)

BUS_FRZ Enable Bused SIGFRZ Output—Enables SIGFRZ from multiple devices to share a common receive system bus connection. When active, SIGFRZ three-states during bus group time slots that are unused by the selected SBI mode [addr 0D0].
0 = SIGFRZ repeats for all bus groups
1 = three-state SIGFRZ during unused bus groups

RSB_CTR Force RSLIP to Center—Writing a one to RSB_CTR forces RSLIP read buffer pointer to its initial delay condition. If RFSYNC or RMSYNC is programmed as an output, RSB_CTR consequently forces a change of system bus sync alignment. The processor must assert RSB_CTR after configuration of the receive slip buffer. Centering RSLIP does not effect RSLIP status reported in ISR.5 [addr 006].
0 = no effect
1 = force RSLIP to center

RSBI[1:0] Receive Slip Buffer Interface Mode—Selects configuration of RSLIP buffer. RSBI determines the total buffer depth and initial delay conditions. While RSLIP is bypassed, RSB outputs and RSBCKI is ignored. RFSYNC and RMSYNC are also ignored in bypass mode if they are programmed as inputs.

RSBI	Mode	Total Depth	Initial Delay	Conditions
00	Normal	2 Frame	1 Frame	When RFSYNC is output
			0.5 to 1.5 Frames	When RFSYNC is input
01	Short	2 Frame	32 bits	Reverts to normal upon slip
10	Elastic	674 bits	32 bits	Recenters automatically upon slip
11	Bypass	0 bits	0 bits	RSBCKI ignored

0D2—RSB Sync Bit Offset (RSYNC_BIT)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	—	—	OFFSET[2]	OFFSET[1]	OFFSET[0]

OFFSET[2:0] RSB Sync Bit Offset—Selects which RSB bit number coincides with RFSYNC and RMSYNC sync pulses. Sync pulses are programmed to align to one bit in relation to RPCMO, RSIGO, RINDO, and SIGFRZ time slots. If the sync pulses are desired to coincide with location of T1 F-bit or time slot zero Bit 1, then OFFSET is programmed to equal zero. Sync bit offset is added to time slot offset [RSYNC_TS; addr 0D3] to form a 10-bit OFFSET value. This value applies to RFSYNC location, which is then added to frame offset [RSYNC_FRM; addr 0D8] to form a 15-bit OFFSET value that applies to RMSYNC location. Both RFSYNC and RMSYNC offsets are expressed as RSB.OFFSET, allowing the system to generate or accept sync pulses at any bit location within the RSB multiframe.

OFFSET[2:0]	RSYNC Location
000	Bit 1 or F-bit
001	Bit 2
|	|
110	Bit 7
111	Bit 8

0D3—RSB Sync Time Slot Offset (RSYNC_TS)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	OFFSET[9]	OFFSET[8]	OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]

OFFSET[9:3] RSB Sync Time Slot Offset—Selects which RSB time slot number coincides with RFSYNC and RMSYNC sync pulses, in the range of Time Slots 0–127. If the sync pulses coincide with location of T1 F-bit or TS0, then OFFSET is programmed to equal zero. Refer also to RSYNC_BIT and RSYNC_FRM [addr 0D2, 0D8].

2048, 1544, and 1536 Kbps/sec SBI Mode

OFFSET[9:3]	RSYNC Time Slot
0000000	0 or F-bit
0000001	1
|	|
0011110	30
0011111	31

4096 Kbps/sec SBI Mode

OFFSET[9:4]	OFFSET[3]	RSYNC Time Slot	Group
000000	0	0	A
000000	1	0	B
000001	0	1	A
000001	1	1	B
|	|	|	|
011110	0	30	A
011110	1	30	B
011111	0	31	A
011111	1	31	B

8192 Kbps/sec SBI Mode

OFFSET[9:5]	OFFSET[4:3]	RSYNC Time Slot	Group
00000	00	0	A
00000	01	0	B
00000	10	0	C
00000	11	0	D
00001	00	1	A
00001	01	1	B
00001	10	1	C
00001	11	1	D
|	|	|	|
11110	00	30	A
11110	01	30	B
11110	10	30	C
11110	11	30	D

8192 Kbps/sec SBI Mode

OFFSET[9:5]	OFFSET[4:3]	RSYNC Time Slot	Group
11111	00	31	A
11111	01	31	B
11111	10	31	C
11111	11	31	D

NOTE(S): Offsets which are outside the RSB timebase range result in no pulses on RFSYNC and RMSYNC outputs.

0D4—Transmit System Bus Configuration (TSB_CR)

7	6	5	4	3	2	1	0
BUS_TSB	TX_ALIGN	TPCM_NEG	TSYN_NEG	TSB_ALIGN	TSB_CTR	TSBI[1]	TSBI[0]

BUS_TSB Enable Bused TSB Output—Applicable only if system bus outputs are controlled by SBI timebases [SBI_OE = 1; addr 0D0]. When BUS_TSB is active, TINDO outputs from multiple devices are allowed to share a common transmit system bus connection. Unused time slots are three-stated during those bus groups that are not selected by SBI mode [addr 0D0]. Otherwise, unused time slots repeat their TINDO value for all bus groups.

0 = TINDO repeated for all bus groups

1 = three-state TINDO during unused time slots

TX_ALIGN Transmitter Output Multiframe Aligns to TSB Timebase—Allows multiframe alignment located at TSB (from TMSYNC or TFRAMER to pass across TSLIP buffer and force the corresponding multiframe alignment onto the transmitter timebase. Used primarily to pass TMSYNC from system bus.

0 = Transmitter multiframe does not follow TSB

1 = Transmitter multiframe follows TSB multiframe

TPCM_NEG Output Data on Falling Edge Clock—Selects TSBCKI rising or falling edge clock signal to output TINDO and the opposite TSBCKI edge to sample TPCMI and TSIGI inputs.

0 = TINDO rising edge output (TPCMI and TSIGI falling edge inputs)

1 = TINDO falling edge outputs (TPCMI and TSIGI rising edge inputs)

TSYN_NEG Output Sync on Falling Edge Clock—Selects TSBCKI rising or falling edge clock signal for TFSYNC or TMSYNC outputs. The opposite TSBCKI edge is used if TFSYNC or TMSYNC is programmed as input.

0 = TFSYNC or TMSYNC rising edge output (falling edge input)

1 = TFSYNC or TMSYNC falling edge output (rising edge input)

TSB_ALIGN Transmit System Bus Multiframe Aligns to Transmit Timebase—Allows multiframe alignment located at TX timebase to pass across TSLIP and force the corresponding multiframe alignment onto the TSB timebase. Used primarily to pass CAS or MFAS alignment located by the transmit online framer onto the TMSYNC output.

0 = TSB multiframe does not follow XMTR

1 = TSB multiframe aligned by XMTR

TSB_CTR Force TSLIP to Center—Writing a one to TSB_CTR forces TSLIP read buffer pointer to its initial delay condition. This can possibly force a change of transmit frame alignment if TSLIP is configured in Elastic or Bypass modes. Writing a zero has no effect. The processor must assert TSB_CTR after configuration of the transmit slip buffer. Afterwards, CX28398 automatically recenters TSLIP buffer according to the configured mode. Centering TSLIP does not effect TSLIP status reported in ISR5[addr 006].

0 = no effect
1 = force TSLIP to center

TSBI[1:0] Transmit Slip Buffer Interface Mode—Selects the configuration of the TSLIP buffer. The TSBI determines the total buffer depth and initial delay conditions. While TSLIP is bypassed, TCKI clocks TSB input/output, and TSBCKI is ignored.

TSBI	Mode	Total Depth	Initial Delay	Conditions
00	Normal	2 Frame	0.5 to 1.5 Frames	Dependent on present depth, no change of output frame.
01	Short	2 Frame	32 Bits	Reverts to normal upon slip
10	Elastic	64 Bits	32 Bits	Recenters automatically upon slip
11	Bypass	0 Bits	0 Bits	TSBCKI ignored

NOTE(S):
1. Bypass requires system bus equal to line rate.
2. Idle code and local signaling insertion apply to all modes.

0D5—TSB Sync Bit Offset (TSYNC_BIT)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	—	—	OFFSET[2]	OFFSET[1]	OFFSET[0]

OFFSET[2:0] TSB Sync Bit Offset—Selects which TSB bit number coincides with TFSYNC and TMSYNC sync pulses. Sync pulses are programmed to align to one bit in relation to TPCMI, TSIGI and TINDO time slots. If the sync pulses are desired to coincide with location of T1 F-bit or time slot zero Bit 1, then OFFSET is programmed to equal zero. Sync bit offset is added to time slot offset [TSYNC_TS; addr 0D6] to form a 10-bit OFFSET value. This value applies to TFSYNC and TMSYNC location. Both TFSYNC and TMSYNC offsets are expressed as TSB.OFFSET, allowing the system to generate or accept sync pulses at any bit location within the TSB frame.

OFFSET[2:0]	TSYNC Location
000	Bit 1 or F-bit
001	Bit 2
|	|
110	Bit 7
111	Bit 8

0D6—TSB Sync Time Slot Offset (TSYNC_TS)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	OFFSET[9]	OFFSET[8]	OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]

OFFSET[9:3] TSB Sync Time Slot Offset—Selects which TSB time slot number coincides with TFSYNC and TMSYNC sync pulses, in the range of Time Slots 0 through 127. If the sync pulses coincide with location of T1 F-bit or TS0, then OFFSET is programmed to equal zero. Refer also to TSYNC_TS [addr 0D6].

2048, 1544, and 1536 Kbps/sec SBI Mode

OFFSET[9:3]	TSYNC Time Slot
0000000	0 or F-bit
0000001	1
|	|
0011110	30
0011111	31

4096 Kbps/sec SBI Mode

OFFSET[9:4]	OFFSET[3]	TSYNC Time Slot	Group
000000	0	0	A
000000	1	0	B
000001	0	1	A
000001	1	1	B
|	|	|	|
011110	0	30	A
011110	1	30	B
011111	0	31	A
011111	1	31	B

8192 Kbps/sec SBI Mode

OFFSET[9:5]	OFFSET[4:3]	TSYNC Time Slot	Group
00000	00	0	A
00000	01	0	B
00000	10	0	C
00000	11	0	D
00001	00	1	A
00001	01	1	B
00001	10	1	C
00001	11	1	D
|	|	|	|
11110	00	30	A

8192 Kbps/sec SBI Mode			
OFFSET[9:5]	OFFSET[4:3]	TSYNC Time Slot	Group
11110	01	30	B
11110	10	30	C
11110	11	30	D
11111	00	31	A
11111	01	31	B
11111	10	31	C
11111	11	31	D

NOTE(S): Offsets which are outside the TSB timebase range result in no pulses on TFSYNC and TMSYNC outputs.

0D7—Receive Signaling Configuration (RSIG_CR)

7	6	5	4	3	2	1	0
—	SET_RSIG	SET_SIG	UNICODE	DEBOUNCE	FRZ_OFF	FRZ_ON	THRU

SET_RSIG Force 2 ms RSIG Interrupt—Allows the processor to receive an interrupt on RSIG [addr 008] at every CAS multiframe boundary. Applicable only to E1 mode with CAS enabled. Overrides STACK interrupt.

0 = RSIG interrupt on signaling STACK change
1 = RSIG interrupts every 2 ms at CAS multiframe

SET_SIG Overwrite Robbed-Bit Signaling—Applicable only during T1 mode and function dependent on RIDLE. When RIDLE is inactive, SET_SIG forces received robbed-bit signaling to one before updating RSLIP time slot value. Therefore, bit 8 of each time slot received during signaling frames 6, 12, 18, and 24 is replaced with a one. This function is particularly useful in cross-connect and exchange systems that strip robbed-bit signaling or use different signaling frame alignment on inbound and outbound ports.

0 = no change to receive signaling
1 = replace robbed-bit signaling

UNICODE Inband Signaling Freeze (applicable to T1 modes only)—If UNICODE is enabled, received ABCD signaling on all channels is searched on a per-channel basis for the 4-bit UNICODE pattern. UNICODE pattern detection inhibits STACK. RSIG buffer updates for that channel as long as UNICODE is present, but does not affect SIGFRZ output and is not reported to the processor. This function is described in Bellcore TR-TSY-000303, Section 4.4.9, Revision 2, July 1989.

0 = no effect
1 = enable UNICODE detection and per-channel signaling freeze

DEBOUNCE Debounce Receive ABCD Signaling—Applicable only to those channels where signaling stack is enabled (SIG_STK; addr 180–19F). Output signaling buffer (RSIG) updates for these channels are evaluated after D-bit signaling is received. New signaling is placed into RSIG and STACK buffers only if the RSIG input and output values differ. DEBOUNCE filters single bit errors on ABCD signaling. This is accomplished by comparing incoming ABCD bits on a bit-by-bit basis with current buffered input and output ABCD bits and inverting the update signaling bit value when incoming and output bits are equal. However, these differ from the buffered input value below. At the end of each multiframe, the entire input ABCD value is copied to the output ABCD value.

0 = no effect

1 = debounce receive ABCD signaling

Sig Input	Current Bit I/O	Update Bit I/O	Notes
0	00	00	—
0	01	00	Change output
0	10	00	Debounce
0	11	01	—
1	00	10	—
1	01	11	Debounce
1	10	11	Change output
1	11	11	—

NOTE(S): Normal (non-debounced) signaling always transfers ABCD input to ABCD output buffer space coincident with the D-bit update.

FRZ_OFF/FRZ_ON Manual Signaling Update and SIGFRZ Output—Allows the processor to manually control updates of the receive signaling buffer [RSIGn; addr 1A0–1BF], the signaling stack [addr 0DA], and the SIGFRZ output pin. FRZ_ON and FRZ_OFF control the SIGFRZ pin's output state, but do not affect normal operations of the SIGFRZ interrupt [ISR7; addr 004]. Receive ABCD input signaling is placed into STACK and RSIG buffers according to the modes shown below. Stack updates are individually enabled on a per-channel basis according to SIG_STK [addr 180–19F].

			SIGFRZ			
FRZ_ON	FRZ_OFF	SIG_STK	Interrupt	Pin	STACK	RSIGn
0	0	0	0	0	No update	All ABCD
0	0	X	1	1	No update	No update
0	0	1	0	0	ABCD Changes	All ABCD
X		0	X	0	No Update	All ABCD
X	1	1	X	0	ABCD Changes	All ABCD
1	0	X	X	1	No update	No Update

THRU Enable Transparent Robbed-Bit Signaling—RMSYNC is forced to align with respect to RX timebase and to follow each change of receiver's multiframe alignment, plus any frame offset caused by RSLIP buffer delay. In this manner, RMSYNC is able to retain its signaling multiframe alignment with respect to RPCMO output data frames. THRU mode is required when RSLIP is configured in bypass mode. It is also useful for ADPCM transcoder systems that utilize robbed-bit signaling during frames other than the normal (modulo 6) signaling frames and therefore cannot utilize RPCMO signaling reinsertion in ADPCM coded channels. During THRU mode, RMSYNC must be programmed as an output [PIO; addr 018]. RMSYNC can follow a change of RX multiframe alignment without generating an alarm indication (e.g., receiver change of SF alignment without accompanying loss of basic frame alignment).

0 = no effect
1 = transparent robbed-bit signaling

0D8—Signaling Reinsertion Frame Offset (RSYNC_FRM)

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	OFFSET[14]	OFFSET[13]	OFFSET[12]	OFFSET[11]	OFFSET[10]

OFFSET[14:10] RSB Sync Frame Offset—Selects which RSB frame number coincides with RMSYNC pulse in the range of frame 0–23. OFFSET specifies the frame in which RMSYNC is applied as an input or in which RMSYNC appears as an output, consequently locating RPCMO signaling frames used for T1 robbed-bit (frames 6,12,18, and 24) or E1 CAS signaling reinsertion. The only RPCMO channels affected are those with signaling insertion enabled [INSERT; addr 0E0–0FF].

T1/E1N	OFFSET[14:10]	RMSYNC Pulse
0	X0000	RSB frame 0
0	X0001	RSB frame 1
|	|	|
0	X1110	RSB frame 14
0	X1111	RSB frame 15
1	00000	RSB frame 1
1	00001	RSB frame 2
|	|	|
1	10110	RSB frame 23
1	10111	RSB frame 24

0D9—Slip Buffer Status (SSTAT)

SSTAT[7:0] are updated at the start of each respective receive/transmit internal frame boundary (i.e. 125 µs interval). Each bit in SSTAT is latched upon event detection and held until read cleared by the processor.

7	6	5	4	3	2	1	0
TSDIR	TFSLIP	TUSLIP	TDLY	RSDIR	RFSLIP	RUSLIP	RDLY

TSDIR Transmit Slip Direction—TSDIR is updated each time a TSLIP error is latched in TFSLIP and TSDIR indicates which direction the slip occurred.

0 = TSLIP error deleted 1 frame on TX data output

1 = TSLIP error repeated 1 frame on TX data output

TFSLIP Controlled TSLIP Event—TUSLIP and TFSLIP event status are latched active high when transmit slip error is detected. Either event reports a TSLIP error in ISR5 [addr 006]. Active high hold interval is defined by LATCH_ERR [addr 046].

Two types of errors are detected:

1. FSLIP = Controlled ± frame slip on TX data output. FSLIP affects transmit time slot data, but does not change transmit timebase or frame alignment.
2. USLIP = Uncontrolled ± 1 to ± 256 bit slip on TX data. USLIP affects both time slot data and frame alignment. TUSLIP and TFSLIP status depends on transmit system bus configuration [TSB_CR; addr 0D4].

TSBI Mode	TUSLIP	TFSLIP	TSLIP Event
Normal	0	0	None
	0	1	FSLIP
	1	0	USLIP
	1	1(1)	Both FSLIP and USLIP
Short	0	0	None
	0	1	FSLIP
	1	0	USLIP
Elastic	0	n/a	None
	1	n/a	USLIP
Bypass	n/a	n/a	—

NOTE(S):

(1) Most recent slip error direction is reported in TSDIR.

2. TFSLIP not applicable (read zero value) if TSLIP is bypassed or configured as elastic store. TUSLIP not applicable if TSLIP bypassed. In short delay mode, if the bus clock is faster than the receive clock, the system bus will resynchronize and USLIP is reported. If the receive clock is faster, RSLIP reverts to normal mode and subsequently reports FSLIP errors.

TUSLIP Uncontrolled TSLIP Event—See TFSLIP description.

TDLY Transmit Slip Buffer Delay > One Frame—Indicates that real-time phase difference between TSLIP read and write pointers is more than 192 bits (T1) or 256 bits (E1). TDLY provides a coarse phase indicator and toggles (low) if transmit system bus clock phase advances with respect to the transmit line rate clock. A finer granularity of TSLIP phase is reported in TPHASE [addr 0DC].

0 = TSLIP delay less than or equal to 1 frame

1 = TSLIP delay greater than 1 frame

RSDIR Receive Slip Direction—RSDIR is updated each time an RSLIP error is latched in RFSLIP or RUSLIP and indicates which direction the slip occurred.

0 = RSLIP error deleted one frame on RPCMO or SBI resync detected

1 = RSLIP error repeated one frame on RPCMO or SBI time slot reassigned

RFSLIP Controlled RSLIP Event—RUSLIP and RFSLIP event status are latched active high when receive slip error is detected. Either event reports RSLIP error in ISR5 [addr 006]. Active high hold interval is defined by LATCH_ERR [addr 046]. Two types of errors are detected:

1. FSLIP = Controlled ± 1 frame slip on RPCMO data output. FSLIP affects RPCMO, but does not change alignment of system bus RFSYNC or RMSYNC signals.
2. USLIP = Uncontrolled ± 1 to ± 256 bit slip on RPCMO. USLIP affects both system bus data and sync outputs. RUSLIP and RFSLIP status depends on receive system bus configuration [RSB_CR; addr 0D1].

RSBI Mode	RUSLIP	RFSLIP	RSLIP Event	Notes
Normal	0	0	None	
	0	1	FSLIP	Most recent slip error direction is reported in RSDIR.
	1	0	USLIP	An uncontrolled slip can occur in Normal mode due to a resync of the SBI, or in T1 rate converted applications, the active time slots are reassigned. The former sets RSDIR = 0, the latter RSDIR = 1.
Short	0	0	None	
	0	1	FSLIP	
	1	0	USLIP	In short delay mode, if bus clock is faster than receive clock, system bus will resynchronize and USLIP is reported. If receive clock is faster, RSLIP reverts to Normal mode and subsequently reports FSLIP errors.
Elastic	0	0	None	
	1	0	USLIP	RFSLIP is not applicable (read zero value) while RSLIP buffer is bypassed or configured as elastic store. FSLIP or USLIP errors reported upon bypass mode initialization should be ignored.
Bypass	–	–	–	

RUSLIP Uncontrolled RSLIP Event—See RFSLIP description.

RDLY Receive Slip Buffer Delay > 1 Frame—Indicates that real-time phase difference between RSLIP read and write pointers is more than 192 bits (T1) or 256 bits (E1). RDLY provides a coarse phase indicator and toggles (low) if receive clock phase advances with respect to receive system bus clock. A finer granularity of RSLIP phase is reported in RPHASE [addr 0DB].

0 = RSLIP delay less than or equal to 1 frame

1 = RSLIP delay greater than 1 frame

0DA—Receive Signaling Stack (STACK)

STACK contains new signaling information from those channels with SIG_STK [addr 180–19F] enabled. STACK allows the processor to conveniently monitor only changed ABCD signaling values from the selected channels. RSIG interrupt [addr 008] is triggered at the end of any multiframe where one or more ABCD signaling values have changed. The processor reads the STACK address twice to retrieve the channel number (WORD = 0) and to retrieve the new ABCD value (WORD = 1). The processor continues to read from STACK until the last new value is retrieved (MORE = 0).

Internal STACK read/write pointers are initialized by RESET [addr 001]. STACK contents are updated for each channel in which the stack is enabled [SIG_STK; addr 180–19F]. STACK contents are updated with new output signaling if the buffered RSIGn input and output ABCD signaling values differ. STACK is evaluated on a channel-by-channel basis after the D-bit is updated. The processor must poll the RSIG interrupt to determine when STACK has new information.

Word 0: Channel Number (first read)

7	6	5	4	3	2	1	0
WORD	MORE	—	CH[4]	CH[3]	CH[2]	CH[1]	CH[0]

WORD Stack Word ID (always 0 in Word 0)

MORE More Stack Contents (always 1 in Word 0)

CH[4:0] Channel Number (E1 range 0–31; T1 range 1–24)

Word 1: New Signaling Value (second read)

7	6	5	4	3	2	1	0
WORD	MORE	—	—	SIG_BITA	SIG_BITB	SIG_BITC	SIG_BITD

WORD Stack Word ID (always 1 in Word 1)

WORD	MORE	MPU Response
0	0	First word, get channel
0	1	Never used
1	0	No change or last change, stop
1	1	New signaling, keep reading

MORE More Stack Contents equal 1 if more available.

SIG_BITA–D Signaling Bit A–D–Processor reads the new ABCD signaling value from this location. The ABCD value is also preset in RSIGn (addr 1A0–1BF) output signaling buffer, so the processor does not need to store a local copy of each channel's signaling status.

0DB—RSLIP Phase Status (RPHASE)

7	6	5	4	3	2	1	0
RDELAY[5]	RDELAY[4]	RDELAY[3]	RDELAY[2]	RDELAY[1]	RDELAY[0]	RSLIP_WR	RSLIP_RD

RDELAY[5:0] RSLIP Buffer Delay—Difference between RX and RSB timebase in time slot intervals. Reported once per frame coincident with RFRAME interrupt [ISR3; addr 008]. Actual delay may vary significantly, depending on which time slots are assigned.

000000 = RX to RSB delay in the range of 0–7 bits
|
111111 = RX to RSB delay in the range of 504–511 bits

RSLIP_WR Active RSB Slip Buffer Half—This bit indicates which half of the receive slip buffer is currently supplying data to the Receive System Bus (0 = RLIP_LO, 1 = RSLIP_HI). The processor can write data to the opposite buffer half.

RSLIP_RD Active Receiver Slip Buffer Half—This bit indicates which half of the receive slip buffer is currently receiving data from the receiver (0 = RSLIP_LO, 1 = RSLIP_HI). The processor can read data from the opposite buffer half.

0DC—TSLIP Phase Status (TPHASE)

7	6	5	4	3	2	1	0
TDELAY[5]	TDELAY[4]	TDELAY[3]	TDELAY[2]	TDELAY[1]	TDELAY[0]	TSLIP_WR	TSLIP_RD

TDELAY[5:0] TSLIP Buffer Delay—Difference between TSB and TX timebase in time slot intervals. Reported once per frame coincident with TFRAME interrupt [ISR3; addr 008]. The actual delay may vary significantly, depending on which time slots are assigned.

000000 = TSB to TX delay in the range of 0–7 bits
|
111111 = TSB to TX delay in the range of 496–503 bits

TSLIP_WR Active Transmitter Slip Buffer Half—This bit indicates which half of the transmit slip buffer is currently supplying data to the transmitter (0 = TSLIP_LO, 1 = TSLIP_HI). The processor can write data to the opposite buffer half.

TSLIP_RD Active TSB Slip Buffer Half—This bit indicates which half of the transmit slip buffer is currently receiving data from the Transmit System Bus (0 = TSLIP_LO, 1 = TSLIP_HI). The processor can read data from the opposite buffer half.

0DD—RAM Parity Status (PERR)

All system bus data, signaling, and controls are transferred through a set of internal RAMs that have parity error detection capabilities. Any parity error that is detected during a RAM access is reported in PERR. Each error event is latched active high and held until the processor read clears PERR. Parity errors are indicative of system clock glitches (REFCKI, TSBCKI, or RSBCKI), a failing or excessively noisy power supply, or general circuit failure.

7	6	5	4	3	2	1	0
—	—	—	—	—	PERR_TPC	PERR_RPC	PERR_SBC

PERR_TPC TPC (Transmit) RAM Parity Error

PERR_RPC RPC (Receive) RAM Parity Error

PERR_SBC SBC (Control) RAM Parity Error

0E0–0FF—System Bus Per-Channel Control (SBCn; n = 0 to 31)

7	6	5	4	3	2	1	0
—	INSERT	SIG_LP	RLOOP	RINDO	TINDO	TSIG_AB	ASSIGN

INSERT Insert RX Signaling on RPCMO—Enables per-channel signaling insertion on RPCMO output, where ABCD signaling is supplied by RLOCAL signaling (RPCn; addr 180–19F) or buffered signaling [RSIGn; addr 1A0–IBF]. INSERT is a lower priority than no signaling (SIG_OFF; addr 0D1). RSB signaling frame locations are specified by RMSYNC signal in conjunction with programmed frame offset [OFFSET; addr 0D8].

SIG_OFF	INSERT	RLOCAL	RPCMO Inserted Signal
1	X	X	None
0	1	0	ABCD from RSIGn output buffer
0	1	1	ABCD from RPCn local buffer

SIG_LP Local Signaling Loopback—RSIGO output signaling supplied from TSIGn buffer contents.
0 = normal
1 = local signaling loopback

RLOOP Local Loopback—RPCMO output data supplied from TSLIP buffer contents.
0 = normal
1 = local loopback

RINDO Activate RINDO Time Slot Indicator—Receive system bus time slots are individually marked (active high for 8 bits) by RINDO. Note that SBI_OE (addr 0D0) overrides RINDO.
0 = RINDO signal inactive (low)
1 = RINDO signal active (high)

TINDO Activate TINDO Time Slot Indicator—Transmit system bus time slots are individually marked (active high for 8 bits) by TINDO.
0 = TINDO inactive
1 = TINDO active

TSIG_AB TSIG_AB—AB Signaling. In T1 mode, only AB signaling bits are updated from TSIGI to the TSIGn buffer. If SIGFRZ active, output CD signaling bits are copied from the buffered output AB bits respectively. In E1 mode, setting TSIG_AB forces C = 0 and D = 1 when updating the TSIGn buffer.

0 = ABCD signaling
1 = AB signaling

ASSIGN Assign System Bus Time Slot—During T1 line applications where the system bus group consists of 32 time slots, ASSIGN selects which 24 of 32 time slots are used to transport line time slots. The number of assigned system bus time slots must always equal the number of line time slots, therefore ASSIGN must be active in all 32 SBCn locations during E1 modes. Unassigned time slots are not updated by the receiver as it fills the RSLIP buffer. T1 time slots are filled sequentially from RSLIP 1 to 24. Time slots 0 and 25 to 31 are reserved for unassigned values. Values are read from either the assigned or unassigned locations in a sequential fashion based upon the ASSIGN bit. System bus output data for unassigned time slots is taken from RSLIP buffer, which the processor can fill with any desired 16-bit fixed value (8 bits in RSLIP_LO, plus 8 bits in RSLIP_HI).

0 = unassigned system bus time slot
1 = assigned system bus time slot

100–11F—Transmit Per-Channel Control (TPCn; n = 0 to 31)

7	6	5	4	3	2	1	0
TB7ZS/EMF-BIT	TLOOP	TIDLE	TLOCAL	TSIGA/TSIGO	TSIGB/RSIGO	TSIGC	TSIGD

TB7ZS/EMF-BIT Bit7 Zero Code Substitution/Embedded F-bit Value (Applicable in T1 mode only)—For assigned system bus time slots [ASSIGN; addr 0E0-0FF], TB7ZS replaces Bit 7 of the time slot with a 1, if examination of 8-bit output detects all zeros. For an unassigned time slot where TIDLE is active, EMF-BIT replaces all embedded F-bit outputs with the programmed EMF-BIT value.

0 = no effect or force embedded F-bit (low)
1 = enable B7ZS or force embedded F-bit (high)

TLOOP Remote DS0 Channel Loopback—Transmit data supplied from RSLIP buffer contents. TLOOP works in conjunction with other TPCn control bits to select the source of transmitted data and signaling (see Table 3-23).

Table 3-23. Remote DS0 Channel Loopback

TLOOP	TIDLE	Data Source	Channel Mode
0	0	TPCMI	Normal
0	1	TSLIP_LO	Transmit Idle
1	0	RXDATA	Remote Loop
1	1	TSLIP_LO	Transmit Idle
NOTE(S): If RX Signaling, then RSIGn output buffer supplies transmit signaling.			

Table 3-24. Signaling Loopback

TLOCAL	TSIGO	RSIGO	Sig Source	Signaling Mode
0	0	0	None	No Transmit Signaling
0	0	1	RSIGn	Remote Signaling Loopback
0	1	0	TSIGn	TX Signaling Loopback
1	X	X	TSIGA–D	Local Signaling
NOTE(S): If RX Signaling, then RSIGn output buffer supplies transmit signaling.				

TIDLE Transmit Idle—Transmit data supplied from TSLIP_LO buffer contents. The processor writes an 8-bit idle pattern to TSLIP_LO for output on the selected time slot or optionally writes real-time data output to TSLIP_LO after each TFRAME interrupt [ISR3; addr 008]. Only the TSLIP_HI buffer is updated from TPCMI to allow continued local DS0 channel loopback.

0 = normal data output
1 = transmit idle data output

TLOCAL Transmit Local Signaling—When active, TLOCAL transmits TSIGA–TSIGD values in output ABCD signaling bits.

0 = TSIGO or RSIGO control output signaling
1 = transmit signaling from TSIGA–TSIGD

TSIGA–TSIGD Transmit Local Signaling—Holds the 4-bit ABCD signaling value, which is output when TLOCAL is active. In AB only applications, such as T1/SF framing, TSIGC and TSIGD must also be written with the same data as TSIGA and TSIGB. In E1 modes, TS0 and TS16 local signaling value determines CAS multiframe alignment signal (MAS) and XYXX output.

TSIGO Transmit Signaling Output—Applicable only if TLOCAL is inactive. ABCD signaling from TSIGn buffer is transmitted.

0 = no effect
1 = transmit signaling from TSIGn buffer

RSIGO Receive Signaling Output—Applicable only if TLOCAL is inactive. Forces transmit ABCD signaling to be supplied from RSIGn buffer, affecting a remote signaling loopback.

0 = no effect
1 = transmit signaling from RSIGn buffer

120–13F—Transmit Signaling Buffer (TSIGn; n = 0 to 31)

Transmit signaling from the TSIGI pin is automatically placed into the TSIGn buffer. Processor controls TSIGn insertion into the transmitter output by selecting TSIGO[inTPCn]. The processor can read monitor TSIGn from system supplied signaling or can use TSIGn for inter-processor communication. During E1 modes, TSIG0 and TSIG16 buffer locations hold the CAS multiframe alignment signal (MAS.1 through MAS.4), Extra bits (X.1 through X.4), and multiframe yellow alarm (MYEL) bits supplied from TSIGI.

Unused bits are reserved and should be written to 0.

7	6	5	4	3	2	1	0
—	—	—	—	TSIGn[3]	TSIGn[2]	TSIGn[1]	TSIGn[0]

		TSIG0 (E1)	TSIG16 (E1)
TSIGn.3.	Input Signaling A Bit	MAS.1	X.1
TSIGn.2.	Input Signaling B Bit	MAS.2	MYEL
TSIGn.1.	Input Signaling C Bit	MAS.3	X.3
TSIGn.0.	Input Signaling D Bit	MAS.4	X.4

140–15F—Transmit PCM Slip Buffer (TSLIP_LOn; n = 0 to 31)

7	6	5	4	3	2	1	0
TPCM[1]	TPCM[2]	TPCM[3]	TPCM[4]	TPCM[5]	TPCM[6]	TPCM[7]	TPCM[8]

TPCM[1] First bit

TPCM[2] Second bit

TPCM[3] Third bit

TPCM[4] Fourth bit

TPCM[5] Fifth bit

TPCM[6] Sixth bit

TPCM[7] Seventh bit

TPCM[8] Eighth bit received on TPCMI

160–17F—Transmit PCM Slip Buffer (TSLIP_HIn; n = 0 to 31)

7	6	5	4	3	2	1	0
TPCM[1]	TPCM[2]	TPCM[3]	TPCM[4]	TPCM[5]	TPCM[6]	TPCM[7]	TPCM[8]

TPCM[1] First bit

TPCM[2] Second bit

TPCM[3] Third bit

TPCM[4] Fourth bit

TPCM[5] Fifth bit

TPCM[6] Sixth bit

TPCM[7] Seventh bit

TPCM[8] Eighth bit received on TPCMI

180–19F—Receive Per-Channel Control (RPCn; n = 0 to 31)

7	6	5	4	3	2	1	0
RSIG_AB/ EMF-BIT	RIDLE	SIG_STK	RLOCAL	RSIGA	RSIGB	RSIGC	RSIGD

RSIG_AB/EMF-BIT AB Signaling (Per-Channel RSIG_AB [without DEBOUNCE])—In E1 mode, received signaling is placed into RSIGn as usual. However, RSIGO output duplicates the buffered AB bit value in the CD output bits, thus sending ABAB on RSIGO instead of ABCD. In T1 mode, RSIG_AB instructs the receiver to use available RSIGn buffer space to meet PUB43801 and TR-170. PUB43801 and TR-170 require three SF multiframes of receive signaling buffer storage before output. Every 24 frames, the received ABCD signaling value is transferred from the RSIGn input buffer space to RSIGn output buffer space, regardless of whether the receiver operates in SF, SLC, or ESF mode. Therefore, in SF mode, the ABCD value contains AB = AB(N-1) and CD = AB(N) from two multiframes. Since multiframe N-1 is the older sample, AB(N-1) replaces AB(N) in the event of signaling freeze. RSIGO and RPCMO signaling bit output values are always taken from the RSIGn output buffer, according to the RSB frame number.

AB Signaling (Per-Channel RSIG_AB [with DEBOUNCE])—Debounce is applicable only for T1 modes and affects the RSIGn input buffer update mechanism. This is accomplished by comparing, on a bit-by-bit basis, the present received input signaling bit value with the current buffered signaling bit values from two prior multiframes. If signaling from prior multiframe (N) differs from input, and input equals buffered value from 2 multiframes prior (N-1), signaling bit value from multiframe N is inverted when the input buffer is updated.

Sig Input	Buffer N, N-1	Update N, N-1	Notes
0	00	00	—
0	01	00	Change update
0	10	00	Debounce
0	11	01	—
1	00	10	—
1	01	11	Debounce
1	10	11	Change update
1	11	11	—

When RIDLE is active in an unassigned time slot defined to carry embedded F-bits, EMFBIT replaces all embedded F-bit outputs on RPCMO with the programmed value.

0 = normal ABCD and embedded F-bit throughput

1 = AB signaling and embedded F-bit replacement

RIDLE Time Slot Idle—When RIDLE is active, the incoming RX time slot data is only updated in the RSLIP_HIn buffer, and the RSB time slot data output is only extracted from RSLIP_LOn buffer. Thus, the processor can write an 8-bit idle code pattern in RSLIP_LOn buffer for output during the RSB time slot.

0 = no effect

1 = RSB time slot replaced by contents of RSLIP_LOn

SIG_STK Receive Signaling Stack—Selects whether changes detected in the ABCD signaling value are reported in signaling stack [addr 0DA]. Note that signaling for all time slots is continuously updated in RSIGn buffer, regardless of the SIG_STK setting.

0 = no effect

1 = signaling stack

RLOCAL Enable Local Signaling Output—Determines whether the RSIGO output signaling and RPCMO inserted signaling [INSERT; addr 0E0-0FF] are supplied from RSIGn output buffer or processor supplied local signaling from RSIGA–RSIGD.

0 = RSIGn buffer signaling

1 = RSIGA-RSIGD local signaling

RSIGA–RSIGD Local Receive Signaling—When RLOCAL is active, these 4 bits are inserted into RSIGO instead of the buffered signaling from RSIGn. If both RLOCAL and INSERT are active, these 4 bits are also inserted into RPCMO during system bus signaling frames.

0 = output signaling bit equals zero

1 = output signaling bit equals one

1A0–1BF—Receive Signaling Buffer (RSIGn; n = 0 to 31)

The Receive Signaling Buffer (RSIGn) contains all ABCD signaling inputs from all channels, regardless of whether signaling is active [SIG_STK; addr 180–19F]. RSIGn is not updated during signaling freeze conditions, or when the receive framer is configured in a non-signaling mode. Normal signaling buffer operation transfers ABCD input to ABCD output coincident with the D-bit update (in T1 mode) or coincident with receipt of respective channel's ABCD signaling during TS16 (in E1 mode). When DEBOUNCE is active, output signaling for active channels is updated coincident with the sampling of each input signaling bit and may cause the buffered output value to transition in the middle of the received multiframe.

7	6	5	4	3	2	1	0
RSIGn[7]	RSIGn[6]	RSIGn[5]	RSIGn[4]	RSIGn[3]	RSIGn[2]	RSIGn[1]	RSIGn[0]

RSIGn[7] Output Signaling A Bit

RSIGn[6] Output Signaling B Bit

RSIGn[5] Output Signaling C Bit

RSIGn[4] Output Signaling D Bit

		RSIG0 (E1)	RSIG16 (E1)
RSIGn[3].	Input Signaling A Bit	MAS.1	X.1
RSIGn[2].	Input Signaling B Bit	MAS.2	MYEL
RSIGn[1].	Input Signaling C Bit	MAS.3	X.3
RSIGn[0].	Input Signaling D Bit	MAS.4	X.4

1C0–1DF—Receive PCM Slip Buffer (RSLIP_LOn; n = 0 to 31)

7	6	5	4	3	2	1	0
RPCM[1]	RPCM[2]	RPCM[3]	RPCM[4]	RPCM[5]	RPCM[6]	RPCM[7]	RPCM[8]

RPCM[1] First bit

RPCM[2] Second bit

RPCM[3] Third bit

RPCM[4] Fourth bit

RPCM[5] Fifth bit

RPCM[6] Sixth bit

RPCM[7] Seventh bit

RPCM[8] Eighth bit received from receiver

1E0–1FF—Receive PCM Slip Buffer (RSLIP_HIn; n = 0 to 31)

7	6	5	4	3	2	1	0
RPCM[1]	RPCM[2]	RPCM[3]	RPCM[4]	RPCM[5]	RPCM[6]	RPCM[7]	RPCM[8]

RPCM[1] First bit

RPCM[2] Second bit

RPCM[3] Third bit

RPCM[4] Fourth bit

RPCM[5] Fifth bit

RPCM[6] Sixth bit

RPCM[7] Seventh bit

RPCM[8] Eighth bit received from receiver

3.17 Register Summary

Table 3-25. Global Control and Status Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
000	DID	R	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]
080	FCR	R/W	GRESET	—	—	—	—	ONESEC_IO	SBIMODE[1]	SBIMODE[0]
081	MIR	R	MIR[7]	MIR[6]	MIR[5]	MIR[4]	MIR[3]	MIR[2]	MIR[1]	MIR[0]
082	MIE	R/W	MIE[7]	MIE[6]	MIE[5]	MIE[4]	MIE[3]	MIE[2]	MIE[1]	MIE[0]
083	TEST	R/W	—	—	—	—	—	—	TEST	—

Table 3-26. Primary Control Register

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
001	CR0	R/W	RESET	—	—	RFRAME[3]	RFRAME[2]	RFRAME[1]	RFRAME[0]	TI/EIN

Table 3-27. Interrupt Control Register

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
003	IRR	R	ALARM1	ALARM2	ERROR	COUNT	TIMER	DL1	DL2	PATT

Table 3-28. Interrupt Status Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
004	ISR7	R	RMYEL	RYEL	RPDV	RAIS	RALOS	RLOS	RLOF	SIGFRZ
005	ISR6	R	LOOPDN	LOOPUP	TPDV	—	TLOC	—	TLOF	ONESEC
006	ISR5	R	TSLIP	RSLIP	—	—	CERR	SERR	MERR	FERR
007	ISR4	R	RLOF[4]	COFA[2]	SEF[2]	BERR[12]	FEBE[10]	LCV[16]	CRC[10]	FERR[12]
008	ISR3	R	TSIG	TMSYNC	TMF	TFRAME	RSIG	RMSYNC	RMF	RFRAME
009	ISR2	R	TBOP	RFULL1	RNEAR1	RMSG1	TDLERR1	TEMPTY1	TNEAR1	TMSG1
00A	ISR1	R	RBOP	RFULL2	RNEAR2	RMSG2	TDLERR2	TEMPTY2	TNEAR2	TMSG2
00B	ISR0	R	—	—	BSLIP	PSYNC	TCERR	TSERR	TMERR	TFERR

Table 3-29. Interrupt Enable Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
00C	IER7	R/W	RMYEL	RYEL	RPDV	RAIS	RALOS	RLOS	RLOF	SIGFRZ
00D	IER6	R/W	LOOPDN	LOOPUP	TPDV	—	TLOC	—	TLOF	ONESEC
00E	IER5	R/W	TSLIP	RSLIP	—	—	CERR	SERR	MERR	FERR
00F	IER4	R/W	LOF	COFA	SEF	BERR	FEBE	LCV	CRC	FERR
010	IER3	R/W	TSIG	TMSYNC	TMF	TFRAME	RSIG	RMSYNC	RMF	RFRAME
011	IER2	R/W	TBOP	RFULL1	RNEAR1	RMSG1	TDLERR1	TEMPTY1	TNEAR1	TMSG1
012	IER1	R/W	RBOP	RFULL2	RNEAR2	RMSG2	RDLERR2	TEMPTY2	TNEAR2	TMSG2
013	IER0	R/W	—	—	BSLIP	PSYNC	TCERR	TSERR	TMERR	TFERR

Table 3-30. Primary Control and Status Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
014	LOOP	R/W	—	—	—	—	PLOOP	LLOOP	FLOOP	—
015	DL3_TS	R/W	DL3EN	ODD	EVEN	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]
016	DL3_BIT	R/W	DL3_BIT[7]	DL3_BIT[6]	DL3_BIT[5]	DL3_BIT[4]	DL3_BIT[3]	DL3_BIT[2]	DL3_BIT[1]	DL3_BIT[0]
017	FSTAT	R	—	—	—	INVALID	FOUND	TIMEOUT	ACTIVE	RX/TXN
018	PIO	R/W	RMSYNC_EN	RDL_IO	TMSYNC_EN	TDL_IO	RFSYNC_IO	RMSYNC_IO	TFSYNC_IO	TMSYNC_IO
019	POE	R/W	—	—	TDL_OE	RDL_OE	INDY_OE	TCKO_OE	—	—
01A	CMUX	R/W	—	RSBCK	—	TSBCK	—	—	TXCLKI[1]	TXCLKI[0]
020	RAC	R/W	—	—	—	RAL_CON	—	—	—	—
021	RSTAT	R	—	—	ZCSUB	EXZ	BPV	—	—	—

Table 3-31. Serial Interface Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
022	SER_CTL	R/W	SER_A[6]	SER_A[5]	SER_A[4]	SER_A[3]	SER_A[2]	SER_A[1]	SER_A[0]	SER_RW
023	SER_DAT	R/W	SER_DAT[7]	SER_DAT[6]	SER_DAT[5]	SER_DAT[4]	SER_DAT[3]	SER_DAT[2]	SER_DAT[1]	SER_DAT[0]
024	SER_STAT	R/W	—	—	—	—	—	—	—	SER_DONE
025	SER_CONFIG	R/W	SER_CS	SER_CLK	—	—	—	—	—	SER_IER
026	RAM Test	R/W	RT[7]	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]

Table 3-32. Receiver Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
040	RCR0	R/W	RAMI	RABORT	RFORCE	RLOFD	RLOFC	RLOFB	RLOFA	RZCS
041	RPATT	R/W	—	—	RESEED	BSTART	FRAMED	ZLIMIT	RPATT[1]	RPATT[0]
042	RLB	R/W	—	—	—	—	DN_LEN[1]	DN_LEN[0]	UP_LEN[1]	UP_LEN[0]
043	LBA	R/W	LBA[1]	LBA[2]	LBA[3]	LBA[4]	LBA[5]	LBA[6]	LBA[7]	—
044	LBD	R/W	LBD[1]	LBD[2]	LBD[3]	LBD[4]	LBD[5]	LBD[6]	LBD[7]	—
045	RALM	R/W	—	—	FS_NFAS	EXZ_LCV	YEL_INTEG	RLOF_INTEG	RPCM_YEL	RPCM_AIS
046	LATCH	R/W	—	—	—	—	STOP_CNT	LATCH_CNT	LATCH_ERR	LATCH_ALM
047	ALM1	R	RMYEL	RYEL	—	RAIS	RALOS	RLOS	RLOF	SIGFRZ
048	ALM2	R	LOOPDN	LOOPUP	—	—	TLOC	—	TLOF	—
049	ALM3	R	—	RMAIS	SEF	SRED	MRED	FRED	LOF[1]	LOF[0]

Table 3-33. Performance Monitoring Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
050	FERR	R	FERR[7]	FERR[6]	FERR[5]	FERR[4]	FERR[3]	FERR[2]	FERR[1]	FERR[0]
051	FERR	R	0	0	0	0	FERR[11]	FERR[10]	FERR[9]	FERR[8]
052	CERR	R	CERR[7]	CERR[6]	CERR[5]	CERR[4]	CERR[3]	CERR[2]	CERR[1]	CERR[0]
053	CERR	R	0	0	0	0	0	0	CERR[9]	CERR[8]
054	LCV	R	LCV[7]	LCV[6]	LCV[5]	LCV[4]	LCV[3]	LCV[2]	LCV[1]	LCV[0]
055	LCV	R	LCV[15]	LCV[14]	LCV[13]	LCV[12]	LCV[11]	LCV[10]	LCV[9]	LCV[8]
056	FEBE	R	FEBE[7]	FEBE[6]	FEBE[5]	FEBE[4]	FEBE[3]	FEBE[2]	FEBE[1]	FEBE[0]
057	FEBE	R	0	0	0	0	0	0	FEBE[9]	FEBE[8]
058	BERR	R	BERR[7]	BERR[6]	BERR[5]	BERR[4]	BERR[3]	BERR[2]	BERR[1]	BERR[0]
059	BERR	R	0	0	0	0	BERR[11]	BERR[10]	BERR[9]	BERR[8]
05A	AERR	R	FRED[3]	FRED[2]	FRED[1]	FRED[0]	COFA[1]	COFA[0]	SEF[1]	SEF[0]

Table 3-34. Receive Sa-Byte Buffers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
05B	RSA4	R	RSA4[7]	RSA4[6]	RSA4[5]	RSA4[4]	RSA4[3]	RSA4[2]	RSA4[1]	RSA4[0]
05C	RSA5	R	RSA5[7]	RSA5[6]	RSA5[5]	RSA5[4]	RSA5[3]	RSA5[2]	RSA5[1]	RSA5[0]
05D	RSA6	R	RSA6[7]	RSA6[6]	RSA6[5]	RSA6[4]	RSA6[3]	RSA6[2]	RSA6[1]	RSA6[0]
05E	RSA7	R	RSA7[7]	RSA7[6]	RSA7[5]	RSA7[4]	RSA7[3]	RSA7[2]	RSA7[1]	RSA7[0]
05F	RSA8	R	RSA8[7]	RSA8[6]	RSA8[5]	RSA8[4]	RSA8[3]	RSA8[2]	RSA8[1]	RSA8[0]

Table 3-35. Transmitter Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
070	TCR0	R/W	—	—	—	—	TFRAME[3]	TFRAME[2]	TFRAME[1]	TFRAME[0]
071	TCR1	R/W	TNRZ	TABORT	TFORCE	TLOFC	TLOFB	TLOFA	TZCS[1]	TZCS[0]
072	TFRM	R/W	—	—	INS_MYEL	INS_YEL	INS_MF	INS_FE	INS_CRC	INS_FBIT
073	TERROR	R/W	TSERR	TMERR	TBERR	BSLIP	TCOFA	TCERR	TFERR	TVERR
074	TMAN	R/W	INS_SA[8]	INS_SA[7]	INS_SA[6]	INS_SA[5]	INS_SA[4]	FEBE_II	FEBE_I	TFEBE
075	TALM	R/W	—	AISCLK	AUTO_MYEL	AUTO_YEL	AUTO_AIS	TMYEL	TYEL	TAIS
076	TPATT	R/W	—	—	—	TPSTART	FRAMED	ZLIMIT	TPATT[1]	TPATT[0]
077	TLB	R/W	—	—	—	—	LB_LEN[1]	LB_LEN[0]	UNFRAMED	LBSTART
078	LBP	R/W	LBP[1]	LBP[2]	LBP[3]	LBP[4]	LBP[5]	LBP[6]	LBP[7]	—

Table 3-36. Transmit Sa-Byte Buffers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
07B	TSA4	R/W	TSA4[7]	TSA4[6]	TSA4[5]	TSA4[4]	TSA4[3]	TSA4[2]	TSA4[1]	TSA4[0]
07C	TSA5	R/W	TSA5[7]	TSA5[6]	TSA5[5]	TSA5[4]	TSA5[3]	TSA5[2]	TSA5[1]	TSA5[0]
07D	TSA6	R/W	TSA6[7]	TSA6[6]	TSA6[5]	TSA6[4]	TSA6[3]	TSA6[2]	TSA6[1]	TSA6[0]
07E	TSA7	R/W	TSA7[7]	TSA7[6]	TSA7[5]	TSA7[4]	TSA7[3]	TSA7[2]	TSA7[1]	TSA7[0]
07F	TSA8	R/W	TSA8[7]	TSA8[6]	TSA8[5]	TSA8[4]	TSA8[3]	TSA8[2]	TSA8[1]	TSA8[0]

Table 3-37. Bit-Oriented Protocol Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0A0	BOP	R/W	RBOP_START	RBOP_INTEG	RBOP_LEN[1]	RBOP_LEN[0]	TBOP_LEN[1]	TBOP_LEN[0]	TBOP_MODE[1]	TBOP_MODE[0]
0A1	TBOP	R/W	—	—	TBOP[5]	TBOP[4]	TBOP[3]	TBOP[2]	TBOP[1]	TBOP[0]
0A2	RBOP	R	RBOP_LOST	RBOP_VALID	RBOP[5]	RBOP[4]	RBOP[3]	RBOP[2]	RBOP[1]	RBOP[0]
0A3	BOP_STAT	R	TBOP_ACTIVE	RBOP_ACTIVE	—	—	—	—	—	—

Table 3-38. Data Link Registers *(1 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0A4	DL1_TS	R/W	DL1_TS[7]	DL1_TS[6]	DL1_TS[5]	DL1_TS[4]	DL1_TS[3]	DL1_TS[2]	DL1_TS[1]	DL1_TS[0]
0A5	DL1_BIT	R/W	DL1_BIT[7]	DL1_BIT[6]	DL1_BIT[5]	DL1_BIT[4]	DL1_BIT[3]	DL1_BIT[2]	DL1_BIT[1]	DL1_BIT[0]
0A6	DL1_CTL	R/W	—	—	—	TDL1_RPT	DL1[1]	DL1[0]	TDL1_EN	RDL1_EN
0A7	RDL1_FFC	R/W	MSG_FILL[1]	MSG_FILL[0]	FFC[5]	FFC[4]	FFC[3]	FFC[2]	FFC[1]	FFC[0]
0A8	RDL1	R	EOM[1]	EOM[0]	RDL1_CNT[5]	RDL1_CNT[4]	RDL1_CNT[3]	RDL1_CNT[2]	RDL1_CNT[1]	RDL1_CNT[0]
			RDL1[7]	RDL1[6]	RDL1[5]	RDL1[4]	RDL1[3]	RDL1[2]	RDL1[1]	RDL1[0]
0A9	RDL1_STAT	R	—	—	—	RMSG1	RSTAT1	RMPTY1	RNEAR1	RFULL1
0AA	PRM	R/W	AUTO_PRM	PRM_CR	PRM_R	PRM_U1	PRM_U2	PRM_SL	AUTO_SL	SEND_PRM
0AB	TDL1_FEC	R/W	—	—	FEC[5]	FEC[4]	FEC[3]	FEC[2]	FEC[1]	FEC[0]
0AC	TDL1_EOM	W	—	—	—	—	—	—	—	—
0AD	TDL1	W	TDL1[7]	TDL1[6]	TDL1[5]	TDL1[4]	TDL1[3]	TDL1[2]	TDL1[1]	TDL1[0]
0AE	TDL1_STAT	R	—	—	—	—	TMSG1	TMPTY1	TNEAR1	TFULL1
0AF	DL2_TS	R/W	DL2_TS[7]	DL2_TS[6]	DL2_TS[5]	DL2_TS[4]	DL2_TS[3]	DL2_TS[2]	DL2_TS[1]	DL2_TS[0]
0B0	DL2_BIT	R/W	DL2_BIT[7]	DL2_BIT[6]	DL2_BIT[5]	DL2_BIT[4]	DL2_BIT[3]	DL2_BIT[2]	DL2_BIT[1]	DL2_BIT[0]
0B1	DL2_CTL	R/W	—	—	—	TDL2_RPT	DL2[1]	DL2[0]	TDL2_EN	RDL2_EN
0B2	RDL2_FFC	R/W	MSG_FILL[1]	MSG_FILL[0]	FFC[5]	FFC[4]	FFC[3]	FFC[2]	FFC[1]	FFC[0]

Table 3-38. Data Link Registers (2 of 2)

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0B3	RDL2	R	EOM[1]	EOM[0]	RDL2_CNT[5]	RDL2_CNT[4]	RDL2_CNT[3]	RDL2_CNT[2]	RDL2_CNT[1]	RDL2_CNT[0]
			RDL2[7]	RDL2[6]	RDL2[5]	RDL2[4]	RDL2[3]	RDL2[2]	RDL2[1]	RDL2[0]
0B4	RDL2_STAT	R	—	—	—	RMSG2	RSTAT2	RMPTY2	RNEAR2	RFULL2
0B6	TDL2_FEC	R/W	—	—	FEC[5]	FEC[4]	FEC[3]	FEC[2]	FEC[1]	FEC[0]
0B7	TDL2_EOM	W	—	—	—	—	—	—	—	—
0B8	TDL2	R/W	TDL2[7]	TDL2[6]	TDL2[5]	TDL2[4]	TDL2[3]	TDL2[2]	TDL2[1]	TDL2[0]
0B9	TDL2_STAT	R	—	—	—	—	TMSG2	TMPTY2	TNEAR2	TFULL2
0BA	DL_TEST1	R/W	—	—	—	—	DL_TEST1[3]	DL_TEST1[2]	DL_TEST1[1]	DL_TEST1[0]
0BB	DL_TEST2	R/W	—	—	DL_TEST2[5]	DL_TEST2[4]	DL_TEST2[3]	DL_TEST2[2]	DL_TEST2[1]	DL_TEST2[0]
0BC	DL_TEST3	R/W	—	—	DL_TEST3[5]	DL_TEST3[4]	DL_TEST3[3]	DL_TEST3[2]	DL_TEST3[1]	DL_TEST3[0]
0BD	DL_TEST4	R/W	—	DL_TEST4[6]	DL_TEST4[5]	DL_TEST4[4]	DL_TEST4[3]	DL_TEST4[2]	DL_TEST4[1]	DL_TEST4[0]
0BE	DL_TEST5	R/W	—	DL_TEST5[6]	DL_TEST5[5]	DL_TEST5[4]	DL_TEST5[3]	DL_TEST5[2]	DL_TEST5[1]	DL_TEST5[0]

Table 3-39. System Bus Registers (1 of 2)

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0D0	SBI_CR	R/W	X2CLK	SBI_OE	EMF	EMBED	SBI[3]	SBI[2]	SBI[1]	SBI[0]
0D1	RSB_CR	R/W	BUS_RSB	SIG_OFF	RPCM_NEG	RSYN_NEG	BUS_FRZ	RSB_CTR	RSBI[1]	RSBI[0]
0D2	RSYNC_BIT	R/W	—	—	—	—	—	OFFSET[2]	OFFSET[1]	OFFSET[0]
0D3	RSYNC_TS	R/W	—	OFFSET[9]	OFFSET[8]	OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]
0D4	TSB_CR	R/W	BUS_TSB	TX_ALIGN	TPCM_NEG	TSYN_NEG	TSB_ALIGN	TSB_CTR	TSBI[1]	TSBI[0]
0D5	TSYNC_BIT	R/W	—	—	—	—	—	OFFSET[2]	OFFSET[1]	OFFSET[0]
0D6	TSYNC_TS	R/W	—	OFFSET[9]	OFFSET[8]	OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]
0D7	RSIG_CR	R/W	—	SET_RSIG	SET_SIG	UNICODE	DEBOUNCE	FRZ_OFF	FRZ_ON	THRU

Table 3-39. System Bus Registers *(2 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0D8	RSYNC_FRM	R/W	—	—	—	OFFSET[14]	OFFSET[13]	OFFSET[12]	OFFSET[11]	OFFSET[10]
0D9	SSTAT	R	TSDIR	TFSLIP	TUSLIP	TDLY	RSDIR	RFSLIP	RUSLIP	RDLY
0DA	STACK	R	WORD	MORE	—	CH[4]	CH[3]	CH[2]	CH[1]	CH[0]
			WORD	MORE	—	—	SIG_BITA	SIG_BITB	SIG_BITC	SIG_BITD
0DB	RPHASE	R	RDELAY[5]	RDELAY[4]	RDELAY[3]	RDELAY[2]	RDELAY[1]	RDELAY[0]	RSLIP_WR	RSLIP_RD
0DC	TPHASE	R	TDELAY[5]	TDELAY[4]	TDELAY[3]	TDELAY[2]	TDELAY[1]	TDELAY[0]	TSLIP_WR	TSLIP_RD
0DD	PERR	R	—	—	—	—	—	PERR_TPC	PERR_RPC	PERR_SBC
0E0–0FF	SBCn; n = 0 to 31	R/W	—	INSERT	SIG_LP	RLOOP	RINDO	TINDO	TSIG_AB	ASSIGN
100–11F	TPCn; n = 0 to 31	R/W	TB7ZS/EMFBIT	TLOOP	TIDLE	TLOCAL	TSIGA/TSIGO	TSIGB/RSIGO	TSIGC	TSIGD
120–13F	TSIGn; n = 00 to 31	R/W	—	—	—	—	TSIGn[3]	TSIGn[2]	TSIGn[1]	TSIGn[0]
140–15F	TSLIP_LOn; n = 0 to 31	R/W	TPCM[1]	TPCM[2]	TPCM[3]	TPCM[4]	TPCM[5]	TPCM[6]	TPCM[7]	TPCM[8]
160–17F	TSLIP–HIn; n = 0 to 31	R/W	TPCM[1]	TPCM[2]	TPCM[3]	TPCM[4]	TPCM[5]	TPCM[6]	TPCM[7]	TPCM[8]
180–19F	RPCn; n = 0 to 31	R/W	RSIG_AB/ EMFBIT	RIDLE	SIG_STK	RLOCAL	RSIGA	RSIGB	RSIGC	RSIGD
1A0–1BF	RSIGn; n = 0 to 31	R/W	RSIGn[7]	RSIGn[6]	RSIGn[5]	RSIGn[4]	RSIGn[3]	RSIGn[2]	RSIGn[1]	RSIGn[0]
1C0–1DF	RSLIP_LOn; n = 0 to 31	R/W	RPCM[1]	RPCM[2]	RPCM[3]	RPCM[4]	RPCM[5]	RPCM[6]	RPCM[7]	RPCM[8]
1E0–1FF	RSLIP_HIn; n = 0 to 31	R/W	RPCM[1]	RPCM[2]	RPCM[3]	RPCM[4]	RPCM[5]	RPCM[6]	RPCM[7]	RPCM[8]

4.0 Electrical/Mechanical Specifications

4.1 Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}	Power Supply (measured to GND)	–0.5	5.75	V
V_{GG}	High Voltage Reference	–0.5	5.75	V
ΔV_{DD}	Voltage Differential (between any 2 V_{DD} pins)	—	0.5	V
V_i	Constant Voltage on any Signal Pin	–1.0	V_{GG} + 0.5	V
ESD	Transient Voltage on any Signal Pin HBM rating CDM rating MMM rating	 — — —	 1.5 200 100	 kV V V
I_i	Constant Current on any Signal Pin	–10	+10	mA
LATCHUP	Transient Current on any Signal Pin	–200	+200	mA
T_s	Storage Temperature	–65	150	°C
T_j	Junction Temperature: (θ_{jA} x V_{DD} x I_{DD}) + T_{amb}	–40	125	°C
T_{vsol}	Vapor Phase Soldering Temperature (1 minute)	—	220	°C
θ_{jA}	Thermal Resistance (208 PQFP), Still Air	—	20	°C/W
θ_{jA}	Thermal Resistance (128 TQFP), Still Air	—	36	°C/W
θ_{jA}	Thermal Resistance (272 BGA), Still Air	—	29	°C/W
θ_{jA}	Thermal Resistance (318 BGA), Still Air	—	29	°C/W
θ_{jA}	Thermal Resistance (208 CABGA), Still Air	—	44.6	°C/W

NOTE(S): Stresses above those listed as Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DD}	Supply Voltage	3.135	3.3	3.465	V
V_{GG}	High Voltage Reference (5 V Tolerant Inputs)	4.75	5.0	5.25	V
V_{GG}	High Voltage Reference (Non-5 V Tolerant Inputs)	3.135	3.3	3.465	V
T_{amb}	Ambient Operating Temperature KPF Suffix EPF Suffix	 0 –40	 25 25	 70 85	 °C °C
V_{ih}	Input High Voltage	2.0	—	V_{GG} + 0.5	V
V_{il}	Input Low Voltage	–0.5	—	0.8	V
SYSCLK	SYSCLK Frequency	32.765	32.768	32.771	MHz

4.3 Electrical Characteristics

Table 4-3. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
I_{DD}	Supply Current (All signals and clocks operating at maximum frequency. All outputs loaded: 85 pF + 1 mA) CX28394 CX28398 CX28395	 — — —	 80 140 280	 90 155 310	 mA mA mA
I_{GG}	High Voltage Reference Current	—	—	1	mA
V_{ih}	Input High Voltage	2.0	—	V_{GG} + 0.5	V
V_{il}	Input Low Voltage	—	—	0.8	V
V_{oh}	Output High Voltage (I_{oh} = –2 mA)	2.4	—	—	V
V_{ol}	Output Low Voltage (I_{ol} = 2 mA)	—	—	0.4	V
I_{od}	Open Drain Output Current Sink	—	—	4	mA
I_{pr}	Resistive Pullup Current	40	100	500	µA
I_{I}	Input Leakage Current	–10	1	10	µA
I_{oz}	Three-state Leakage Current	–10	1	10	µA
C_{in}	Input Capacitance (f = 1MHz, Vin = 2.4V)	—	2	5	pF
C_{io}	I/O Capacitance (PIO, AD[7:0] pins)	—	5	10	pF
C_{out}	Output Capacitance	—	2	5	pF
C_{ld}	Capacitive Loading (Test Condition)	—	70	85	pF
I_{osc}	Short Circuit Output Current	37	50	160	mA

NOTE(S):

1. All typical values are at V_{DD} = 3.3 V and T_{amb} = 25 °C.
2. Maximum and minimum values are over V_{DD} = 3.3 V + 5% and T_{amb} = appropriate temperature range: KPF suffix (0 to 70 °C) or EPF suffix (–40 to 85 °C).

4.4 AC Characteristics

Table 4-4. Input Clock Timing

Symbol	Parameter	Minimum	Maximum	Units
1	MCLK Frequency	8.0	35.7	MHz
	SYSCLK Frequency	32.765	32.771	MHz
	RCKI, TCKI, ACKI Frequency	1.5	2.1	MHz
	RSBCKI, TSBCKI Frequency	1.5	8.2	MHz
	TCK Frequency	0	5.0	MHz
2	Clock Width High	0.4 x t(1)	0.6 x t(1)	ns
3	Clock Width Low	0.4 x t(1)	0.6 x t(1)	ns
4	Clock Rise Time	—	20	ns
5	Clock Fall Time	—	20	ns

Figure 4-1. Minimum Clock Pulse Widths

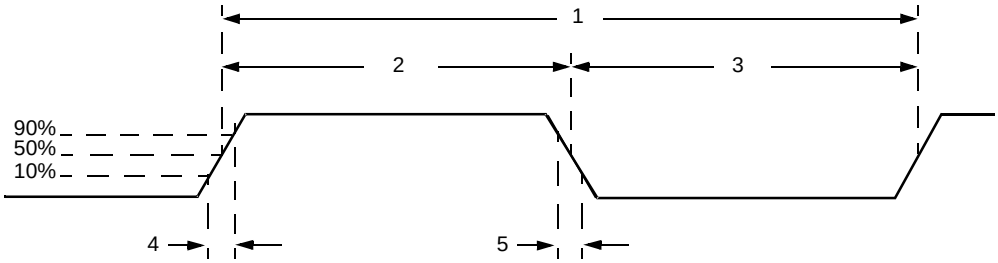


Table 4-5. Input Data Setup and Hold Timing

Symbol	Clock	Edge	Input Data	Minimum	Maximum	Units
1 (t_{setup})	MCLK	Rising	ONESEC	5	—	ns
			RST*	5	—	ns
	RCKI	Rising	RPOSI	2	—	ns
			RNEGI	2	—	ns
	TDLCKO	Falling	TDLI	6	—	ns
	RSBCKI	RSYN_NEG (addr 0D1)	RMSYNC	5	—	ns
			RFSYNC	5	—	ns
	TSBCKI TCKI(1)	TPCM_NEG (addr 0D4)	TPCMI	5	—	ns
			TSIGI	5	—	ns
		TSYN_NEG (addr 0D4)	TFSYNC	5	—	ns
			TMSYNC	5	—	ns
2 (t_{hold})	MCLK	Rising	ONESEC	5	—	ns
			RST*	5	—	ns
	RCKI	Rising	RPOSI	3	—	ns
			RNEGI	3	—	ns
	TDLCKO	Falling	TDLI	2	—	ns
	RSBCKI	RSYN_NEG (addr 0D1)	RMSYNC	5	—	ns
			RFSYNC	5	—	ns
	TSBCKI TCKI(1)	TPCM_NEG (addr 0D4)	TPCMI	2	—	ns
			TSIGI	5	—	ns
		TSYN_NEG (addr 0D4)	TFSYNC(2)	2	—	ns
			TMSYNC	2	—	ns

NOTE(S):
(1) If the TSLIP buffer is bypassed (TSB_CR; addr OD4), TCKI is used; otherwise, TSBCKI is used.

Table 4-6. Output Data Delay Timing

Symbol	Clock	Edge	Output Data	Minimum	Maximum	Units
1 (t_{delay})	MCLK	Rising	ONESEC	0	10	ns
			INTR	0	10	ns
	TCKI or ACKI	—	TCKO	0	15	ns
		—	TDLCKO	0	20	ns
		Rising	TNRZO	0	28	ns
			MSYNCO	0	28	ns
	TCKO	Rising	TPOSO	0	10	ns
			TNEGO	0	10	ns
	RDLCKO	Rising	RDLO	0	20	ns
	RSBCKI	RPCM_NEG (addr 0D1)	RPCMO	0	20	ns
			RSIGO	0	10	ns
			RINDO	0	20	ns
			SIGFRZ	0	20	ns
		RSYN_NEG (addr 0D1)	RFSYNC	0	10	ns
			RMSYNC	0	10	ns
	TSBCKI TCKI(1)	TPCM_NEG (addr 0D4)	TINDO	0	10	ns
		TSYN_NEG (addr 0D4)	TFSYNC	0	10	ns
			TMSYNC	0	10	ns

NOTE(S):
(1) If the TSLIP buffer is bypassed (TSB_CR; addr OD4), TCKI is used; otherwise, TSBCKI is used.

Table 4-7. One-Second Input/Output Timing

Symbol	Parameter	Minimum	Maximum	Units
1	Input Pulse Width	1/MCLK	1 second – 125 µs	As shown
2	Output Pulse Width	125	250	µs

Figure 4-2. Input Data Setup/Hold Timing

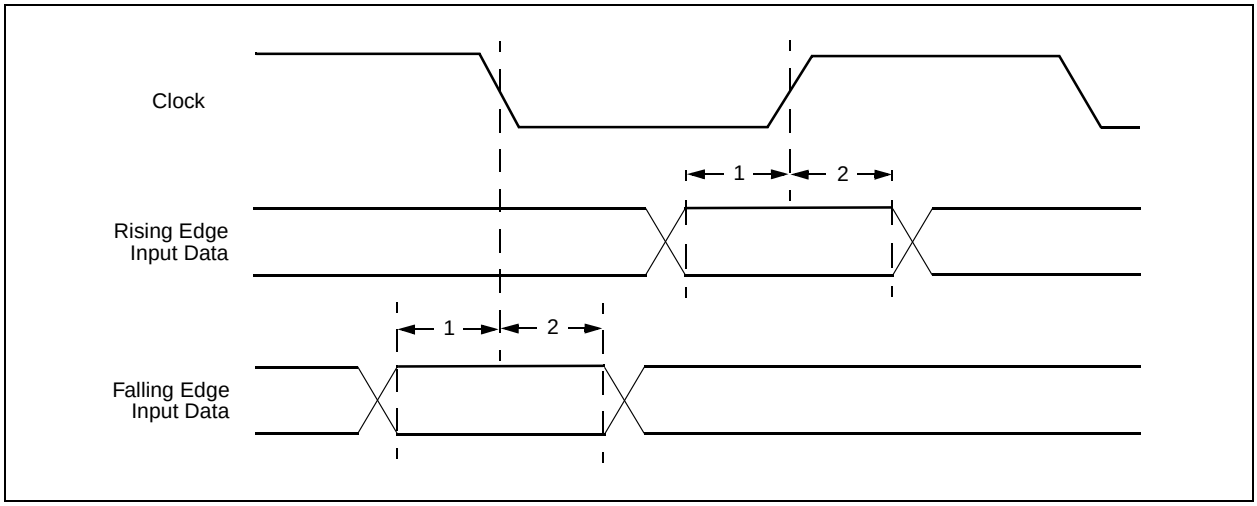


Figure 4-3. Output Data Delay Timing

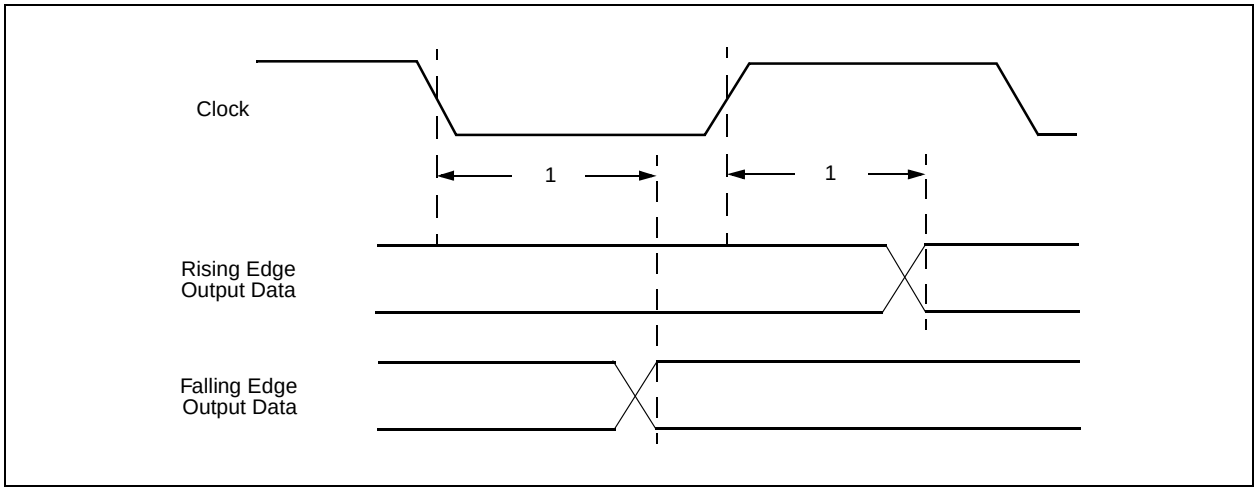
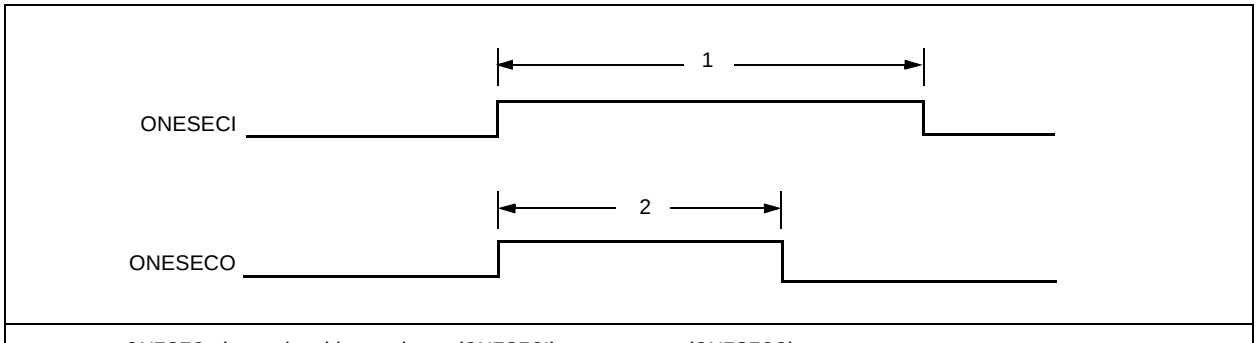


Figure 4-4. One-Second Input/Output Timing



NOTE(S): ONESEC pin can be either an input (ONESECI) or an output (ONESECO).

4.5 MPU Interface Timing

Figure 4-5. Motorola Asynchronous Read Cycle

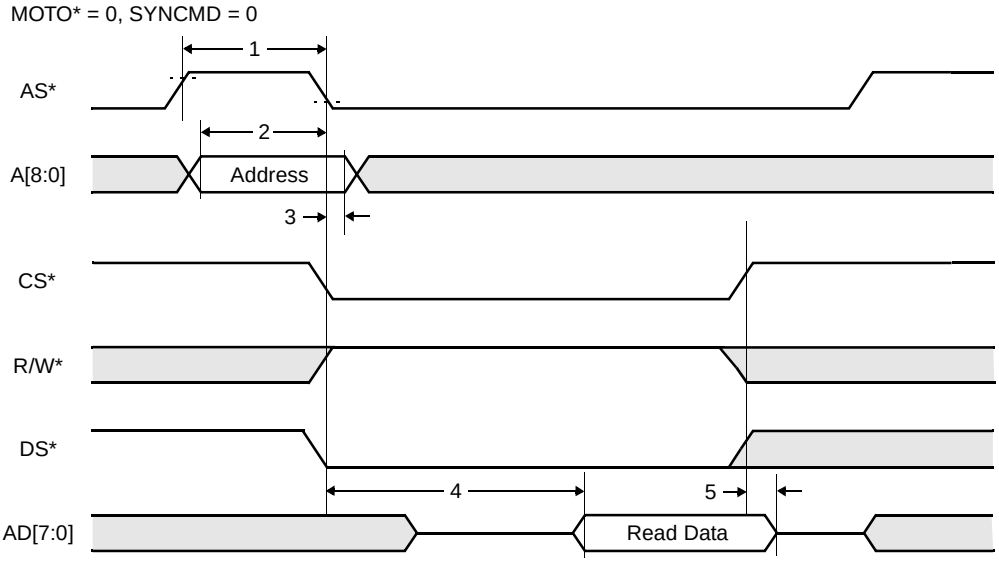


Table 4-8. Motorola Asynchronous Read Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	AS* high pulse width	15	—	ns
2	A[8:0] Address setup to AS* low	5	—	ns
3	A[8:0] Address hold after AS* low	10	—	ns
4	CS* low and R/W* high, and DS* low to AD[7:0] valid	—	80	ns
5	CS* high and DS* high, and R/W* low to AD[7:0] invalid/three-state	5	20	ns

Figure 4-6. Motorola Asynchronous Write Cycle

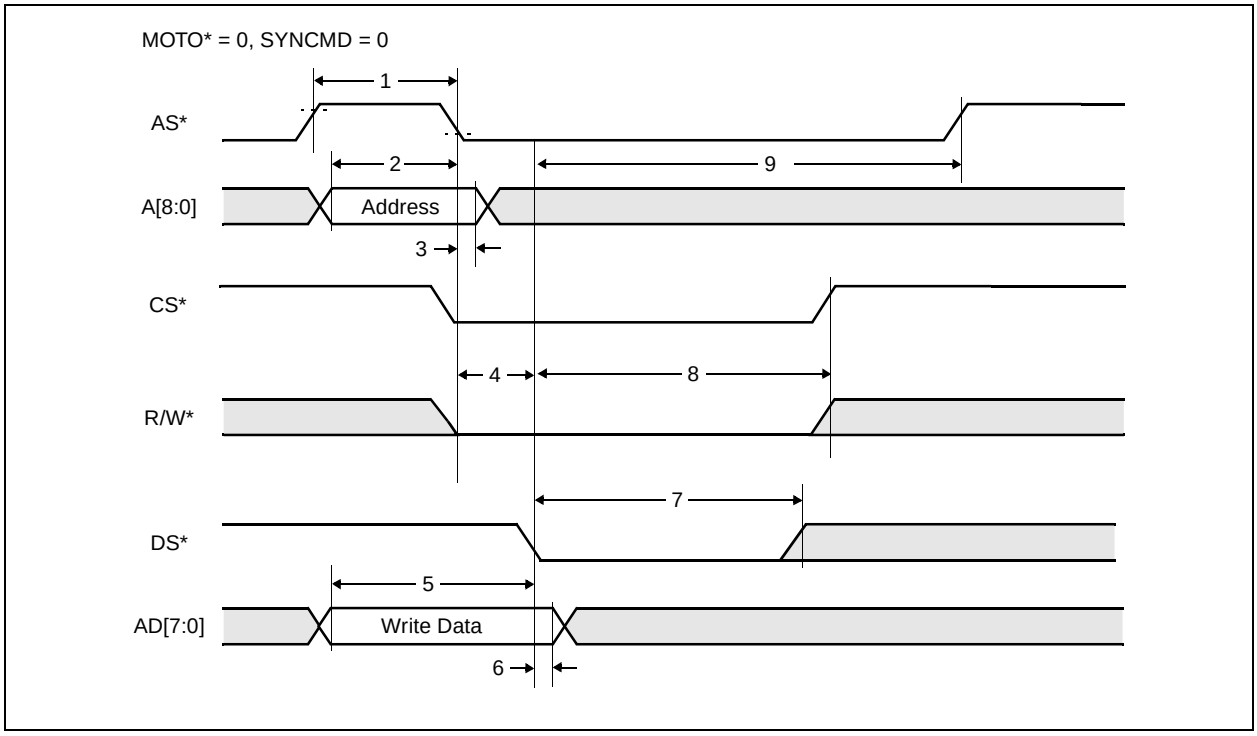


Table 4-9. Motorola Asynchronous Write Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	AS* high pulse width	15	—	ns
2	A[8:0] Address setup to AS* low	5	—	ns
3	A[8:0] Address hold after AS* low	2	—	ns
4	CS* low and R/W* low to DS* low	5	—	ns
5	AD[7:0] setup to DS* low	0	—	ns
6	AD[7:0] hold after DS* low	15	—	ns
7	DS* low pulse width	38	—	ns
8	CS*, R/W* hold after DS* low	38	—	ns
9	DS* low to AS* high	70	—	ns

Figure 4-7. Intel Asynchronous Read Cycle

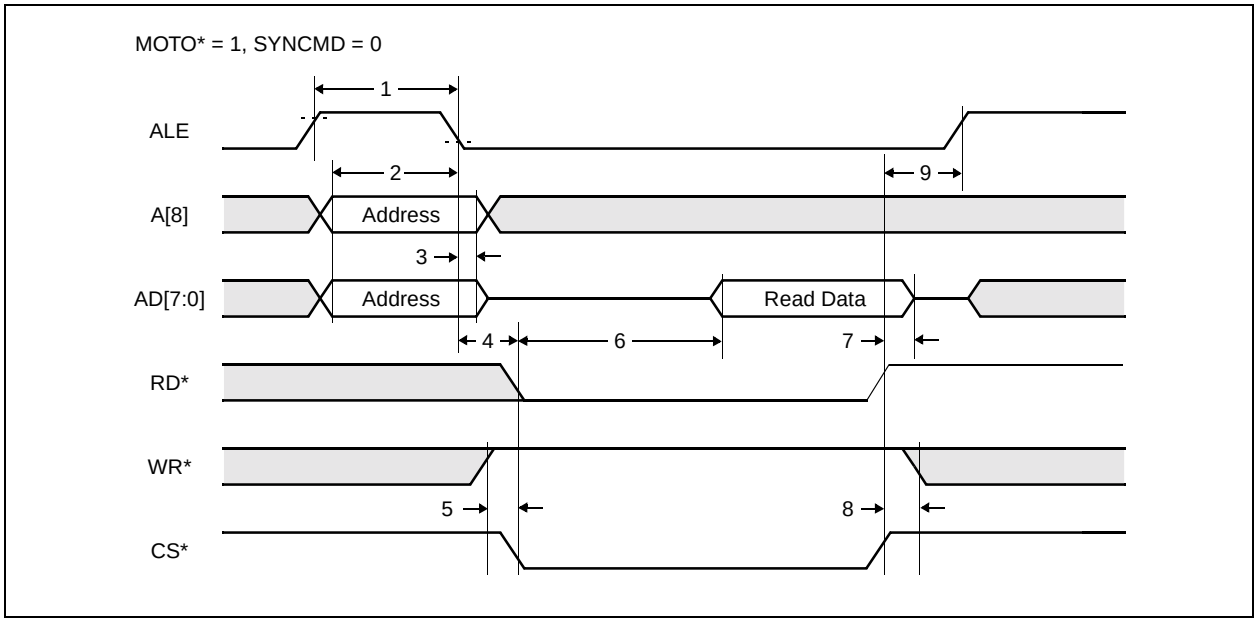


Table 4-10. Intel Asynchronous Read Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	2	—	ns
3	A[8], AD[7:0] Address hold after ALE low	5	—	ns
4	ALE low to RD* and CS* both low	0	—	ns
5	WR* high setup to RD* and CS* both low	0	—	ns
6	RD* and CS* both low to AD[7:0] valid	—	80	ns
7	RD* or CS* high to AD[7:0] invalid/three-state	0	25	ns
8	WR* high hold after RD* or CS* high	0	—	ns
9	RD* or CS* high to next ALE	0	—	ns

Figure 4-8. Intel Asynchronous Write Cycle

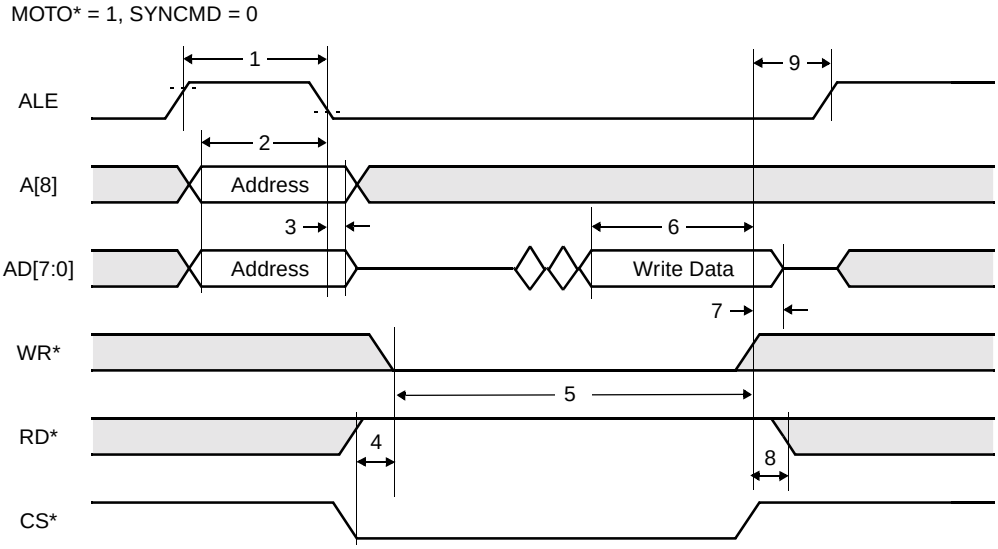


Table 4-11. Intel Asynchronous Write Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	2	—	ns
3	A[8], AD[7:0] Address hold after ALE low	5	—	ns
4	CS*, RD* setup to WR* low	0	—	ns
5	WR* pulse width low	20	—	ns
6	AD[7:0] input data setup to WR* or CS* high	2	—	ns
7	AD[7:0] input data hold after WR* or CS* high	10	—	ns
8	RD* hold after WR* or CS* high	0	—	ns
9	End write cycle to next ALE high	55	—	ns

Figure 4-9. Motorola Synchronous Read Cycle

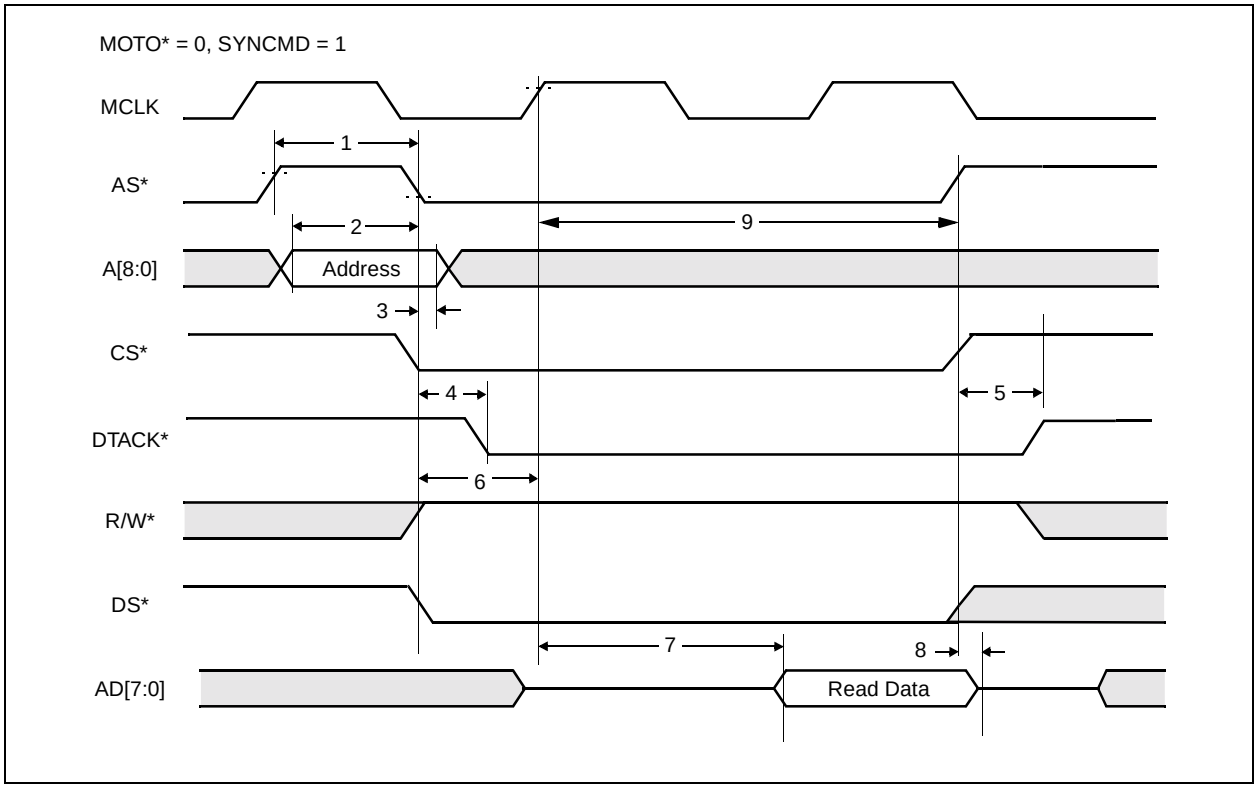


Table 4-12. Motorola Synchronous Read Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	AS* high pulse width	15	—	ns
2	A[8:0] Address setup to AS* low	2	—	ns
3	A[8:0] Address hold after AS* low	2	—	ns
4	AS* and CS* low to DTACK* low	0	10	ns
5	AS* or CS* high to DTACK* high	0	10	ns
6	AS*, DS*, CS*, R/W* setup to MCLK high	15	—	ns
7	DS* sampled low to AD[7:0] valid	—	0.5/MCLK +20	ns
8	CS* or DS* high to AD[7:0] invalid/three-state	0	30	ns
9	MCLK high to AS* high	1/MCLK + 12	—	ns

Figure 4-10. Motorola Synchronous Write Cycle

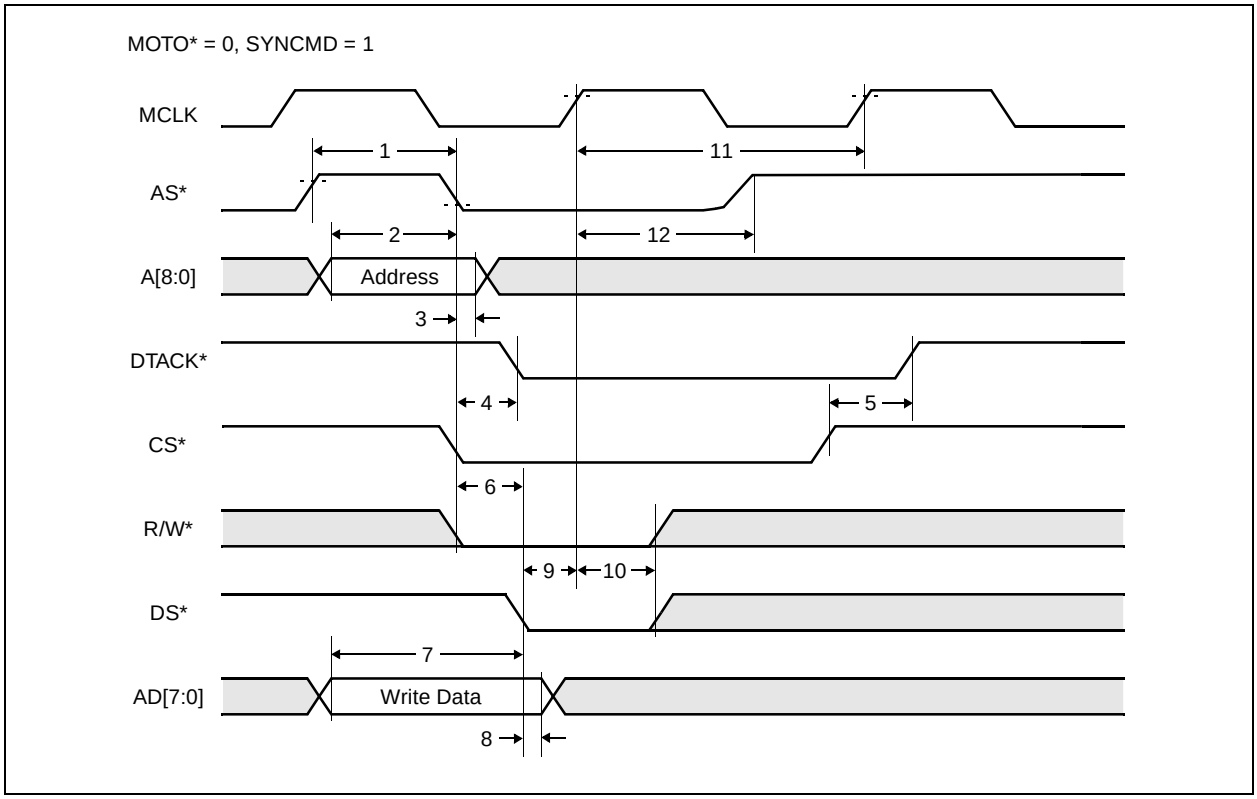


Table 4-13. Motorola Synchronous Write Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	AS* high pulse width	15	—	ns
2	A[8:0] Address setup to AS* low	5	—	ns
3	A[8:0] Address hold after AS* low	2	—	ns
4	AS* and CS* low to DTACK* low	0	10	ns
5	AS* or CS* high to DTACK* high	0	10	ns
6	CS* and R/W* low to DS* low	2	—	ns
7	AD[7:0] setup to DS* low	2	—	ns
8	AD[7:0] hold after DS* low	5	—	ns
9	DS* setup to MCLK high	2	—	ns
10	DS* hold after MCLK high	5	—	ns
11	DS* sampled low to data latch (internal)	—	1/MCLK+15	ns
12	DS* sampled low to AS* high	1/2 MCLK + 15	—	ns

Figure 4-11. Intel Synchronous Read Cycle

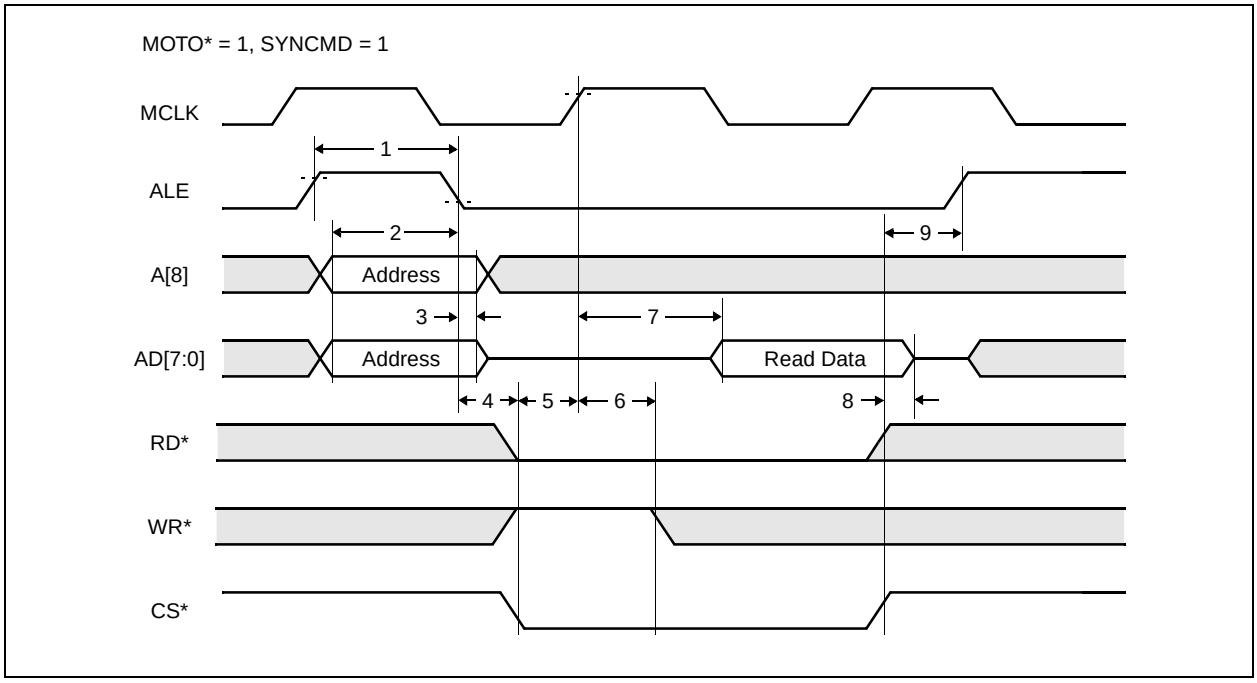


Table 4-14. Intel Synchronous Read Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	2	—	ns
3	A[8], AD[7:0] Address hold after ALE low	5	—	ns
4	ALE low to RD* and CS* both low	5	—	ns
5	RD*, CS*, WR* setup to MCLK high (Start RD cycle)	3	—	ns
6	RD*, CS*, WR* hold after MCLK high	5	—	ns
7	Start RD* cycle to AD[7:0] valid	—	(1)	ns
8	RD* or CS* high to AD[7:0] invalid/three-state	0	25	ns
9	End RD cycle to next ALE high	0	—	ns

NOTE(S):
(1) Parameter 7 equals 40 ns or 1/2* MCLK + 17 ns, whichever is greater.

Figure 4-12. Intel Synchronous Write Cycle

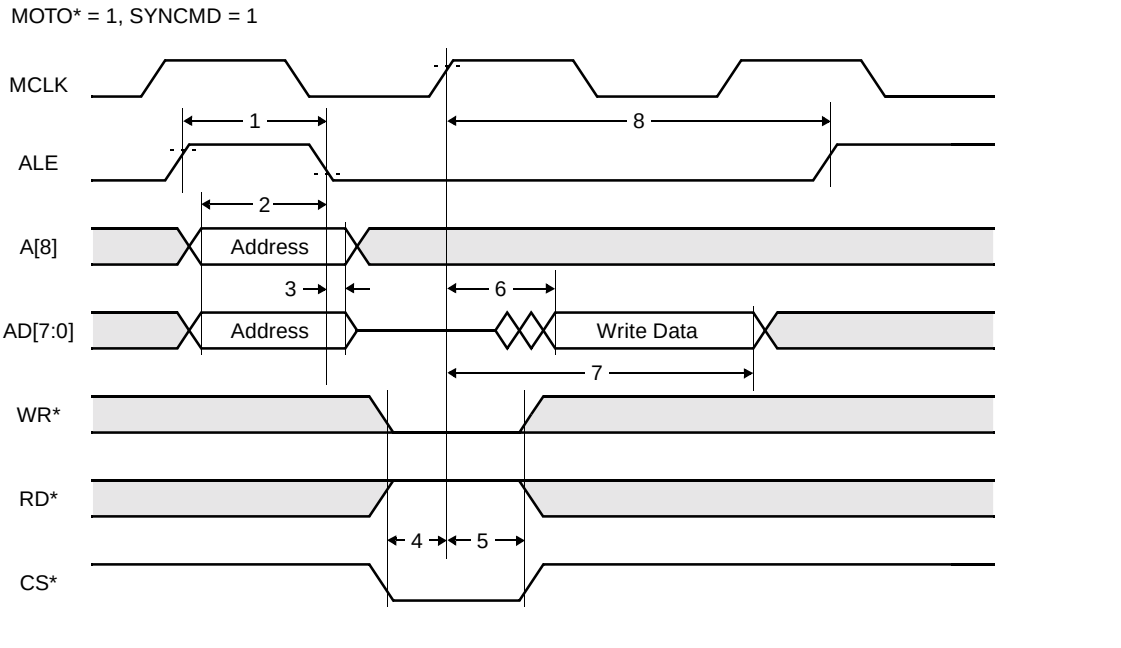


Table 4-15. Intel Synchronous Write Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	2	—	ns
3	A[8], AD[7:0] Address hold after ALE low	5	—	ns
4	WR*,RD*,CS* setup to MCLK high (start WR cycle)	2	—	ns
5	WR*,RD*,CS* hold after MCLK high	5	—	ns
6	Start WR* cycle to AD[7:0] input data valid	—	1/MCLK–10	ns
7	AD[7:0] input data hold after Start WR cycle	1/MCLK+9	—	ns
8	Start WR cycle to next ALE high	1/MCLK+10	—	ns

Figure 4-13. Serial Control Port Timing

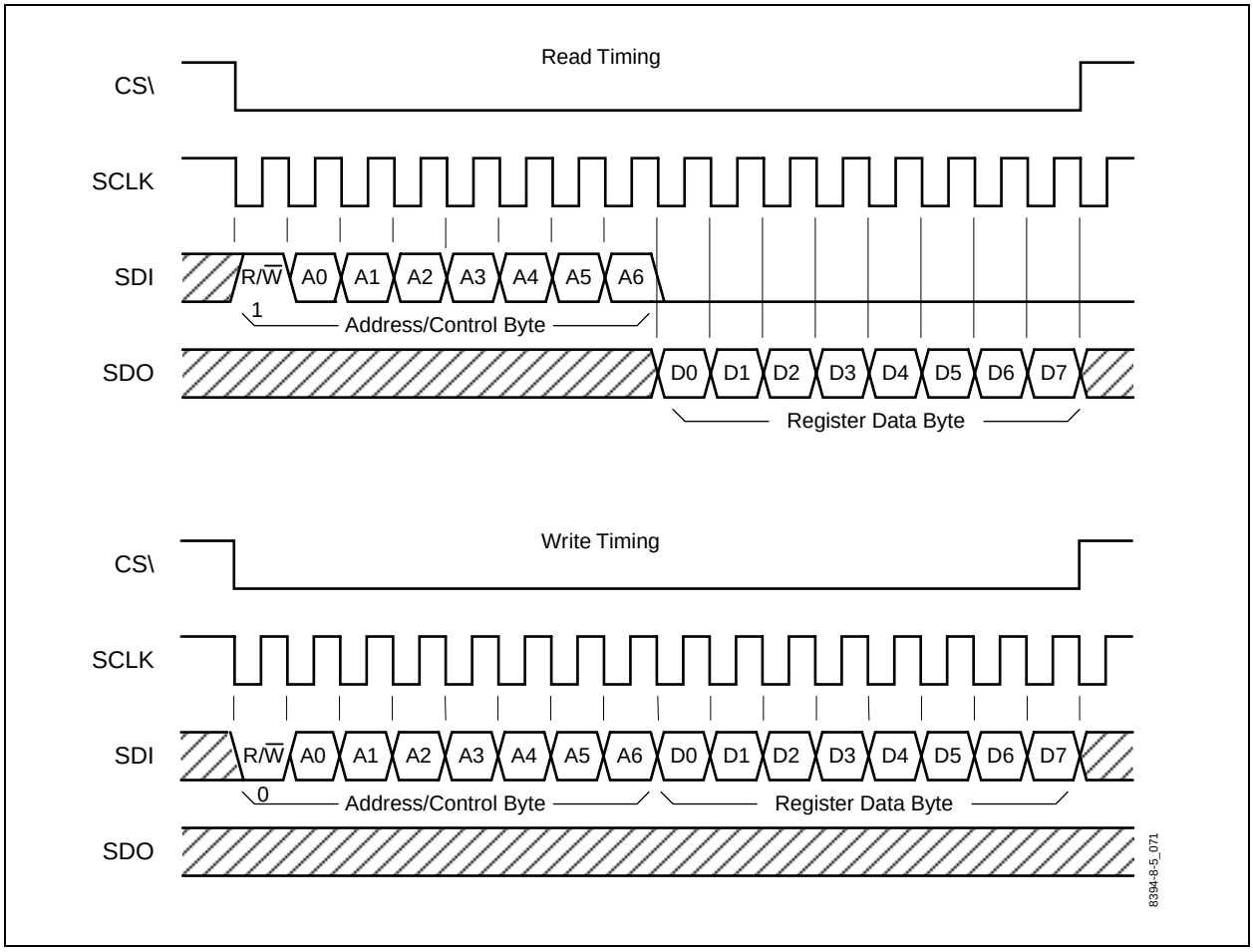


Figure 4-14. Serial Control Port Write Timing

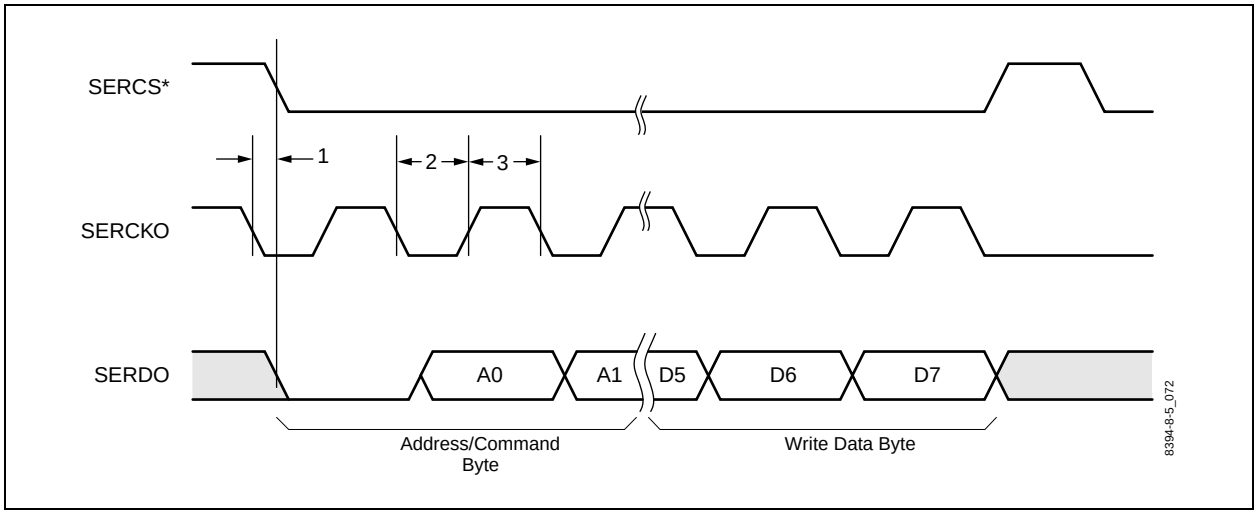


Figure 4-15. Serial Control Port Read Timing

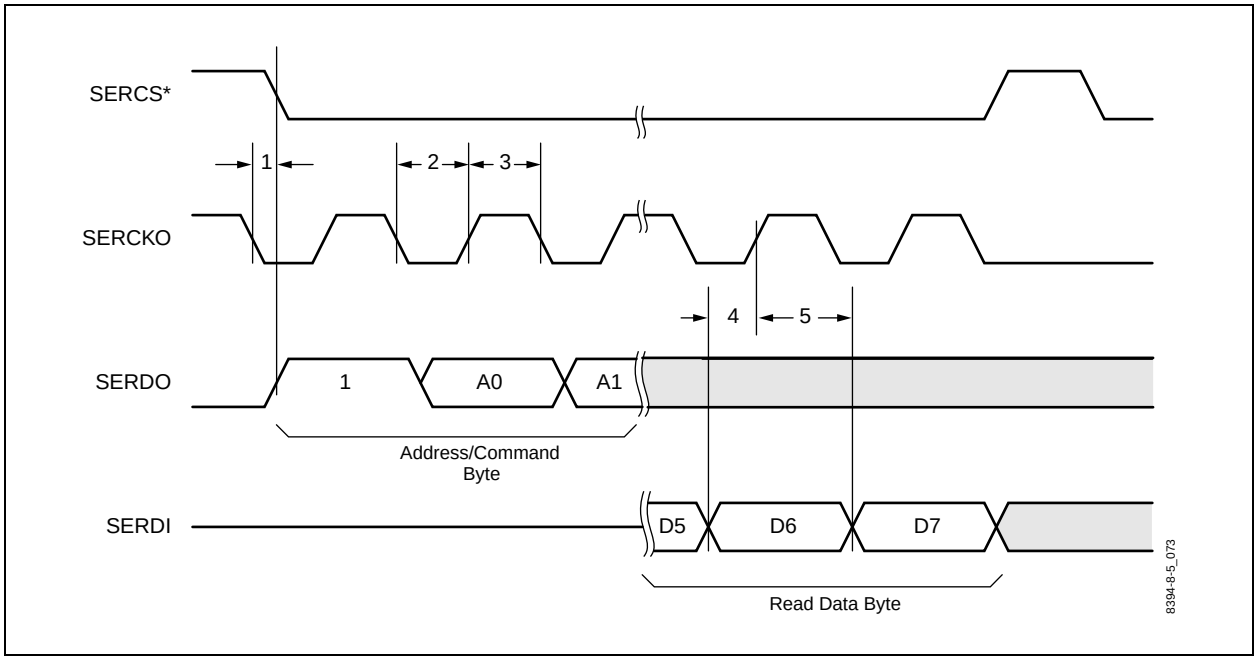
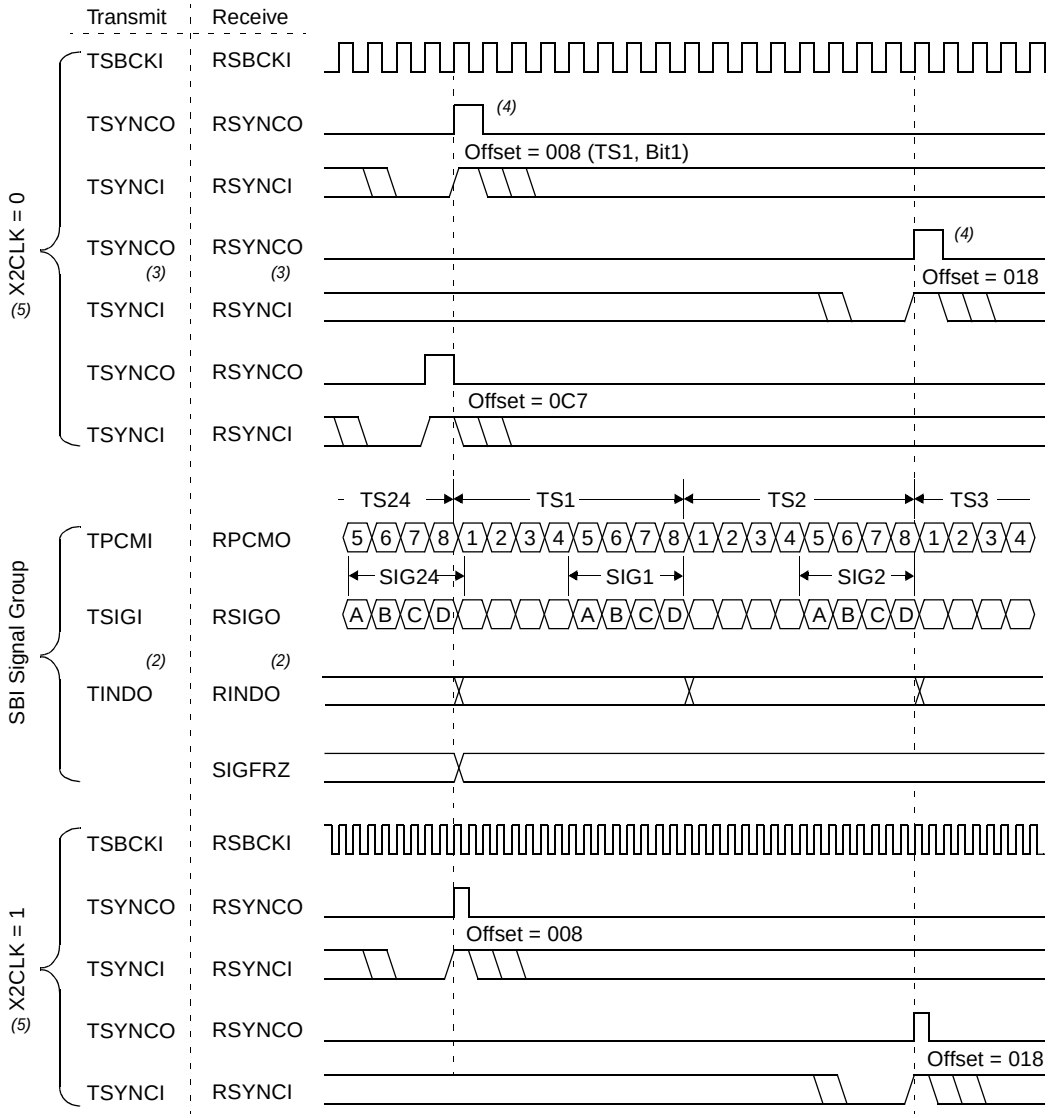


Table 4-16. Host Serial Port Timing

Symbol	Parameter	Minimum	Maximum	Units
1	SERCKO Falling Edge to SERCS* and SERDO	10	—	ns
2, 3	SERCKO Duty Cycle	40	60	%
2, 3	SERCKO Frequency (Programmable)	1.024	8.192	MHz
4	SERDI to SERCKO Rising Edge Setup Time	10	—	ns
5	SERCKO Rising Edge to SERDI Hold Time	5	—	ns
—	Rise/Fall Time (10% to 90%) SERCKO, SERDI, SERDO	—	20	ns

4.6 System Bus Interface (SBI) Timing

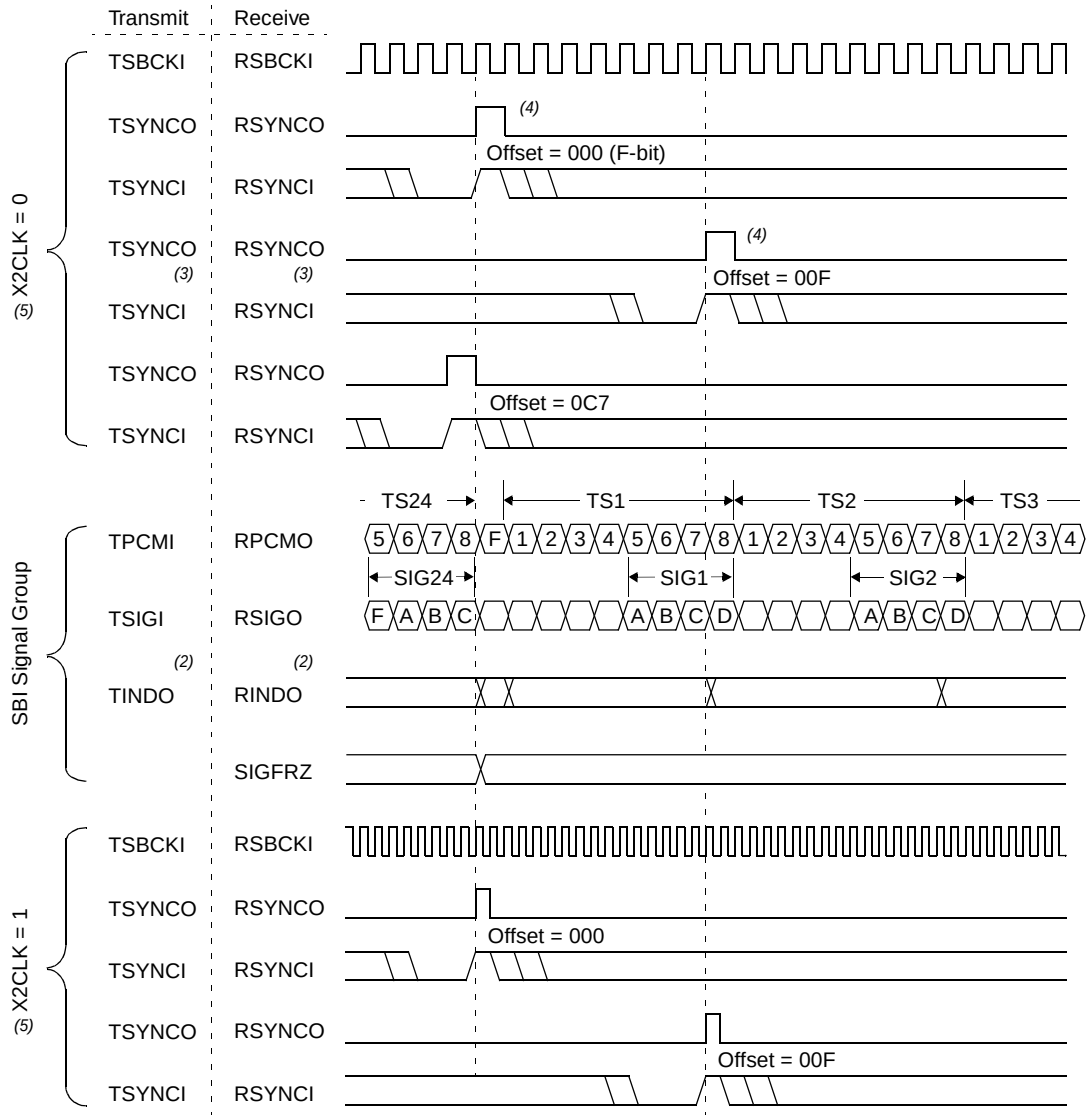
Figure 4-16. SBI Timing—1536K Mode[1]



NOTE(S):

(1) Rising edge outputs and falling edge inputs shown. Refer to Table 4-21 for other edge combinations.
(2) RINDO/TINDO programmed high or low on a per-time slot basis (SBCn; addr 0E0-0FF).
(3) TSYNC/RSYNC represents frame (TFSYNC/RFSYNC) and multiframe (TMSYNC/RMSYNC) offset.
(4) Multiple offset values shown for illustration, refer to OFFSET controls (addr 0D2-0D3, 0D5-0D6).
(5) X2CLK control bit located in SBI_CR (addr 0D0).

Figure 4-17. SBI Timing—1544K Mode(1)



NOTE(S):

(1) Rising edge outputs and falling edge inputs shown. Refer to Table 4-21 for other edge combinations.

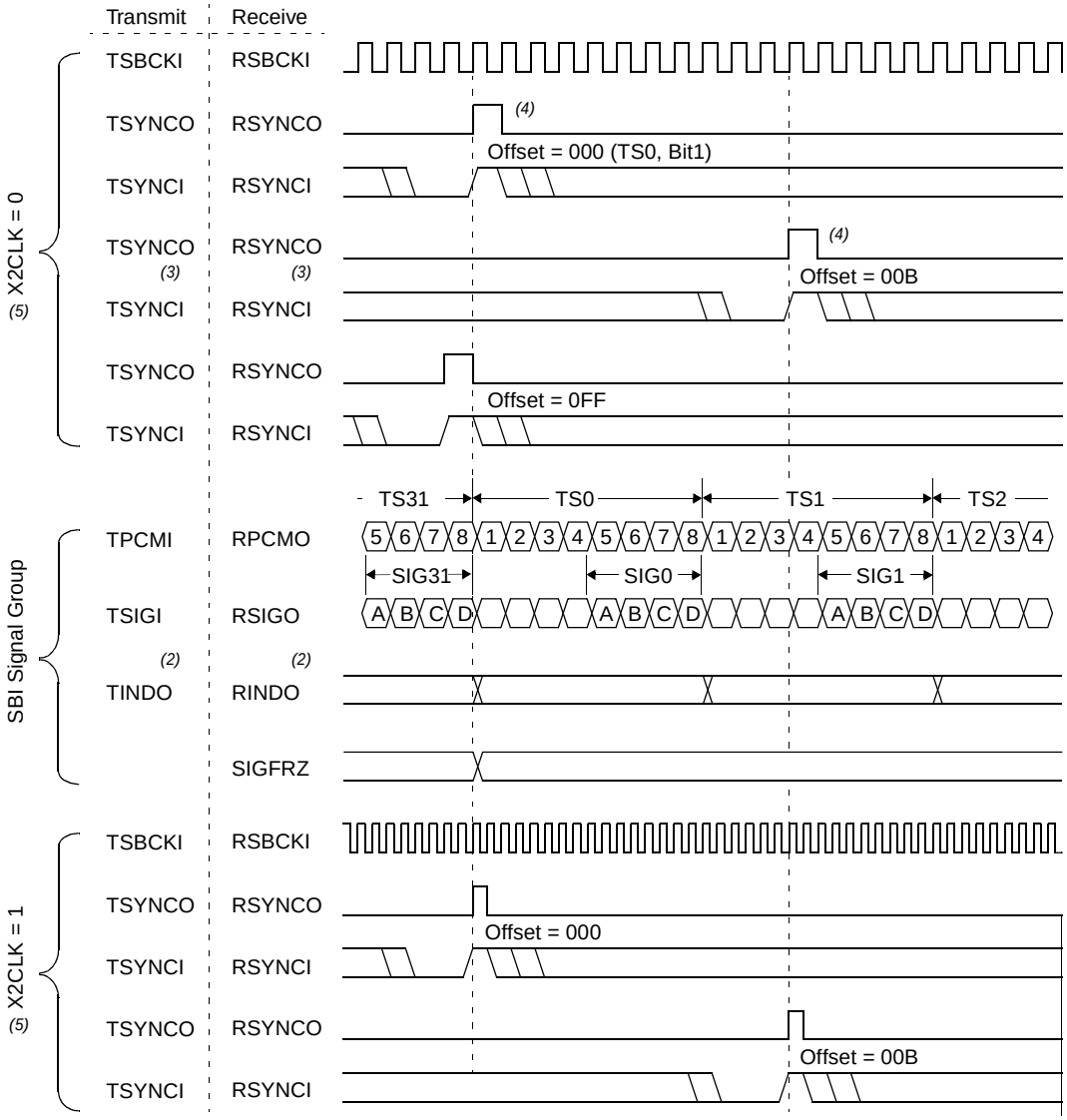
(2) RINDO/TINDO programmed high or low during F-bit (SBC0; addr 0E0).

(3) TSYNC/RSYNC represents frame (TFSYNC/RFSYNC) and multiframe (TMSYNC/RMSYNC) offset.

(4) Multiple offset values shown for illustration, refer to OFFSET controls (addr 0D2-0D3, 0D5-0D6).

(5) X2CLK control bit located in SBI_CR (addr 0D0).

Figure 4-18. SBI Timing—2048K Mode[1]



NOTE(S):

(1) Rising edge outputs and falling edge inputs shown. Refer to Table 4-21 for other edge combinations.

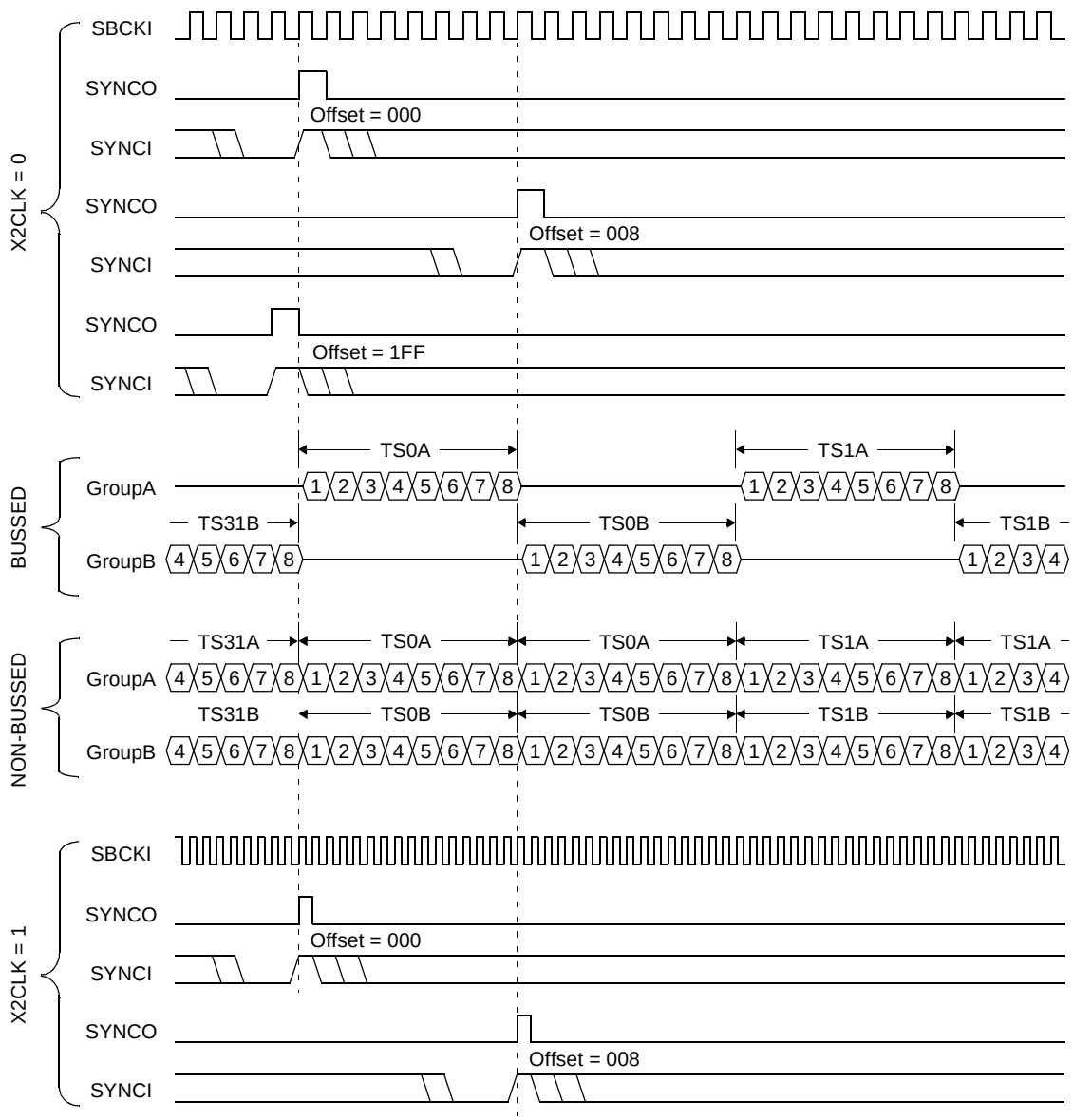
(2) RINDO/TINDO programmed high or low on a per-time slot basis (SBCn; addr 0E0-0FF).

(3) TSYNC/RSYNC represents frame (TFSYNC/RFSYNC) and multiframe (TMSYNC/RMSYNC) offset.

(4) Multiple offset values shown for illustration, refer to OFFSET controls (addr 0D2-0D3, 0D5-0D6).

(5) X2CLK control bit located in SBI_CR (addr 0D0).

Figure 4-19. SBI Timing—4096K Mode[1],[5]



NOTE(S):

1. Rising edge outputs and falling edge inputs shown. Refer to Table 4-21 for other edge combinations.
5. BUSSED or NON-BUSSED signal group controls located in BUS_RSB, BUS_FRZ (addr 0D1) and BUS_TSB (addr 0D4).

Figure 4-20. SBI Timing—8192K Mode

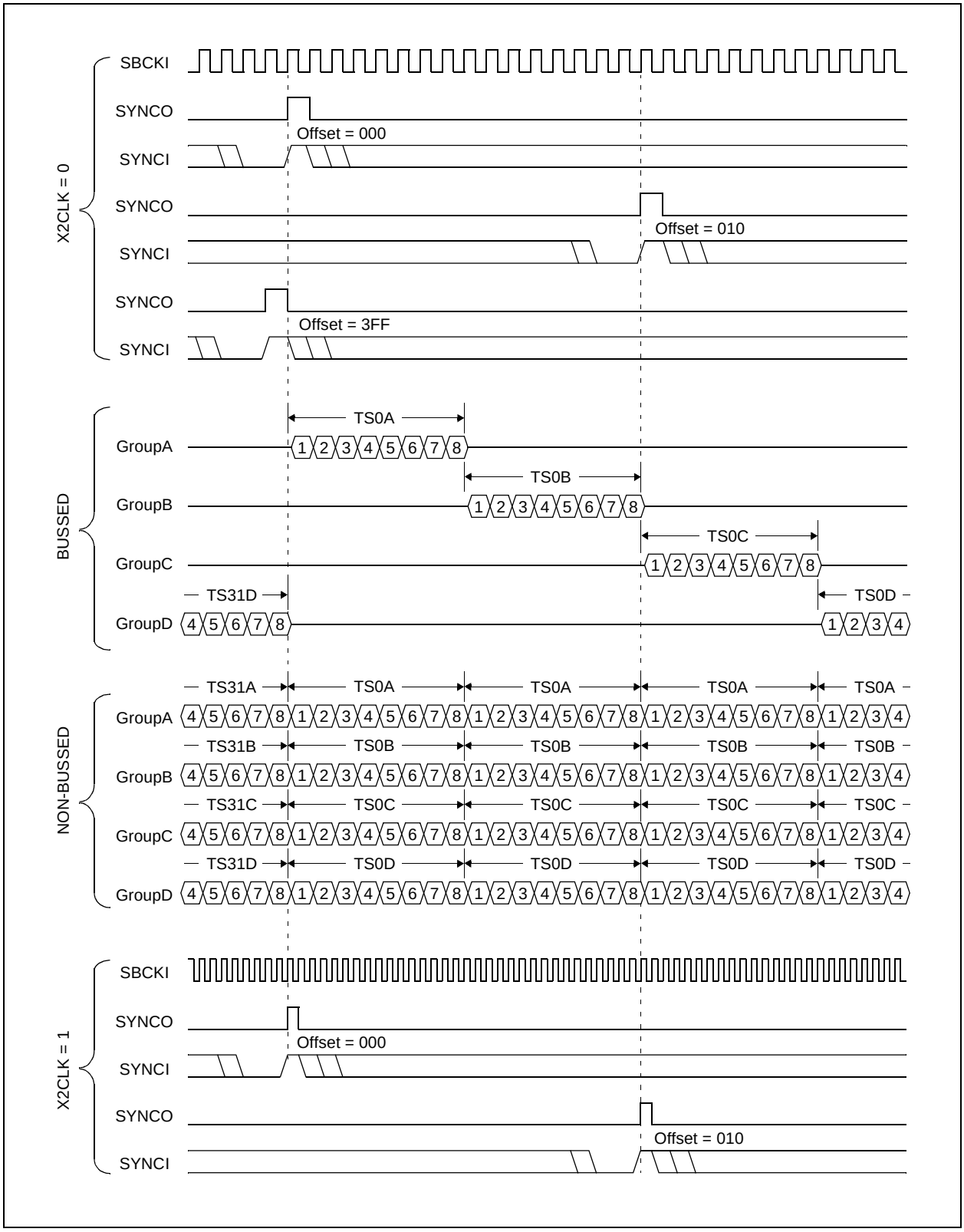
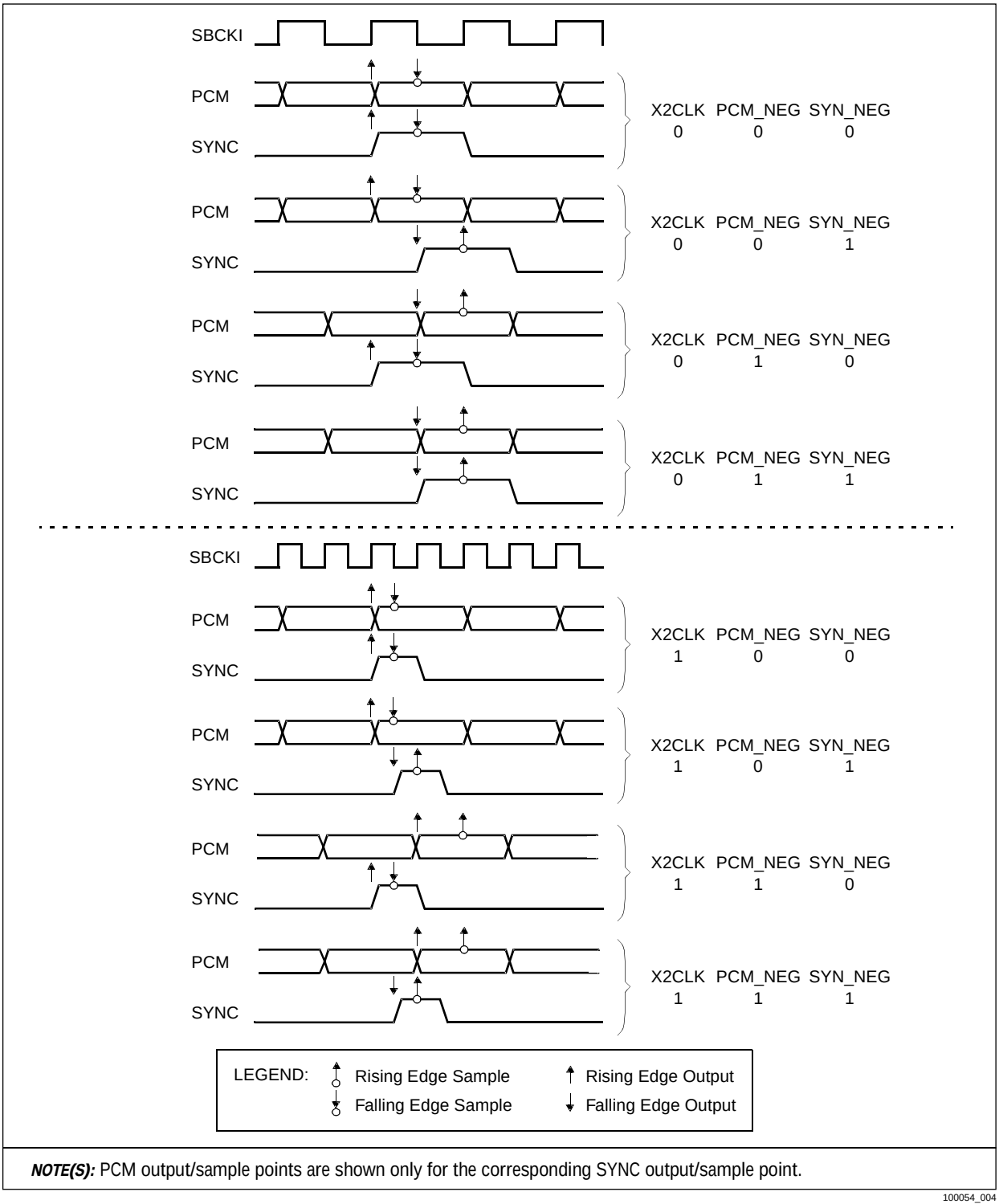


Figure 4-21. SBI Timing—Eight Clock Edge Combinations (Applicable to Any SBI Mode)



NOTE(S): PCM output/sample points are shown only for the corresponding SYNC output/sample point.

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4.7 JTAG Interface Timing

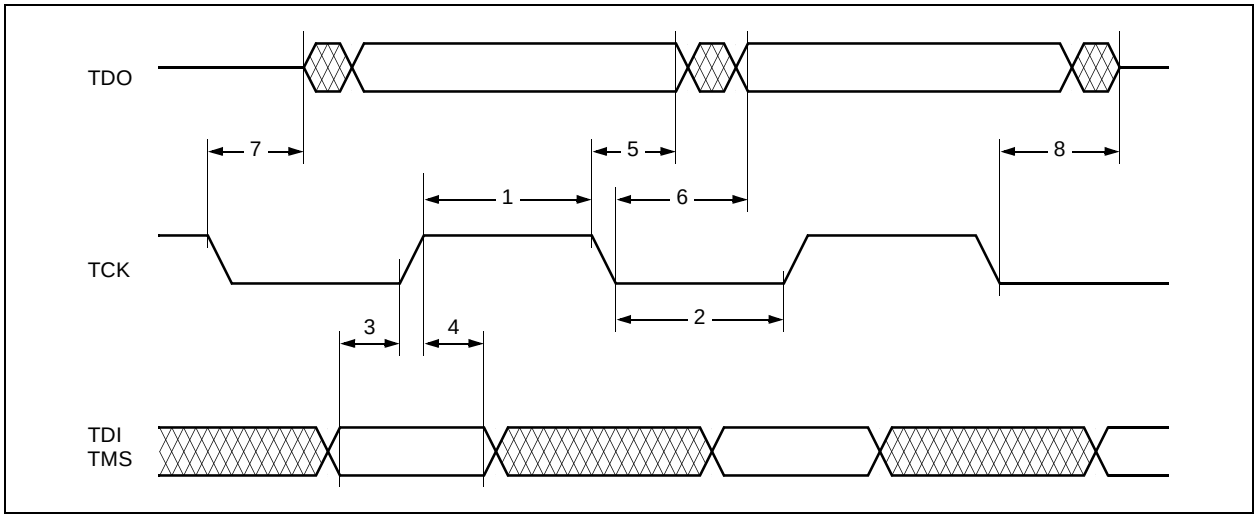
Table 4-17. Test and Diagnostic Interface Timing Requirements

Symbol	Parameter	Minimum	Maximum	Units
1	TCK pulse width high	80	—	ns
2	TCK pulse width low	80	—	ns
3	TMS, TDI setup to TCK rising edge	5	—	ns
4	TMS, TDI hold after TCK high	20	—	ns

Table 4-18. Test and Diagnostic Interface Switching Characteristics

Symbol	Parameter	Minimum	Maximum	Units
5	TDO hold after TCK falling edge	0	—	ns
6	TDO delay after TCK low	—	20	ns
7	TDO enable (Low Z) after TCK falling edge	10	—	ns
8	TDO disable (High Z) after TCK low	—	10	ns

Figure 4-22. JTAG Interface Timing



4.8 Mechanical Specifications

Figure 4-23. 318-Pin Ball Grid Array (BGA)

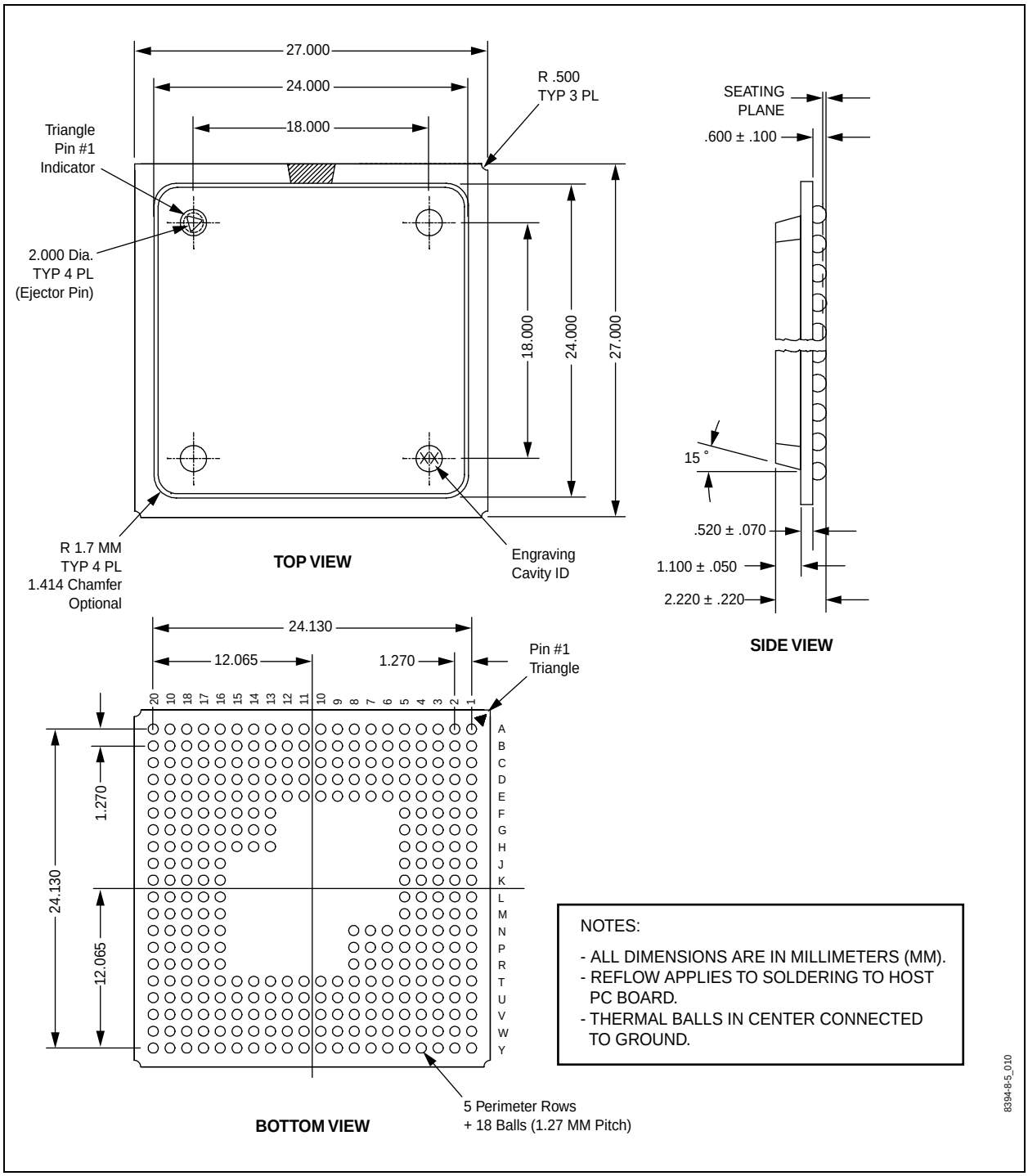


Figure 4-24. 272-Pin Ball Grid Array (BGA)

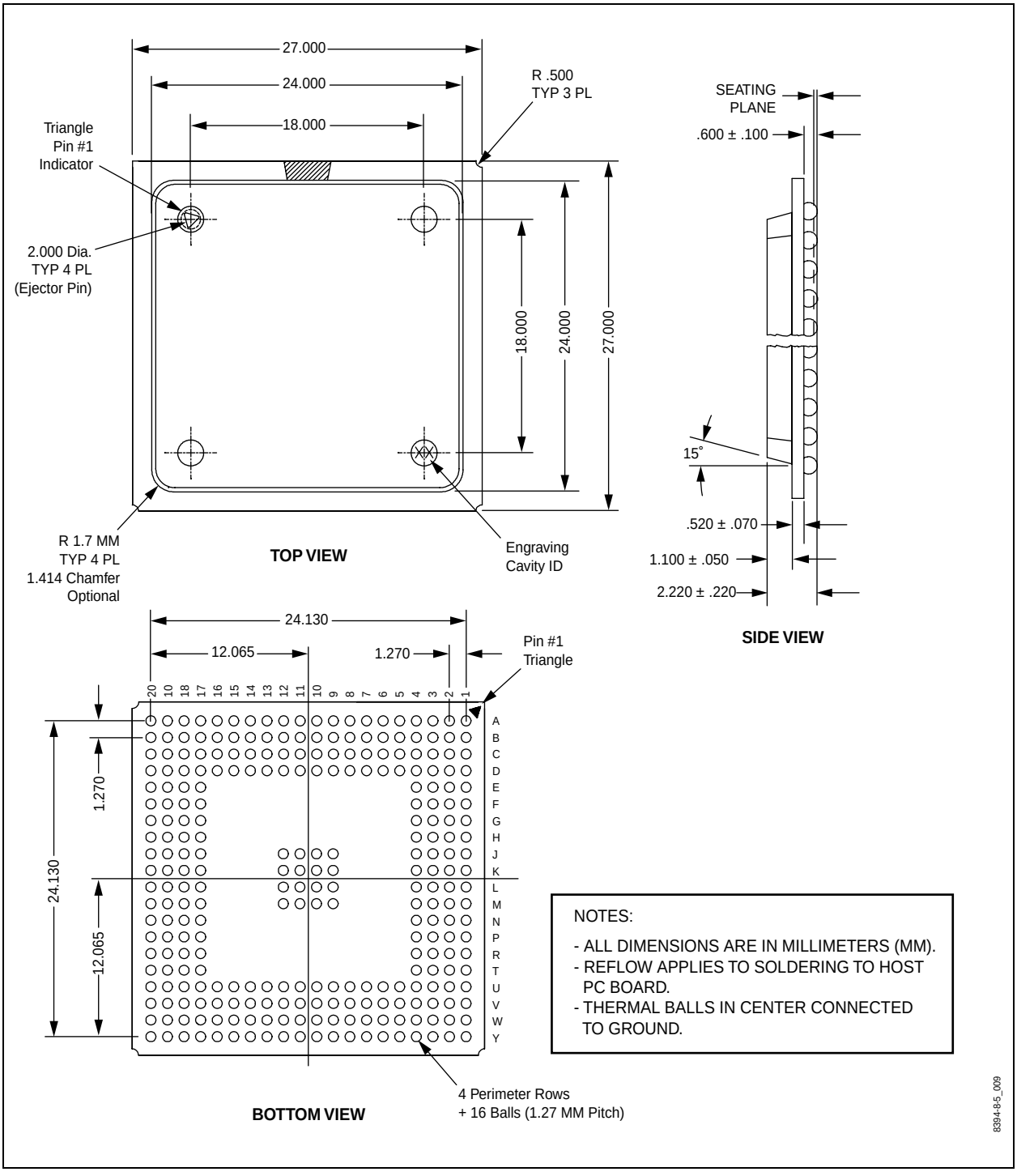
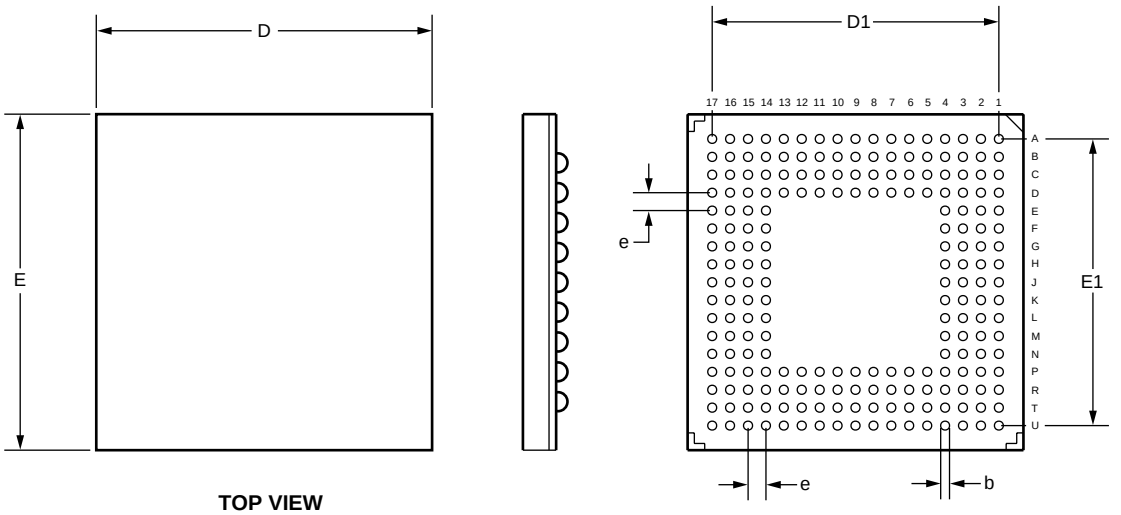
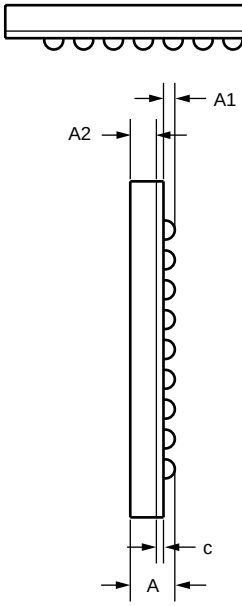


Figure 4-25. 208-Pin Ball Grid Array (CABGA)

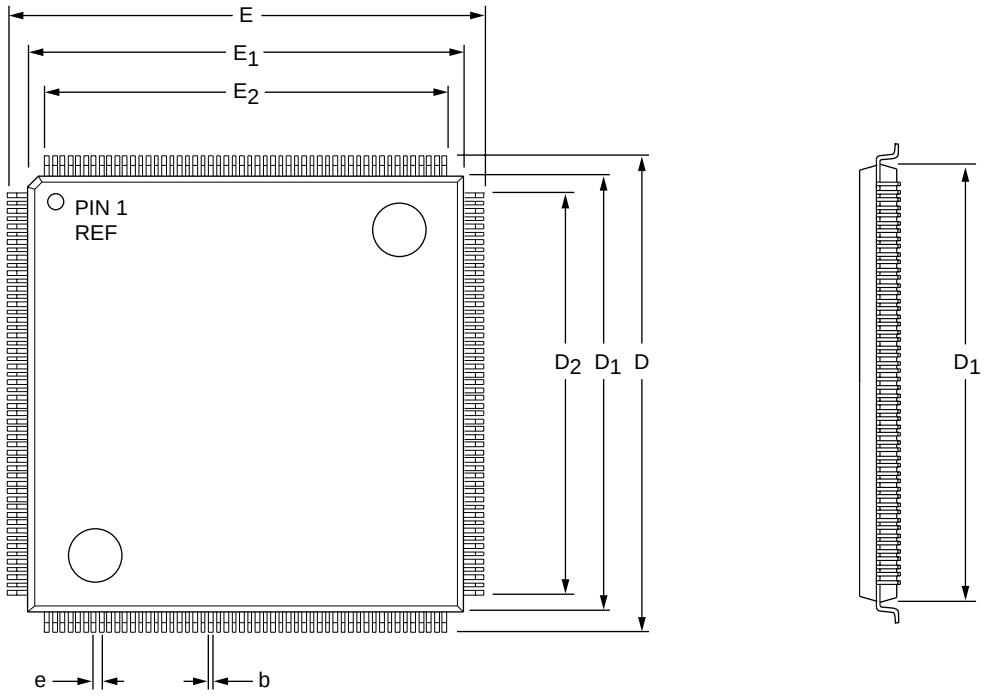


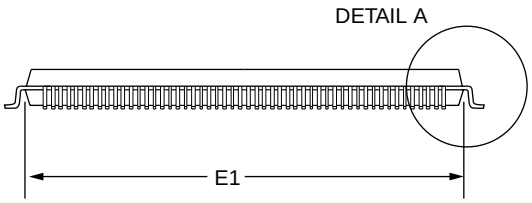


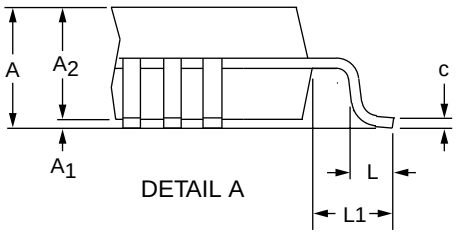
Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.50		1.059	
A1	0.31	0.41	0.12	0.016
A2	0.65	0.76	0.026	0.030
D	15.00 REF.		0.591 REF.	
D1	12.80 REF.		0.504 REF.	
E	15.00 REF.		0.591 REF.	
E1	12.80 REF.		0.504 REF.	
M	17			
N	208			
e	0.80 REF.		0.031 REF.	
b	0.48 REF.		0.018 REF.	
c	0.29	0.39	0.011	0.015
Coplanarity	0.12 MAX.		0.005 MAX.	
Warpage	0.10 MAX.		0.004 MAX.	
Ref: 208-Pin CABGA (GP00-D576-001)				

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Figure 4-26. 208-Pin Plastic Quad Flat Pack (PQFP)



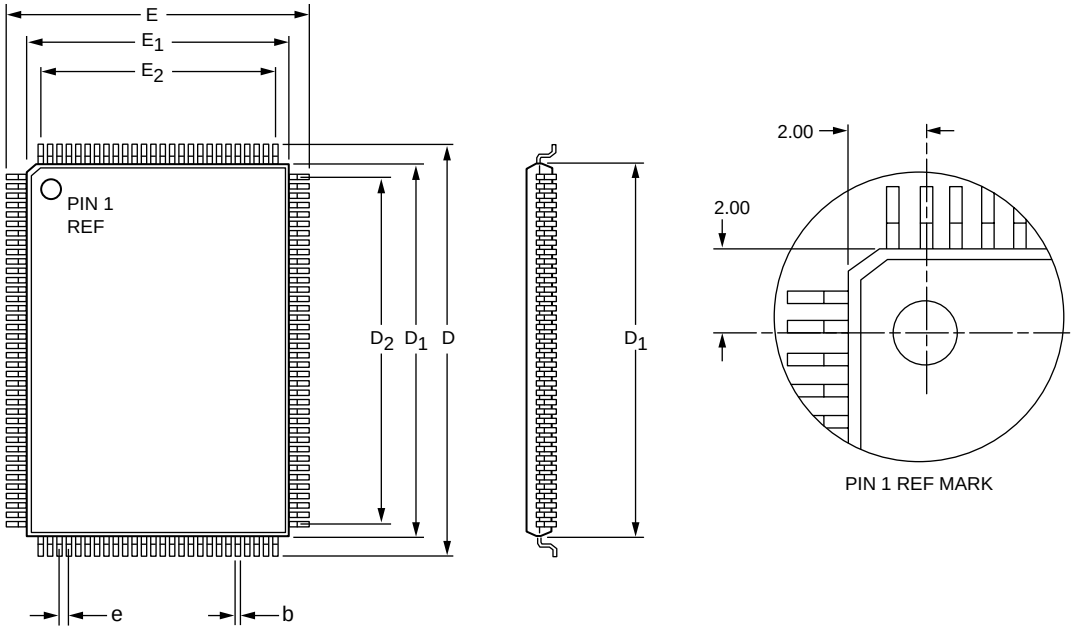




SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX
A	3.64		4.09
A_1	0.25		0.50
A_2	3.39		3.50
D	30.40		30.80
D_1	27.90		28.10
D_2			
E	30.40		30.80
E_1	27.29		27.99
E_2			
L	0.50		0.75
L_1	1.00 REF.		
e	0.500		
b	0.215		0.225
c			

8394-9-5_008

Figure 4-27. 128-Pin (TQFP) Mechanical Drawing



SYMBOL	ALL DIMENSIONS IN MILLIMETERS	
	MIN.	MAX
A	1.6 MAX.	
A_1	0.10	0.15
A_2	1.4 REF	
D	21.85	22.15
D_1	20.0 REF	
D_2	18.5 REF	
E	15.8	16.15
E_1	14.0 REF	
E_2	12.5 REF	
L	0.4	0.65
L_1	1.0 REF	
e	0.50 BSC	
b	0.17	0.27
c	0.11	0.17
Ref. 128-PIN TQFP (GP00-D268)		

8394-8-5_002

Appendix A

A.1 Superframe Format (SF)

The Superframe Format (SF), is also referred to as the D4 format. The requirement for associated signaling in frames 6 and 12 dictates that the frames be distinguishable. This leads to a multiframe structure consisting of 12 frames per superframe (SF). See Figure A-1 and Tables A-1 and A-2.

The SF structure consists of a multiframe of 12 frames. Each frame has 24 channels, plus an F-bit, and 8 bits per channel. A channel is equivalent to one voice circuit or one 64 kbps data circuit.

This structure of frames and multiframes is defined by the F-bit pattern. The F-bit is designated alternately as an Ft bit (terminal framing bit) or Fs bit (signalling framing bit). The Ft bit carries a pattern of alternating zeros and ones (101010) in odd frames that defines the frame boundaries so that one channel may be distinguished from another. The Fs bit carries a pattern of (001110) in even frames and defines the multiframe boundaries so that one frame may be distinguished from another.

Figure A-1. T1 Superframe PCM Format

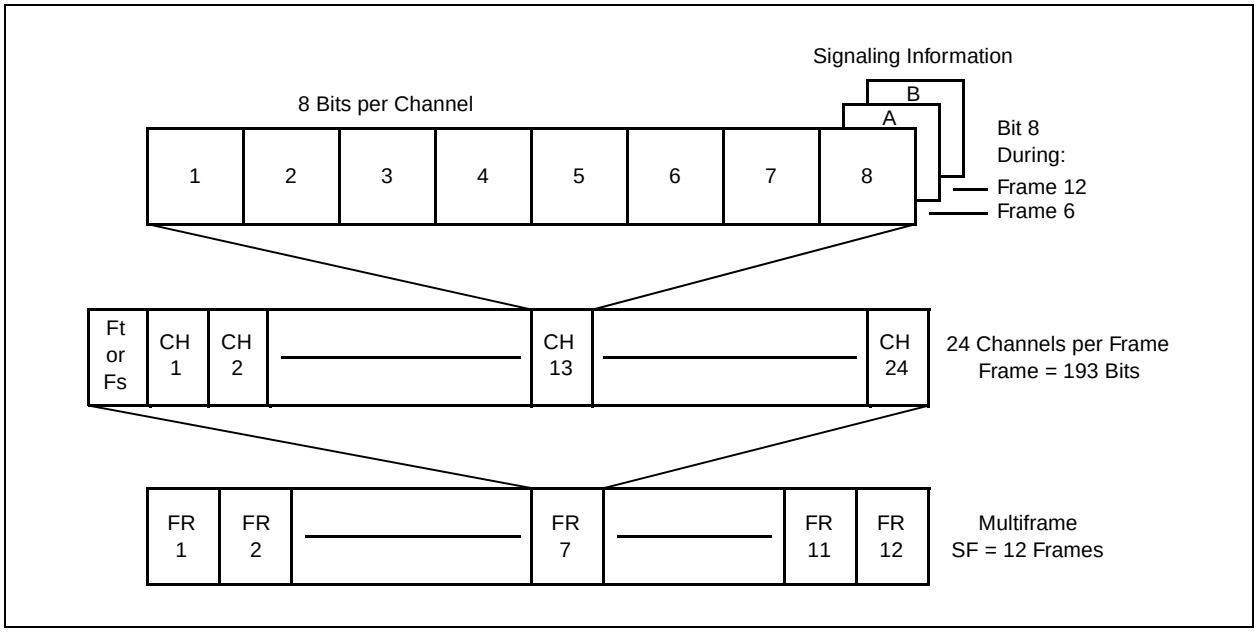


Table A-1. Superframe Format

Frame #	Bit #	F-Bits		Bit Use in Each Time Slot		Signaling Channel
		Terminal Framing Ft	Signaling Framing Fs	Traffic	Sig	
1	0	1	—	1–8	—	—
2	193	—	0	1–8	—	—
3	386	0	—	1–8	—	—
4	579	—	0	1–8	—	—
5	772	1	—	1–8	—	—
6	965	—	1	1–7	8	A
7	1158	0	—	1–8	—	—
8	1351	—	1	1–8	—	—
9	1544	1	—	1–8	—	—
10	1737	—	1	1–8	—	—
11	1930	0	—	1–8	—	—
12	2123	—	0	1–7	8	B

A.2 T1DM Format

Table A-2. T1DM Frame Format

Frame #	Bit #	F-Bits			Bit Use in Each Time Slot	
		Terminal Framing Ft	Signaling Framing Fs	Sync Byte	Info	Ctrl
1	0	1	—	—	1–7	8
1	185–192	—	—	10111YR0	—	—
2	193	—	0	—	1–7	8
2	378–385	—	—	10111YR0	—	—
3	386	0	—	—	1–7	8
3	571–578	—	—	10111YR0	—	—
4	579	—	0	—	1–7	8
4	764–771	—	—	10111YR0	—	—
5	772	1	—	—	1–7	8
5	957–964	—	—	10111YR0	—	—
6	965	—	1	—	1–7	8
6	1150–1157	—	—	10111YR0	—	—
7	1158	0	—	—	1–7	8
7	1343–1350	—	—	10111YR0	—	—
8	1351	—	1	—	1–7	8
8	1536–1543	—	—	10111YR0	—	—
9	1544	1	—	—	1–7	8
9	1729–1736	—	—	10111YR0	—	—
10	1737	—	1	—	1–7	8
10	1922–1929	—	—	10111YR0	—	—
11	1930	0	—	—	1–7	8
11	2115–2122	—	—	10111YR0	—	—
12	2123	—	0	—	1–7	8

Note(s):
1. Y bit is used to indicate a Yellow Alarm (active low).
2. R bit is used solely by AT&T as an 8Kpbs communications channel to collect performance data on long haul DDS facilities.

A.3 SLC 96 Format (SLC)

SLC framing mode allows synchronization to the SLC 96 data link pattern. This pattern, described in the Bellcore TR-TSY-000008, contains both signaling information and a framing pattern that overwrites the Fs bit of the SF framer pattern. (See Table A-3).

Table A-3. SLC-96 Fs Bit Contents

Frame #	Fs Bit	Frame #	Fs Bit	Frame #	Fs Bit
2	0	26	C2	50	0
4	0	28	C3	52	M1
6	1	30	C4	54	M2
8	1	32	C5	56	M3
10	1	34	C6	58	A1
12	0	36	C7	60	A2
14	0	38	C8	62	S1
16	0	40	C9	64	S2
18	1	42	C10	66	S3
20	1	44	C11	68	S4
22	1	46	0	70	1
24	C1	48	1	72	0

Note(s):
1. The SLC-96 frame format is similar to that of SF as shown in Table A-1 with the exceptions shown in this table.
2. C1 to C11 are concentrator field bits.
3. M1 to M3 are maintenance field bits.
4. A1 and A2 are alarm field bits.
5. S1 to S4 are line switch field bits.
6. The Fs bits in frames 46, 48, and 70 are spoiler bits which are used to protect against false multiframing.

A.4 Extended Superframe Format (ESF)

In Extended Superframe Format (ESF), as illustrated in Figure A-2 and Table A-4, the multiframe structure is extended to 24 frames. The channel structure is identical to D4 (SF) format. Robbed-bit signaling is accommodated in frame 6 (A-bit), frame 12 (B-bit), frame 18 (C-bit), and frame 24 (D-bit).

The F-bit pattern of ESF contains three functions:

1. Framing Pattern Sequence (FPS), which defines the frame and multiframe boundaries.
2. Facility Data Link (FDL), which allows data such as error performance to be passed within the T1 link.
3. Cyclic Redundancy Check (CRC), which allows error performance to be monitored and enhances the reliability of the receiver's framing algorithm.

Figure A-2. T1 Extended Superframe Format

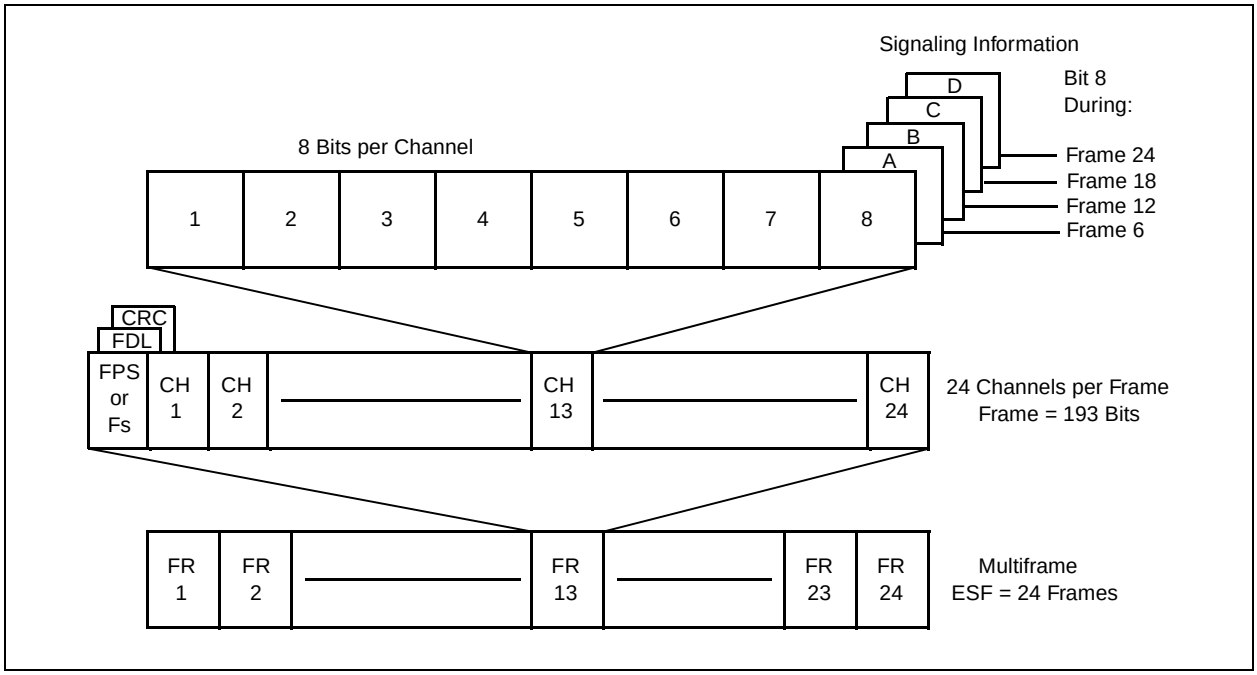


Table A-4. Extended Superframe Format

Frame #	Bit #	F-Bits			Bit Use in Each Time Slot		Signaling Channel		
		FPS	DL	CRC	Traffic	Sig	16	4	2
1	0	—	m	—	1–8	—	—	—	—
2	193	—	—	C1	1–8	—	—	—	—
3	386	—	m	—	1–8	—	—	—	—
4	579	0	—	—	1–8	—	—	—	—
5	772	—	m	—	1–8	—	—	—	—
6	965	—	—	C2	1–7	8	A	A	A
7	1158	—	m	—	1–8	—	—	—	—
8	1351	0	—	—	1–8	—	—	—	—
9	1544	—	m	—	1–8	—	—	—	—
10	1737	—	—	C3	1–8	—	—	—	—
11	1930	—	m	—	1–8	—	—	—	—
12	2123	1	—	—	1–7	8	B	B	A
13	2316	—	m	—	1–8	—	—	—	—
14	2509	—	—	C4	1–8	—	—	—	—
15	2702	—	m	—	1–8	—	—	—	—
16	2895	0	—	—	1–8	—	—	—	—
17	3088	—	m	—	1–8	—	—	—	—
18	3281	—	—	C5	1–7	8	C	A	A
19	3474	—	m	—	1–8	—	—	—	—
20	3667	1	—	—	1–8	—	—	—	—
21	3860	—	m	—	1–8	—	—	—	—
22	4053	—	—	C6	1–8	—	—	—	—
23	4246	—	m	—	1–8	—	—	—	—
24	4439	1	—	—	1–7	8	D	B	A

Note(s):
1. FPS indicates the Framing Pattern Sequence (...001011...).
2. DL indicates the 4Kbps Data Link with message bits m.
3. CRC indicates the cyclic redundancy check with bits C1 to C6.
4. Signaling options include 16 state, 4 state, and 2 state.

Table A-5. Performance Report Message Structure

Octet No.	LSB							MSB
1	FLAG							
2	SAPI						C/R	EA
3	TEI							EA
4	CONTROL							
5	G3	LV	G4	U1	U2	G5	SL	G6
6	FE	SE	LB	G1	R	G2	Nm	NI
7	G3	LV	G4	U1	U2	G5	SL	G6
8	FE	SE	LB	G1	R	G2	Nm	NI
9	G3	LV	G4	U1	U2	G5	SL	G6
10	FE	SE	LB	G1	R	G2	Nm	NI
11	G3	LV	G4	U1	U2	G5	SL	G6
12	FE	SE	LB	G1	R	G2	Nm	NI
13	FCS (Most Significant Byte)							
14	FCS (Least Significant Byte)							

Note(s):
1. The 1-second report consists of octets 5–12.
2. R, U1, and U2 are reserved for future standardization and should be set to 0.

A.5 E1 Frame Format

Figure A-3. E1 Format

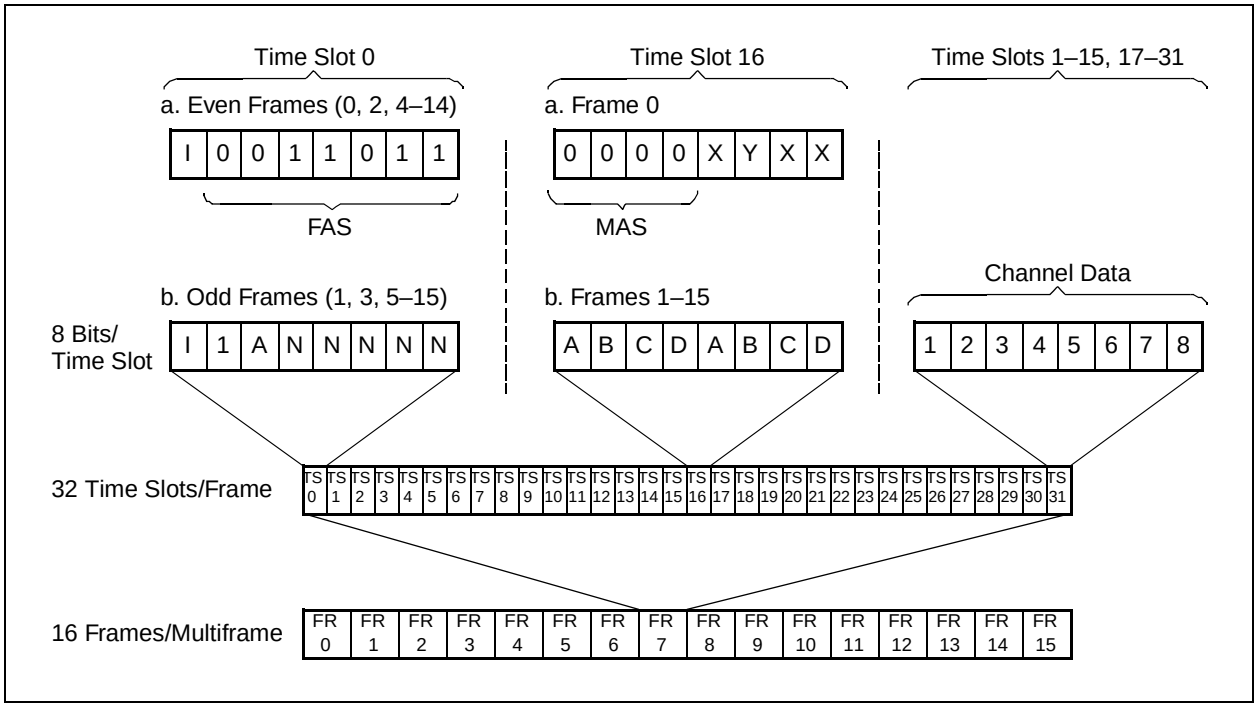


Table A-6. ITU–T CEPT Frame Format Time Slot 0 Bit Allocations

SMF	Frame #	Time Slot 0 Bits 1 to 8 of each frame							
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
I	0	C1/Si	0	0	1	1	0	1	1
	1	0/Si	1	A	SA4	SA5	SA6	SA7	SA8
	2	C2/Si	0	0	1	1	0	1	1
	3	0/Si	1	A	SA4	SA5	SA6	SA7	SA8
	4	C3/Si	0	0	1	1	0	1	1
	5	1/Si	1	A	SA4	SA5	SA6	SA7	SA8
	6	C4/Si	0	0	1	1	0	1	1
	7	0/Si	1	A	SA4	SA5	SA6	SA7	SA8
II	8	C1/Si	0	0	1	1	0	1	1
	9	1/Si	1	A	SA4	SA5	SA6	SA7	SA8
	10	C2/Si	0	0	1	1	0	1	1
	11	1/Si	1	A	SA4	SA5	SA6	SA7	SA8
	12	C3/Si	0	0	1	1	0	1	1
	13	E/Si	1	A	SA4	SA5	SA6	SA7	SA8
	14	C4/Si	0	0	1	1	0	1	1
	15	E/Si	1	A	SA4	SA5	SA6	SA7	SA8

Note(s):
1. SMF indicates the sub-multiframe. This partitioning is used in the CRC-4 calculation.
2. Si bits are International Spare Bits.
3. A bit is used to indicate a remote alarm condition (active high).
4. SA4 to SA8 are spare bits that may be recommended by ITU–T for use in specific point-to-point applications (e.g., transcoder equipment conforming to Recommendation G.761).
5. SA4 to SA8 where these are not used should be set to 1 on links crossing an international border.
6. E bit is used to indicate a CRC-4 error. The normal state is both bits set to 1; when a CRC-4 error is detected, one of the E bits is set to 0.
7. C1 to C4 bits are used to carry the CRC-4 code.
8. Time slot 0 that contains the 0011011 sequence is defined as the FAS word. Time slot 0 that does not contain the FAS is the Not-Word.

A.6 IRSM CEPT Frame Format

Table A-7. IRSM CEPT Frame Format Time Slot 0 Bit Allocations

SMF	Frame #	Time Slot 0 Bits 1 to 8 of each frame							
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
I	0	C1/Si	0	0	1	1	0	1	1
	1	0/Si	1	A	D	E0	E1	E16	E17
	2	C2/Si	0	0	1	1	0	1	1
	3	0/Si	1	A	D	E2	E3	E18	E19
	4	C3/Si	0	0	1	1	0	1	1
	5	1/Si	1	A	D	E4	E5	E20	E21
	6	C4/Si	0	0	1	1	0	1	1
	7	0/Si	1	A	D	E6	E7	E22	E23
II	8	C1/Si	0	0	1	1	0	1	1
	9	1/Si	1	A	D	E8	E9	E24	E25
	10	C2/Si	0	0	1	1	0	1	1
	11	1/Si	1	A	D	E10	E11	E26	E27
	12	C3/Si	0	0	1	1	0	1	1
	13	E/Si	1	A	D	E12	E13	E28	E29
	14	C4/Si	0	0	1	1	0	1	1
	15	E/Si	1	A	D	E14	E15	E30	E31

Note(s):
1. SMF indicates the sub-multiframe. This partitioning is used in the CRC-4 calculation.
2. Si bits are International Spare Bits.
3. NA bit is used to indicate a remote alarm condition (active high).
4. Ei are per channel control bits.
5. E bit is used to indicate a CRC-4 error. The normal state is both bits set to 1; when a CRC-4 error is detected, one of the E bits is set to 0.
6. C1 to C4 bits are used to carry the CRC-4 code.
7. Time slot 0 that contains the 0011011 sequence is defined as the FAS word. Time slot 0 that does not contain the FAS is the Not-Word.
8. D bits are a 4 kbps data link.
9. Bit 2 of the Not-Word is defined as the alternate framing bit.

Table A-8. CEPT (ITU–T and IRSM) Frame Format Time Slot 16 Bit Allocations

SMF	Frame #	Time Slot 16 Bits 1 to 8 of each frame							
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
I	0	0	0	0	0	X0	Y	X1	X2
	1	A1	B1	C1	D1	A17	B17	C17	D17
	2	A2	B2	C2	D2	A18	B18	C18	D18
	3	A3	B3	C3	D3	A19	B19	C19	D19
	4	A4	B4	C4	D4	A20	B20	C20	D20
	5	A5	B5	C5	D5	A21	B21	C21	D21
	6	A6	B6	C6	D6	A22	B22	C22	D22
	7	A7	B7	C7	D7	A23	B23	C23	D23
II	8	A8	B8	C8	D8	A24	B24	C24	D24
	9	A9	B9	C9	D9	A25	B25	C25	D25
	10	A10	B10	C10	D10	A26	B26	C26	D26
	11	A11	B11	C11	D11	A27	B27	C27	D27
	12	A12	B12	C12	D12	A28	B28	C28	D28
	13	A13	B13	C13	D13	A29	B29	C29	D29
	14	A14	B14	C14	D14	A30	B30	C30	D30
	15	A15	B15	C15	D15	A31	B31	C31	D31

Note(s):
1. SMF indicates the sub-multiframe.
2. Ai–Di are the per channel signaling bits.
3. X0–X2 are the X spare bits normally set to 1.
4. Y is the Remote Multiframe Yellow Alarm Indication bit. When Y is set to a 1, this indicates that the alarm is active.
5. The Multiframe Alignment Sequence (MAS) is defined as the Time Slot 16 word that contains the 0000XYXX sequence.

Appendix B

B.1 Applicable Standards

Table B-1. Applicable Standards *(1 of 3)*

Standard	Title
ANSI	
T1.101-1987	Digital Hierarchy—Timing Synchronization
T1.102-1993	Digital Hierarchy—Electrical Interfaces
T1.107-1991 (Newer Draft Standard T1X1.4/93-002R3)	Digital Hierarchy—Formats Specification
T1.403-1995	Network to Customer Installation—DS1 Metallic Interface
T1.408-1990	ISDN Primary Rate—Customer Installation Metallic Interfaces
T1.231-1993	Layer 1 In-Service Digital Transmission Performance Monitoring
AT&T	
TR 41449-1986	ISDN Primary Rate Interface Specification
TR 43801(A)-1985	Digital Channel Bank—Requirements and Objectives
TR 54016-1989	Rqts. for Interfacing DTE to Services Employing Extended Superframe Format
TR 62411-1990	Accunet T1.5 Service Description and Interface Specification
Bellcore	
TR-TSY-000008 Issue 2, 1987	Digital Interface Between the SLC 96 Digital Loop Carrier System and a Local Digital Switch
TR-TSY-000009 Issue 1, 1986	Asynchronous Digital Multiplexer Requirements and Objectives
TR-NPL-000054 Issue 1, 1989	High-Capacity Digital Service (HCDS) Interface Generic Requirements
TR-NWT-000057 Issue 2, 1993	Functional Criteria for Digital Loop Carrier Systems
TA-TSY-000147 Issue 1, 1987	DS1 Rate Digital Service Monitoring Unit
TR-TSY-000170 Issue 2, 1993	Digital Cross-Connect System (DCS) Requirements and Objectives
TR-TSY-000191 Issue 1, 1986	Alarm Indication Signal (AIS) Requirements and Objectives

Table B-1. Applicable Standards *(2 of 3)*

Standard	Title
TR-TSY-000194 Issue 1, 1987	The Extended Superframe Format Interface
TA-TSY-000278 Issue 1, 1985	Digital Data System (DDS)—T1 Digital Multiplexer (T1DM) Requirements
TR-TSY-000303 Issue 2, 1992	Integrated Digital Loop Carrier (IDLC) System Generic Requirements
TR-TSY-000312 Issue 1, 1988	Functional Criteria for the DS1 Interface Connector
TR-NPL-000320 Issue 1, 1988	Fundamental Generic Requirements for Metallic Digital Signal Cross-connect Systems
TA-TSY-000435 Issue 1, 1987	DS1 Automatic Facility Protection Switching (AFPS) Rqts. and Objectives
TR-NWT-000499 Issue 5, 1993	Transport Systems Generic Requirements
TR-TSY-000510 Issue 2, 1987	LSSGR: System Interfaces, Section 10
TR-NWT-000773 Issue 1, 1991	Local Access System Requirements, Objectives and Interfaces for SMDS
TR-TSY-000776 Issue 2, 1993	Network Interface Description for ISDN Customer Access
GR-820-CORE Issue 1, 1994 (replaced TR-NWT-000820)	Generic Digital Transmission Surveillance
TA-NWT-000821 Issue 1, 1991 (replaced TR-TSY-000821)	Additional Transport and Transport-Based Surveillance Generic Rqts.
SR-TSY-000977 Issue 1, 1988	ISDN Primary Rate Access Maintenance
TR-NWT-001219 Issue 1, 1992 (Rev 1, 1993)	ISDN Primary Rate Access Testing Requirements
SR-NWT-002343 Issue 1, 1993	ISDN Primary Rate Interface Guidelines for Customer Premises Equipment
ETSI	
ETS 300 011 (4/92)	ISDN Primary Rate User-Network Interface Specification and Test Principles
ETS 300 233	Access Digital Section for ISDN Primary Rate
ITU-T	
Recommendation G.703 (1991)	Physical/Electrical Characteristics of Hierarchical Digital Interfaces
Recommendation G.704 (1991)	Synchronous Frame Structures used at Primary Hierarchical Levels
Recommendation G.706 (1991)	Frame Alignment and CRC Procedures Relating to G.704 Frame Structures
Recommendation G.732	Characteristics of Primary PCM Multiplex Equipment at 2048 kbps
Recommendation G.733	Characteristics of Primary PCM Multiplex Equipment at 1544 kbps
Recommendation G.734	Characteristics of Synchronous Digital Multiplex Equipment at 1544 kbps
Recommendation G.735	Characteristics of Primary PCM Multiplex Equipment at 2048 kbps; offering Synchronous Digital Access at 384 kbps and/or 64 kbps
Recommendation G.736	Characteristics of Synchronous Digital Multiplex Equipment at 2048 kbps
Recommendation G.737	Characteristics of External Access Equipment at 2048 kbps; offering Synchronous Digital Access at 384 kbps and/or 64 kbps
Recommendation G.738	Characteristics of Primary PCM Multiplex Equipment at 2048 kbps; offering Synchronous Digital Access at 320 kbps and/or 64 kbps
Recommendation G.739 Recommendation G.761	Characteristics of External Access Equipment at 2048 kbps; Offering Synchronous Digital Access at 320 kbps and/or 64 kbps

Table B-1. Applicable Standards *(3 of 3)*

Standard	Title
Draft Recommendation G.775	Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection
Recommendation G.796	Characteristics of 64 kbps Cross-Connect Equipment with 2048 kbps Access Ports
Recommendation G.802 (1988)	Interworking between Networks based on Different Digital Hierarchies
Recommendation G.821	Error Performance Monitoring on International Connections
Recommendation G.823 (3/93)	Control of Jitter and Wander in Digital Networks based on 2048 kbps
Recommendation G.824 (3/93)	Control of Jitter and Wander in Digital Networks based on 1544 kbps
Recommendation G.921	Digital Sections based on 2048 kbps Hierarchy
Recommendation G.962 (3/93)	Access Digital Section for ISDN Primary Rate at 2048 kbps
Recommendation G.963 (3/93)	Access Digital Section for ISDN Primary Rate at 1544 kbps
Recommendation I.411	ISDN User-Network Interfaces—References Configurations
Recommendation I.412	ISDN User-Network Interfaces—Structures and Access Capabilities
Recommendation I.421	Primary Rate User-Network Interface
Recommendation I.431	Primary Rate User-Network Interface—Layer 1 Specification
Recommendation K.10	Unbalance about Earth of Telecommunication Installations
Recommendation K.20	Resistibility of Switching Equipment to Overvoltages and Overcurrents
Recommendation M.3604	Application of Maintenance Principles to ISDN Primary Rate Access
Recommendation O.150	Digital Test Patterns for Performance Measurements
Recommendation O.151	Error Performance Measuring Equipment Operating at Primary Rate and Above
Recommendation O.152	Error Performance Measuring Equipment for Bit Rates of 64 kbit/s and NX 64 kbit/s
Recommendation O.162 (10/92)	Equipment to Perform In-Service Monitoring on 2048 kbps Signals
Recommendation Q.921	ISDN User-Network Interface - Data Link Layer Specification
IEEE Std 1149.1a-1993	IEEE Standard Test Access Port and Boundary Scan Architecture (JTAG)
Natural Microsystems Corporation, Release 1.0, March 1993	Multi-Vendor Integration Protocol (MVIP) Reference Manual
FCC Part 68.302 (d)	Environment Simulation metallic voltage surge
FCC Part 68.308	Signal Power Limitations

Appendix C

C.1 System Bus Compatibility

C.1.1 AT&T Concentration Highway Interface (CHI):

DX = RPCMO
+ output on rising or falling edge of clock
+ output on every CLKXR or CLKXR/2
+ Tri-stated during inactive time slots

DR = TPCMI
+ sampled on rising or falling edge of clock
+ sampled on every CLKXR or CLKXR/2 (see X2CLK mode)

FS = TFSYNC
+ sampled on rising or falling edge of clock (FE select)
+ rising edge determines frame start
+ 8 kHz rate

TSC* = RINDO
+ Optional CHI pin is driven low during active DX time slots

CLKXR = TSBCLKI = RSBCLKI
+ N x 64 kHz rates, where N = 4, 8, 16, 32, 48 or 64

C.1.2 CHI Programming Options:

CMS = clock mode select
0 = line rate
1 = 2X line rate

XEN = transmitter enable
0 = disable (DX tri-stated)
1 = enable (DX driven during active time slots)

FE = frame edge select
0 = falling edge
1 = rising edge

XCE = CLKXR output edge select for DX
0 = falling edge
1 = rising edge

RCE = CLKXR input edge select for DR
0 = falling edge
1 = rising edge

XBOFF = 3-bit transmit output bit offset
000-1111 = CLKXR (or 2xCLKXR) delay from FS to DX bit0

RBOFF = 3-bit receive input bit offset
000-111 = CLKXR (or 2xCLKXR) delay from FS to DR bit0

XTS = 6-bit transmit output TS offset
00-3F = CLKXR (or 2xCLKXR) TS delay from FS to DX bit0

RTS = 6-bit receive input TS offset
00-3F = CLKXR (or 2xCLKXR) TS delay from FS to DR bit0

The device only supports CHI and GCI buses if N = 24, 32, or 48, although either bus is defined to operate at N x 64 from N = 4 to N = 48. The device does not support AT&T's Dual CHI (separate A/B buses) or K2 buses, nor does it support INTEL's SLD (ping/pong) 3-pin bus.

Appendix D

D.1 Notation and Acronyms

D.1.1 Arithmetic Notation

Time Slot Bit Numbering associated with time slots in the primary rate channel, are numbered 1 to 8, where bit number 1 is transmitted first and is specified as the MSB.

Configuration and Status Word Bit Numbering, associated with configuration or status words, 7 to 0, where bit number 7 is specified as the MSB, and bit number 0 is specified as the LSB.

D.2 Acronyms and Abbreviations

ADC	Analog to Digital Converter
AFPS	Automatic Facility Protection Switching
AGC	Automatic Gain Control
AIS	Alarm Indication Signal
ALBO	Automatic Line Build Out
ALOS	Analog Loss of Signal
AMI	Alternate Mark Inversion
ANSI	American National Standards Institute
B8ZS	Binary with 8 Zero Substitution
BER	Bit Error Rate
BERR	Bit Error Counter
BFA	Basic Frame Alignment
BOP	Bit-Oriented Protocol
BPV	Bipolar Violation
BSDL	Boundary Scan Description Language
CAS	Channel Associated Signaling
ITU–T	International Telegraph and Telephone Consultative Committee
CCS	Common Channel Signaling
CERR	CRC Errors
CGA	Carrier Group Alarm
CI	Customer Installation
CLAD	Clock Rate Adapter
CMOS	Complementary Metal Oxide Semiconductor
COFA	Change of Frame Alignment
CRC	Cyclic Redundancy Check
CSU	Channel Service Unit
DAC	Digital to Analog Converter
DCS	Digital Cross-Connect System
DDS	Digital Data System
DMI	Digital Multiplexed Interface
DPLL	Digital Phase Locked Loop
DPM	Driver Performance Monitor
DS1	Digital Signal Level 1
DSU	Data Service Unit
ESF	Extended Superframe
EXZ	Excessive Zeros

FAS	Frame Alignment Sequence (E1 Format)
FCC	Federal Communications Committee
FCS	Frame Check Sequence
FDL	Facility Data Link
FEBE	Far End Block Error
FERR	Framing Bit Error
FPS	Frame Pattern Sequence (EFS Format)
HCDS	High-Capacity Digital Service
HDB3	High-Density Bipolar of Order 3
ICOT	Intercity and Outstate Trunk
IDLC	Integrated Digital Loop Carrier
ISDN	Integrated Service Digital Network
JAT	Jitter Attenuator
JCLK	Jitter Attenuated Clock
JTAG	Joint Test Action Group
LBO	Line Build Out
LCV	Line Code Violation
LEC	Local Exchange Carrier
LIU	Line Interface Unit
LOAS	Loss of Analog Signal
LOF	Loss of Frame
LOS	Loss of Signal –DS1
LSB	Least Significant Bit
MAIS	Multiframe AIS
MART	Maximum Average Reframe Time
MAS	Multiframe Alignment Sequence (CAS Format)
MAT	Metropolitan Area Trunk
MERR	MFAS Error
MFAS	Multiframe Alignment Sequence (CRC4 format)
MOP	Message Oriented Protocol
MOS	Message Oriented Signaling
MPU	Microprocessor Interface
MQFP	Metric Quad Flat Pack
MSB	Most Significant Bit
MUX	Multiplexer
MVIP	Multi-Vendor Integration Protocol
MYEL	Multiframe Yellow Alarm
NCO	Numerical Controlled Oscillator
NI	Network Interface
NRZ	Non-Return to Zero
OOF	Out of Frame

PCM	Pulse Code Modulation
PDV	Pulse Density Violation
PIC	Polyethylene-Insulated Cable
PLCC	Plastic Leaded Chip Carrier
PLL	Phase Locked Loop
PM	Performance Monitoring
PQFP	Plastic Quad Flat Pack
PRBS	Pseudo-Random Bit Sequence
PRI	Primary Rate Interface
PRM	Performance Report Message
RAI	Remote Alarm Indication
RBOP	Bit-Oriented Protocol Detector
RBS	Robbed Bit Signaling
RCVR	Receiver
RDL1	Receive Data Link 1
RDL2	Receive Data Link 2
RDL3	External Receive Data Link
RFRAME	Receive Framer
RJAT	Receive Jitter Attenuator
RLIU	Receive Line Interface Unit
RMAIS	Receive Multiframe AIS
RPDV	Receive Pulse Density Violation
RPLL	Receive Phase Locked Loop
RSB	Receive System Bus
RSBI	Receive System Bus Interface
RSIG	Receive Signaling Buffer
RSLIP	Receive Slip Buffer
RXCLK	Receive Clock
RZCS	AMI/HDB3/B8ZS Line Decoder
QRSS	Quasi-Random Signal Source
SEF	Severely Errored Framing Event
SERR	CAS Error
SF	Super Frame
SLC	Subscriber Loop Carrier
TAP	Test Access Port
TBOP	Bit Oriented Protocol Formatter
TDL1	Transmit Data Link 1
TDL2	Transmit Data Link 2
TDL3	External Transmit Data Link
TDM	Time Division Multiplexed
TSB	Transmit System Bus
TSBI	Transmit System Bus Interface
TJAT	Transmit Jitter Attenuator
TLIU	Transmit Line Interface Unit

TLOS	Transmit Loss of Signal
TSB	Transmit System Bus
TSIC	Time Slot Interchange
TSIG	Transmit Signaling Buffer
TSLIP	Transmit Slip Buffer
TZCS	AMI/HDB3/B8ZS Line Encoder
UI	Unit Interval
UMC	Unassigned Mux Code
UNICODE	Universal Trunk Out of Service Code
UTP	Unshielded Twisted Pair
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VGA	Variable Gain Amplifier
XMTR	Digital Transmitter
YEL	Yellow Alarm
ZCS	Zero Code Suppression

Appendix E

E.1 Revision History

Table E-1. Document Revision History

Revision	Level	Date	Description
A	Advanced	July 1998	Created
B	Preliminary	April 1999	1. Added two new products to the data sheet: CX28394 (quad framer) and CX28395 (x16 framer). 2. Re-named data sheet. 3. Changed the device part number from RS8398 to CX28398. 4. *Transmitter, Overhead Pattern Generator, Alarm Generator* section rewritten for clarity. Removed RLOC from automatic AIS generation description. Removed reference to RDIGI bit. Added description of RLOF integration to automatic Yellow Alarm/RAI generation description. 5. Removed 2Kbps datalink mode and ZBTSI support. 6. Added chapter: *System Bus*, to describe multiplexed and non-multiplexed modes. 7. Changed RLOS clearing criteria for T1 to “at least 12.5% density over a period of 114 bits.” 8. Changed default register settings for registers 040, 041, 042, and 043. These registers are not reset. 9. Removed 8398 Embedded mode from the *System Bus* description and SBI_CR register description.
C	Preliminary	May 1999	1. Incorporated edits from Errata #N8398ER1A dated May 13, 1999.
D	Final	November 1999	1. Incorporated edits from Errata #100354C, formerly N8398ER1C. 2. Updated timing parameters.
E	Preliminary	May 2000	1. Updated marking numbers.



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