# ST2601B

## 8-bit Integrated Microcontroller

# Datasheet

**Version 1.1**

**2009/05/07**

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# 1 GENERAL DESCRIPTION

The ST2601B is a 8-bit integrated microcontroller designed with CMOS silicon gate technology. The true static CPU core, power down modes and dual oscillators design makes the ST2601B suitable for power saving and long battery life designs. The ST2601B integrates various logic to support functions on-chip which are needed by system designers.
The ST2601B features the capacity of memory access of maximum 44M bytes and DMA function for fast memory transfer. Six chip-select pins are equipped for direct connection to external ROM, SRAM, Flash memory or other devices. The maximum size for a single external memory device can be 16M bytes.

The ST2601B has 39 I/Os grouped into 5 ports. They are Port-C, Port-D, Port-E (7 pins), Port-F and Port-L, where the Port-F consists of 8 open-drain output pins shared with LCD COMs. Each I/O pins can be programmed to input or output individually. Port-C input pins provide both pull-up and pull-down options. The other input pins only support the pull-up option. In the case of output mode, Port-C output pins have open-drain type and CMOS type options; while the other ports are fixed at CMOS type. The Port-C/D/E/F/L are shared with other system functions. All the properties of the I/O pins are still programmable when they are configured as other special functional signals. This enlarges the flexibility of the usage of the functional signals.

The ability of driving large LCD panels, up to 100X100in BW mode, and hardware gray-level support may enrich the display information and the diversify the display contents as well. By the patented sharing mechanism design of internal memory, the LCD display function can be done without the need of external display RAM. The variable LCD buffer design also makes it feasible to use small internal display RAM as the buffer of large-sized display. User may free major internal RAM for computing or temporary access while keeping the display content. The clock of LCD (LCDCK) is not only sourced from main-frequency (OSC), it can also be sourced by OSCX (32KHz crystal) to make current consumption to be minimum. Besides, Vlcd has excellent voltage variation when Vdd changes from 2.4V to 3.6V. Further more, ST2601B has inside trimming fuse function for Vlcd and LVD.So every ST2601B real-chip will have almost the same default Vlcd and LVD voltage.

The ST2601B equips 2 serial communication ports, one UART port and one SPI port, to perform different communications, ex.: RS-232 and IrDA, with system components or other products such as PC, Notebook, and popular PDA. Three clocking outputs can produce synthesized PWM signals or high frequency carrier for IR remote control. This helps products become more useful in our daily life.

The built-in four-channel PSG are designed to generate key tone, melody, voice, and speech. Two dedicated pins with large driving capacity can drive a buzzer/speaker directly.

The ST2601B has a Low Voltage Detector (LVD) for power management usage. The status of internal or external power can be detected and reported to the management software.

Power bouncing during power-on is a major problem when designing a reliable system. The ST2601B equips a Low Voltage Reset function to keep the whole system in reset status when power is low. After the power returns to normal level, the system may recover its original states and keeps working correctly.

With these integrated functions inside, the ST2601B single chip microcontroller is a right solution for PDA, translator, databank and other consumer products.

The block diagram of ST2601B is shown in the following figure.

# 2 BLOCK DIAGRAM

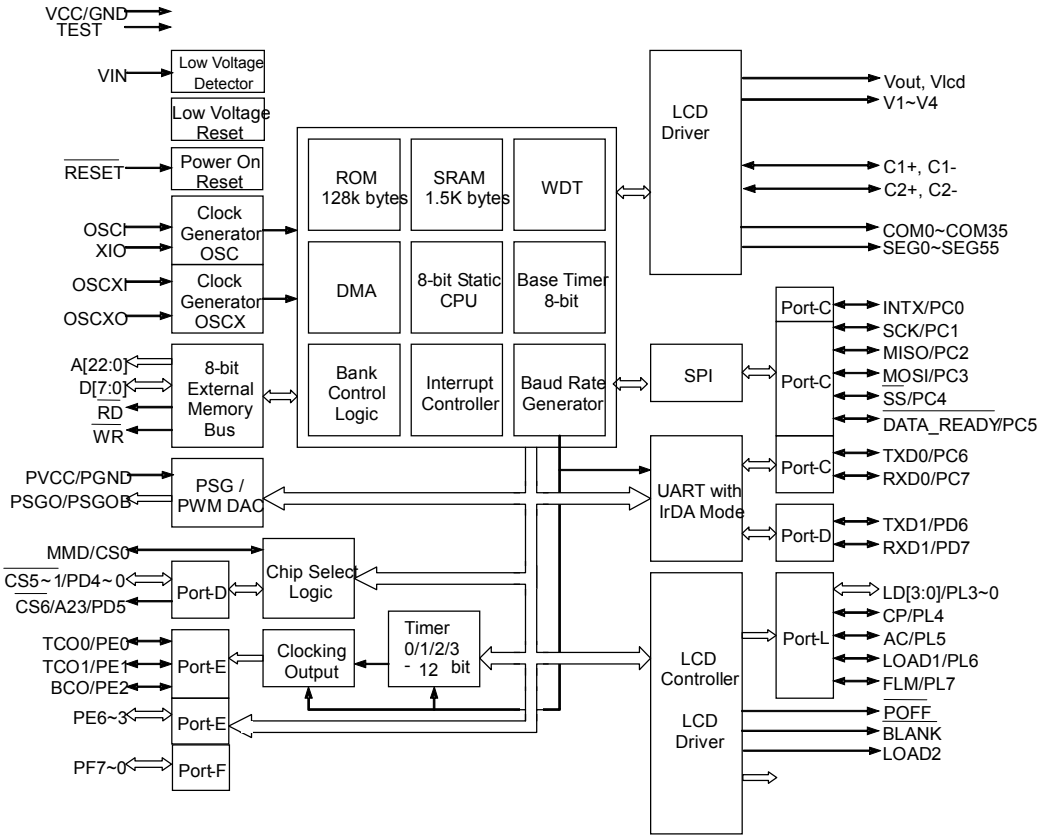



**FIGURE 2-1 ST2601B Block Diagram**

# 3 FEATURES

- **Totally static 8-bit CPU**
- **ROM: 128k x 8-bit**
- **RAM: 1.5K x 8-bit**
- **Stack: Up to 128-level deep**
- **Operation voltage: 2.4V ~ 3.6V**
- **Operation frequency:**
  – 3.0Mhz@2.4V(Min.)
  – 4.0Mhz@2.7V(Min.)
- **LCD Drives**
  – COM: 36 outputs. Eight shared with one output port
  – SEG: 56 outputs. Shared with 3 I/O ports and memory bus signals.
- **One 8x8 Signed Multiplier**
- **Low Voltage Reset (LVR)**
  – Two levels by code option
- **Low Voltage Detector (LVD)**
  – Programmable 4 levels
  – System power or external battery level can be detected.
- **Programmable Watchdog Timer (WDT)**
- **Memory interface to ROM, RAM, Flash**
- **Memory configuration**
  – Three kinds of banks for program, data and interrupt
  – 12-bit bank registers support up to 44M bytes
  – Six programmable chip-selects with 4 modes
  – Maximum single device of 16M bytes
- **General-Purpose I/O (GPIO) ports**
  – Up to 39 bit programmable I/Os
  8 dedicated CMOS I/Os
  23 shared with LCD SEGs
  8 open drain output pins shared with LCD COMs
  – Bit programmable pull-up for input pins
  – Pull-up/down and open-drain/CMOS control for Port-C
- **Timer/Counter**
  – Four 12-bit timers.
  – One 8-bit base timer
  – Seven fixed base timers
- **Three clocking outputs**
  – Clock sources including Timer0/1, baud rate generator
- **Eleven prioritized interrupts with dedicated exception vectors**
  – External interrupt (edge triggered)
  – LCD buffer interrupt
  – Base timer interrupt
  – Timer0~3 interrupts (x4)
  – SPI interrupts (x2)
  – UART interrupts (x2)
- **Dual clock sources with warm-up timer**
  – Low frequency crystal oscillator (OSCX) ..... 32768 Hz
  – High frequency resistor or crystal/resonator oscillator (OSC) selected by pin option ..... 455K~4M Hz
- **Direct Memory Access (DMA)**
  – Block-to-Block transfer
  – Block to Single port
- **LCD Power Management**
  – DC-DC converter with 8-level output control
  – LC driving voltage regulator with 16-level control
  – 1/4, 1/5, 1/6 bias options with 4 voltage followers
- **LCD Driver**
  – 32x28~56x36 resolution, maximum 2016 dots
  – One clock source from osc / oscx
  – Internal bias resistors(1/4, 1/5, 1/6 bias).
- **LCD Controller (LCDC)**
  – Software programmable display size up to 100X100
  – B/W, Hardware 4/16 gray levels with 5-bit palette
  – Support 1-/4-/8-bit LCD data bus
  – Share system memory with display buffer and with no loss of the CPU time
  – LCD buffer extension function to combine both internal and external RAM for larger display
  – Diverse functions including virtual screen, panning, scrolling, contrast control and alternating signal generator
- **Programmable Sound Generator (PSG)**
  – Four channels with three playing modes: 9-bit ADPCM, 8-bit PCM and 8-bit melody
  – One 16-byte buffer and 6-bit volume control per channel
  – Wavetable melody support
  – Two dedicated PWM outputs for direct driving
  – One 12-bit current DAC
- **Universal Asynchronous Receiver/Transmitter (UART)**
  – Full-duplex operation
  – Baud rate generator with one digital PLL
  – Standard baud rates of 600 bps to 115.2 kbps
  – Both transmitter and receiver buffers supported
  – Direct glueless support of IrDA physical layer protocol
  – Two sets of I/Os (TX,RX) for two independent devices
- **Serial Peripheral Interface (SPI)**
  – Master and slave modes
  – Five serial signals including enable and data-ready
  – Both transmitter and receiver buffers supported
  – Programmable data length from 7-bit to 16-bit
- **Vlcd/LVD trimming fuse function:**
  – Vlcd default voltage variation trimming.
  – 4-level LVD voltage variation trimming.
- **Three power down modes**
  – WAI0 mode
  – WAI1 mode
  – STP mode

# 4 SIGNAL DESCRIPTIONS

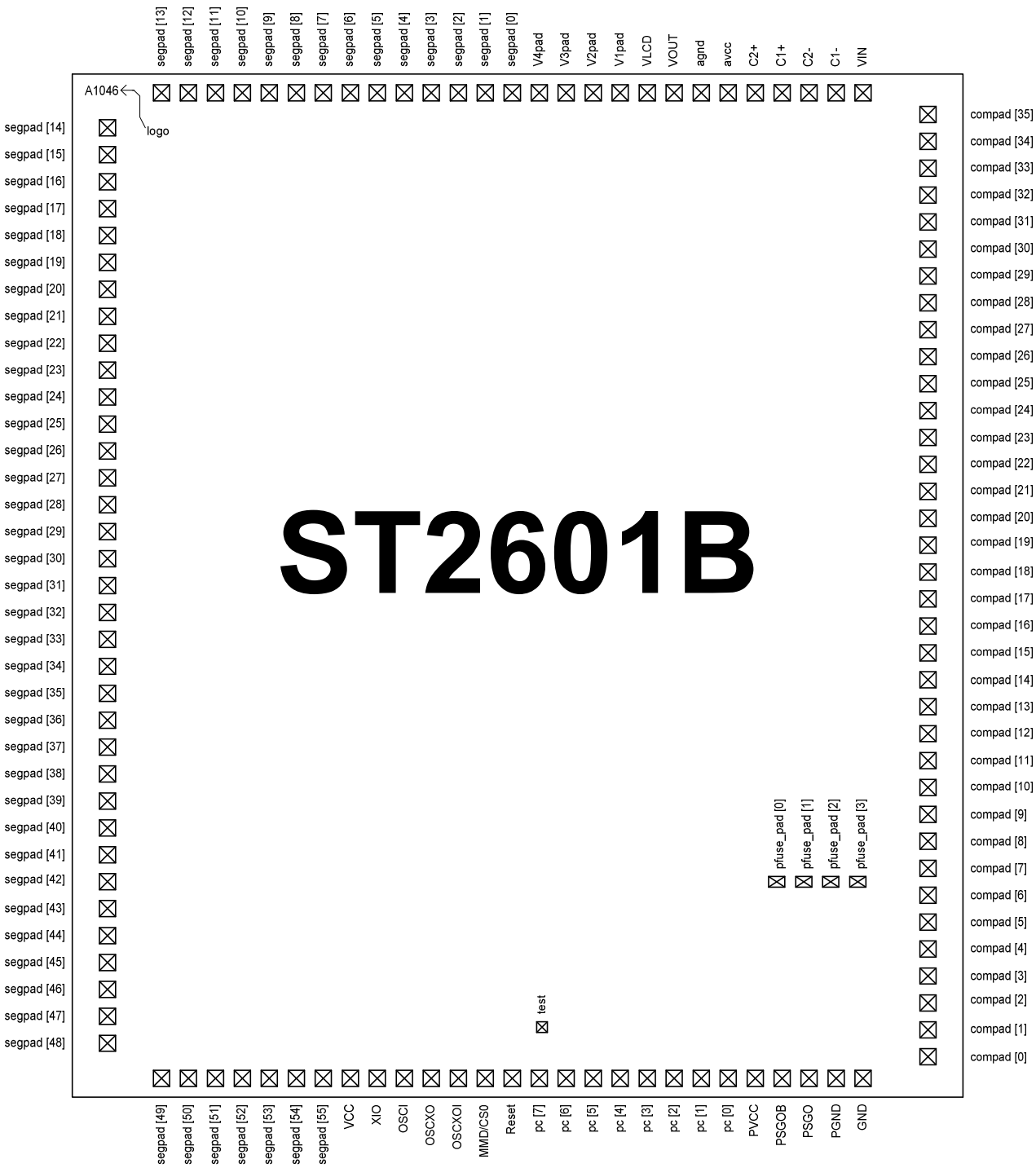
**TABLE 4-1 Signal Function Groups**

| Function Group | Pad No. | Designation | Description |
|---|---|---|---|
| Power | | VCC , PVCC, AVCC | **VCC:** Power supply for system<br>**AVCC:** Power supply for LCD function<br>**PVCC:** Power supply for PSGO and PSGOB |
| Ground | | GND , PGND, AGND | **GND:** System power ground<br>**AGND:** Power ground for LCD function<br>**PGND:** Power ground for PSGO and PSGOB |
| System control | | $\overline{\text{RESET}}$,<br>TEST,<br>MMD/$\overline{\text{CS0}}$ | $\overline{\text{RESET}}$ **:** Active low system reset signal input<br>**TEST:** Leave this pin open when normal operation<br>**MMD/**$\overline{\text{CS0}}$**:** Memory modes selection pin<br>**Normal mode:** Enable internal ROM.<br>MMD/$\overline{\text{CS0}}$ is connected to GND.<br>**Emulation mode:** Disable internal ROM.<br>MMD/$\overline{\text{CS0}}$ is connected to the chip-select pin of external ROM. During reset period, the MMD/$\overline{\text{CS0}}$ is an internally pulled-up input pin. After reset cycles, MMD/$\overline{\text{CS0}}$ is changed to be an output pin. It will output signal $\overline{\text{CS0}}$. |
| Clock | | XIO,OSCI<br>OSCXO,OSCXI, , | High frequency oscillator (OSC) mode selected by code-option<br>**Crystal mode:** One crystal or resonator should be connected between OSCI and XIO<br>**Resistor oscillator mode:** One resistor should be connected between OSCI and VCC<br>**OSCXI, OSCXO:** Connect one 32768Hz crystal between these two pins when using low frequency oscillator |
| External memory bus signals / LCD drivers | | $\overline{\text{WR}}$ / SEG9,<br>$\overline{\text{RD}}$ / SEG8 | External memory R/W control signals / LCD Segment drivers |
| | | A[22:0]/SEG32~SEG10 | External memory address bus / LCD Segment drivers |
| | | D[7:0]/SEG7~SEG0 | External memory data bus / LCD Segment drivers |
| PSG/PWM DAC | | PSGO, PSGOB | PSG outputs. Connect to one buzzer or speaker |
| Chip selects / LCD drivers | | $\overline{\text{CS5}} \sim \overline{1}$/PD4~0 / SEG33~SEG37,<br>$\overline{\text{CS6}}$ /A23/PD5 /SEG38 | I/O port D and chip-select outputs / LCD Segment drivers |
| UART | | RXD0/PC7,TXD0/PC6, RXD1/PD7/SEG40,TXD1/ PD6/SEG39 | UART signals and I/Os / LCD Segment drivers |
| SPI | | $\overline{\text{DATA\_READY}}$/PC5 , $\overline{\text{SS}}$/PC4 , SDO/PC3 , SDI/PC2 , SCK/PC1 | SPI signals and I/Os |

**TABLE 4-2 Signal Function Groups (continued)**

| Function Group | Pad No. | Designation | Description |
|---|---|---|---|
| External clock/signal interrupt | | INTX/PC0 | External interrupt inputs |
| Clocking output | | BCO/PE2/SEG43 , TCO1/PE1/SEG42 , TCO0/PE0/SEG41 | Clocking outputs / LCD Segment drivers |
| GPIO / LCD drivers | | PE6~3/SEG47~SEG44 | I/O port E/ LCD Segment drivers |
| LCD control signals (for controller mode) | | BLANK/COM0, POFF/COM1, FLM/COM2, LOAD1/COM3, LOAD2/COM4, AC/COM5,CP/COM6, EIO/COM7, LD7~LD0/COM15/COM8 | LCD control signals |
| LCD voltage source | | Vout, Vlcd, V1, V2, V3, V4 | LCD voltage sources |
| LCD voltage booster | | C1+, C1-, C2+, C2- | Connect a 0.1 uF between C1+ and C1-, C2+ and C2- repectively. |
| Low Voltage Detector | | VIN | Analog input pin of Low Voltage Dector module |

# 5 PAD DIAGRAM



# 6 DEVICE INFORMATION

1. **Pad size: 90um x 90um**
2. **Substrate: GND**
3. **Chip size: 3520 um x 3800 um**

| PAD No. | Symbol | X | Y |
|---|---|---|---|
| 1 | SEG[14] | -1690.0 | 1750.5 |
| 2 | SEG[15] | -1690.0 | 1640.5 |
| 3 | SEG[16] | -1690.0 | 1530.5 |
| 4 | SEG[17] | -1690.0 | 1420.5 |
| 5 | SEG[18] | -1690.0 | 1315.0 |
| 6 | SEG[19] | -1690.0 | 1215.0 |
| 7 | SEG[20] | -1690.0 | 1115.0 |
| 8 | SEG[21] | -1690.0 | 1015.0 |
| 9 | SEG[22] | -1690.0 | 915.0 |
| 10 | SEG[23] | -1690.0 | 808.0 |
| 11 | SEG[24] | -1690.0 | 702.5 |
| 12 | SEG[25] | -1690.0 | 602.5 |
| 13 | SEG[26] | -1690.0 | 502.5 |
| 14 | SEG[27] | -1690.0 | 402.5 |
| 15 | SEG[28] | -1690.0 | 302.5 |
| 16 | SEG[29] | -1690.0 | 202.5 |
| 17 | SEG[30] | -1690.0 | 102.5 |
| 18 | SEG[31] | -1690.0 | 2.5 |
| 19 | SEG[32] | -1690.0 | -101.0 |
| 20 | SEG[33] | -1690.0 | -201.0 |
| 21 | SEG[34] | -1690.0 | -306.5 |
| 22 | SEG[35] | -1690.0 | -416.5 |
| 23 | SEG[36] | -1690.0 | -522.0 |
| 24 | SEG[37] | -1690.0 | -622.0 |
| 25 | SEG[38] | -1690.0 | -722.0 |
| 26 | SEG[39] | -1690.0 | -822.0 |
| 27 | SEG[40] | -1690.0 | -922.0 |
| 28 | SEG[41] | -1690.0 | -1029.0 |
| 29 | SEG[42] | -1690.0 | -1134.5 |
| 30 | SEG[43] | -1690.0 | -1234.5 |
| 31 | SEG[44] | -1690.0 | -1334.5 |
| 32 | SEG[45] | -1690.0 | -1434.5 |
| 33 | SEG[46] | -1690.0 | -1540.0 |
| 34 | SEG[47] | -1690.0 | -1650.0 |
| 35 | SEG[48] | -1690.0 | -1760.0 |

| PAD No. | Symbol | X | Y |
|---|---|---|---|
| 36 | SEG[49] | -1348.3 | -1830.0 |
| 37 | SEG[50] | -1238.3 | -1830.0 |
| 38 | SEG[51] | -1128.3 | -1830.0 |
| 39 | SEG[52] | -1028.3 | -1830.0 |
| 40 | SEG[53] | -928.3 | -1830.0 |
| 41 | SEG[54] | -828.3 | -1830.0 |
| 42 | SEG[55] | -728.3 | -1830.0 |
| 43 | VCC | -607.0 | -1830.0 |
| 44 | XIO | -502.0 | -1830.0 |
| 45 | OSCI | -402.0 | -1830.0 |
| 46 | OSCXO | -302.0 | -1830.0 |
| 47 | OSCXI | -202.0 | -1830.0 |
| 48 | MMD/CS0 | -102.0 | -1830.0 |
| 49 | RESETB | -2.0 | -1830.0 |
| 50 | PC[7] | 101.7 | -1830.0 |
| 51 | TEST | 103.2 | -1650.95 |
| 52 | PC[6] | 201.7 | -1830.0 |
| 53 | PC[5] | 301.7 | -1830.0 |
| 54 | PC[4] | 401.7 | -1830.0 |
| 55 | PC[3] | 501.7 | -1830.0 |
| 56 | PC[2] | 601.7 | -1830.0 |
| 57 | PC[1] | 701.7 | -1830.0 |
| 58 | PC[0] | 801.7 | -1830.0 |
| 59 | PVCC | 918.8 | -1830.0 |
| 60 | PSGOB | 1031.9 | -1830.0 |
| 61 | PSGO | 1158.1 | -1830.0 |
| 62 | PGND | 1271.2 | -1830.0 |
| 63 | GND | 1389.9 | -1830.0 |
| 64 | COM[0] | 1690.0 | -1786.6 |
| 65 | COM[1] | 1690.0 | -1676.6 |
| 66 | COM[2] | 1690.0 | -1566.6 |
| 67 | COM[3] | 1690.0 | -1466.6 |
| 68 | COM[4] | 1690.0 | -1366.6 |
| 69 | COM[5] | 1690.0 | -1266.6 |
| 70 | COM[6] | 1690.0 | -1166.6 |

| PAD No. | Symbol | X | Y |
|---|---|---|---|
| 71 | COM[7] | 1690.0 | -1066.6 |
| 72 | COM[8] | 1690.0 | -966.6 |
| 73 | COM[9] | 1690.0 | -866.6 |
| 74 | COM[10] | 1690.0 | -766.6 |
| 75 | COM[11] | 1690.0 | -666.6 |
| 76 | COM[12] | 1690.0 | -566.6 |
| 77 | COM[13] | 1690.0 | -466.6 |
| 78 | COM[14] | 1690.0 | -366.6 |
| 79 | COM[15] | 1690.0 | -266.6 |
| 80 | COM[16] | 1690.0 | -166.6 |
| 81 | COM[17] | 1690.0 | -66.6 |
| 82 | COM[18] | 1690.0 | 33.4 |
| 83 | COM[19] | 1690.0 | 133.4 |
| 84 | COM[20] | 1690.0 | 233.4 |
| 85 | COM[21] | 1690.0 | 333.4 |
| 86 | COM[22] | 1690.0 | 433.4 |
| 87 | COM[23] | 1690.0 | 533.4 |
| 88 | COM[24] | 1690.0 | 633.4 |
| 89 | COM[25] | 1690.0 | 733.4 |
| 90 | COM[26] | 1690.0 | 833.4 |
| 91 | COM[27] | 1690.0 | 933.4 |
| 92 | COM[28] | 1690.0 | 1033.4 |
| 93 | COM[29] | 1690.0 | 1133.4 |
| 94 | COM[30] | 1690.0 | 1233.4 |
| 95 | COM[31] | 1690.0 | 1333.4 |
| 96 | COM[32] | 1690.0 | 1434.6 |
| 97 | COM[33] | 1690.0 | 1534.6 |
| 98 | COM[34] | 1690.0 | 1644.6 |
| 99 | COM[35] | 1690.0 | 1754.6 |
| 100 | VIN | 1362.1 | 1830.0 |
| 101 | C1- | 1234.35 | 1830.0 |
| 102 | C2- | 1124.35 | 1830.0 |
| 103 | C1+ | 1021.05 | 1830.0 |
| 104 | C2+ | 921.05 | 1830.0 |
| 105 | AVCC | 819.05 | 1830.0 |

| PAD No. | Symbol | X | Y |
|---|---|---|---|
| 106 | AGND | 717.45 | 1830.0 |
| 107 | VOUT | 615.45 | 1830.0 |
| 108 | VLCD | 515.45 | 1830.0 |
| 109 | V1 | 413.95 | 1830.0 |
| 110 | V2 | 313.95 | 1830.0 |
| 111 | V3 | 213.95 | 1830.0 |
| 112 | V4 | 113.55 | 1830.0 |
| 113 | SEG[0] | 7.95 | 1830.0 |
| 114 | SEG[1] | -92.05 | 1830.0 |
| 115 | SEG[2] | -192.05 | 1830.0 |
| 116 | SEG[3] | -292.05 | 1830.0 |
| 117 | SEG[4] | -392.05 | 1830.0 |
| 118 | SEG[5] | -492.05 | 1830.0 |
| 119 | SEG[6] | -592.05 | 1830.0 |
| 120 | SEG[7] | -692.05 | 1830.0 |
| 121 | SEG[8] | -792.05 | 1830.0 |
| 122 | SEG[9] | -892.05 | 1830.0 |
| 123 | SEG[10] | -992.05 | 1830.0 |
| 124 | SEG[11] | -1092.05 | 1830.0 |
| 125 | SEG[12] | -1202.05 | 1830.0 |
| 126 | SEG[13] | -1312.05 | 1830.0 |

| PAD No. | Symbol | X | Y |
|---|---|---|---|

| PAD No. | Symbol | X | Y |
|---|---|---|---|

# 7 ELECTRICAL CHARACTERISTICS

## 7.1 Absolute Maximum Rations

DC Supply Voltage ---------- -0.3V to +4.5V
Operating Ambient Temperature ---------- -10°C to +60°C
Storage Temperature ---------- -10°C to +125°C

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. All the ranges are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

## 7.2 DC/AC Electrical Characteristics

Standard operation conditions: VCC = 3.0V, GND = 0V, $T_A$ = 25°C, OSC = 4M Hz, unless otherwise specified

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating Voltage | VCC | 2.4 | 3.0 | 3.6 | V | Fosc = 3MHz |
| | | 2.7 | 3.0 | 3.6 | V | Fosc = 4MHz |
| Operating Frequency | $F_1$ | - | - | 3 | MHz | VCC = 2.4V ~ 3.6V |
| Operating Frequency | $F_2$ | - | - | 4 | MHz | VCC = 2.7 ~ 3.6V |
| Operating Current | $I_{OP}$ | | 2.5 | 3 | mA | All I/O port are input and pull-up, execute NOP instruction, LCDC on |
| Standby Current | $I_{SB0}$ | | 450 | 550 | μA | All I/O port are input and pull-up, OSCX on, LCDC off (WAIT0 mode) |
| Standby Current | $I_{SB1}$ | | 3.5 | 5 | μA | All I/O port are input and pull-up, OSCX on, LCDC off (WAIT1 mode) |
| Standby Current | $I_{SB2}$ | | 0.5 | 1 | μA | All I/O port are input and pull-up, OSCX off, LCDC off (WAIT1 mode) |
| Standby Current | $I_{SB3}$ | | 100 | 130 | υA | LCD on, sysck = LCDCK = OSCX, OSC off, Wait0, no panel (fast B/W mode) |
| Input High Voltage | $V_{IH}$ | 0.7Vcc | | Vcc+0.3 | V | Port-C/D/E/L |
| | | 0.85Vcc | | | V | $\overline{\text{RESET}}$ |
| Input Low Voltage | $V_{IL}$ | GND-0.3 | | 0.3Vcc | V | Port-C/D/E/L |
| | | | | 0.15Vccc | V | $\overline{\text{RESET}}$ |
| Pull-up resistance | $R_{IH}$ | | 150 | | KΩ | Port-C/D/E/L (input Voltage=0.7VCC) |
| Output high voltage | $V_{OH1}$ | 0.7Vcc | | | V | Port-C/D/L ($I_{OH}$ =-6mA) |
| Output low voltage | $V_{OL1}$ | | | 0.3Vcc | V | Port-C/D/E/L ($I_{OL}$ =9mA) |
| Output high voltage | $V_{OH2}$ | 0.7Vcc | | | V | PSG0/PSG0B( in PWM mode), $I_{OH}$ = 35mA. |
| Output low voltage | $V_{OL2}$ | | | 0.3Vcc | V | PSG0/PSG0B( in PWM mode), $I_{OL}$ = -65mA. |
| DAC current | | 2.4mA | 3 | 3.6mA | | DAC output current of maximum digital input value |
| Low Voltage Detector current | $I_{LVR}$ | | 30 | 60 | μA | Total LVD current consumption |
| Vlcd variation | | -3% | | +3% | | |
| INT LVD variation | | -4% | | +4% | | |
| EXT LVD variation | | -4% | | +4% | | |
| SPI clock frequency | | | - | 4.0 | MHz | SPI slave mode |

## 7.3 AC Electrical Characteristics

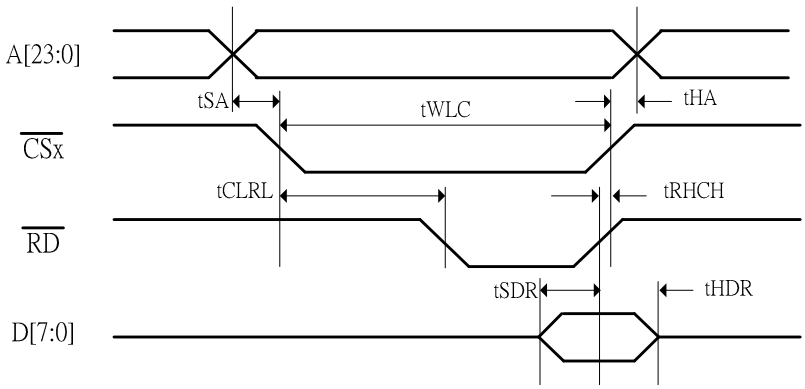



**FIGURE 7-1 External Read Timing Diagram**

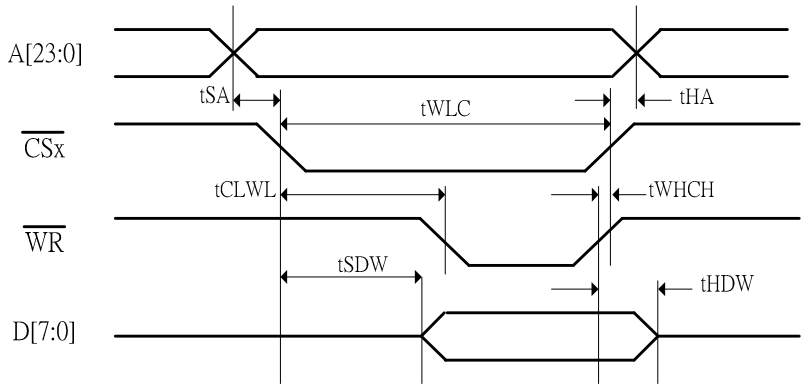



**FIGURE 7-2 External Write Timing Diagram**

**TABLE 7-1 Timing parameters for FIGURE 7-1 and FIGURE 7-2**

Standard operation conditions: VCC = 3.0V, GND = 0V, $T_A$ = 25°C

| Symbol | Characteristic | Rating | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| tSA | Address setup time | — | — | 10 | ns |
| tHA | Address hold time | 0 | — | — | ns |
| tWLC | CS "L" pulse width | 166 | — | — | ns |
| tCLWL | CS asserted to $\overline{WR}$ asserted | — | 1/2 tWLC | — | ns |
| tWHCH | CS negated after $\overline{WR}$ is negated | 10 | — | — | ns |
| tSDW | CS asserted to data-out is valid | — | 1/2 tWLC | — | ns |
| tHDW | Data-out hold time after $\overline{WR}$ is negated | 20 | — | | ns |
| tCLRL | CS asserted to $\overline{RD}$ asserted | — | 1/2 tWLC | — | ns |
| tRHCH | CS negated after $\overline{RD}$ is negated | 10 | — | — | ns |
| tSDR | Data-in valid before $\overline{RD}$ is negated | 30 | — | — | ns |
| tHDR | Data-in hold time after $\overline{RD}$ is negated | 10 | — | — | ns |
| tR | Signal rise time | — | 20 | — | ns |
| tF | Signal fall time | — | 10 | — | ns |

## 7.4 Characteristic Charts

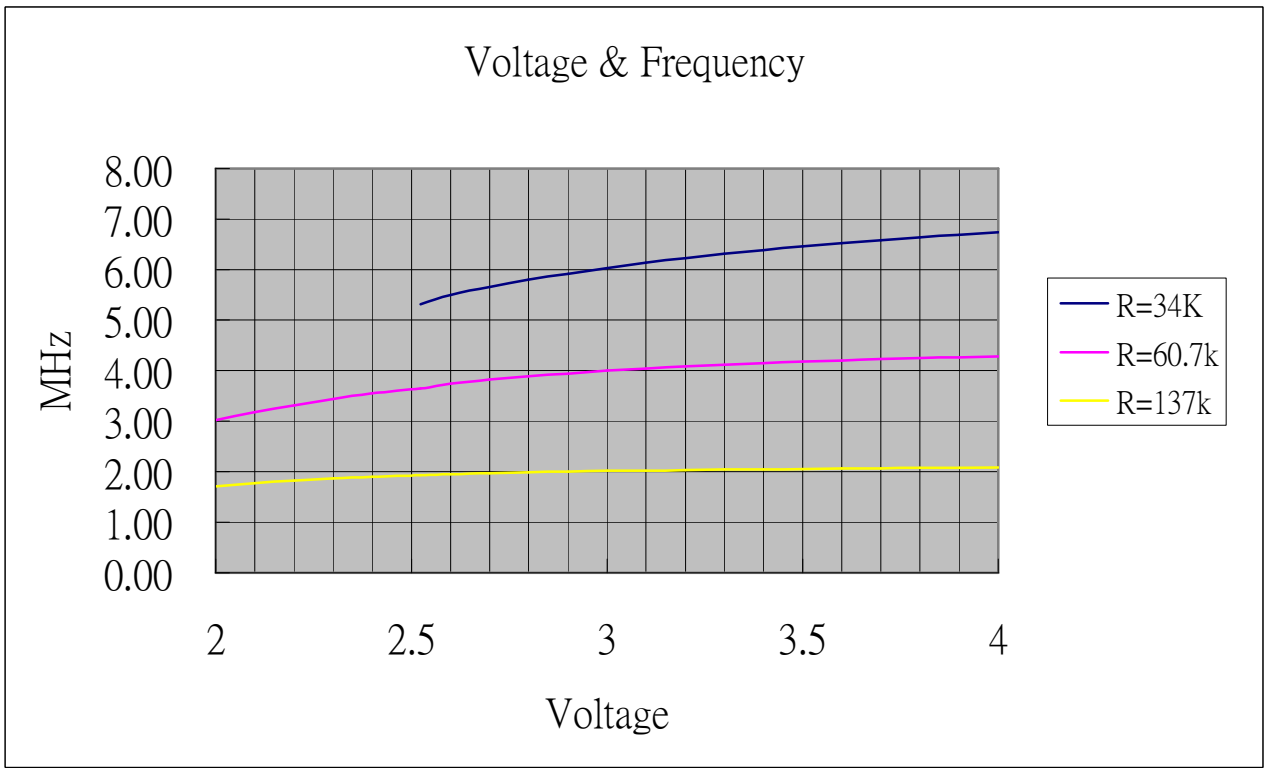



**FIGURE 7-3 Frequency of R-OSC as a function of VCC**

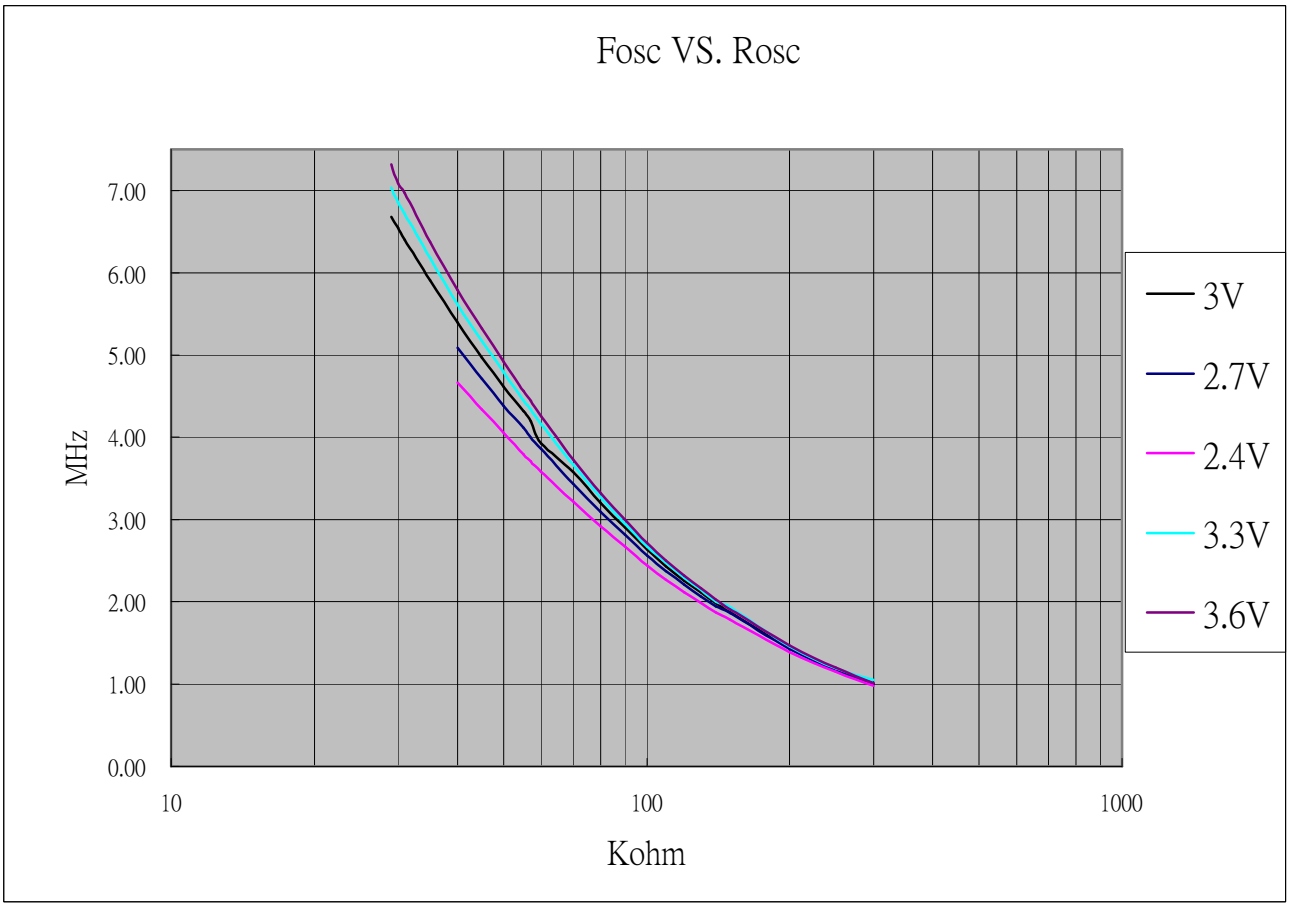
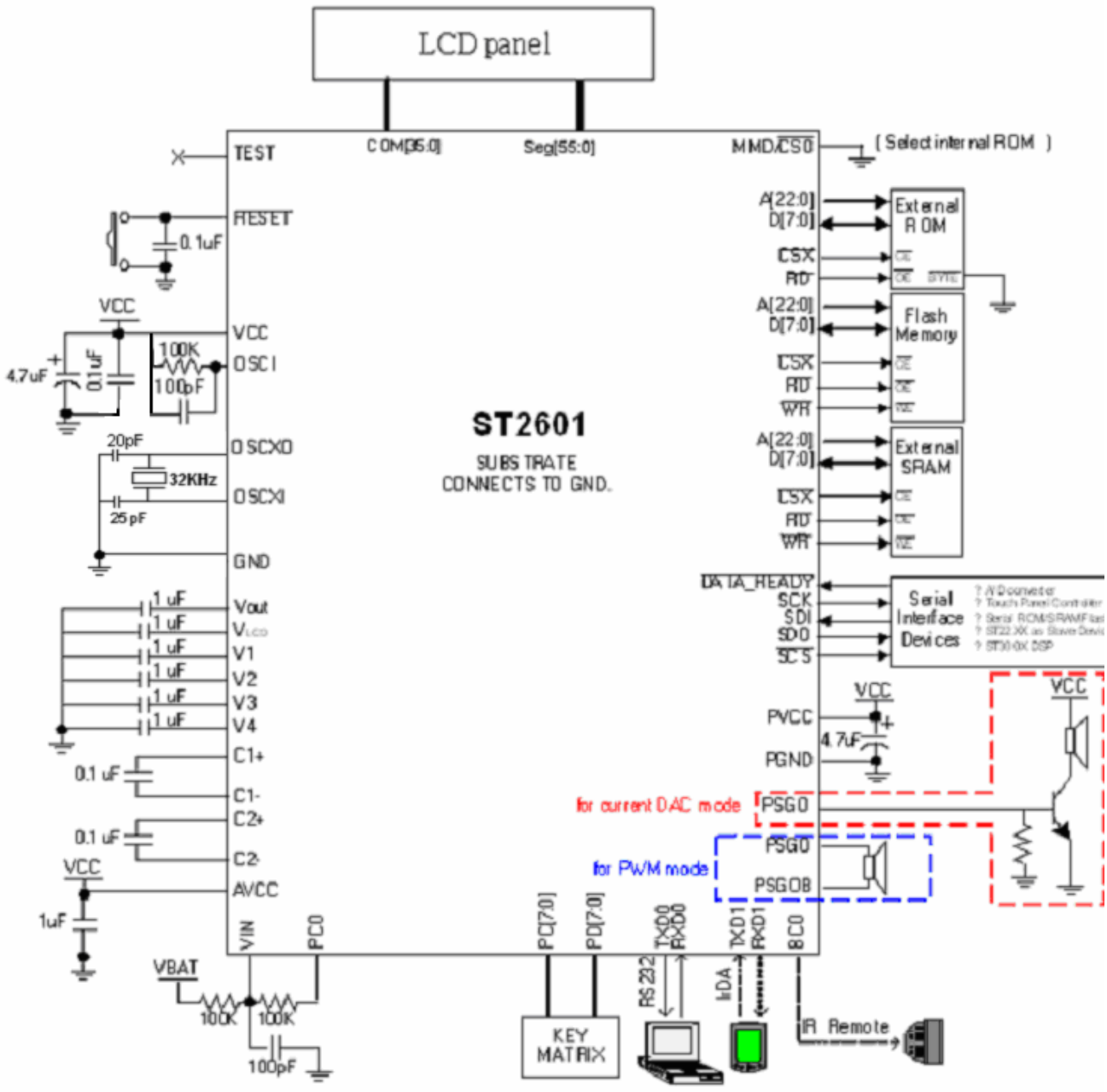



**FIGURE 7-4 Frequency of R-OSC as a function of RESISTANCE**

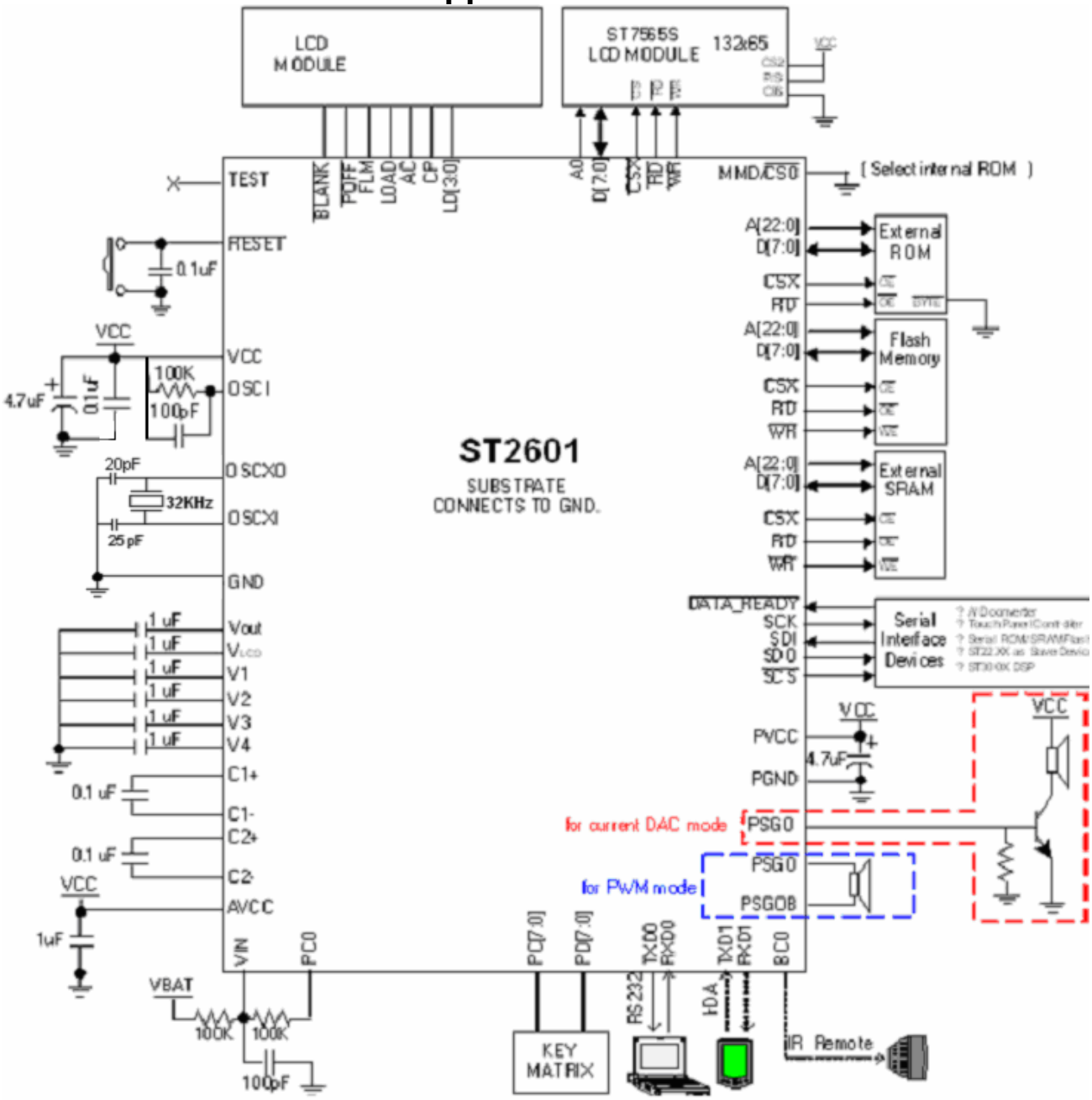
| Voltage / Frequency | 3V |
|---|---|
| 4MHz | 60K Ohm |
| 3MHz | 90K Ohm |
| 2MHz | 140K Ohm |
| 1MHz | 300K Ohm |
| | |

# 8 APPLICATION CIRCUITS

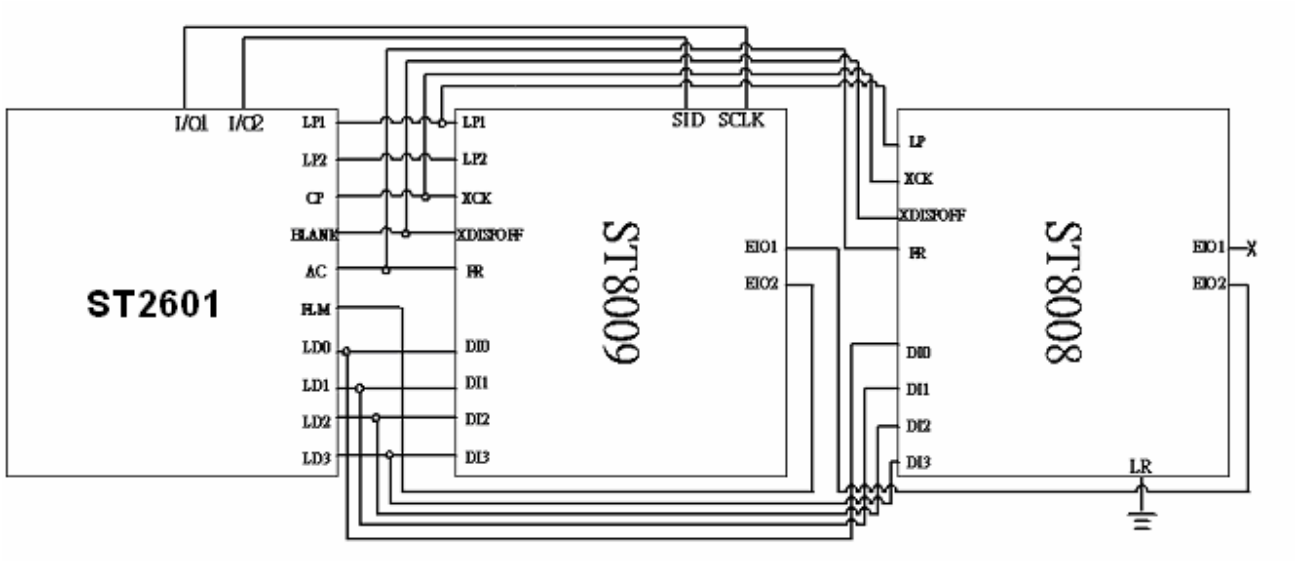
## ST2601B Application Circuit 1



# ST2601B Application Circuit 2



# ST2601B+ST8008+ST8009 Application Circuit




Note:
LR pin of ST8008 is connected to GND.
L/R bit of ST8009 is configured as low by “interface control selection” instruction

# 9 FEATURE COMPARISON OF ST26XXB SERIES

| Part Number | ST2608B | ST2604B | ST2602B | ST2601B |
|---|---|---|---|---|
| ROM | 1M Byte | 512K Byte | 256K Byte | 128K Byte |
| RAM | 5K Byte | 3.5K Byte | 2.5K Byte | 1.5K Byte |
| Built-in LCD Driver | 36 COMs X 72 SEGs | 36 COMs X 64 SEGs | 36 COMs X 56 SEGs | 36 COMs X 56 SEGs |
| Driving LCD with ext. driver | ~9000 dots (16 gray)<br>~36000 dots (mono) | ~6000 dots (16 gray)<br>~24000 dots (mono) | ~4000 dots (16 gray)<br>~16000 dots (mono) | ~2500dots (16 gray)<br>~10000 dots (mono) |
| Dedicated I/O | 24 (PA, PC, PL) | 16 (PA, PC) | 8 (PC) | 8 (PC) |
| LCD-Shared I/O | 32 (PB, PD, PE, PF) | 39 (PB[6:0], PD, PE, PL, PF) | 31 (PD, PE[6:0], PL, PF) | 31 (PD, PE[6:0], PL, PF) |
| LCD gray level | 16 gray levels | | | |
| PSG / volume-control | 4-channel wavetable / 64 levels | | | |
| DAC | 9-bit PWM, 12-bit current DAC | | | |
| Low voltage detector | 4 levels | | | |
| Low voltage reset | Yes | | | |
| Watchdog timer | Yes | | | |
| Serieal interface | UART, SPI, IrDA | | | |
| | | | | |
| Trimming fuse | YES | | | |
| LCDCK=32KHz | YES | | | |

## 9.1 LCFG Setting Difference of ST2600B series

ST2608B

| CFGS[2~0] | Pad Definition | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | SEG0~31 | SEG32 | SEG33~38 | SEG39 | SEG40 | SEG41~47 | SEG48~55 | SEG56~63 | SEG64~71 |
| 00X | SEG0~71 | | | | | | | | |
| 010 | SEG0~63 | | | | | | | | PE0~PE7 |
| 011 | SEG0~55 | | | | | | | PB0~PB7 | PE0~PE7 |
| 100 | SEG0~47 | | | | | | No Use | PB0~PB7 | PE0~PE7 |
| 101 | SEG0~31 | No Use | PD0~PD7 | | | No Use | | PB0~PB7 | PE0~PE7 |
| 110 | A/D Bus | | PD0~PD6 | | SEG0~31 | | | | |
| 111 | A/D Bus | | PD0~PD7 | | | No Use | | PB0~PB7 | PE0~PE7 |

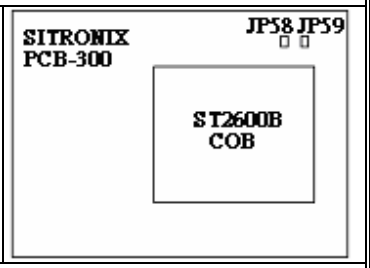
ST2604/ST2604B

| CFGS[2~0] | Pad Definition | | | | | | |
|---|---|---|---|---|---|---|---|
| | SEG0~31 | SEG32 | SEG33~39 | SEG40 | SEG41~47 | SEG48~55 | SEG56~63 |
| 000 | SEG0 ~ 63 | | | | | | |
| 001 | SEG0 ~ 39 | | | PD7 | PB0 ~ 6 | PE0 ~ 7 | PL0 ~ 7 |
| 010 | SEG0 ~ 63 | | | | | | |
| 011 | SEG0 ~ 55 | | | | | | PL0 ~ 7 |
| 100 | SEG0 ~ 47 | | | | | PE0 ~ 7 | PL0 ~ 7 |
| 101 | SEG0 ~ 31 | A22 | PD0 ~ 7 | | PB0 ~ 6 | PE0 ~ 7 | PL0 ~ 7 |
| 110 | A/D bus | | PD0 ~ 7 | | PB0 ~ 6 | PE0 ~ 7 | PL0 ~ 7 |
| 111 | A/D bus | | PD0 ~ 7 | | PB0 ~ 6 | PE0 ~ 7 | PL0 ~ 7 |

ST2601B / ST2602B

| CFGS[2~0] | Pad Definition | | | | | |
|---|---|---|---|---|---|---|
| | SEG0~31 | SEG32 | SEG33~39 | SEG40 | SEG41~47 | SEG48~55 |
| 000 | SEG0 ~ 55 | | | | | |
| 001 | SEG0 ~ 39 | | | PD7 | PE0 ~ 6 | PL0 ~ 7 |
| 010 | SEG0 ~ 55 | | | | | |
| 011 | SEG0 ~ 55 | | | | | |
| 100 | SEG0 ~ 47 | | | | | PL0 ~ 7 |
| 101 | SEG0 ~ 31 | A22 | PD0 ~ 7 | | PE0 ~ 6 | PL0 ~ 7 |
| 110 | A/D bus | | PD0 ~ 7 | | PE0 ~ 6 | PL0 ~ 7 |
| 111 | A/D bus | | PD0 ~ 7 | | PE0 ~ 6 | PL0 ~ 7 |

# 10 CHECK LIST

| Check List of ST2601B-□□□□ | |
|---|---|
| 8-Bit Microcontroller With 128K Bytes ROM | |
| CODE OPTION<br>LOW VOLTAGE RESET | □1.4 Volt □2.1 Volt |
| OSCILLATOR | □32768 Hz Crystal<br>□R-OSC MHz (Resistor = KΩ)<br>□Resonator □Crystal MHz |
| OPERATING VOLTAGE | □2.4V ~ 3.6V □2.7V ~ 3.6V<br>□Regulator V □Other Range ~ V |
| | Note: Maximum operating frequency = 4.0 Mhz@2.7V, 3.0 Mhz@2.4V |
| BATTERY | □CR20 x □AAx □AAAx □ |
| POWER DOWN MODES | □WAI-0 □WAI-1 |
| LOW VOLTAGE DETECTOR | Disabled<br>□Internal-LVD level1(2.4V) □Internal-LVD level2(2.6V)<br>□Internal-LVD level3(2.8V) □Internal-LVD level4(3.0V)<br>□External-LVD level1(1.2V) □External-LVD level2(1.3V)<br>□External-LVD level3(1.4V) □External-LVD level4(1.5V) |
| UART | □Enabled, Baud Rate: bps □Disabled |
| SPI | □Enabled, Bit Rate: bps □Disabled |
| ST2600B EV<br>mode Selection<br>Please check ST2600B DVB<br>(PCB-300) | □ ST2601B EV mode: JP58 2→3 JP59 1→2<br>  |
| LCD SPECIFICATIONS | Resolution: x Duty: 1/ Bias: 1/ VLCD: V<br>Frame Rate: Hz Alternation: Every □Frame □ Lines |
| | Driver: □ST8012x □ST8008x □ST8009x □ST8011x |
| LCD Gray-level | □Black and White □4 Gray-level □16 Gray-level |
| PSG mode | Current-type DAC<br>□ PWM-single pin □ PWM-two pin push pull □PWM-two pin two end |
| Register Value | When playing sound: the PSGC = ,<br>When LCD is on: LCKR= , LCTR= , LFRA = ,LXMAX= ,<br>LYMAX= , LPOW = LREG = , LCFG =<br>When LVD is on: LVCTR =<br>When power down: SYS = (WAIT0 or WAIT1) |

| | | |
|---|---|---|
| Data sheet | ST2601B user's manual Ver | |
| CODE FILE: .BIN | | DATE(Y/M/D): 20 / / |
| CHECK SUM: □□□□H (Byte Mode) | | |
| Note: a. File format must be binary and the extension should be ".BIN".<br>b. File should be wrapped in ZIP format for transferring or e-mailing.<br>c. Only single file is allowed.<br>d. File length is 128K bytes.<br>e. Functions should be checked on the emulation board or by real chip.<br>f. Electric characteristics of the emulation board are not identical with those of the real chip. | | |
| CUSTOMER | | |
| COMPANY | | |
| SIGNATURE | | |
| SITRONIX | | |
| FAE/SA | | |
| SALSE | | |

**Project Name** _____ DATE: _____

| | ITEM | CHECK | NOTE |
|---|---|---|---|
| 1. | Make sure the resistor of R-OSC matches the desired frequency and VCC | | |
| 2. | Make sure the referenced data sheet is the most updated version | | |
| 3. | After power on, enter wait-1 mode for0.5 second before normal operation | | |
| 4. | Initialize user RAM and every related control register | | |
| 5. | Confirm Vlcd level, duty, bias, frame rate, alternating rate and the display quality of LCD | | |
| 6. | Make sure to set LCKR=00h before turning off LCD function | | |
| 7. | Make sure to implement a mechanism to fine-tune LCD contrast level. The mechanism could be pin-option or keying-adjustment. | | |
| 8. | Confirm PSG output mode: Current DAC or one of three PWM modes | | |
| 9. | Before entering power down mode, turn off unused peripheral such as LCD controller, PSG, Current DAC and LVD | | |
| 10. | Confirm I/O direction, default state and function-enable bits. Enable pull-up for unused input pins | | |
| 11. | Read from an input port after the signals are stable. Ex. when doing key scan, delay 12 us from a new scan value then read the return lines. | | |
| 12. | If an input connects to VCC or GND directly, make sure to remove any DC current from internal pull-up/down resistor after the status is read. | | |
| 13. | Do not use “read-modify-write” instructions, e.g. ROR and SMB0, to the registers that are read-only, write-only or have different functions for read and write. The registers at least include PA ~ PF, PL, PCL, PSGxA, PSGxB, TxCH, TxCL, PRS, BTSR, BTC, MULL, MULH, MISC, SYS, IREQL, IREQH, LSSAL, LSSAH, LVPW, LCKR, LFRA, LPAL, SDATAH, SDATAL, SSR, DMSL, DMSH, DMDL, DMDH, DCNTL, DCNTH, LVCTR, UDATA and USR. | | |
| 14. | Disable unused functions and reserve “RTI” instruction for unused interrupt vectors | | |
| 15. | Always disable interrupt function (by an ‘SEI’ instruction) when modifying the IENAL, IENAH, IREQL and IREQH registers. | | |
| 16. | Check stack memory is limited within 256 bytes. | | |
| 17. | Design a test mode to check every possible function | | |
| 18. | Follow the standard operation flow of using LCDCK=32KHz. | | |
| 19. | Use ST2600B (enable ST2602B EV mode), to develop the whole system., and verify every functions, especially sound quality and LCD performance. | | |
| 20. | RC-type OSC has inter-sample variation.<br>For frequency-sensitive application (for example:IR communication and speech sampling rate), please use 32KHz_OSC to calibrate RC-type OSC by firmware | | |
| 21. | Fill up ROM until there has no empty place. (total 131072 bytes) | | |

**Engineer** _____ **Manager** _____

# ST26xxB application note:

## Content:

1. PSG: Current-DAC and PWM application circuit
2. Methods to make up LCD voltage deviation
3. Vertical Cross talk on LCD display
4. How to use IrDA mode to generate 38kHz carrier with data?
5. LCDCK=32k clock source on ST2602B/ST2608B display
6. System clock switching from OSC to OSCX
7. Measure RC-OSC system clock
8. IrDA mode application note
9. ST26xx UART details
10. IrDA BGRCK generation source
11. OC-OSC / X'tal application circuit
12. LCD blink cause by PSG
13. How to measure the internal current of ST2600B?
14. Ways to save power consumption
15. 32KHz (OSCX) application circuit
16. ST26XX+ST8008 CASCADE MODE CONNECTION
17. Standard flow for switching I/O and segment
18. LCDCK=32K with cascade mode
19. User Manual for ST2600B external bus usage
20. Pull-up resistance of D0~D7 for current issue when using ST75xx

**Version 1.09**

## <PSG: Current-DAC and PWM application circuit>

**Description:**

**(These AP circuits are suitable for ST26xx series IC)**

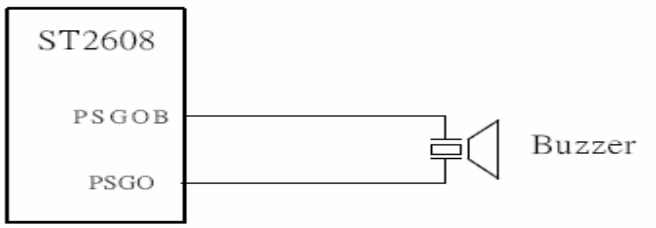



**Figure 1 PWM mode application circuit**

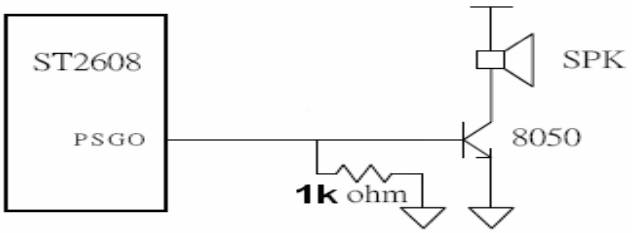



**Figure 2 Current-DAC mode application circuit**

## <Methods to make up LCD voltage deviation >

**Notice1:** **In order to cover the variation of VLCD of LCD panel, be sure to reserve pin-option by GPIO to change the status of VLCD( bit0:3 of register LREG). Here we suggest that there are at least 5-level of voltage pin-option for VLCD. If the GPIO is not enough to make pin-option, programmer can use key-return-line method for power on pin-option.**

For example: make pin-option for change VLCD at…/5.6/5.8/**6.0V**/6.2V/6.4/…

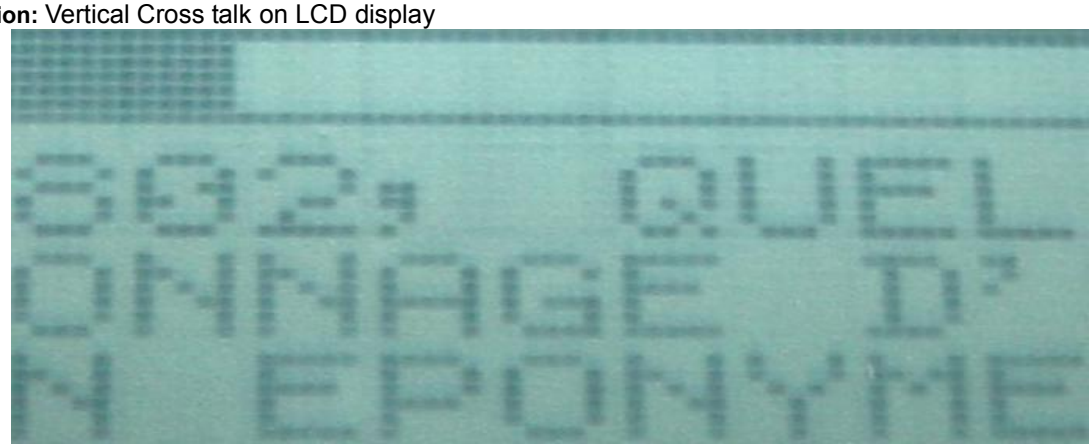
**Notice2:** **Programmer should add a contrast controller function to adjust VLCD for the convenience of end-user to change the contrast as they like.**

For example: VLCD is pre-set at **6.2** by pin-option, end-users can also adjust the contrast…/5.8/5.9V/6.0V/**6.2V**/6.2V/6.3/6.4/…by using contrast controller function.

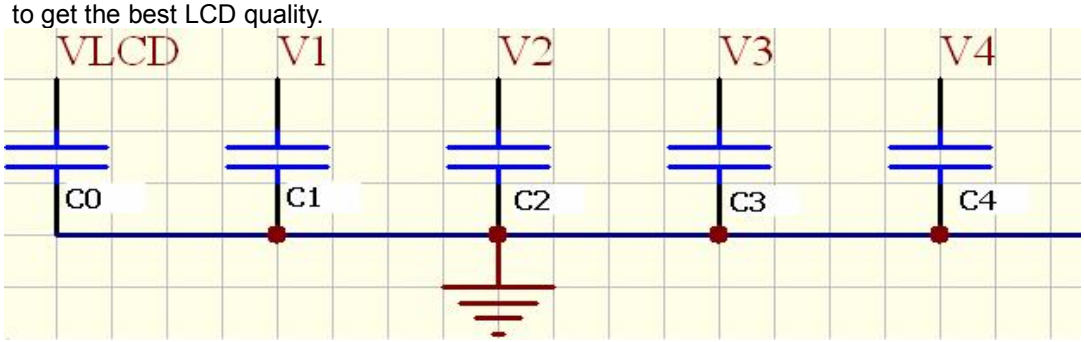
**Notice3:** **Verifying the performance of voice on ST2602/2604/2608 DEMO boards.** Because ST2600B DVB can not provide the totally voice efficacy, such like the volume and the quality of voice. So we strongly suggest to verify voice playing on ST2602B/ST2608B DEMO boards before MASK.
(Ps…Because LCD SEG pins are shared with external EPROM, so the picture can not be verified on DEMO boards.)

## <Vertical Cross talk on LCD display>

**Description:** Vertical Cross talk on LCD display



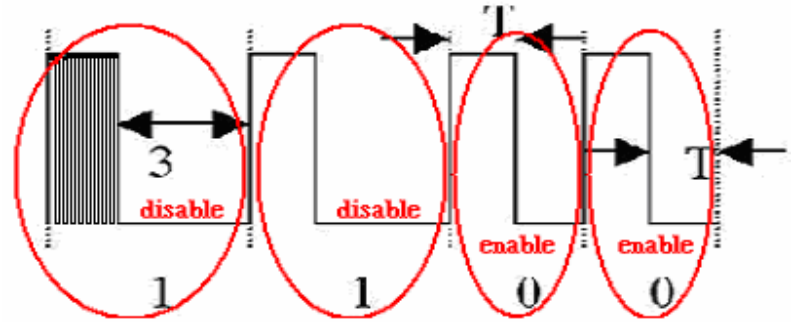
**Solution:** Vertical cross talk usually happens when the differential voltage of V0~V4 are not closely. In this case, increase C0~C4 (recommend > 1uF) will eliminate this problem. Fine tuning the value of capacitance to get the best LCD quality.



## <How to use IrDA mode to generate 38kHz carrier with data?>

Port-E-2 (PE2) is shared with clock signal output function, and the frequency of this pin is programmable. Programmer can define which signal pattern is "0", and which signal is "1"

For example, using Timer_interrupt to enable/disable PE2 function, and programmers can produce the signal pattern which means "0" or "1"
The same way, receive side can decode the signal by encode information.



## <LCDCK=32k clock source on ST2602B/ST2608B display>

**(1)** Control register

| Address | Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **$047** | **LCTR** | R/W | LPWR | BLNK | REV | CAS | GL[3] | GL[2] | GL[1] | GL[0] | 1000 0000 |

Bit 3~2: **GL[3:2]** : LCD gray-level selection bit
00 = B/W.
01 = 4 gray
10 = 16gray
11 = fast B/W mode

**(2)**

| Address | Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **$048** | **LCKR** | W | - | - | LMOD[1] | LMOD[0] | LCK[3] | LCK[2] | LCK[1] | LCK[0] | - - 00 0000 |

Bit [5:4]: **LMOD** : LCD data bus mode selection
00 = 1-bit mode
01 = 4-bit mode
1X = 8-bit mode

Bit 3~0: **LCKR[3:0]** : LCD clock selection (when SYSCK=OSCK)

| LCKR[3:0] | LCDCK (B/W, 4G, 16G mode) | | | LCDCK (fast B/W mode) | | |
|---|---|---|---|---|---|---|
| | 1-bit mode (**LMOD**=00) | 4-bit mode (**LMOD**=01) | 8-bit mode (**LMOD**=1X) | 1-bit mode (**LMOD**=00) | 4-bit mode (**LMOD**=01) | 8-bit mode (**LMOD**=1X) |
| **0000** | SYSCK | | | SYSCK/8 | | |
| 0001 | SYSCK/2 | | | SYSCK/16 | | |
| 0010 | SYSCK /4 | | | SYSCK /32 | | |
| 0011 | SYSCK /6 | | | SYSCK /48 | | |
| 0100 | SYSCK /8 | | | SYSCK /64 | | |
| 0101 | SYSCK /10 | | | SYSCK /80 | | |
| 0110 | SYSCK /12 | | | SYSCK /96 | | |
| 0111 | SYSCK /14 | | | SYSCK /112 | | |
| 1000 | SYSCK /16 | | | SYSCK /128 | | |
| 1001 | SYSCK /18 | | | SYSCK /144 | | |
| 1010 | SYSCK /20 | | | SYSCK /160 | | |
| 1011 | SYSCK /22 | | | SYSCK /176 | | |
| 1100 | SYSCK /24 | | | SYSCK /192 | | |
| 1101 | SYSCK /26 | | | SYSCK /208 | | |
| 1110 | SYSCK /28 | | | SYSCK /224 | | |
| 1111 | SYSCK /30 | | | SYSCK /240 | | |

**(3)** Sysclk is RC:
1. Lcd clock source is Sysclk. If Sysclk is RC, LCD clock source will be RC.
2. In ST2602B, if LCD clock source is RC, B/W, 4G, 16G mode are the same as ST2602.
3. The fast B/W mode is added. In fast B/W mode, the LCDCK will be divided by 8.
4. IF Sysclk is RC and in fast B/W mode, the frame rate is determined as below.

$$Frame\ Rate = \frac{LCDCK}{(LXMAX + LFRA + 1) \cdot (LYMAX * 2)}$$

**(4)** Sysclk is 32K:
1. If Sysclk is 32k, LCD clock source will be 32k.
2. If Sysclk is 32k, LCD can only display B/W.
3. If LCD clock source is 32k, please set GL[3:2]=11(fash B/W mode) . In this condition, LCKR and LPAN control registers will avoid. LCDCK is always 32k hz and the frame rate is only controlled by LFRA control register.
4. If LCD clock source is 32k, DC-DC converter clock (LPCK) will also become 32k. So, user must to change LPCK register to get higher pump frequency(We will provide a macro to take care this part).
5. IF Sysclk is 32K and in fast B/W mode, the frame rate is determined by below equation.

$$Frame\ Rate = \frac{LCDCK}{(LXMAX + LFRA + 1) \cdot (LYMAX * 2)}$$, where LCDCK is 32K hz.

**(5)** change Sysclk from RC to 32K
Step1: let LCD in fast B/W mode
Step2: use the macro “SWITCH_SYSCLK_RC_TO_32K” to change Sysclk to 32K
**(6)** change Sysclk from 32K to RC

Step1: use the macro “SWITCH_SYSCLK_32K_TO_RC ” to change Sysclk to RC
**(7)** sample code
**1.** When B/W, 4G, 16G mode change to fast B/W mode or fast B/W mode change to B/W, 4G, 16G mode, must turn off LCD.
for example: B/W, 4G, 16G mode change to fast B/W mode.

```
;====Step1 LCD OFF ===
        LDA  LCTR
        ORA  #10000000B
        STA          LCTR

;====Step2 set GL[3:2]=11, fast B/W mode ===
        LDA  LCTR
        ORA  #00001100B
        STA          LCTR

;=== Step3 set Frame rate about 65 Hz ===
LDA  #6                 ;when Sysclk is changed to 32k, LFRA can’t be modified. Thus LFRA
STA          LFRA       ;is determined by equation2. Let the frame rate in sysclk=32k mode is
                            ;about 65hz
LDA  #00001000B         ;since LFRA has been determined, LCKR is determined by frame rate equation.
STA          LCKR       ;Let the frame rate in Sysclk=RC mode is about 65hz

;===Step4 LCD ON ===
        LDA  LCTR
        AND  #~10000000B
        STA          LCTR
```

**[After setting up fast B/W mode, then switch SYSCK from RC to 32k]**

**2.** Sysck from RC change to 32k…
Please use the macro “SWITCH_SYSCLK_RC_TO_32K”.
This macro will use 4 bytes RAM. They are show below.

```
;===== used ram ====
LCD_FLAG        DS    1
IENAL_BAK               DS    1
IENAH_BAK               DS    1
LPCK_BAK         DS   1
```

And this macro will also use LCD interrupt. Please copy below program in LCD interrupt service routine.

```
;==== LCD interrupt service routine ===
LCDFR_ISR:
        PHA
        LDA  #FFH
        STA          LCD_FLAG
        RMB7         IENAL                  ;DISABPLE LCD INTERRUPT
        PLA
        RTI
```

The declaration of this macro is show below (please don’t modify this macro)

```
SWITCH_SYSCLK_RC_TO_32K             .MACRO

;=== backup LPCK ===
        LDA  LPCK
        STA          LPCK_BAK
        LDA  #2
        STA          LPCK

;=== BACKUP IENAL/H AND ONLY ENABLE LCD INT ===
        SEI
        LDA  IENAL
        STA          IENAL_BAK
        LDA  IENAH
        STA          IENAH_BAK
        LDA  #10000000B              ;ONLY ENABLE LCD INT
        STA          IENAL
        STZ          IENAH
        LDA  #01111111B
```

```
        STA         IREQL                   ;CLEAR LCD INT REQUEST
        STZ         LCD_FLAG
        CLI
?WAIT_LCD_INT_RC232K:
        LDA  LCD_FLAG
        BEQ  ?WAIT_LCD_INT_RC232K

        ;=== change SYSCLK = 32K ===
        LDA  SYS
        ORA  #10000000B
        STA         SYS
        NOP
        NOP
        NOP
        BBR7 SYS,$
        ;=== RECOVERY IENAL/H ===
        SEI
        LDA  IENAL_BAK
        STA         IENAL
        LDA  IENAH_BAK
        STA         IENAH
        CLI
        .ENDM
```

**3.** Sysck from 32K change to RC. (After changing to RC, LCD must be in fast B/W mode.)
Please use the macro “SWITCH_SYSCLK_32K_TO_RC”.

```
SWITCH_SYSCLK_32K_TO_RC         .MACRO
        ;=== BACKUP IENAL/H AND ONLY ENABLE LCD INT ===
        SEI
        LDA  IENAL
        STA         IENAL_BAK
        LDA  IENAH
        STA         IENAH_BAK
        LDA  #10000000B             ;ONLY ENABLE LCD INT
        STA         IENAL
        STZ         IENAH
        LDA  #01111111B
        STA         IREQL                   ;CLEAR LCD INT REQUEST
        STZ         LCD_FLAG
        CLI

?WAIT_LCD_INT_32K2RC:
        LDA  LCD_FLAG
        BEQ  ?WAIT_LCD_INT_32K2RC

;=== change SYSCLK = RC ===
        LDA  SYS
        AND  #~10000000B
        STA         SYS
        NOP
        NOP
        NOP
        BBS7 SYS,$
        ;=== RECOVERY IENAL/H ===
        SEI
        LDA  IENAL_BAK
        STA         IENAL
        LDA  IENAH_BAK
        STA         IENAH
        CLI
        LDA  LPCK_BAK
        STA         LPCK
        .ENDM
```

## <System clock switching from OSC to OSCX>

Cause warm-up time is different when OSC is RC-OSC or X'tal.
To make sure the system clock has switched to OSCX, or error will happen.
Sample code, please follow up…

```
LDA     SYS
ORA     #80H
STA     SYS     ;switch OSC to OSCX
NOP
NOP
NOP
BBR7  SYS,$  ; branch self until OSC is changed to OSCX
```

## <Measure RC-OSC system clock>

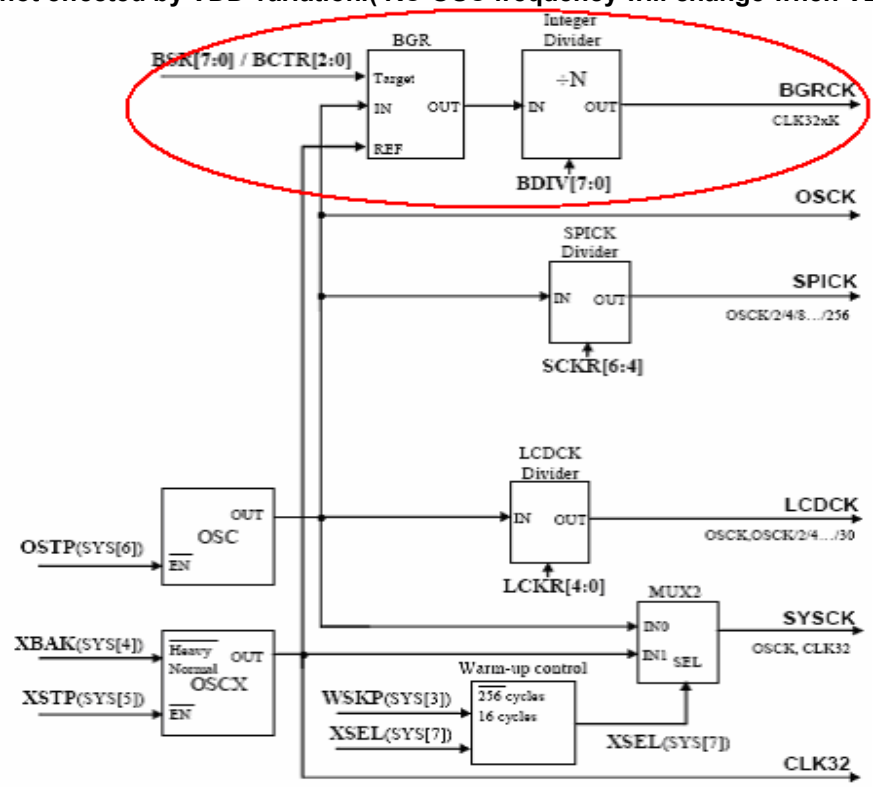
Since programmer wants to measure the system clock when using RC-OSC, please follow up.
Please connect a 3K-Ohm resistor between Vdd and XIO. You can get a periodic signal output from the XIO pin. It's RC osc signal.

## <IrDA mode application note>

Since IrDA has strictly protocol when transmit/receive data.
We suggest programmers use **X'tal** to be system clock instead of RC-OSC if IrDA signals are needed.
Programmer can use ceramic-OSC to gain some profit since it's cheaper than X'tal.

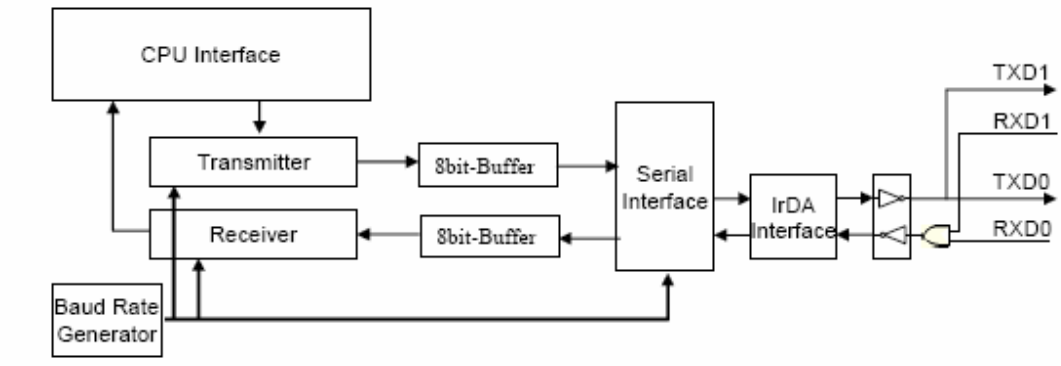
## <ST26xx UART details>

**BGRCK: BGRCK is used to produce UART baud rate, and BGRCK comes from OSC(main frequency) and fine tuning by 32768Hz crystal(REF) to make output baud rate is a stable frequency signal and will not effected by VDD variation.( RC-OSC frequency will change when VDD changes.)**




**Baud rate: Baud rate comes from BGRCK, and is determined by BDIV and BRS registers. The "Error rate" of baud rate is the maximum positive/negative inaccuracy of output baud rate.**

**For example:** If baud rate = 9600bps and OSC is in the rage of 3.72~4.28MHz, programmer should set BRS=61, BDIV=13 to get the best output baud rate which has error of 0.1%.So the real output baud rate will be in the range of [9600x0.999:9600x1.001].



## < IrDA BGRCK generation source >

BGRCK can be generated by two ways.

1. When bit7 of BCTR is 0,Haredware PLL which is used to stable BGRCK output will be operated. Cause BGRCK comes from OSC, since RC-OSC can't produce stable frequency, ST26xx hardware will fine tune BGRCK output frequency referenced from 32768Hz crystal to make BGRCK is in the range no matter VDD variation.
2. When bit7 of BCTR is 1:

It's used when OSC is X'tal. Since X'tal can produce stable frequency, and BGRCK comes from OSC, so BGRCK will also be stable if OSC is X'tal. Programmer can get better BGRCK output to make UART signal much more accurate by this way.

When bit7 of BCTR is 1, UART baud rate will be get in the following formula:

**baud rate = Sysclk/(BDIV*16) (no need to set "BRS")**

## < How to avoid LCD blink caused by PSG >

**Description:**

LCD display may blink when LCD function and PSG function are playing in the same time. LCD blink caused by CPU can't stand the load of calculation. So the LCD display my lag. And We can find there has blink problem.

**Solution:**

By using internal DMA function to move LCD data instead of programming method can solve part of this kind of problem. If there still has the same problem, we can separate LCD data into 16 parts and use DMA method to move into LCD RAM. The LCD blink problem can be totally solved.

Example program can be found by SA engineer. !!Please email us!!!

## < How to measure the internal current of ST2600B?>

When finish developing program by ST2600B, programmer should measure the current consumption of totally possible situations. In that time programmer can use ST2600B stand alone mode with running external ROM. In order to only measure the current from IC, the power for External ROM should be independent. And then we can measure the current from IC only!!

## < Ways to save power consumption >

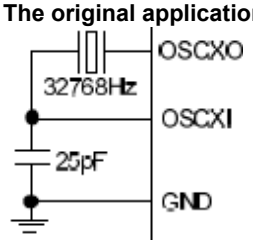
There are some factors which can effect current consumption…

(1) Main-frequency : Higher frequency needs more current
(2) DAC mode cost much current than PWM mode
(3) Vlcd voltage level : Higher Vlcd pays higher current.
(4) Using EPROM will cost more current than no use.
(5) Input without any connection will randomly cost power
(6) WAIT mode with considerable program can save lots of power
(7) Larger panel will pay more current.
(8) Un-ideal hardware connection will cause unknown current waste.

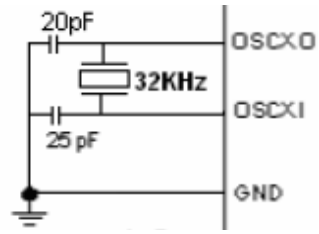
## <32KHz (OSCX) application circuit >

Below shows the application circuit of 32KHz X'tal connection. Please follow it.

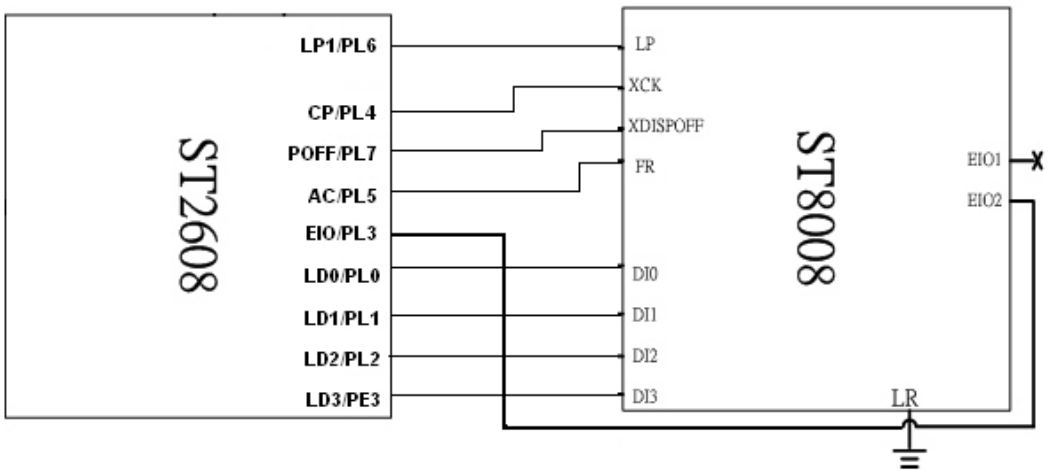
**The original application circuit as below:**




**The modified circuit as follow:**




## <ST26XX+ST8008 CASCADE MODE CONNECTION>




This interface is suitable for ST26xx series IC.

**Notice:** ST26xxB can only output common signal when cascade mode.

User **can not mix** the segment from ST26xxB and the segment from other LCD drivers. It's because the LCD driving ability of ST26xxB and other LCD drivers are not the same. If user mix them, the performance of LCD display may be bad. (Color block or cross-talk)

## < Standard flow for switching I/O and segment >

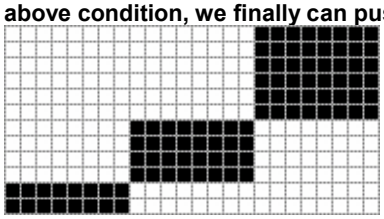
We know that there are many I/O which are shared with LCD segment.
And the configure is determined by **LCFG** register.
Here is the standard flow of configure I/O or segment, please follow up. Or programmer will not configure I/O possibly.
(1) Please configure **LCFG** first!!
(2) And then configure **PCA/PCB/PCC/PCD/PCE/PCL**
(3) Finally configure **PA/PB/PC/PD/PE/PL**

**Sample code:**

```
LDA     #FFH
STA     LCFG      ; enable all I/O
STA     PCL       ; configure PL as output
STA     PL        ; PL0~PL7 high status
```

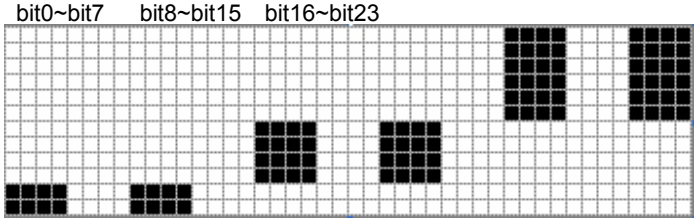
## < LCDCK=32K with cascade mode >

**There has some limit when programmer use LCDCK=32K and cascade.**
Programmer can use ST26 with LCD cascade mode, it's no doubt. Also, programmer can use cascade mode combine with LCDCK from 32KHz(OSCX).
But user should take care one thing as following:
We know ST26 can support Cascade 1/2/4-bit data bus mode, however, LCDCK=32K function can only support 8-bit mode!!
So, when programmer use these two functions in the same time, MCU will push 8-bit data per clock cause LCDCK=32K function, but cascade mode maximum push 4-bit data out to LCD driver per clock, so you will lose 4-bit data(bit4~bit7) and make display data wrong.
**The solution is to modify the picture, let MCU push 8-bit every clock, and we separate it every 4-bit data into 8 bit data as picture 2. and we can solve it. Mention that because LCDCK=32K can maximum load 36 x 80 dots picture, by above condition, we finally can push 36x40 dots picture to show on LCD since we only use half of data (first 4-bit).**



**←The original picture information**

bit0~bit7 bit8~bit15 bit16~bit23



**←picture 2 : modified picture**

**Notice:** ST26xxB can only output common signal when cascade mode.
User **can not mix** the segment from ST26xxB and the segment from other LCD drivers. It's because the LCD driving ability of ST26xxB and other LCD drivers are not the same. If user mix them, the performance of LCD display may be bad. (Color block or cross-talk)

## < User Manual for ST2600B external bus usage >

### [Description]

Since users may use external memory bus to access external ROM, FLASH, or LCD driver, we draw this manual to tell the

details and notice when using external bus by ST2600B in two mode: (1)Stand alone mode (2) ICE-mode

**(1) When using ST2600B Stand alone mode:**

External memory bus can be output directly by ST2600B DVB (PCB-300) J22 pin-1 to pin-32

**(2) When using ST2600B ICE mode:**

Because external data can be controlled by PC through ST-ICE, so the external bus will be shared with ICE connector pins (PCB-300 - J15)

(a) Please first amount 74hc32 on U11 and U12.

(b) PCB-300 J15 pins allocation as following:

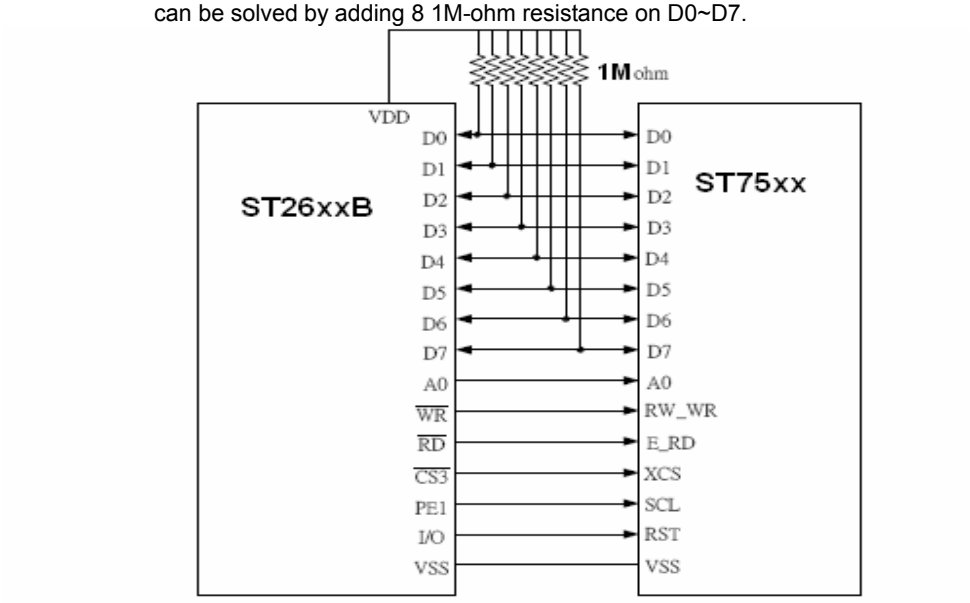
J15

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 | vcc | A18 | A19 | A20 | A21 | A22 | A23 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | WR | RD | gnd |
| 1 | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 | A13 | A14 | A15 | A16 | A17 |

(c) ST2600B DVB should be connected to ST-ICE by J15, and also be connected to external bus by above table

## < Pull-up resistance of D0~D7 for current issue when using ST75xx >

**Description:** When entering sleep mode, D0~D7 of ST75xx will be floating, and make current consumption (about 120uA). It can be solved by adding 8 1M-ohm resistance on D0~D7.




Note: The pull up resister of D7~ D0 are necessary to avoid the current issue.

# 11 REVISIONS

| REVISION | DESCRIPTION | PAGE | DATE |
|---|---|---|---|
| 1.00 | First Release | | 2006/11 |
| 1.15 | Add ST26xx application note | 22 | 2009/5/7 |
| | | | |
| | | | |
| | | | |
| | | | |

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