To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

3885 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

GENERAL DESCRIPTION

The 3885 group is the 8-bit microcomputer based on the 740 family core technology.

The 3885 group is designed for Keyboard Controller for the note book PC.

The multi-master I^2C-bus interface can be added by option.

FEATURES

<Microcomputer mode>

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 0.5 µs
  (at 8 MHz oscillation frequency)
- Memory size
  ROM ..... 32K to 60K bytes
  RAM ..... 1024 to 2048 bytes
- Programmable input/output ports 72
- Software pull-up transistors 8
- Interrupts ..... 22 sources, 16 vectors
- Timers ..... 8-bit × 4
- Watchdog timer ..... 16-bit × 1
- PWM output ..... 14-bit × 2
- Serial I/O ..... 8-bit × 1(UART or Clock-synchronized)
- Multi-master I^2C bus interface (option) ..... 1 channel
- LPC interface ..... 2 channels
- Serialized IRQ ..... 3 factor
- A-D converter ..... 10-bit × 8 channels
- D-A converter ..... 8-bit × 2 channels
- Comparator circuit ..... 8 channels
- Clock generating circuit ..... Built-in 2 circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage ..... 3.0 to 3.6 V
- Power dissipation
  In high-speed mode ..... 20 mW
  (at 8 MHz oscillation frequency, at 3.3 V power source voltage)
  In low-speed mode ..... 330 mW
  (at 32 kHz oscillation frequency, at 3.3 V power source voltage)
- Operating temperature range ..... –20 to 85°C

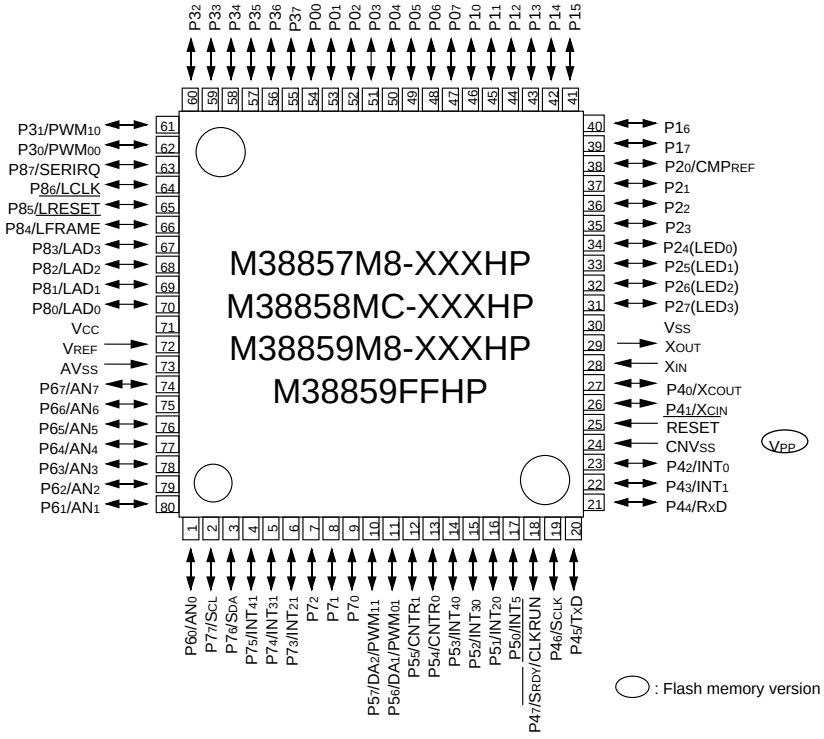
<Flash memory mode>

- Supply voltage ..... V_{CC} = 3.3 ± 0.3V
- Program/Erase voltage ..... V_{PP} = 5.0 V ± 10 %
- Programming method ..... Programming in unit of byte
- Erasing method
  Parallel I/O mode
  CPU reprogramming mode
- Program/Erase control by software command
- Number of times for programming/erasing 100
- Operating temperature range (at programming/erasing)
  ..... Room temperature

APPLICATION

Note book PC

PIN CONFIGURATION (TOP VIEW)



Package type : 80P6Q-A

Fig. 1 Pin configuration

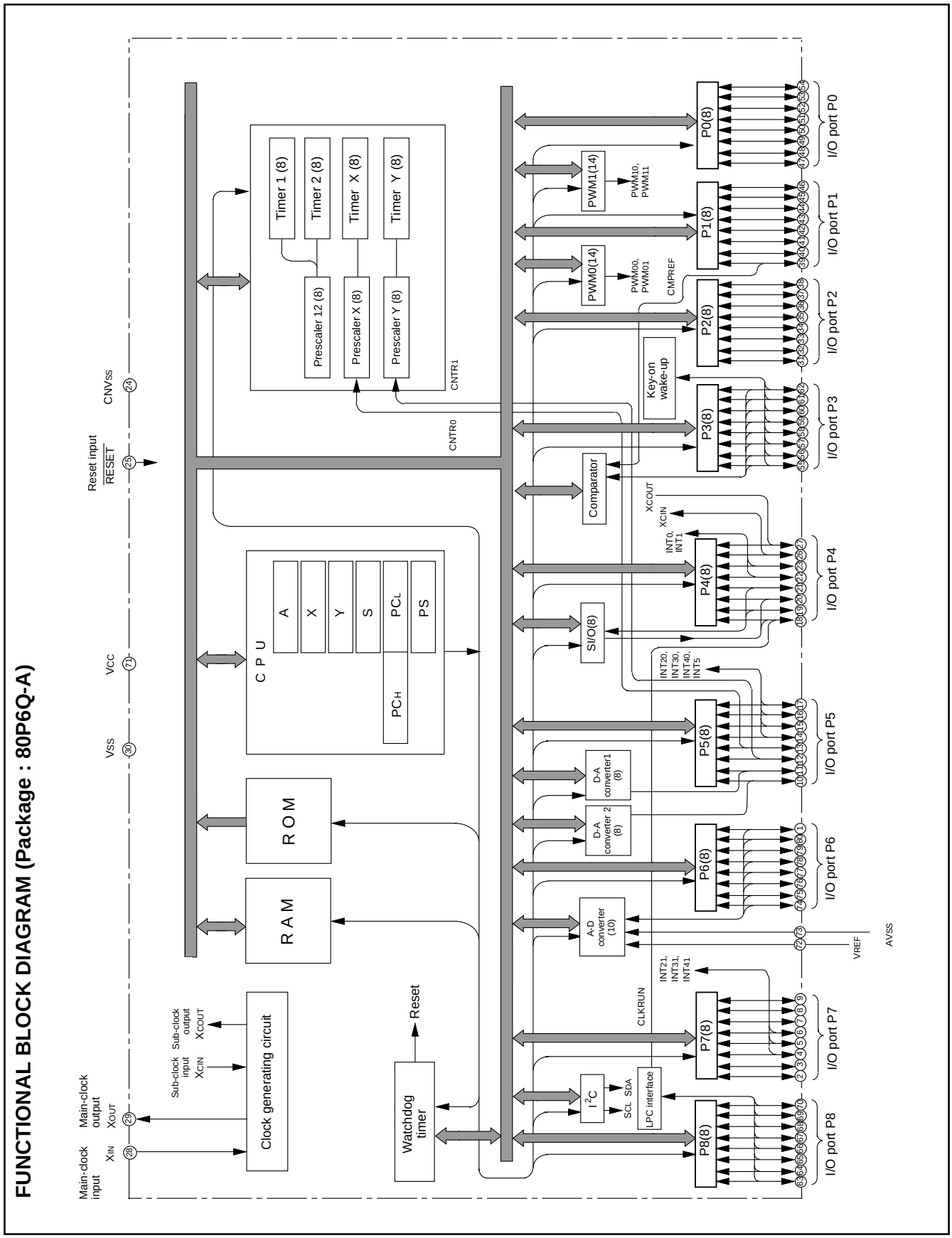


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Functions	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of 3.0 V ±10 % to Vcc, and 0 V to Vss.	
CNV_{SS}	CNV_{SS} input	•Connected to V_{SS}. •In the flash memory version, this pin functions as the V_{PP} power source input pin.	
V_{REF}	Reference voltage	•Reference voltage input pin for A-D and D-A converters.	
AV_{SS}	Analog power source	•Analog power source input pin for A-D and D-A converters. •Connect to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active “L”.	
X_{IN}	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0$–$P0_7$	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure or N-channel open-drain output structure.	
$P1_0$–$P1_7$	I/O port P1	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure or N-channel open-drain output structure.	
$P2_0/CMP_{REF}$	I/O port P2	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •$P2_4$ to $P2_7$ (4 bits) are enabled to output large current for LED drive.	•Comparator reference power source input pin
$P2_1$–$P2_7$			
$P3_0/PWM_{00}$ $P3_1/PWM_{10}$	I/O port P3	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •These pins function as key-on wake-up and comparator input. •These pins are enabled to control pull-up.	•Key-on wake-up input pins •Comparator input pins •PWM output pins
$P3_2$–$P3_7$			•Key-on wake-up input pins •Comparator input pins

Table 2 Pin description (2)

Pin	Name	Functions	Function except a port function
P40/XCOUT P41/XCIN	I/O port P4	•8-bit I/O port with the same function as port P0 <Input level> CMOS compatible input level <Output level> P40, P41 : CMOS 3-state output structure P42-P47 : CMOS 3-state output structure or N-channel open-drain output structure •Each pin level of P42 to P46 can be read even in output port mode.	•Sub-clock generating circuit I/O pins (Connect a resonator.)
P42/INT0 P43/INT1			•Interrupt input pins
P44/RxD P45/TxD P46/SCLK			•Serial I/O function pins
P47/SRDY /CLKRUN			•Serial I/O function pins •Serialized IRQ function pin
P50/INT5 P51/INT20 P52/INT30 P53/INT40	I/O port P5	•8-bit I/O port with the same function as port P0 •CMOS compatible input level •CMOS 3-state output structure	•Interrupt input pins
P54/CNTR0 P55/CNTR1			•Timer X, timer Y function pins
P56/DA1/PWM01 P57/DA2/PWM11			•D-A converter output pins •PWM output pins
P60/AN0–P67/AN7	I/O port P6	•8-bit I/O port with the same function as port P0 •CMOS compatible input level. •CMOS 3-state output structure.	•A-D converter output pins
P70 P71 P72	I/O port P7	•8-bit CMOS I/O port with the same function as port P0 <Input level> P70–P75 : CMOS compatible input level or TTL compatible input level P76, P77 : CMOS compatible input level or SMBUS input level in the I2C-BUS interface function, <Output structure> N-channel open-drain output structure •Each pin level of P70 to P75 can be read evev in output port mode.	
P73/INT21 P74/INT31 P75/INT41			•Interrupt input pins
P76/SDA P77/SCL			•I2C-BUS interface function pins
P80/LAD0 P81/LAD1 P82/LAD2 P83/LAD3 P84/LFRAME P85/LRESET P86/LCLK	I/O port P8	•8-bit CMOS I/O port with the same function as port P0 •CMOS compatible input level. •CMOS 3-state output structure.	•LPC interface function pins
P87/SERIRQ			•Serialized IRQ function pin

PART NUMBERING

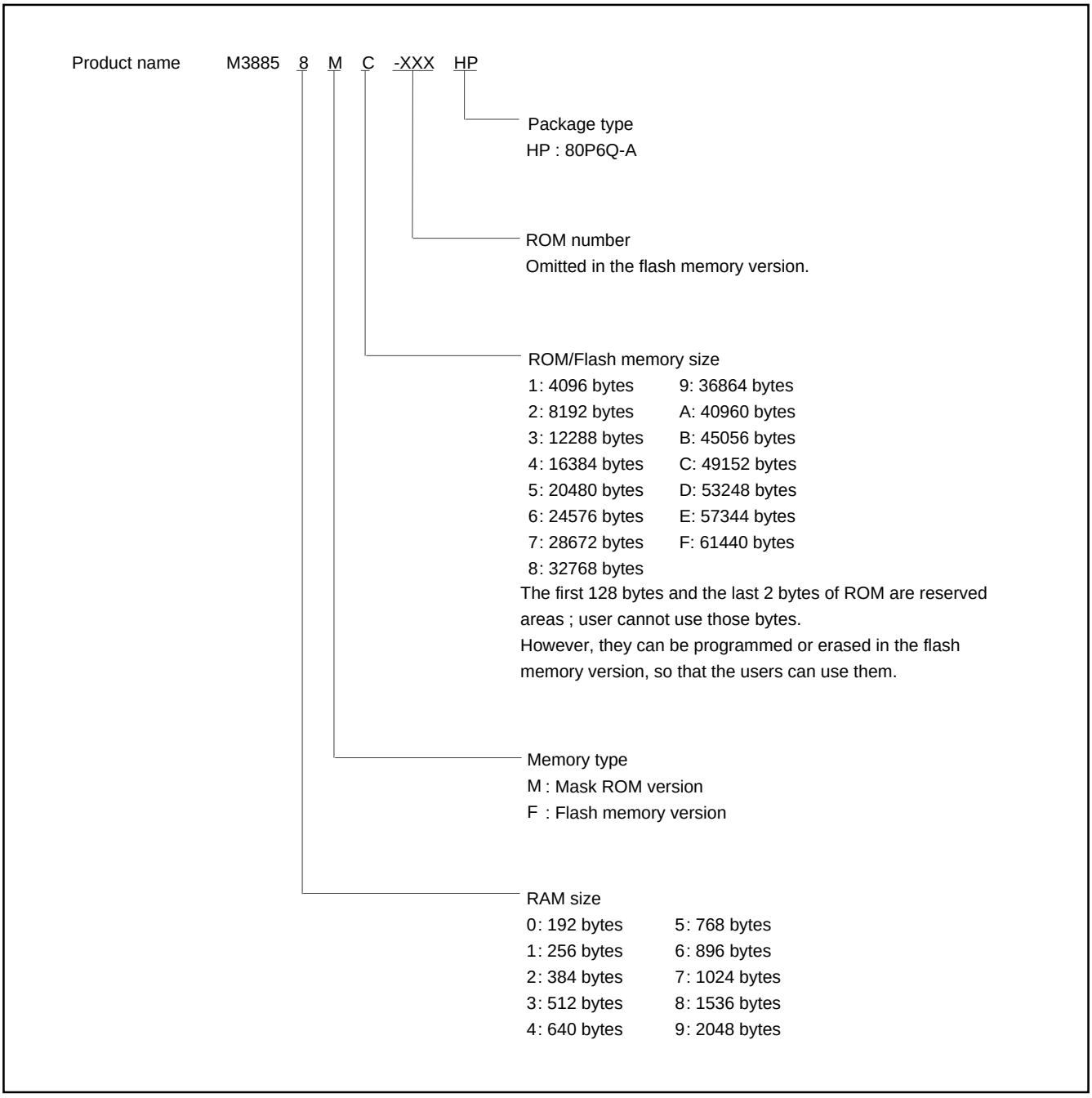


Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 3885 group as follows.

Memory Type

Support for mask ROM, flash memory version.

Memory Size

ROM size ..... 32 K to 60 K bytes
RAM size ..... 1024 to 2048 bytes

Packages

80P6Q-A ..... 0.5 mm-pitch plastic molded LQFP

Memory Expansion

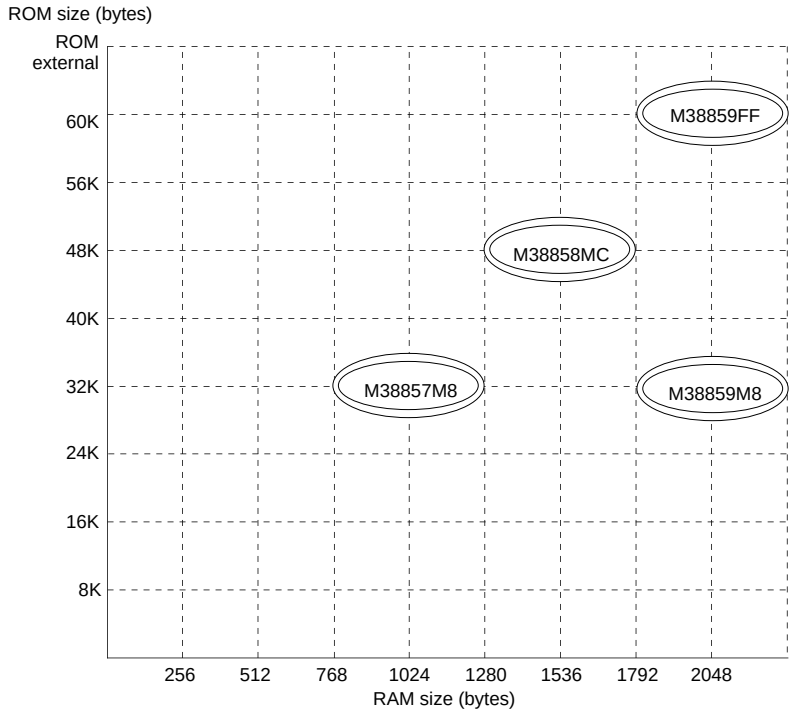


Fig. 4 Memory expansion plan

Table 3 Products plan list **As of May 2002**

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38857M8-XXXHP	32768 (32638)	1024	80P6Q-A	Mask ROM version
M38858MC-XXXHP	49152 (19022)	1536		
M38859M8-XXXHP	32768 (32638)	2048		
M38859FFHP	61440	2048		Flash memory version

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3885 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 7.

Store registers other than those described in Figure 7 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

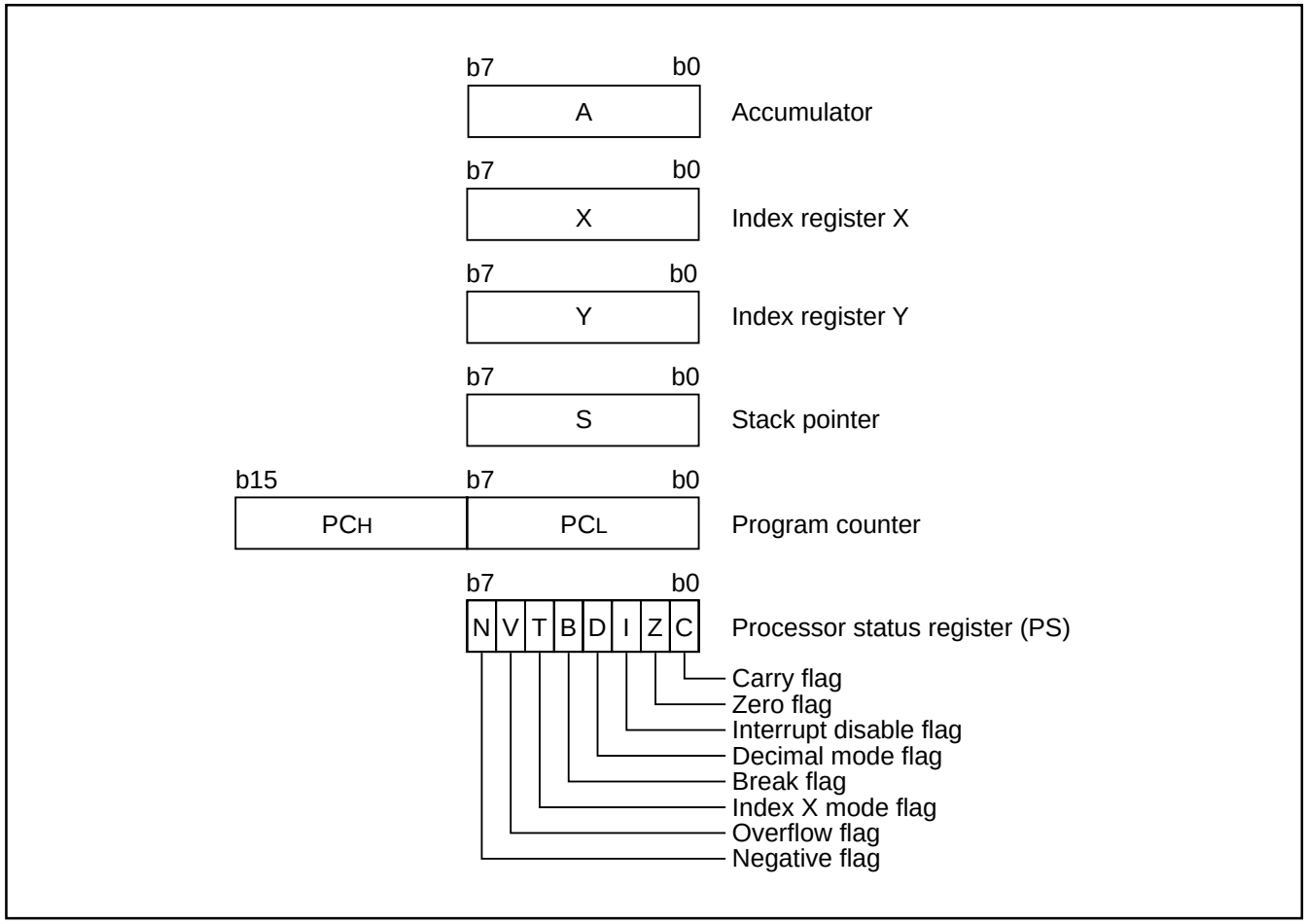


Fig. 5 740 Family CPU register structure

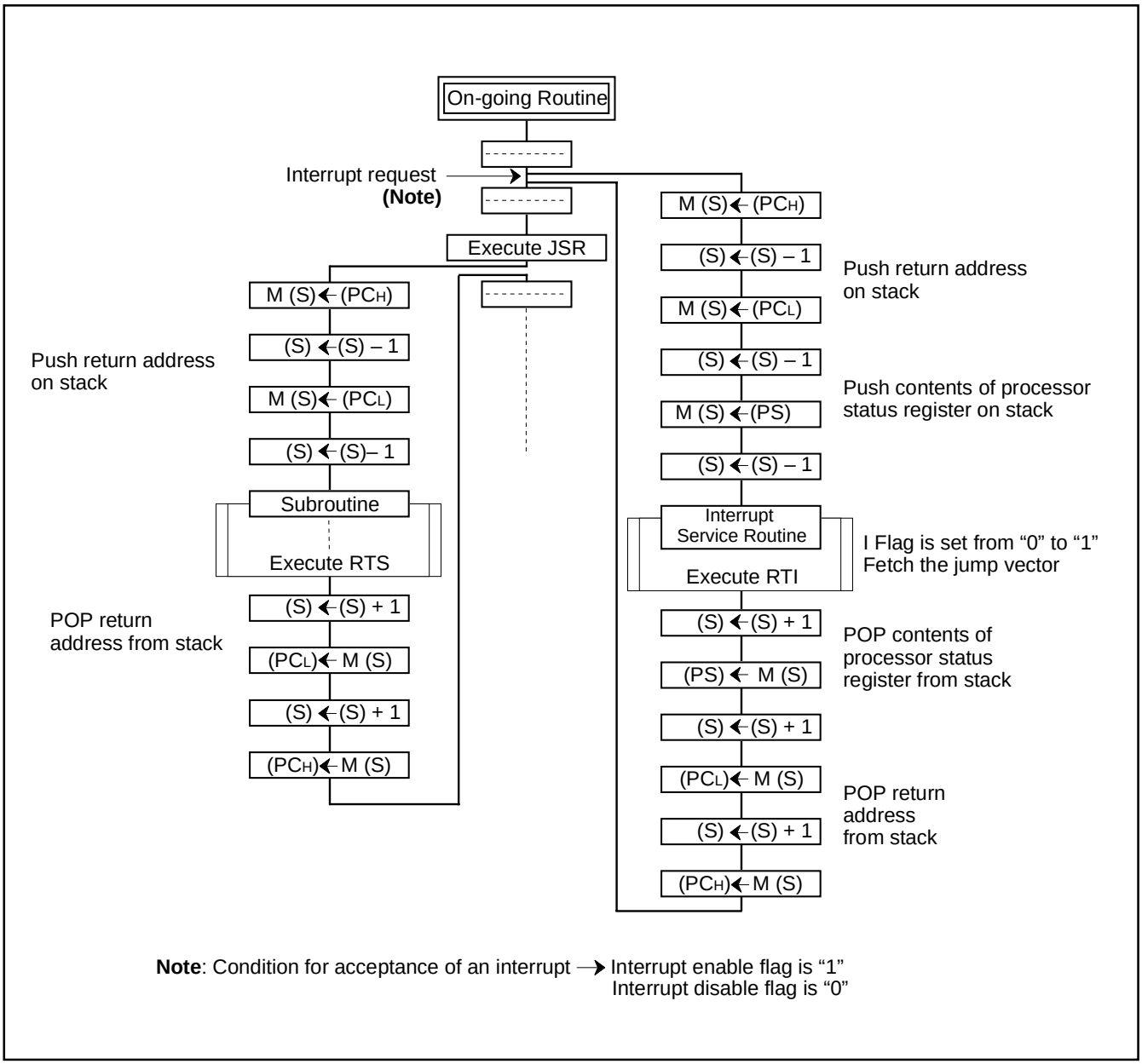


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)
The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)
The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)
The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)
The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC

•Bit 4: Break flag (B)
The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)
When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)
The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc.
The CPU mode register is allocated at address 003B16.

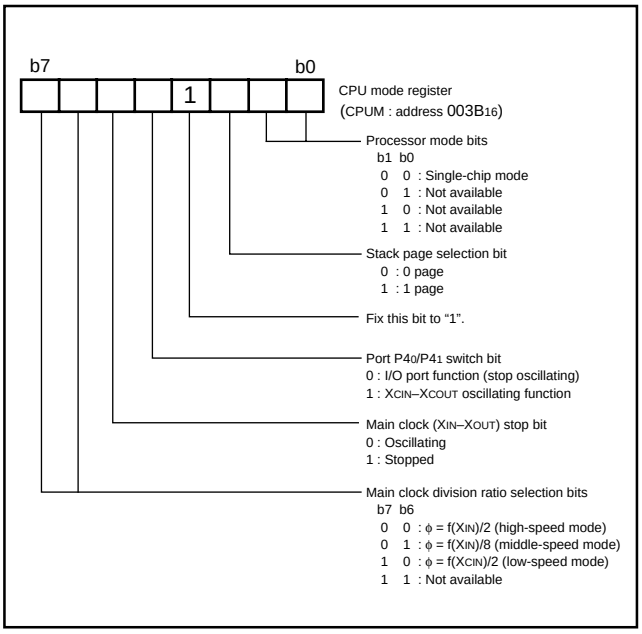


Fig. 7 Structure of CPU mode register

MEMORY

RAM
RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM
ROM is used for program code and data table storage.
The first 128 bytes and the last 2 bytes of ROM are reserved for device testing code and the rest is user area. Programming/Erasing of the reserved ROM area is possible in the flash memory version.

Zero Page
Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page
Access to this area with only 2 bytes is possible in the special page addressing mode.

Interrupt Vector Area
The interrupt vector area contains reset and interrupt vectors.

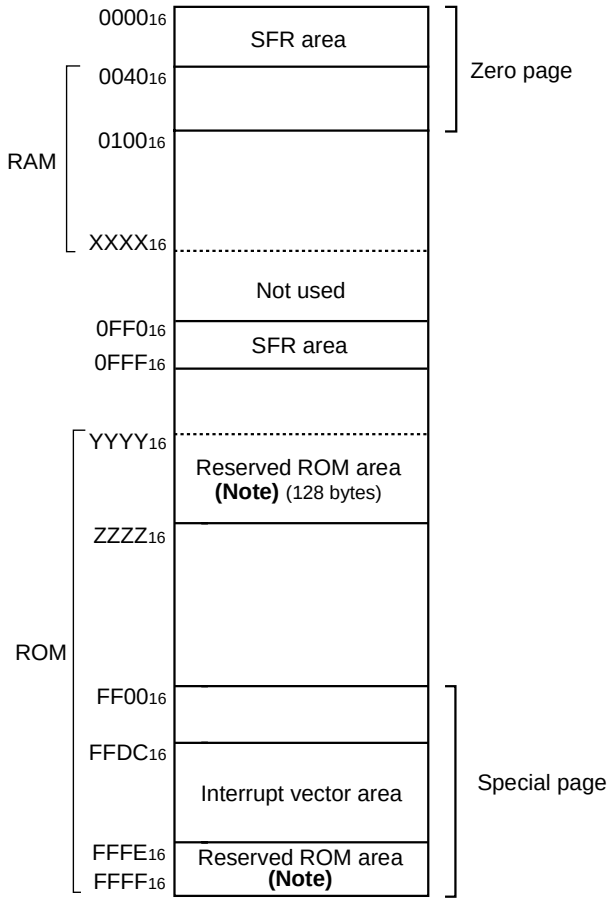
Special Function Register (SFR) Area
The special function register area contains the control registers such as I/O ports, timers, serial I/O, etc.

RAM area

RAM size (bytes)	Address XXXX16
1024	043F16
1536	063F16
2048	083F16

ROM area

ROM size (bytes)	Address YYYY16	Address ZZZZ16
32768	800016	808016
49152	400016	408016
61440	100016	108016



Notes: This area is reserved in the mask ROM version.
This area is usable in flash memory version.

Fig. 8 Memory map diagram

0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	Port P5 (P5)
$000B_{16}$	Port P5 direction register (P5D)
$000C_{16}$	Port P6 (P6)
$000D_{16}$	Port P6 direction register (P6D)
$000E_{16}$	Port P7 (P7)
$000F_{16}$	Port P7 direction register (P7D)
0010_{16}	Port P8 (P8)/Port P4 input register (P4I)
0011_{16}	Port P8 direction register (P8D)/Port P7 input register (P7I)
0012_{16}	I^2C data shift register (S0)
0013_{16}	I^2C address register (S0D)
0014_{16}	I^2C status register (S1)
0015_{16}	I^2C control register (S1D)
0016_{16}	I^2C clock control register (S2)
0017_{16}	I^2C start/stop condition control register (S2D)
0018_{16}	Transmit/Receive buffer register (TB/RB)
0019_{16}	Serial I/O status register (SIOSTS)
$001A_{16}$	Serial I/O control register (SIOCON)
$001B_{16}$	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)
$001D_{16}$	Serialized IRQ control register (SERCON)
$001E_{16}$	Watchdog timer control register (WDTCON)
$001F_{16}$	Serialized IRQ request register (SERIRQ)

0020_{16}	Prescaler 12 (PRE12)
0021_{16}	Timer 1 (T1)
0022_{16}	Timer 2 (T2)
0023_{16}	Timer XY mode register (TM)
0024_{16}	Prescaler X (PREX)
0025_{16}	Timer X (TX)
0026_{16}	Prescaler Y (PREY)
0027_{16}	Timer Y (TY)
0028_{16}	Data bas buffer register 0 (DBB0)
0029_{16}	Data bas buffer status register 0 (DBBSTS0)
$002A_{16}$	LPC control register (LPCCON)
$002B_{16}$	Data bas buffer register 1 (DBB1)
$002C_{16}$	Data bas buffer status register 1 (DBBSTS1)
$002D_{16}$	Comparator data register (CMPD)
$002E_{16}$	Port control register 1 (PCTL1)
$002F_{16}$	Port control register 2 (PCTL2)
0030_{16}	PWM0H register (PWM0H)
0031_{16}	PWM0L register (PWM0L)
0032_{16}	PWM1H register (PWM1H)
0033_{16}	PWM1L register (PWM1L)
0034_{16}	AD/DA control register (ADCON)
0035_{16}	A-D conversion register 1 (AD1)
0036_{16}	D-A1 conversion register (DA1)
0037_{16}	D-A2 conversion register (DA2)
0038_{16}	A-D conversion register 2 (AD2)
0039_{16}	Interrupt source selection register (INTSEL)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

$0FF0_{16}$	LPC0 address register L (LPC0ADL)
$0FF1_{16}$	LPC0 address register H (LPC0ADH)
$0FF2_{16}$	LPC1 address register L (LPC1ADL)
$0FF3_{16}$	LPC1 address register H (LPC1ADH)

$0FF8_{16}$	Port P5 input register (P5I)
$0FF9_{16}$	Port control register 3 (PCTL3)

$0FFE_{16}$	Flash memory control register (FMCR)	**(Note)**
$0FFF_{16}$	Reserved	**(Note)**

Note: This applies to only flash memory version.

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

All I/O pins are programmable as input or output. All I/O ports have direction registers which specify the data direction of each pin like input/output. One bit in a direction register corresponds to one pin. Each pin can be set to be input or output port.

Writing "0" to the bit corresponding to the pin, that pin becomes an input mode. Writing "1" to the bit, that pin becomes an output mode.

When the data is read from the bit of the port register corresponding to the pin which is set to output, the value shows the port latch data, not the input level of the pin. When a pin set to input, the pin comes floating. In input port mode, writing the port register changes only the data of the port latch and the pin remains high impedance state.

When the P8 function selection bit of the port control register 2 is set to "1", reading from address 0010_{16} reads the port P4 register, and reading from address 0011_{16} reads the port P7 register.

Especially, the input level of $P4_2$ to $P4_6$ pins and $P7_0$ to $P7_5$ pins can be read regardless of the data of the direction registers in this case.

Table 6 I/O port function (1)

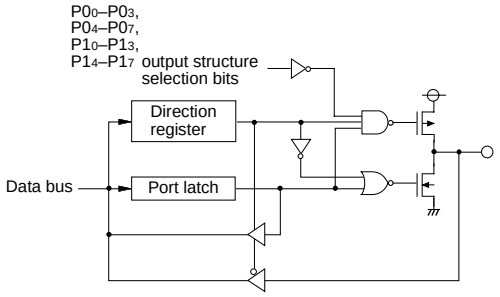
Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
$P0_0$-$P0_7$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output or N-channel open-drain output		Port control register 1	(1)
$P1_0$–$P1_7$	Port P1					
$P2_0$/CMPREF	Port P2		CMOS compatible input level CMOS 3-state output	Analog comparator power source input pin	Port control register 1 Port control register 2	(2)
$P2_1$–$P2_7$						(3)
$P3_0$/PWM00 $P3_1$/PWM10	Port P3			PWM output Key-on wake up input Comparator input	Port control register 1 AD/DA control register	(4) (5)
$P3_2$–$P3_7$				Key-on wake up input Comparator input	Port control register 1	(6)
$P4_0$/XCOUT $P4_1$/XCIN	Port P4			Sub-clock generating circuit	CPU mode register	(7) (8)
$P4_2$/INT0 $P4_3$/INT1			CMOS compatible input level CMOS 3-state output or N-channel open-drain output	External interrupt input	Interrupt edge selection register Port control register 2	(9) (10)
$P4_4$/RxD				Serial I/O function input	Serial I/O control register Port control register 2	(11)
$P4_5$/TxD				Serial I/O function output	Serial I/O control register UART control register Port control register 2	(12)
$P4_6$/SCLK				Serial I/O function I/O	Serial I/O control register Port control register 2	(13)
$P4_7$/$\overline{SRDY}$ /CLKRUN				Serial I/O function output Serialized IRQ function output	Serial I/O control register Serialized IRQ control register	(14)

Table 7 I/O port function (2)

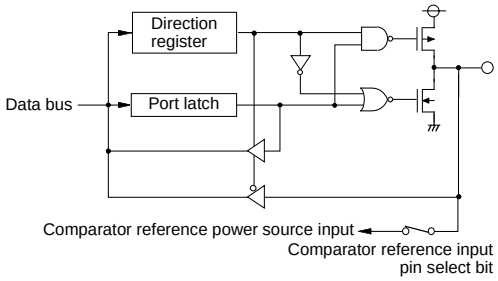
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
P5$_0$/INT$_5$ P5$_1$/INT$_{20}$ P5$_2$/INT$_{30}$ P5$_3$/INT$_{40}$	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output or N-channel opendrain output	External interrupt input	Interrupt edge selection register	(15) (16)
P5$_4$/CNTR$_0$ P5$_5$/CNTR$_1$			CMOS compatible input level CMOS 3-state output	Timer X, timer Y function I/O	Timer XY mode register	(17)
P5$_6$/DA$_1$/PWM$_{01}$ P5$_7$/DA$_2$/PWM$_{11}$				D-A converter output PWM output	AD/DA control register UART control register	(18) (19)
P6$_0$/AN$_0$–P6$_7$/AN$_7$	Port P6			A-D converter input	AD/DA control register	(20)
P7$_0$ P7$_1$ P7$_2$	Port P7		CMOS compatible input level or TTL input level Pure N-channel open-drain output		Port control register 2	(21) (22) (23) (24)
P7$_3$/INT$_{21}$ P7$_4$/INT$_{31}$ P7$_5$/INT$_{41}$				External interrupt input	Interrupt edge selection register Port control register 2	(25)
P7$_6$/SDA P7$_7$/SCL			CMOS compatible input level or SMBUS input level Pure N-channel open-drain output	I^2C-BUS interface function I/O	I^2C control register	(26)
P8$_0$/LAD$_0$ P8$_1$/LAD$_1$ P8$_2$/LAD$_2$ P8$_3$/LAD$_3$ P8$_4$/$\overline{\text{LFRAME}}$ P8$_5$/$\overline{\text{LRESET}}$ P8$_6$/LCLK	Port P8		CMOS compatible input level CMOS 3-state output	LPC interface function I/O	Data bus buffer control register	(27) (28)
P8$_7$/SERIRQ				Serialized IRQ function I/O		

Notes1: For details usage of double-function ports as function I/O ports, refer to the applicable sections.
2: Make sure that the input level of each pin should be either 0 V or V_{CC} in STP mode.
When an input level is at an intermediate voltage level, the I_{CC} current will become large because of the input buffer gate.

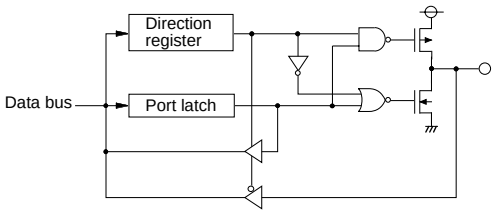
(1) Ports P0, P1



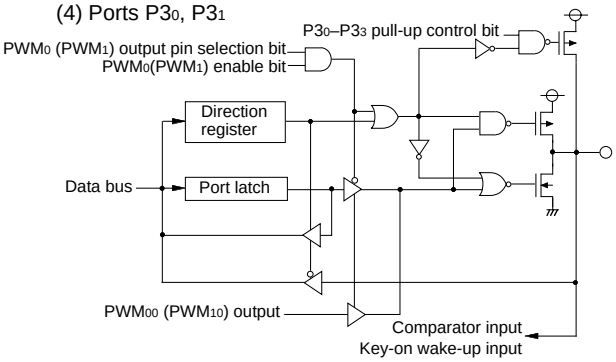
(2) Port P2₀



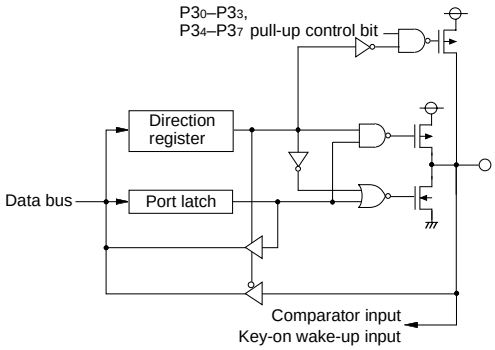
(3) Port P2₁–P2₇



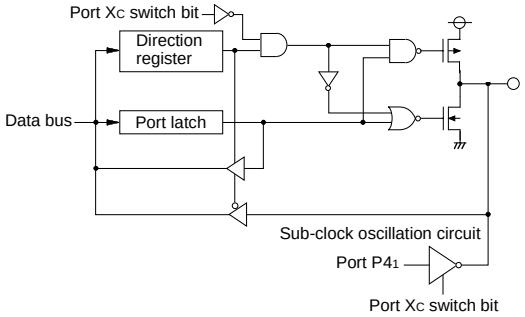
(4) Ports P3₀, P3₁



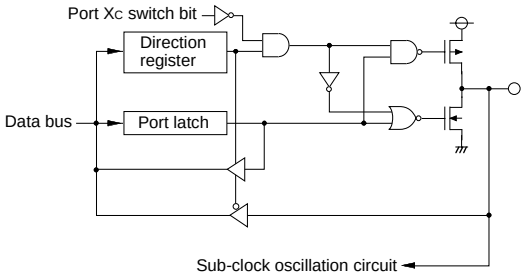
(5) Ports P3₂–P3₇



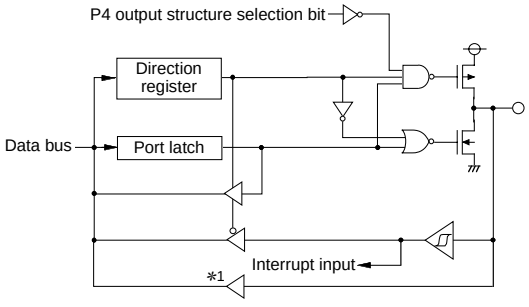
(6) Port P4₀



(7) Port P4₁



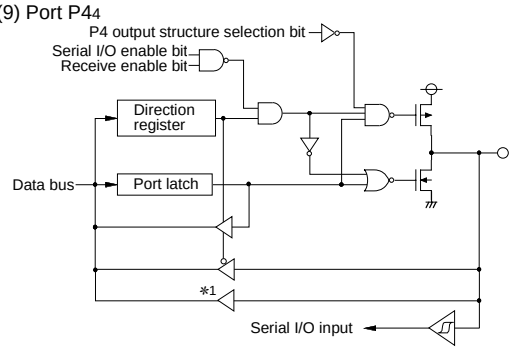
(8) Ports P4₂ , P4₃



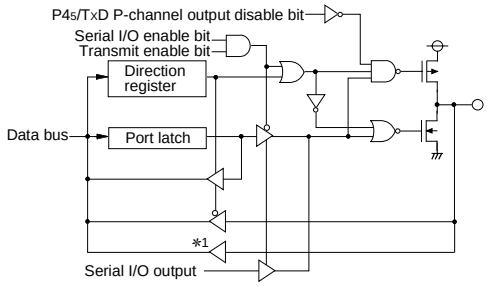
*1. Reading the port P8 register (address 001016) is switched to port P4 pin input level by the P8 function selection bit of the port control register 2 (PCTL2).

Fig. 10 Port block diagram (1)

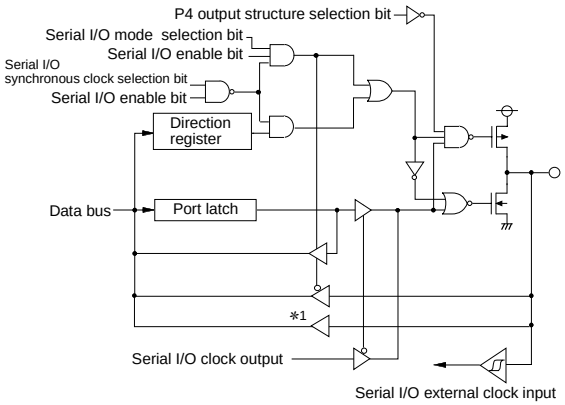
(9) Port P4$_4$



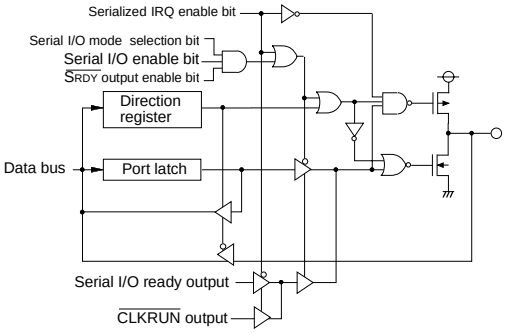
(10) Port P4$_5$



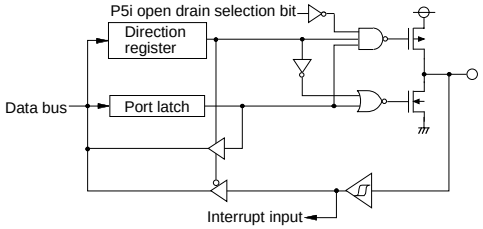
(11) Port P4$_6$



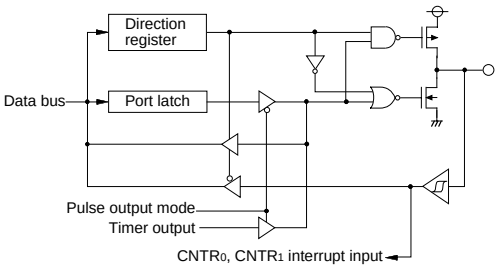
(12) Port P4$_7$



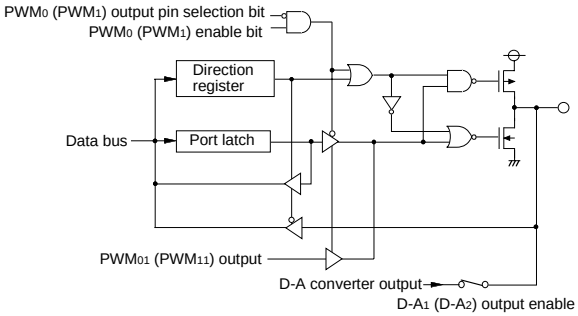
(13) Ports P5$_0$ to P5$_3$



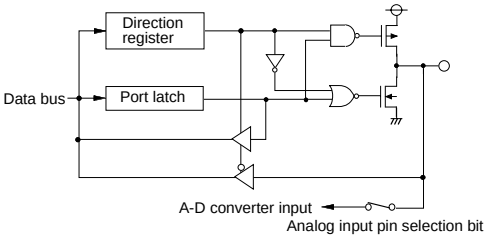
(14) Ports P5$_4$, P5$_5$



(15) Ports P5$_6$, P5$_7$



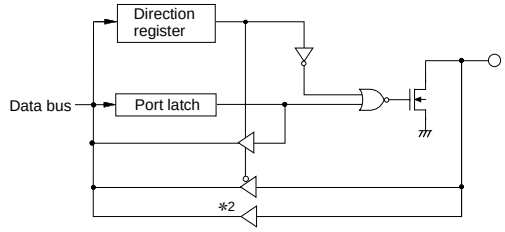
(16) Port P6



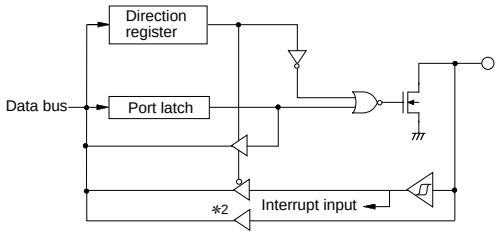
*1. Reading the port P8 register (address 001016) is switched to port P4 pin input level by the P8 function selection bit of the port control register 2 (PCTL2).

Fig. 11 Port block diagram (2)

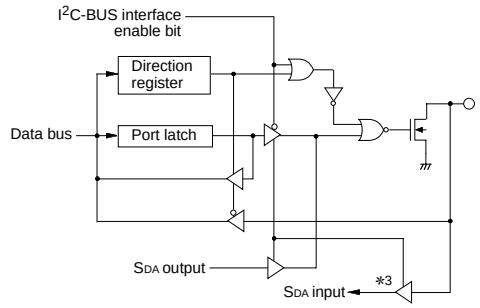
(17) Ports $P7_0$ to $P7_2$



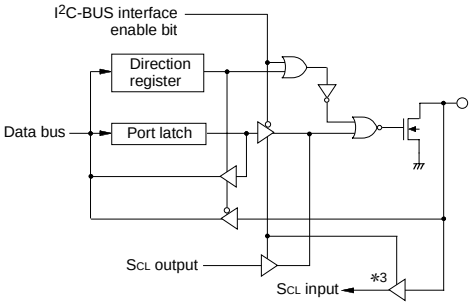
(18) Ports $P7_3$ to $P7_5$



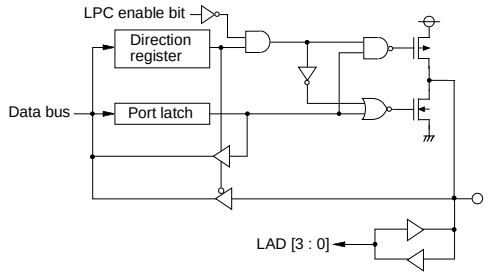
(19) Port $P7_6$



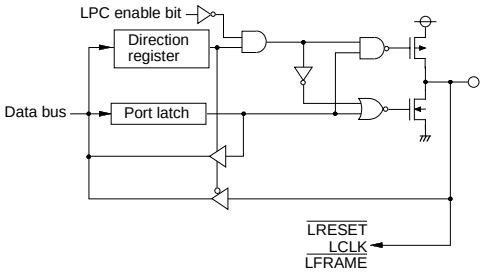
(20) Port $P7_7$



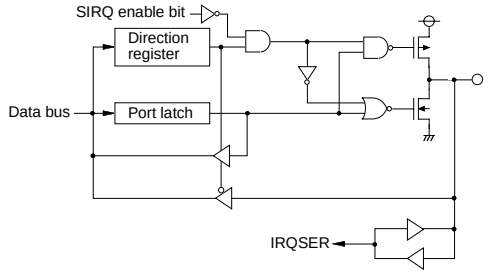
(21) Ports $P8_0$ to $P8_3$



(22) Ports $P8_4$ to $P8_6$



(23) Port $P8_7$



*2. The input level can be switched between CMOS compatible input level and TTL level by the P7 input level selection bit of the port control register 2 (PCTL2).
Reading the port P8 direction register is switched to port P7 pin input level by the P8 function selection bit of the port control register 2 (PCTL2).

*3. The input level can be switched between CMOS compatible input level and SMBUS level by the I^2C-BUS interface pin input selection bit of the I^2C control register (SID).

Fig. 12 Port block diagram (3)

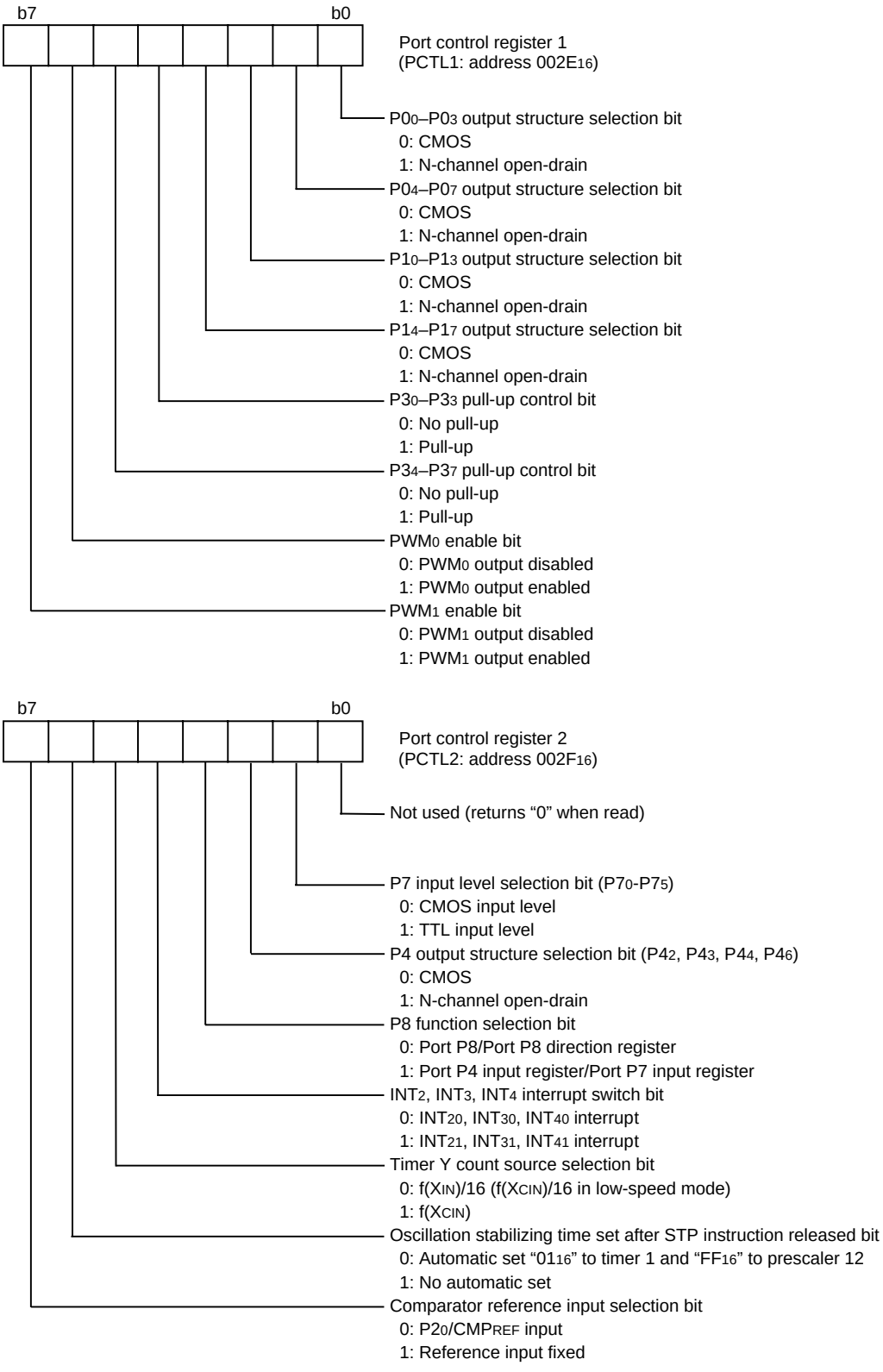


Fig. 13 Structure of port I/O related registers (1)

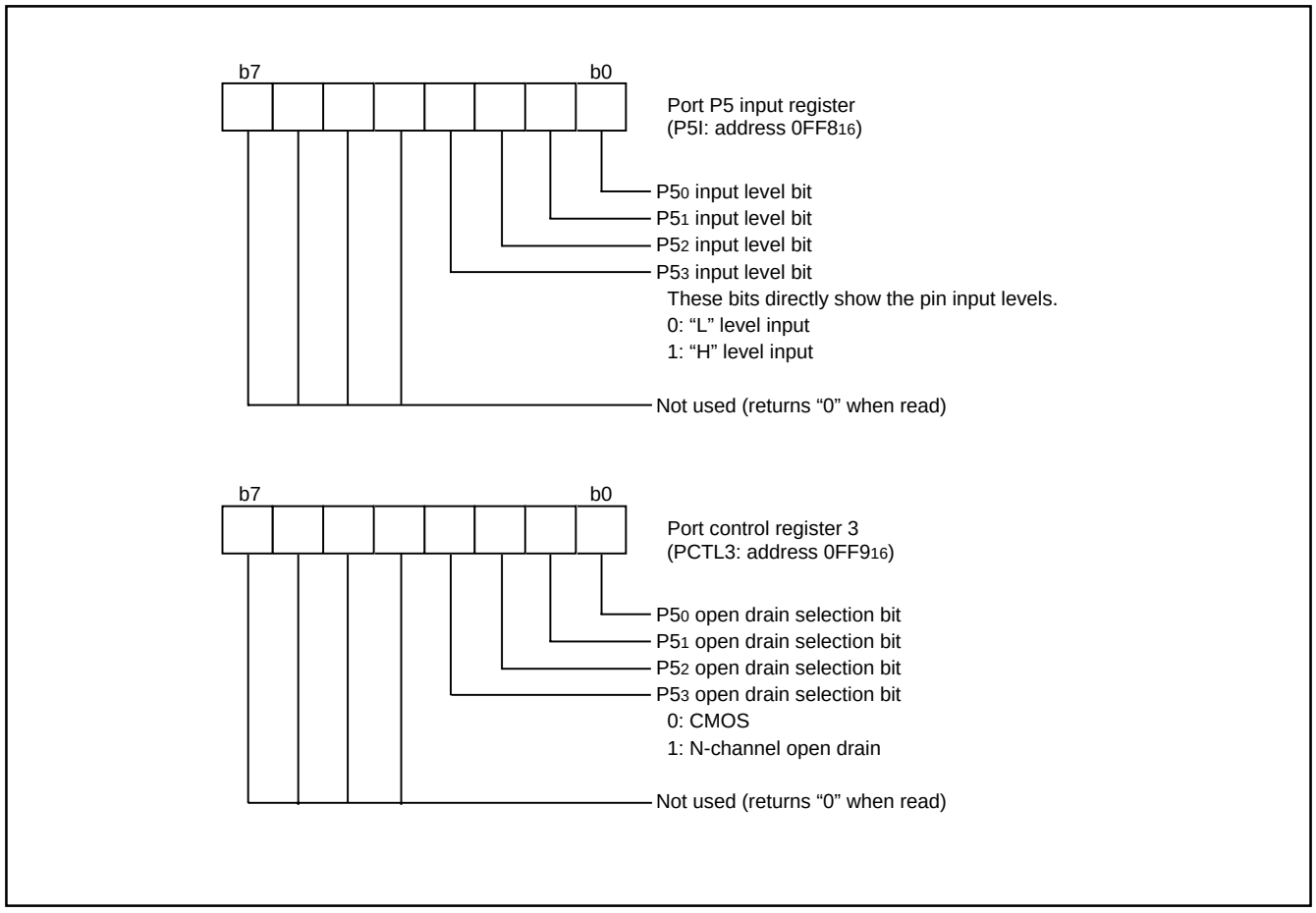


Fig. 14 Structure of port I/O related registers (2)

INTERRUPTS

Interrupts occur by 16 sources among 22 sources: thirteen external, nine internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt caused by the BRK instruction. An interrupt occurs when both the corresponding interrupt request bit and interrupt enable bit are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction interrupt cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are serviced according to the priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table and stored into the program counter.

Interrupt Source Selection

Any of the following interrupt sources can be selected by the interrupt source selection register (INTSEL).

1. INT_0 or Input buffer full
2. INT_1 or Output buffer empty
3. Serial I/O receive or $\overline{LRESET}$
4. Serial I/O transmission or SCL_{SDA}
5. Timer 2 or INT_5
6. $CNTR_0$ or INT_0
7. $CNTR_1$ or INT_1
8. A-D conversion or Key-on wake-up

External Interrupt Pin Selection

The external interrupt sources of INT_2, INT_3, and INT_4 can be selected from either input pin from INT_{20}, INT_{30}, INT_{40} or input pin from INT_{21}, INT_{31}, INT_{41} by the INT_2, INT_3, INT_4 interrupt switch bit (bit 4 of PCTL2).

■ Notes

When setting the followings, the interrupt request bit may be set to "1".

•When setting external interrupt active edge
Related register: Interrupt edge selection register (address $003A_{16}$); Timer XY mode register (address 0023_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: Interrupt source selection register (address 0039_{16})

•When setting input pin of external interrupts INT_2, INT_3 and INT_4
Related register: INT_2, INT_3, INT_4 interrupt switch bit of Port control register 2 (bit 4 of address $002F_{16}$)

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

① Set the corresponding interrupt enable bit to "0" (disabled).
② Set the active edge selection bit or the interrupt source selection bit to "1".
③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the corresponding interrupt enable bit to "1" (enabled).

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
Input buffer full (IBF)				At input data bus buffer writing	
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Output buffer empty (OBE)				At output data bus buffer reading	
Serial I/O reception	4	FFF716	FFF616	At completion of serial I/O data reception	Valid when serial I/O is selected
$\overline{\text{LRESET}}$				At falling edge of $\overline{\text{LRESET}}$ input	External interrupt
Serial I/O transmission	5	FFF516	FFF416	At completion of serial I/Otransfer shift or when transmission buffer is empty	Valid when serial I/O is selected
SCL, SDA				At detection of either rising or falling edge of SCL or SDA	External interrupt (active edge selectable)
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer Y	7	FFF116	FFF016	At timer Y underflow	
Timer 1	8	FFEF16	FFEE16	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED16	FFEC16	At timer 2 underflow	
INT5				At detection of either rising or falling edge of INT5 input	External interrupt (active edge selectable)
CNTR0	10	FFEB16	FFEA16	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
INT0				At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
CNTR1	11	FFE916	FFE816	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
INT1				At detection of either rising or falling edge of INT1 input	External interrupt (falling valid)
I^2C	12	FFE716	FFE616	At completion of data transfer	
INT2	13	FFE516	FFE416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
INT3	14	FFE316	FFE216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
INT4	15	FFE116	FFE016	At detection of either rising or falling edge of INT4 input	External interrupt (active edge selectable)
A-D converter	16	FFDF16	FFDE16	At completion of A-D conversion	
Key-on wake-up				At falling of port P3 (at input) input logical level AND	External interrupt (falling valid)
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset functions in the same way as an interrupt with the highest priority.

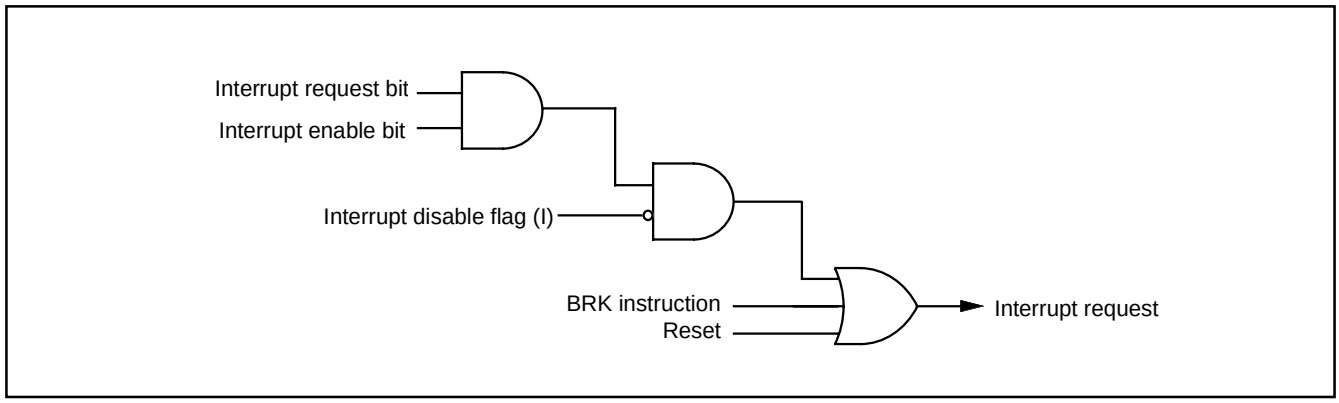


Fig. 15 Interrupt control

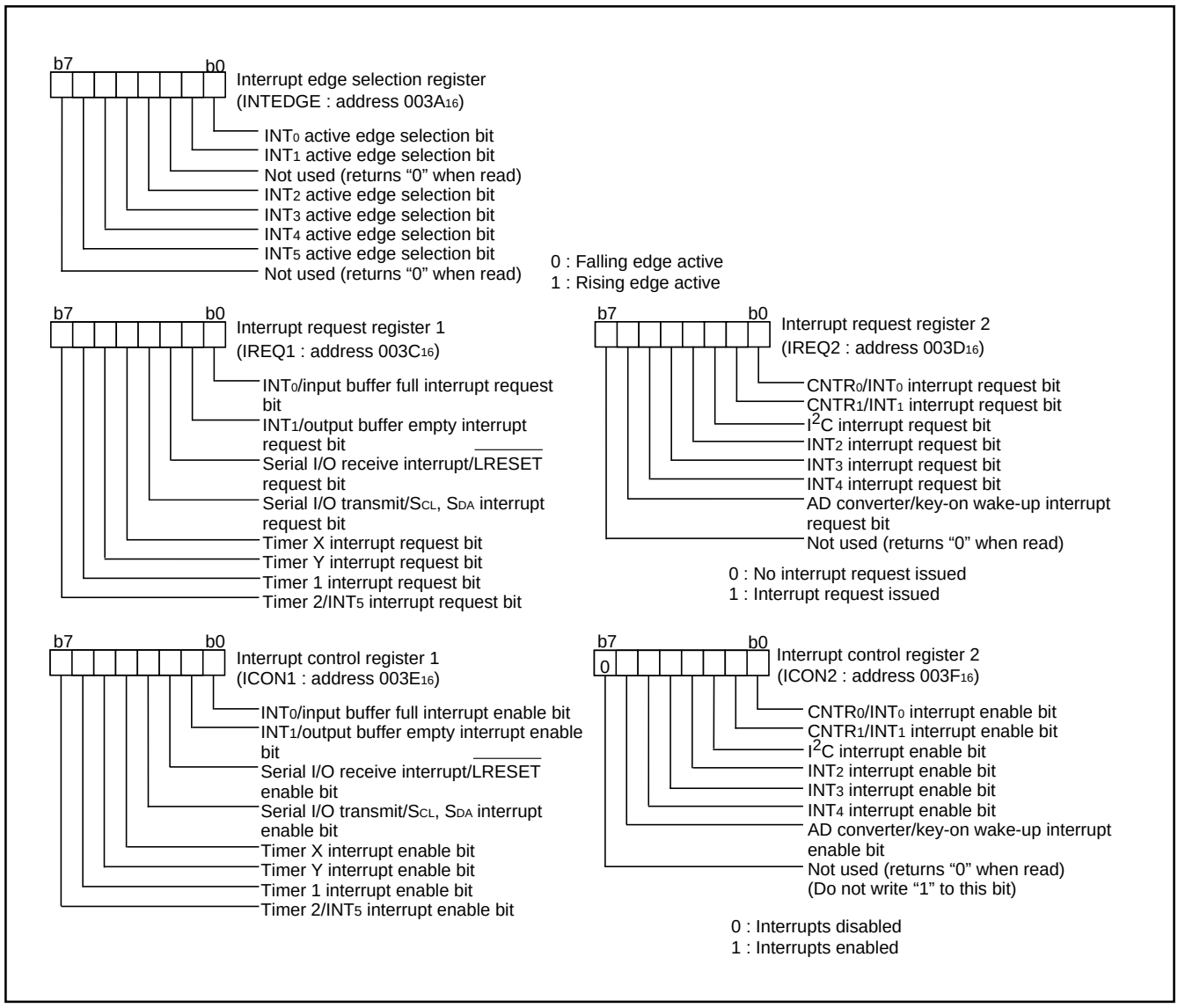


Fig. 16 Structure of interrupt-related registers (1)

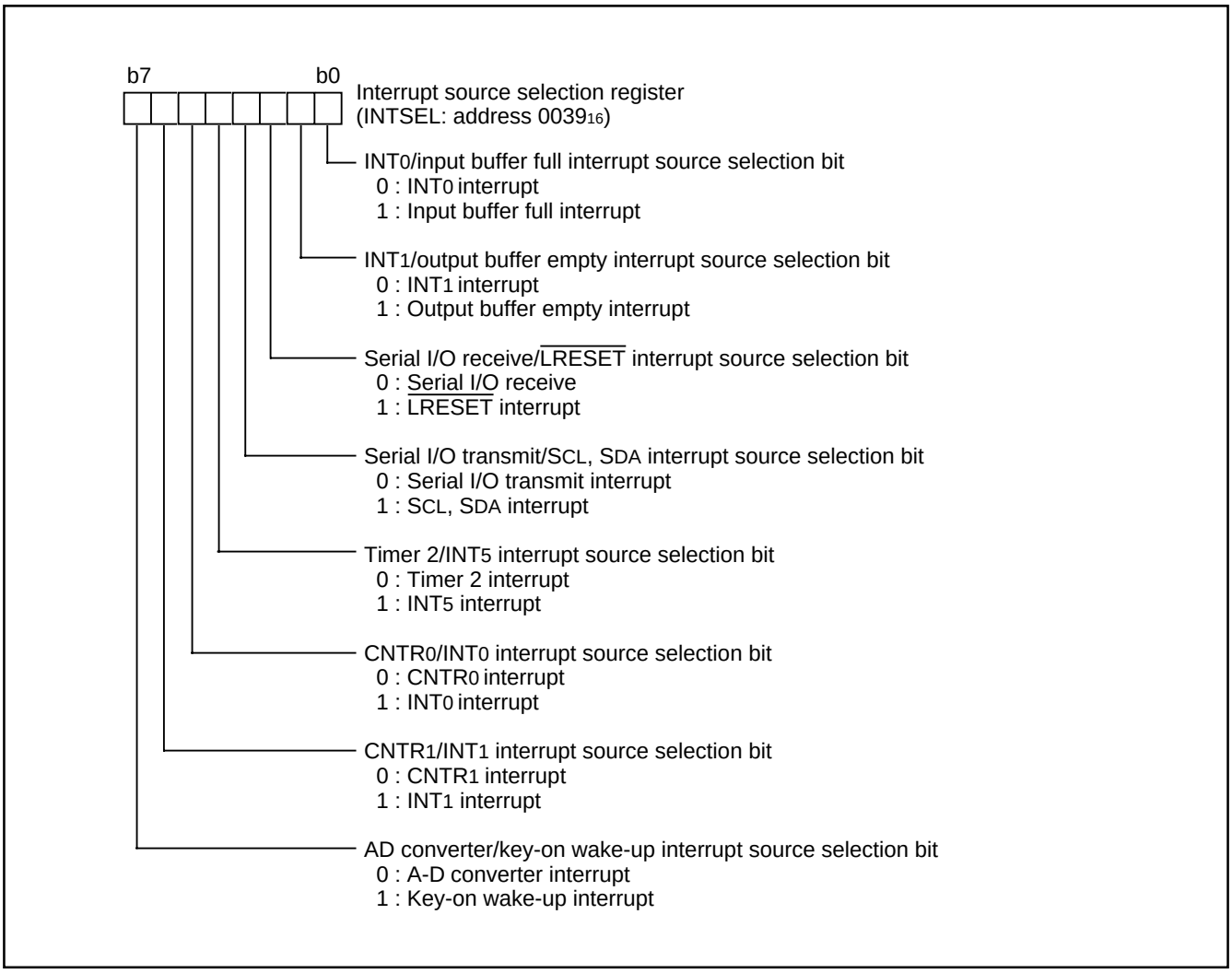


Fig. 17 Structure of interrupt-related registers (2)

Key Input Interrupt (Key-on Wake Up)

A Key input interrupt request is generated by applying "L" level to any pin of port P3 that have been set to input mode. In other words, it is generated when the logical AND of all port P3 input goes from "1" to "0". An example of using a key input interrupt is shown in Figure 18, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P3$_0$–P3$_3$.

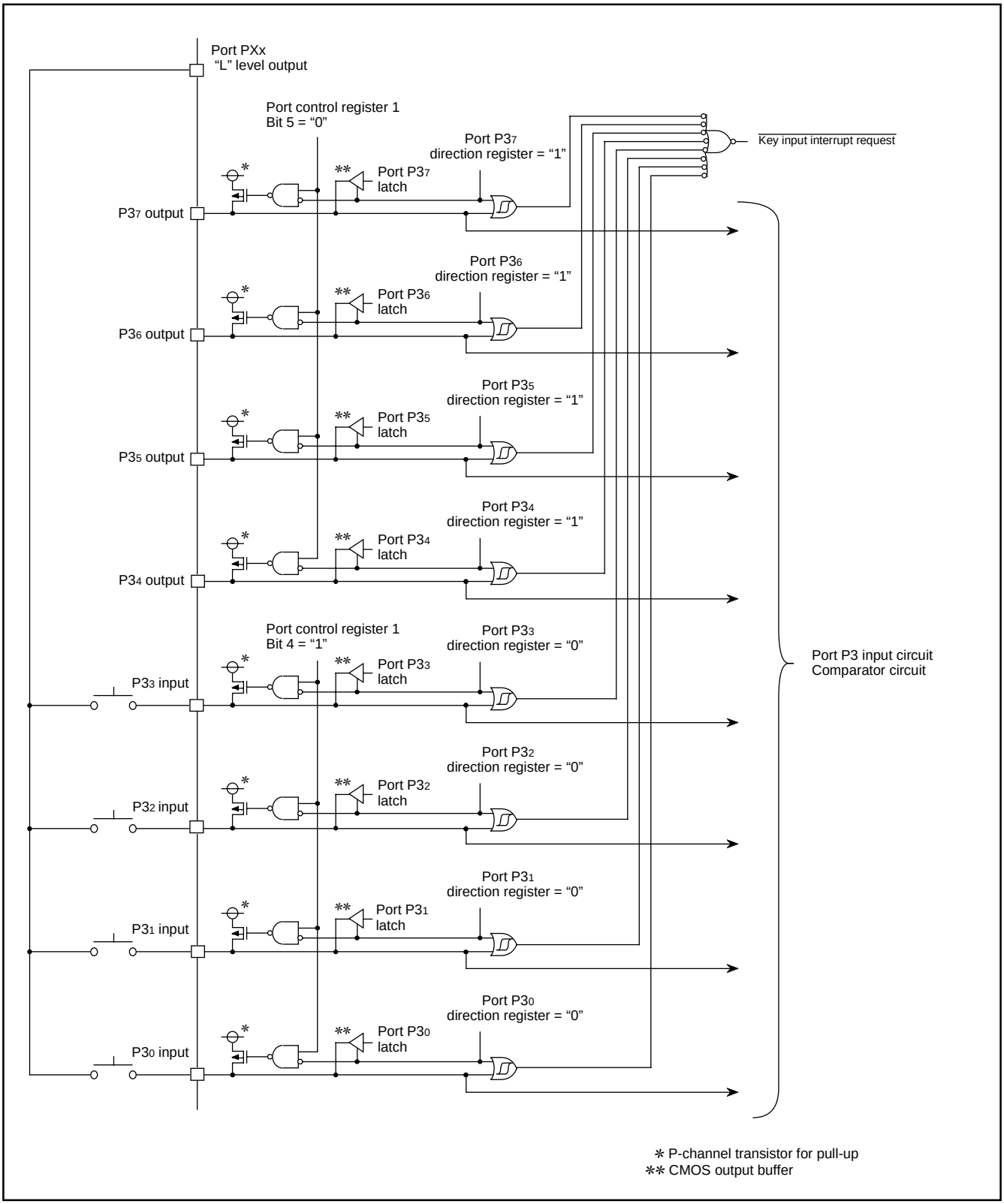


Fig. 18 Connection example when using key input interrupt and port P3 block diagram

TIMERS

The 3885 group has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are count down structure. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

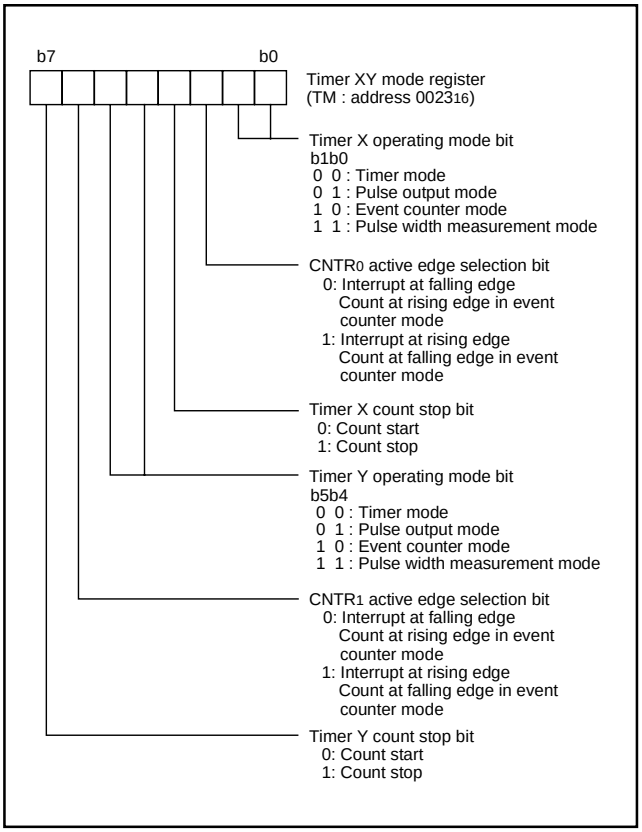


Fig. 19 Structure of timer XY mode register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each select one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts f(X_{IN})/16.

(2) Pulse Output Mode

Timer X (or timer Y) counts f(X_{IN})/16. Whenever the contents of the timer reach "00_{16}", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", output begins at " H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P5_4$ (or port $P5_5$) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the rising edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the falling edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

(4) Pulse Width Measurement Mode

If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the timer counts f(X_{IN})/16 while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the timer counts while the $CNTR_0$ (or $CNTR_1$) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer overflows.

The count source for timer Y in the timer mode or the pulse output mode can be selected from either f(X_{IN})/16 or f(X_{CIN}) by the timer Y count source selection bit of the port control register 2 (bit 5 of PCTL2).

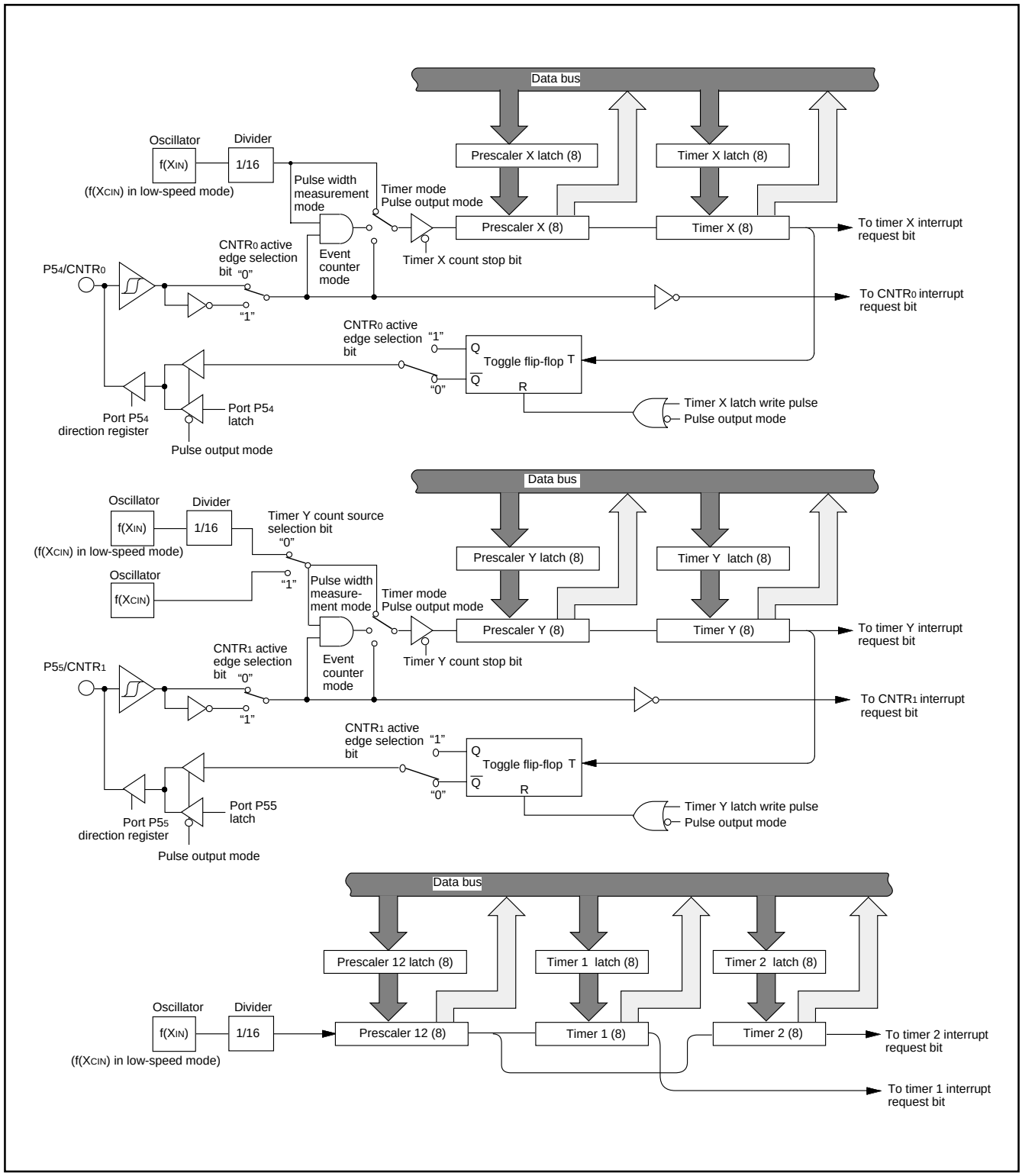


Fig. 20 Block diagram of timer X, timer Y, timer 1, and timer 2

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Basic Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (WDTCON) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (WDTCON) and an internal reset occurs at an underflow of the watchdog timer H.
Accordingly, programming is usually performed so that writing to the watchdog timer control register (WDTCON) may be started before an underflow. When the watchdog timer control register (WDTCON) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

Initial Value of Watchdog Timer

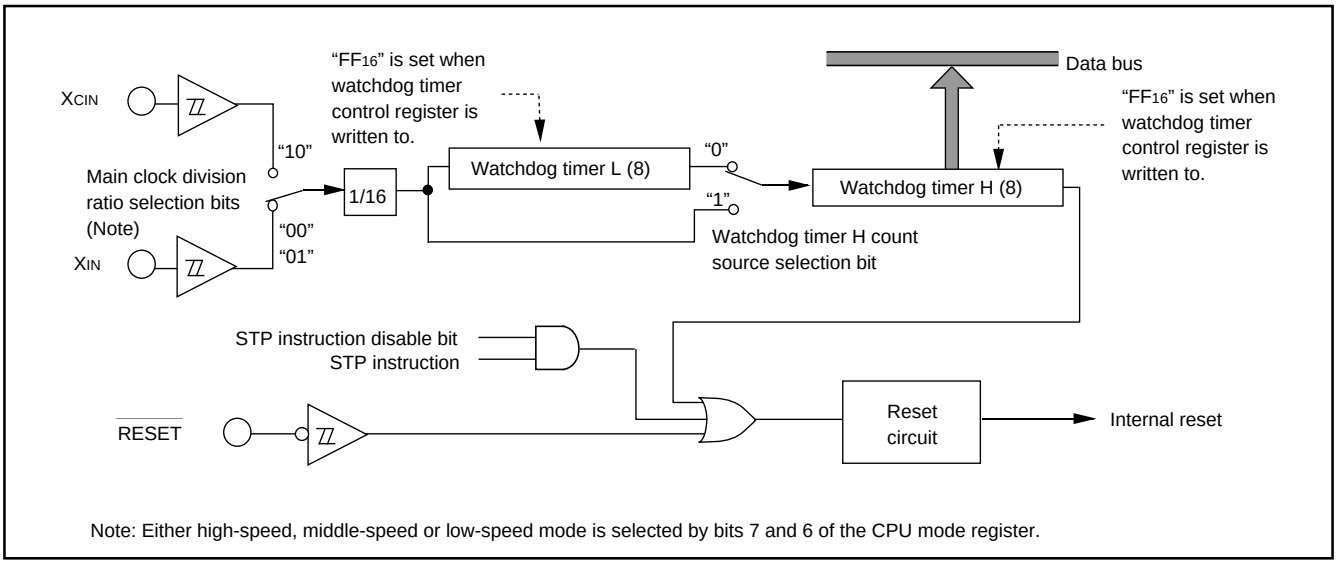
At reset or writing to the watchdog timer control register (WDTCON), each watchdog timer H and L is set to "FF16".

●Watchdog timer H count source selection bit operation

Bit 7 of WDTCON permits selecting a watchdog timer H count source. When this bit is set to "0", the count source becomes the underflow signal of watchdog timer L. The detection time is set to 131.072 ms at f(XIN)=8 MHz and 32.768 s at f(XCIN)=32 kHz .
When this bit is set to "1", the count source becomes the signal divided by 16 for f(XIN) (or f(XCIN) in low speed mode). The detection time in this case is set to 512 μs at f(XIN)=8 MHz and 128 ms at f(XCIN)=32 kHz . This bit is cleared to "0" after resetting.

●STP instruction disable bit

Bit 6 of WDTCON permits disabling the STP instruction when the watchdog timer is in operation.
When this bit is "0", the STP instruction is enabled.
When this bit is "1", the STP instruction is disabled.
When this bit is "1", the STP instruction execution cause an internal reset. When this bit is set to "1", it cannot be rewritten to "0" by program. This bit is cleared to "0" after resetting.



Note: Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register.

Fig. 21 Block diagram of Watchdog timer

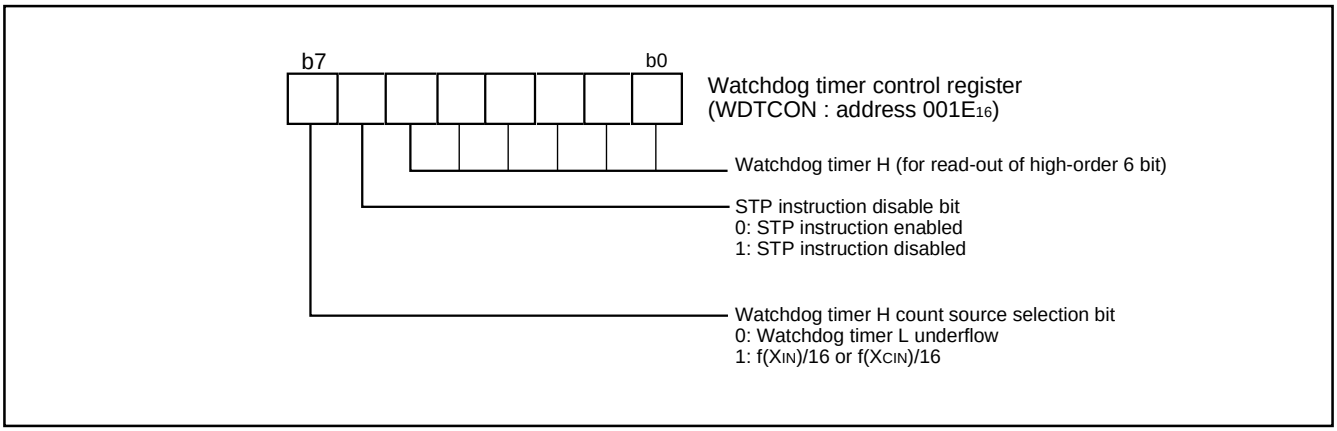


Fig. 22 Structure of Watchdog timer control register

PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT

The 3885 group has two PWM output circuits, PWM0 and PWM1, with 14-bit resolution respectively. These can operate independently. When the oscillation frequency XIN is 8 MHz, the minimum resolution bit width is 250 ns and the cycle period is 4096 µs. The PWM timing generator supplies a PWM control signal based on a signal that is the frequency of the XIN clock.

The following explanation assumes f(XIN) = 8 MHz.

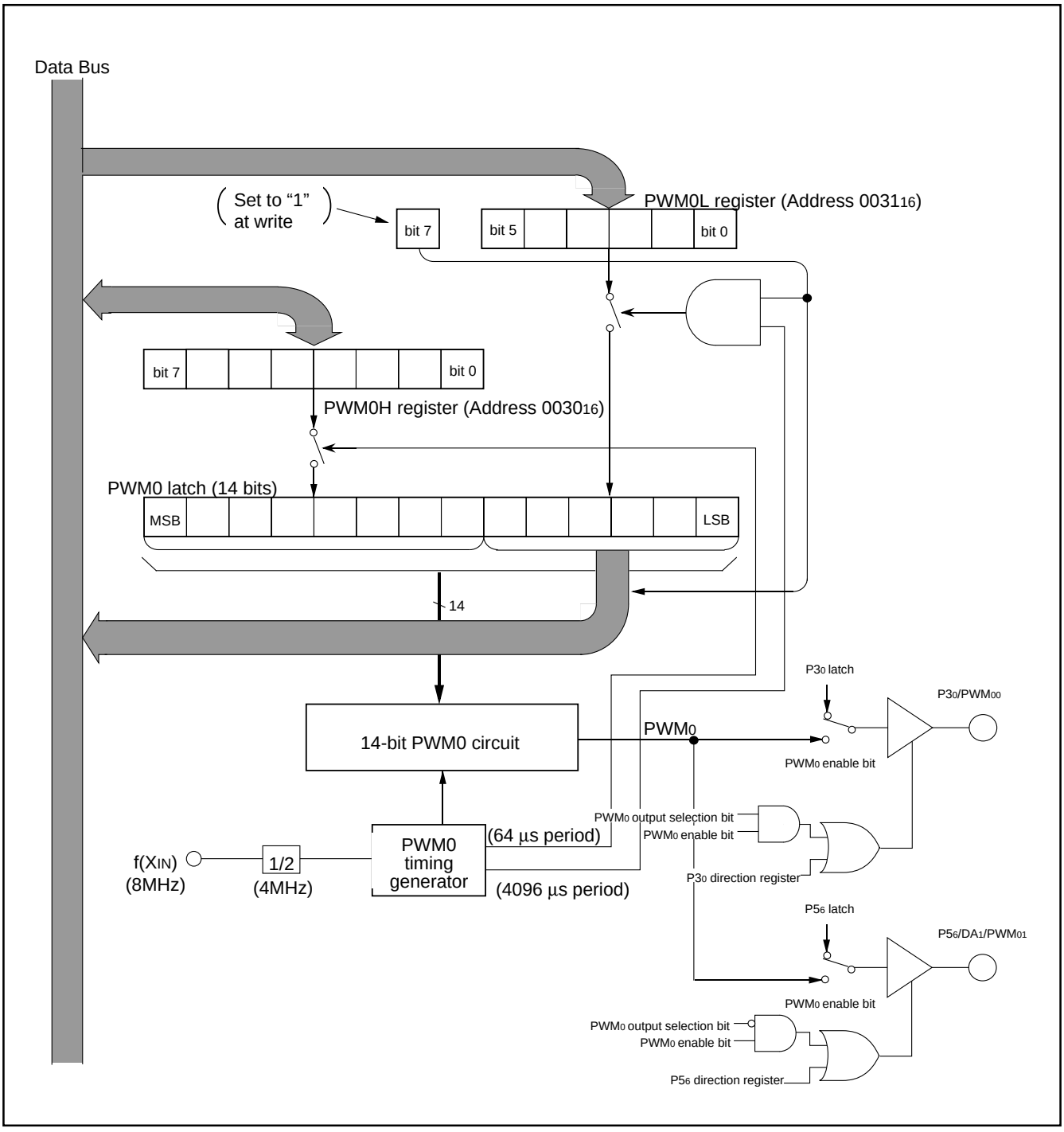


Fig. 23 PWM block diagram (PWM0)

Data Setup (PWM0)

The PWM0 output pin also functions as port $P3_0$ or $P5_6$. The PWM0 output pin is selected from either $P3_0/PWM_{00}$ or $P5_6/PWM_{01}$ by PWM_0 output pin selection bit (bit 4 of ADCON).
The PWM0 output becomes enabled state by setting PWM_0 enable bit (bit 6 of PCTL1). The high-order eight bits of output data are set in the PWM0H register and the low-order six bits are set in the PWM0L register.
PWM1 is set as the same way.

PWM Operation

The 14-bit PWM data is divided into the low-order six bits and the high-order eight bits in the PWM latch.
The high-order eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is 256 × τ (64 μs) long. The signal is "H" for a length equal to N times τ, where τ is the minimum resolution (250 ns).
"H" or "L" of the bit in the ADD part shown in Figure 24 is added to this "H" duration by the contents of the low-order 6-bit data according to the rule in Table 9.
That is, only in the sub-period tm shown by Table 9 in the PWM cycle period T = 64t, its "H" duration is lengthened to the minimum resolution τ added to the length of other periods.

For example, if the high-order eight bits of the 14-bit data are 03_{16} and the low-order six bits are 05_{16}, the length of the "H"-level output in sub-periods t_8, t_{24}, t_{32}, t_{40}, and t_{56} is 4 τ, and its length is 3 τ in all other sub-periods.
Time at the "H" level of each sub-period almost becomes equal, because the time becomes length set in the high-order 8 bits or becomes the value plus τ, and this sub-period t (= 64 μs, approximate 15.6 kHz) becomes cycle period approximately.

Table 9 Relationship between low-order 6 bits of data and period set by the ADD bit

Low-order 6 bits of data (PWML) LSB	Sub-periods tm Lengthened (m=0 to 63)
0 0 0 0 0 0	None
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m=8, 24, 40, 56
0 0 1 0 0 0	m=4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m=1, 3, 5, 7, ... ,57, 59, 61, 63

Transfer From Register to Latch

Data written to the PWML register is transferred to the PWM latch at each PWM period (every 4096 μs), and data written to the PWMH register is transferred to the PWM latch at each sub-period (every 64 μs). The signal which is output to the PWM output pin is corresponding to the contents of this latch. When the PWML register is read, the latch contents are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0" and it is not done when bit 7 is "1".

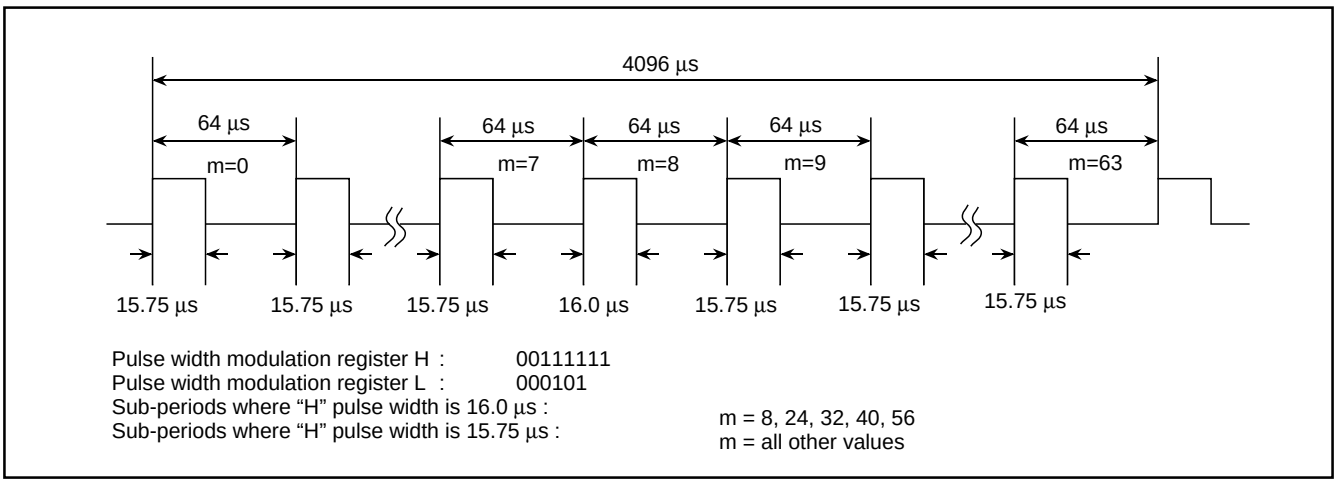


Fig. 24 PWM timing

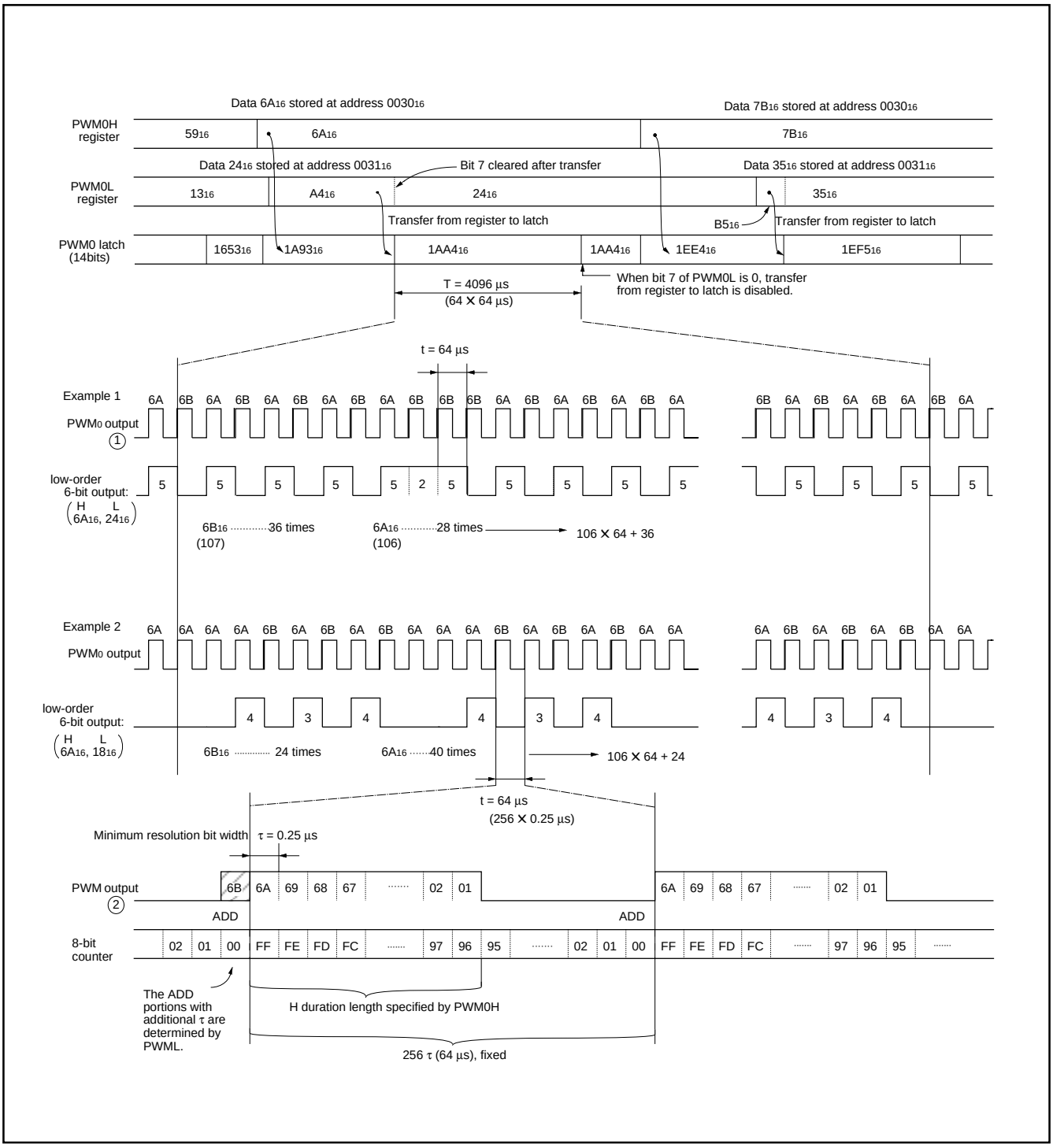


Fig. 25 14-bit PWM timing (PWM0)

SERIAL I/O
Serial I/O

Serial I/O works as either clock synchronous serial I/O mode or universal asynchronous receiver transmitter (UART) serial I/O mode. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register (bit 6 of SIOCON) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. When an internal clock is used, the transfer starts by writing to the TB.

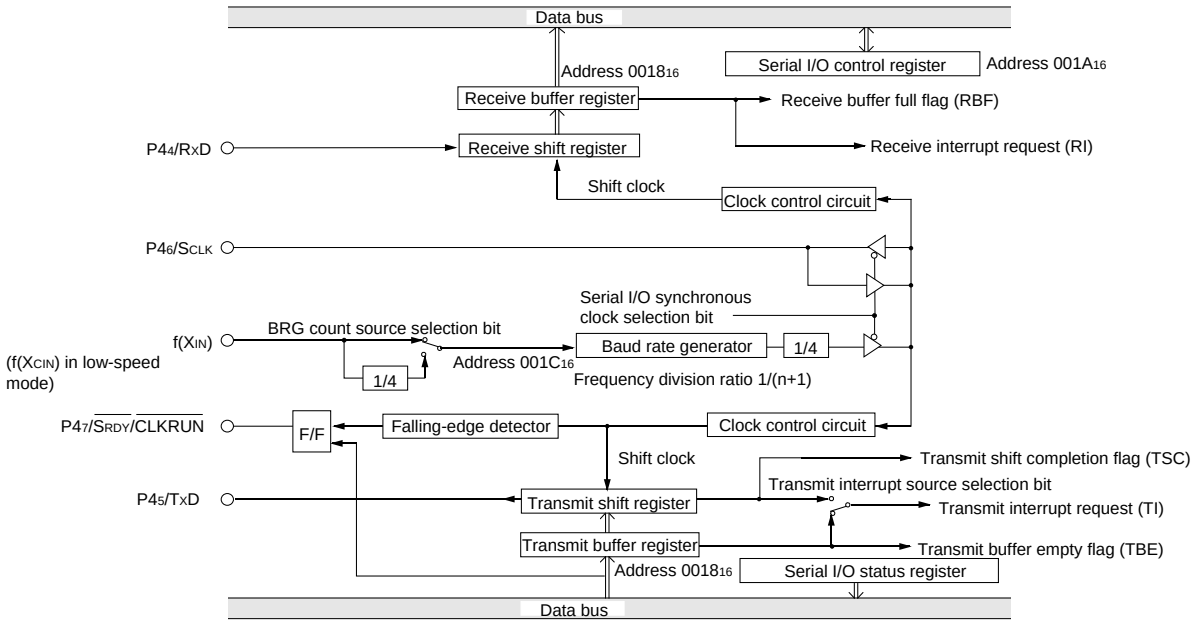
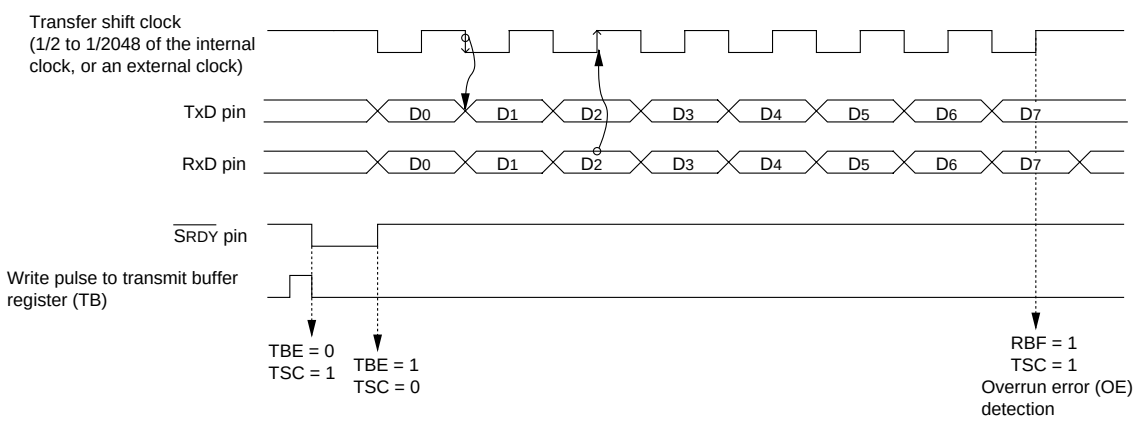


Fig. 26 Block diagram of clock synchronous serial I/O



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and the next serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 27 Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

Universal asynchronous transmitter receiver (UART) serial I/O mode can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

Both the transmit and receive shift registers have a buffer, but the two buffers assigned the same address. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

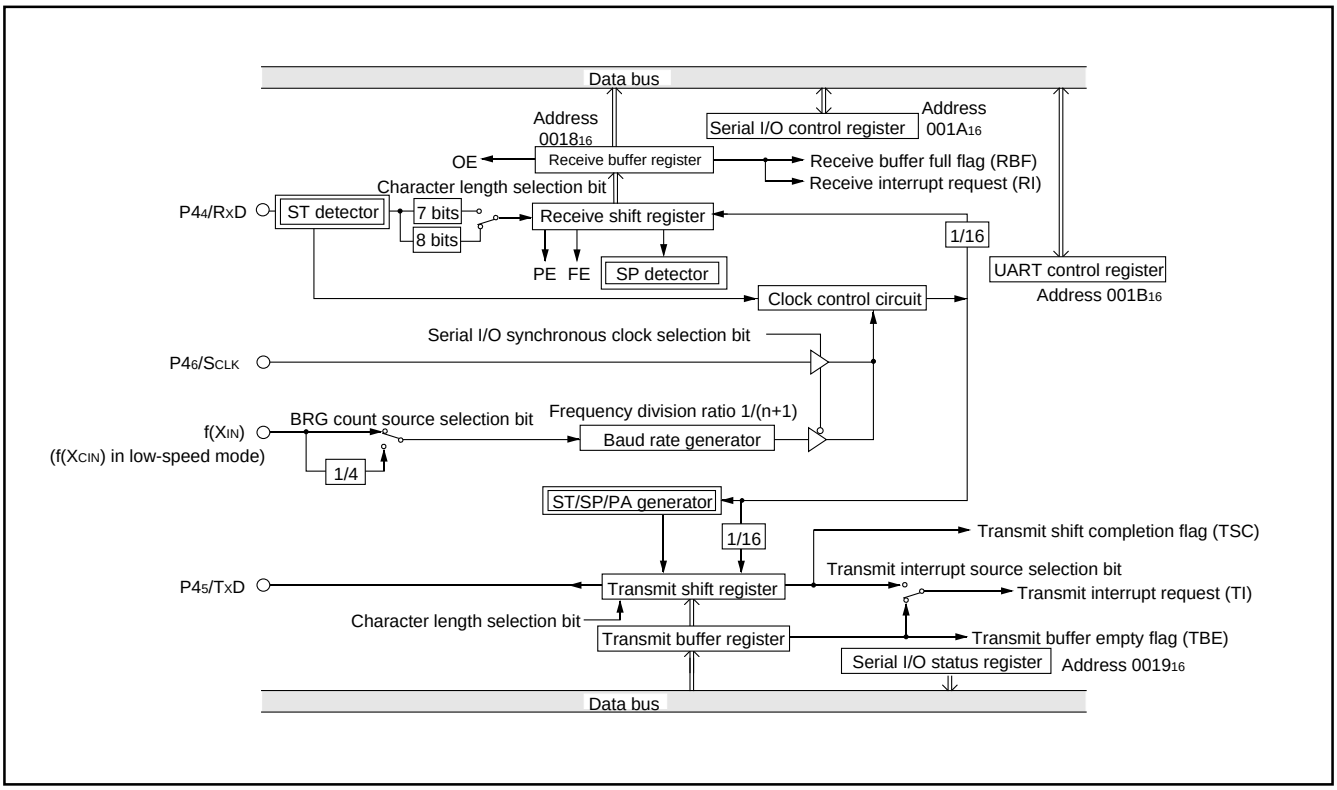
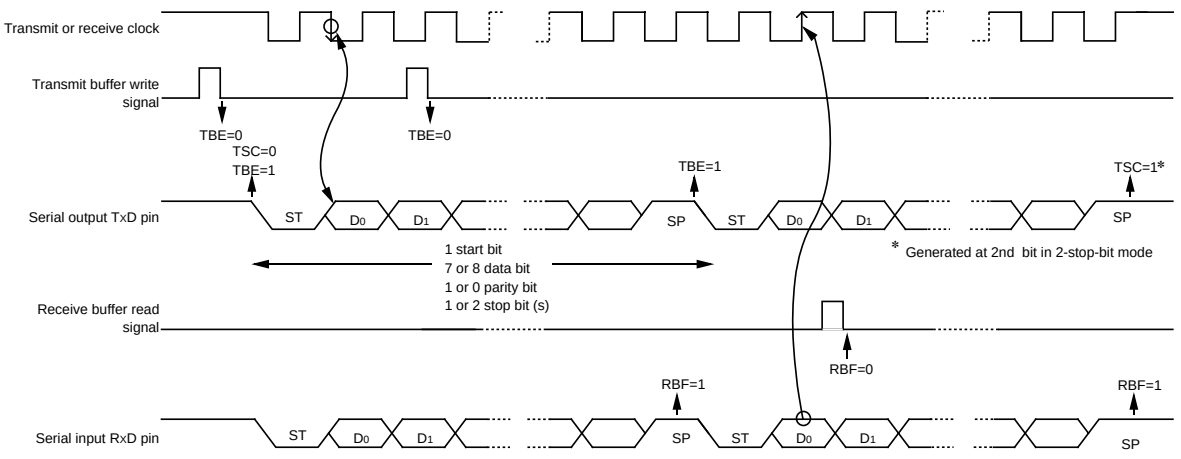


Fig. 28 Block diagram of UART mode



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1", can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1".
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 29 Operation of UART mode function

[Serial I/O Control Register (SIOCON)] 001A16

The serial I/O control register consists of eight control bits for the serial I/O function.

[UART Control Register (UARTCON)] 001B16

The UART control register consists of four control bits (bits 0 to 3) which are valid in UART mode and set the data format of an data transfer. The POFF bit (bit4) is always valid and define the output structure of the P45/TxD pin.

[Serial I/O Status Register (SIOSTS)] 001916

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit (SIOE, bit 7 of SIDCON) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (TE, bit 4 of SIOCON) has been set to "1", the transmit shift completion flag (TSC, bit 2) and the transmit buffer empty flag (TBE, bit 0) become "1".

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 001816

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character length is 7 bits, the MSB data stored in the receive buffer is "0".

[Baud Rate Generator (BRG)] 001C16

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■ Notes

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
② Set the transmit enable bit to "1".
③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

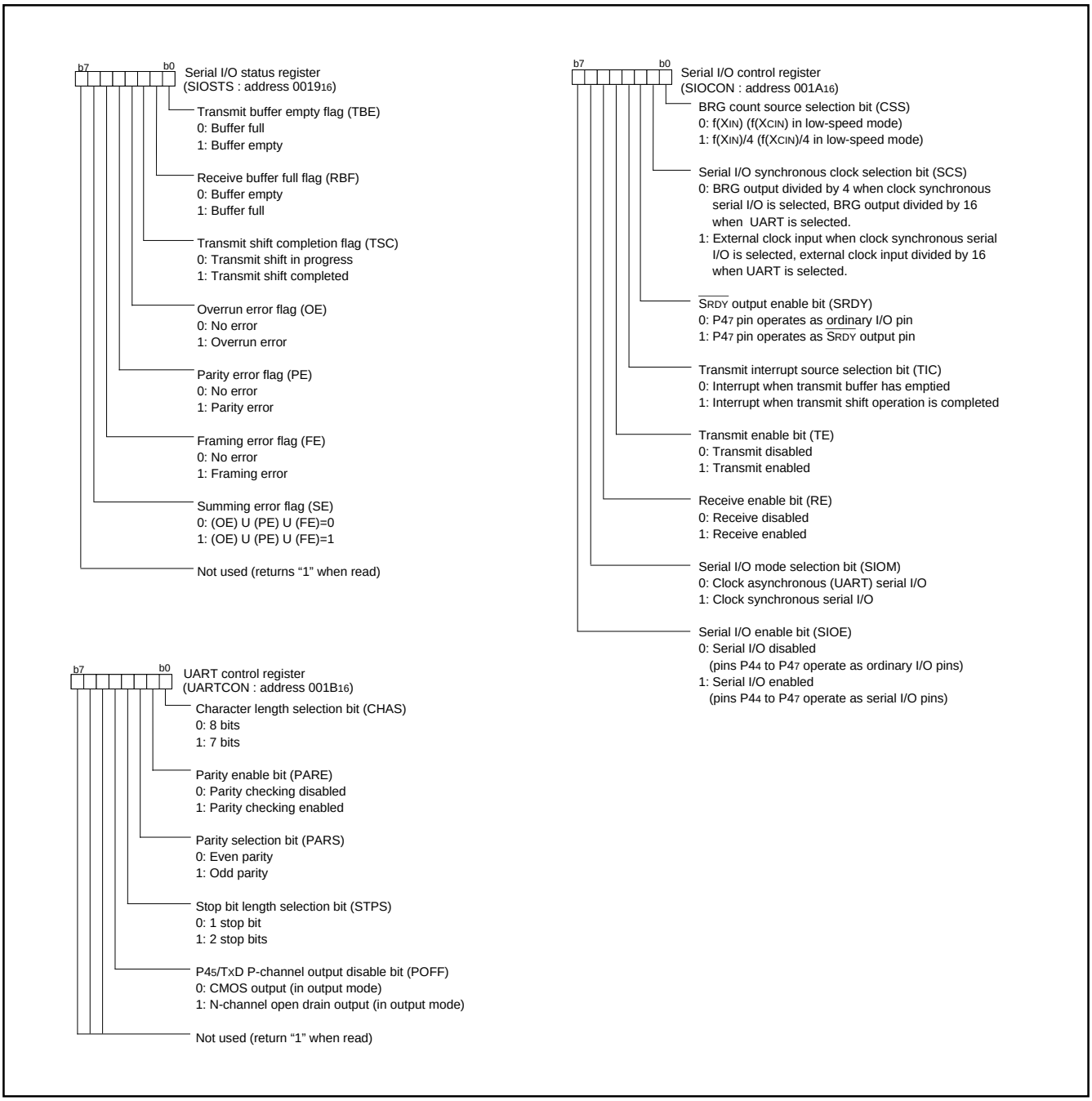


Fig. 30 Structure of serial I/O control registers

MULTI-MASTER I²C-BUS INTERFACE

The multi-master I²C-BUS interface is a serial communications circuit, conforming to the Philips I²C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 31 shows a block diagram of the multi-master I²C-BUS interface and Table 10 lists the multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C address register, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register, the I²C start/stop condition control register and other control circuits.

When using the multi-master I²C-BUS interface, set 1 MHz or more to system clock ϕ.

Table 10 Multi-master I²C-BUS interface functions

Item	Function
Format	In conformity with Philips I²C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I²C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ = 4 MHz)

System clock ϕ = f(XIN)/2 (high-speed mode)
ϕ = f(XIN)/8 (middle-speed mode)

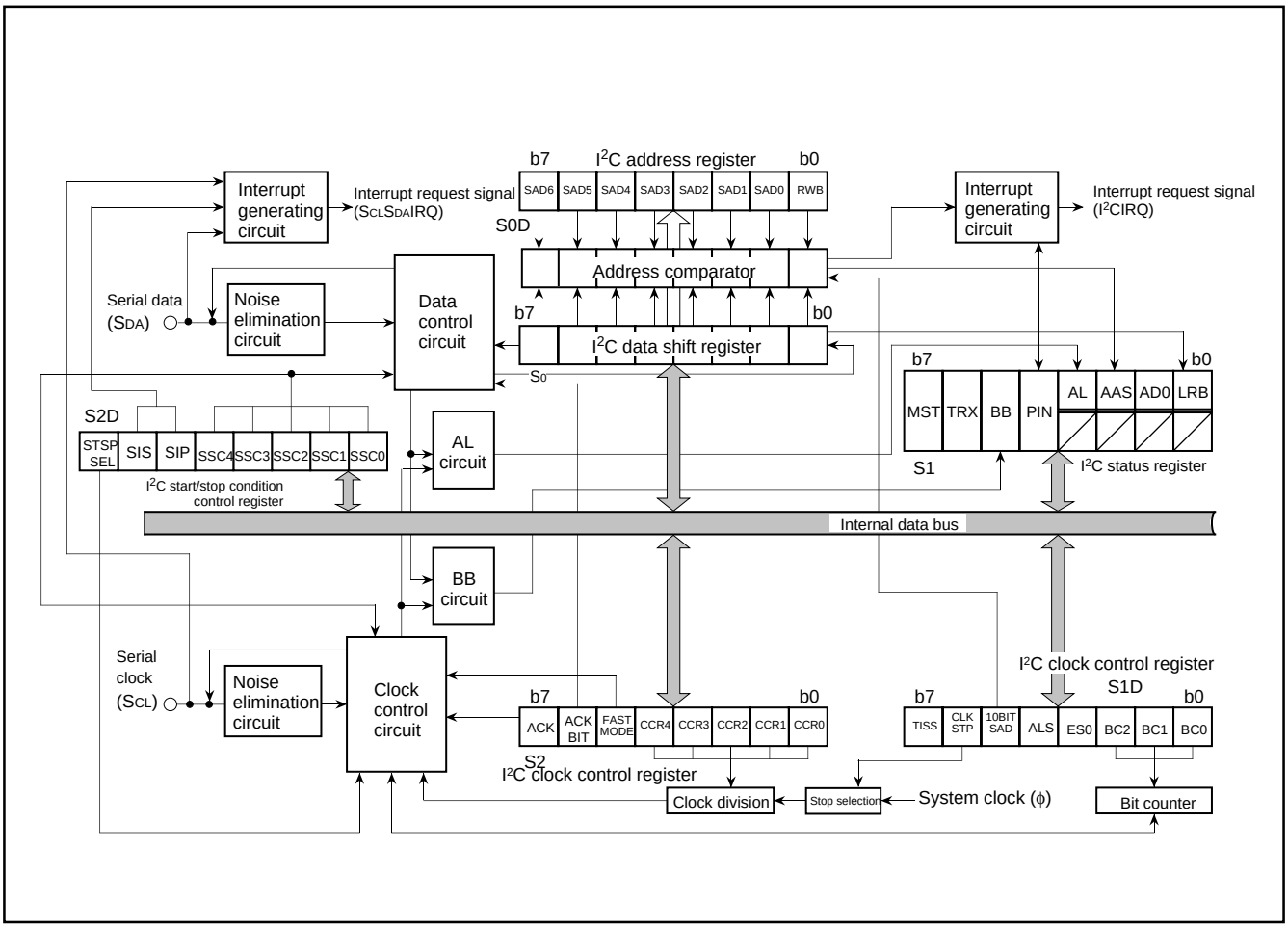


Fig. 31 Block diagram of multi-master I²C-BUS interface

✻ : Purchase of MITSUBISHI ELECTRIC CORPORATIONS I²C components conveys a license under the Philips I²C Patent Rights to use these components an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

[I²C Data Shift Register (S0)] 0012₁₆

The I²C data shift register (S0) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted by one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted by one bit to the left. The minimum 2 cycles of ϕ are required from the rising of the SCL clock until input to this register.

The I²C data shift register is in a write enable status only when the I²C-BUS interface enable bit (ES0 bit : bit 3 S1D) of the I²C control register is "1". The bit counter is reset by a write instruction to the I²C data shift register. When both the ES0 bit and the MST bit of the I²C status register (S1) are "1", the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ES0 bit value.

[I²C Address Register (S0D)] 0013₁₆

The I²C address register (S0D) consists of a 7-bit slave address and a read/$\overline{\text{write}}$ bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition is detected.

•Bit 0: Read/$\overline{\text{write}}$ bit (RWB)

This is not used in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RWB) of the I²C address register.

The RWB bit is cleared to "0" automatically when the stop condition is detected.

•Bits 1 to 7: Slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared these bits.

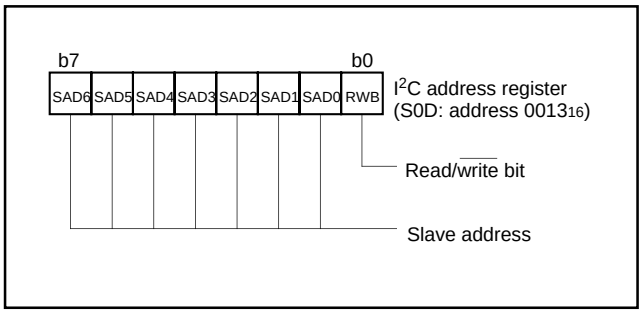


Fig. 32 Structure of I²C address register

[I²C Clock Control Register (S2)] 0016₁₆

The I²C clock control register (S2) is used to set ACK control, SCL mode and SCL frequency.

•Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 11.

•Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0", the standard clock mode is selected. When the bit is set to "1", the high-speed clock mode is selected.

When connecting the bus of the high-speed mode I²C bus standard (maximum 400 kbits/s), use 8 MHz or more oscillation frequency f(XIN) and high-speed mode (2 division main clock).

•Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0", the ACK return mode is selected and SDA goes to "L" at the occurrence of an ACK clock. When the bit is set to "1", the ACK non-return mode is selected. The SDA is held in the "H" status at the occurrence of an ACK clock.

However, when the slave address matches with the address data in the reception of address data at ACK BIT = "0", the SDA is automatically made "L" (ACK is returned). If there is a unmatch between the slave address and the address data, the SDA is automatically made "H" (ACK is not returned).

*ACK clock: Clock for acknowledgment

•Bit 7: ACK clock bit (ACK)

This bit specifies the mode of acknowledgment which is an acknowledgment response of data transfer. When this bit is set to "0", the no ACK clock mode is selected. In this case, no ACK clock occurs after data transmission. When the bit is set to "1", the ACK clock mode is selected and the master generates an ACK clock each completion of each 1-byte data transfer. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (makes SDA "H") and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transfer. If data is written during transfer, the I²C clock generator is reset, so that data cannot be transferred normally.

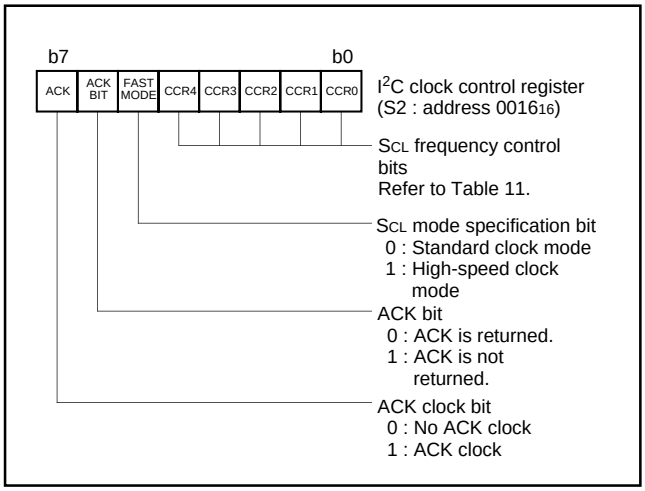


Fig. 33 Structure of I²C clock control register

Table 11 Set values of I²C clock control register and SCL frequency

Setting value of CCR4–CCR0					SCL frequency (at ϕ = 4 MHz, unit : kHz) **(Note 1)**	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard clock mode	High-speed clock mode
0	0	0	0	0	Setting disabled	Setting disabled
0	0	0	0	1	Setting disabled	Setting disabled
0	0	0	1	0	Setting disabled	Setting disabled
0	0	0	1	1	– **(Note 2)**	333
0	0	1	0	0	– **(Note 2)**	250
0	0	1	0	1	100	400 **(Note 3)**
0	0	1	1	0	83.3	166
⋮	⋮	⋮	⋮	⋮	500/CCR value **(Note 3)**	1000/CCR value **(Note 3)**
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Notes 1: Duty of SCL clock output is 50 %. The duty becomes 35 to 45 % only when the high-speed clock mode is selected and CCR value = 5 (400 kHz, at ϕ = 4 MHz). "H" duration of the clock fluctuates from –4 to +2 cycles of ϕ in the standard clock mode, and fluctuates from –2 to +2 cycles of ϕ in the high-speed clock mode. In the case of negative fluctuation, the frequency does not increase because "L" duration is extended instead of "H" duration reduction.
These are value when SCL clock synchronization by the synchronous function is not performed. CCR value is the decimal notation value of the SCL frequency control bits CCR4 to CCR0.

2: Each value of SCL frequency exceeds the limit at ϕ = 4 MHz or more. When using these setting value, use ϕ of 4 MHz or less.

3: The data formula of SCL frequency is described below:
ϕ/(8 × CCR value) Standard clock mode
ϕ/(4 × CCR value) High-speed clock mode (CCR value ≠ 5)
ϕ/(2 × CCR value) High-speed clock mode (CCR value = 5)
Do not set 0 to 2 as CCR value regardless of ϕ frequency.
Set 100 kHz (max.) in the standard clock mode and 400 kHz (max.) in the high-speed clock mode to the SCL frequency by setting the SCL frequency control bits CCR4 to CCR0.

[I²C Control Register (S1D)] 0015₁₆

The I²C control register (S1D) controls data communication format.

•Bits 0 to 2: Bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. The I²C interrupt request signal occurs immediately after the number of count specified with these bits (ACK clock is added to the number of count when ACK clock is selected by ACK bit (bit 7 of S2)) have been transferred, and BC0 to BC2 are returned to "000₂".

Also when a START condition is received, these bits become "000₂" and the address data is always transmitted and received in 8 bits.

•Bit 3: I²C interface enable bit (ES0)

This bit enables to use the multi-master I²C BUS interface. When this bit is set to "0", the use disable status is provided, so that the SDA and the SCL become high-impedance. When the bit is set to "1", use of the interface is enabled.

When ES0 = "0", the following is performed.

- PIN = "1", BB = "0" and AL = "0" are set (which are bits of the I²C status register at S1).
- Writing data to the I²C data shift register (S0) is disabled.

•Bit 4: Data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to "0", the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "I²C Status Register", bit 1) is received, transfer processing can be performed. When this bit is set to "1", the free data format is selected, so that slave addresses are not recognized.

•Bit 5: Addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0", the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (S0D) are compared with address data. When this bit is set to "1", the 10-bit addressing format is selected, and all the bits of the I²C address register are compared with address data.

•Bit 6: System clock stop selection bit (CLKSTP)

When executing the WIT or STP instruction, this bit selects the condition of system clock provided to the multi-master I²C-BUS interface. When this bit is set to "0", system clock and operation of the multi-master I²C-BUS interface stop by executing the WIT or STP instruction.

When this bit is set to "1", system clock and operation of the multi-master I²C-BUS interface do not stop even when the WIT instruction is executed.

When the system clock stop selection bit is "1", do not execute the STP instruction.

•Bit 7: I²C-BUS interface pin input level selection bit

This bit selects the input level of the SCL and SDA pins of the multi-master I²C-BUS interface.

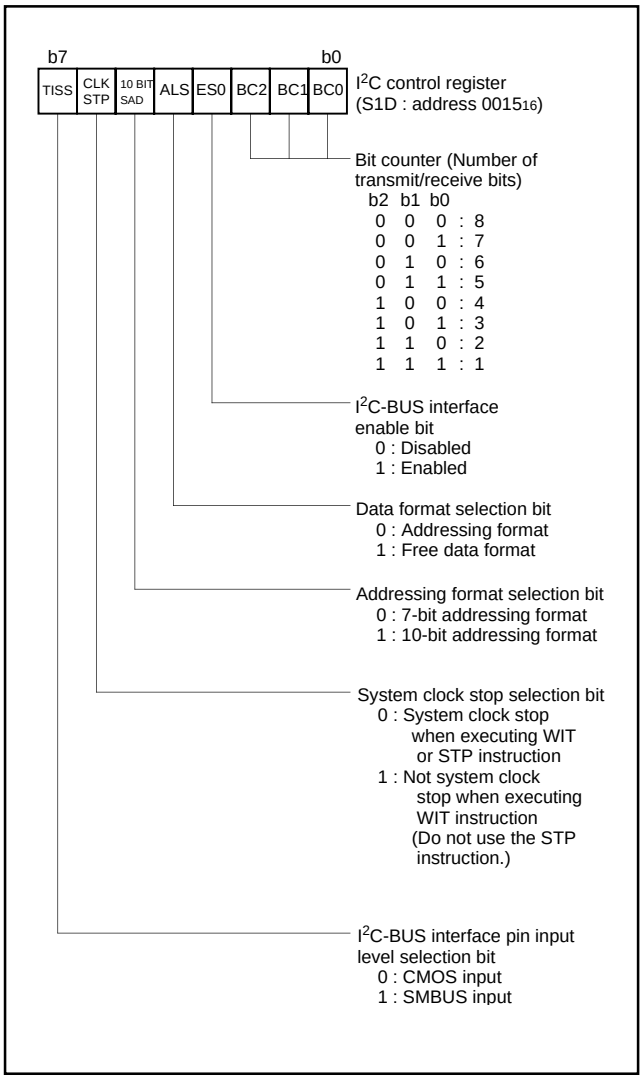


Fig. 34 Structure of I²C control register

[I²C Status Register (S1)] 0014₁₆

The I²C status register (S1) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

Set "0000₂" to the low-order 4 bits, because these bits become the reserved bits at writing.

•Bit 0: Last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0". If ACK is not returned, this bit is set to "1". Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (S0).

•Bit 1: General call detecting flag (AD0)

When the ALS bit is "0", this bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition, or reset.

*General call: The master transmits the general call address "00₁₆" to all slaves.

•Bit 2: Slave address comparison flag (AAS)

This flag indicates a comparison result of address data when the ALS bit is "0".

① In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions:
- The address data immediately after occurrence of a START condition agrees with the slave address stored in the high-order 7 bits of the I²C address register (S0D).
- A general call is received.

② In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition:
- When the address data is compared with the I²C address register (8 bits consisting of slave address and RWB bit), the first bytes agree.

③ This bit is set to "0" by executing a write instruction to the I²C data shift register (S0) when ES0 is set to "1" or reset.

•Bit 3: Arbitration lost* detecting flag (AL)

In the master transmission mode, when the SDA is made "L" by any other device, arbitration is judged to have been lost, so that this bit is set to "1". At the same time, the TRX bit is set to "0", so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0". The arbitration lost can be detected only in the master transmission mode. When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to detect the agreement of its own slave address and address data transmitted by another master device.

*Arbitration lost : The status in which communication as a master is disabled.

•Bit 4: SCL pin low hold bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the PIN bit changes from "1" to "0". At the same time, an interrupt request signal occurs to the CPU. The PIN bit is set to "0" in synchronization with a falling of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling of the PIN bit. When the PIN bit is "0", the SCL is kept in the "0" state and clock generation is disabled. Figure 42 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in one of the following conditions:
- Executing a write instruction to the I²C data shift register (S0). (This is the only condition which the prohibition of the internal clock is released and data can be communicated except for the start condition detection.)
- When the ES0 bit is "0"
- At reset
- When writing "1" to the PIN bit by software

The conditions in which the PIN bit is set to "0" are shown below:
- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address agreement or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

•Bit 5: Bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0", this bus system is not busy and a START condition can be generated. The BB flag is set/reset by the SCL, SDA pins input signal regardless of master/slave. This flag is set to "1" by detecting the start condition, and is set to "0" by detecting the stop condition. The condition of these detecting is set by the start/stop condition setting bits (SSC4–SSC0) of S2D. When the ES0 bit (bit 3 of S1D) is "0" or reset, the BB flag is set to "0".

For the writing function to the BB flag, refer to the sections "START Condition Generating Method" and "STOP Condition Generating Method" described later.

•Bit 6: Communication mode specification bit (transfer direction specification bit: TRX)

This bit decides a direction of transfer for data communication. When this bit is "0", the reception mode is selected and the data of a transmitting device is received. When the bit is "1", the transmission mode is selected and address data and control data are output onto the SDA in synchronization with the clock generated on the SCL.

This bit is set/reset by software and hardware. About set/reset by hardware is described below. This bit is set to "1" by hardware when all the following conditions are satisfied:

- When ALS is "0"
- In the slave reception mode or the slave transmission mode
- When the R/$\overline{W}$ bit reception is "1"

This bit is set to "0" in one of the following conditions:

- When arbitration lost is detected.
- When a STOP condition is detected.
- When writing "1" to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

•Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is "0", the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1", the master is specified and a START condition and a STOP condition are generated. Additionally, the clocks required for data communication are generated on the SCL.

This bit is set to "0" in one of the following conditions.

- Immediately after completion of 1-byte data transfer when arbitration lost is detected
- When a STOP condition is detected.
- Writing "1" to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- At reset

Note: START condition duplication preventing function
The MST, TRX, and BB bits is set to "1" at the same time after confirming that the BB flag is "0" in the procedure of a START condition occurrence. However, when a START condition by another master device occurs and the BB flag is set to "1" immediately after the contents of the BB flag is confirmed, the START condition duplication preventing function makes the writing to the MST and TRX bits invalid. The duplication preventing function becomes valid from the rising of the BB flag to reception completion of slave address.

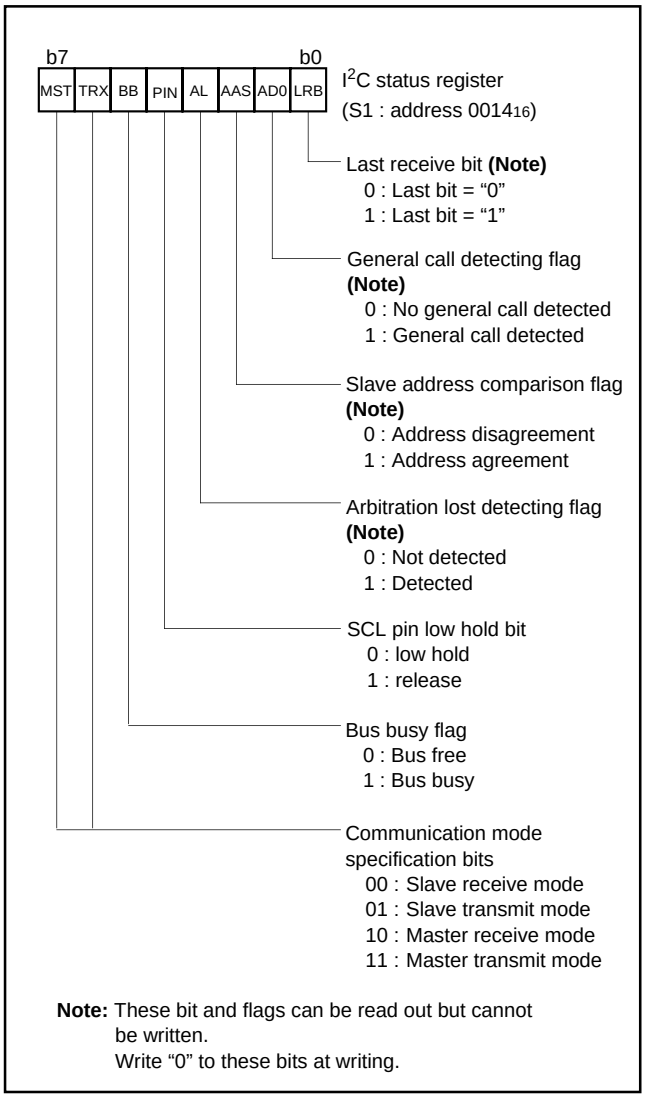


Fig. 35 Structure of I2C status register

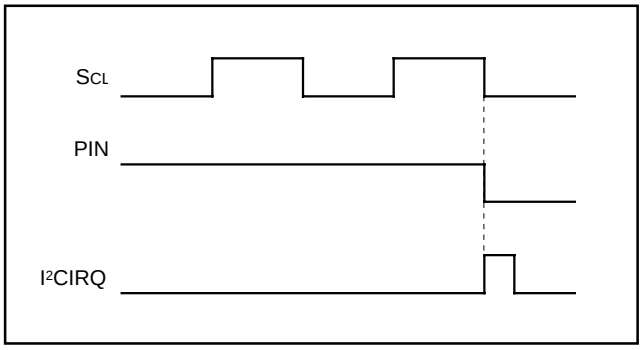


Fig. 36 Interrupt request signal generating timing

START Condition Generating Method

When writing "1" to the MST, TRX, and BB bits of the I²C status register (S1) at the same time after writing the slave address to the I²C data shift register (S0) with the condition in which the ES0 bit of the I²C control register (S1D) and the BB flag are "0", a START condition occurs. After that, the bit counter becomes "000₂" and an SCL for 1 byte is output. The START condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 37, the START condition generating timing diagram, and Table 12, the START condition generating timing table.

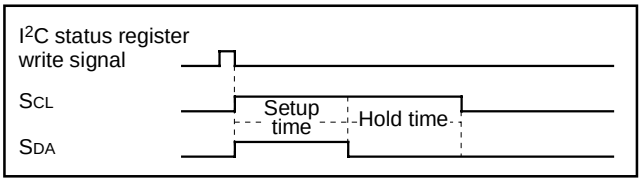


Fig. 37 START condition generating timing diagram

Table 12 START condition generating timing table

Item	START/STOP condition generating selection bit	Standard clock mode	High-speed clock mode
Setup time	"0"	5.0 µs (20 cycles)	2.5 µs (10 cycles)
	"1"	13.0 µs (52 cycles)	6.5 µs (26 cycles)
Hold time	"0"	5.0 µs (20 cycles)	2.5 µs (10 cycles)
	"1"	13.0 µs (52 cycles)	6.5 µs (26 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

STOP Condition Generating Method

When the ES0 bit of the I²C control register (S1D) is "1", write "1" to the MST and TRX bits, and write "0" to the BB bit of the I²C status register (S1) simultaneously. Then a STOP condition occurs. The STOP condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 38, the STOP condition generating timing diagram, and Table 13, the STOP condition generating timing table.

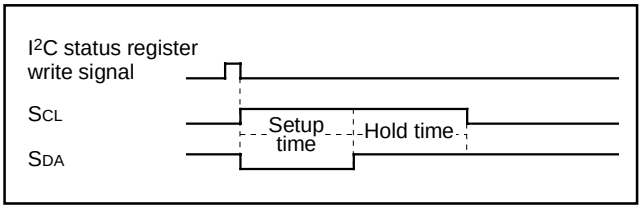


Fig. 38 STOP condition generating timing diagram

Table 13 STOP condition generating timing table

Item	START/STOP condition generating selection bit	Standard clock mode	High-speed clock mode
Setup time	"0"	5.5 µs (22 cycles)	3.0 µs (12 cycles)
	"1"	13.5 µs (54 cycles)	7.0 µs (28 cycles)
Hold time	"0"	5.5 µs (22 cycles)	3.0 µs (12 cycles)
	"1"	13.5 µs (54 cycles)	7.0 µs (28 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

START/STOP Condition Detecting Operation

The START/STOP condition detection operations are shown in Figures 39, 40, and Table 14. The START/STOP condition is set by the START/STOP condition set bit.

The START/STOP condition can be detected only when the input signal of the SCL and SDA pins satisfy three conditions: SCL release time, setup time, and hold time (see Table 14).

The BB flag is set to "1" by detecting the START condition and is reset to "0" by detecting the STOP condition.

The BB flag set/reset timing is different in the standard clock mode and the high-speed clock mode. Refer to Table 14, the BB flag set/reset time.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "I²CIRQ" occurs to the CPU.

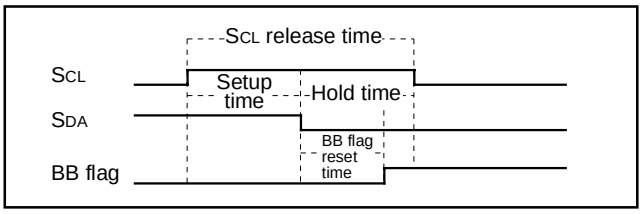


Fig. 39 START condition detecting timing diagram

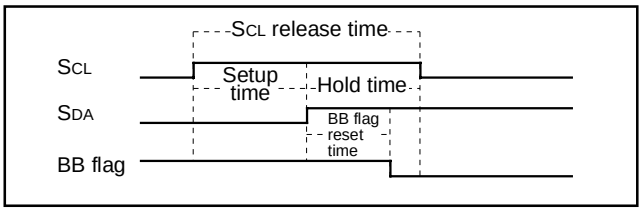


Fig. 40 STOP condition detecting timing diagram

Table 14 START condition/STOP condition detecting conditions

	Standard clock mode	High-speed clock mode
SCL release time	SSC value + 1 cycle (6.25 µs)	4 cycles (1.0 µs)
Setup time	$\frac{\text{SSC value}}{2}$ + 1 cycle < 4.0 µs (3.25 µs)	2 cycles (1.0 µs)
Hold time	$\frac{\text{SSC value}}{2}$ cycle < 4.0 µs (3.0 µs)	2 cycles (0.5 µs)
BB flag set/ reset time	$\frac{\text{SSC value} - 1}{2}$ + 2 cycles (3.375 µs)	3.5 cycles (0.875 µs)

Note: Unit : Cycle number of system clock ϕ
SSC value is the decimal notation value of the START/STOP condition set bits SSC4 to SSC0. Do not set "0" or an odd number to SSC value. The value in parentheses is an example when the I²C START/STOP condition control register is set to "18₁₆" at ϕ = 4 MHz.

[I²C START/STOP Condition Control Register (S2D)] 0017₁₆

The I²C START/STOP condition control register (S2D) controls START/STOP condition detection.

•Bits 0 to 4: START/STOP condition set bits (SSC4–SSC0)

SCL release time, setup time, and hold time change the detection condition by value of the main clock divide ratio selection bit and the oscillation frequency f(XIN) because these time are measured by the internal system clock. Accordingly, set the proper value to the START/STOP condition set bits (SSC4 to SSC0) in considered of the system clock frequency. Refer to Table 14.

Do not set "00000₂" or an odd number to the START/STOP condition set bits (SSC4 to SSC0).

Refer to Table 15, the recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency.

•Bit 5: SCL/SDA interrupt pin polarity selection bit (SIP)

An interrupt can occur when detecting the falling or rising edge of the SCL or SDA pin. This bit selects the polarity of the SCL or SDA pin interrupt pin.

•Bit 6: SCL/SDA interrupt pin selection bit (SIS)

This bit selects the pin of which interrupt becomes valid between the SCL pin and the SDA pin.

Note: When changing the setting of the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0, the SCL/SDA interrupt request bit may be set. When selecting the SCL/SDA interrupt source, disable the interrupt before the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0 is set. Reset the request bit to "0" after setting these bits, and enable the interrupt.

•Bit 7: START/STOP condition generating selection bit (STSPSEL)

Setup/Hold time when the START/STOP condition is generated can be selected.

Cycle number of system clock becomes standard for setup/hold time. Additionally, setup/hold time is different between the START condition and the STP condition. (Refer to Tables 12 and 13.) Set "1" to this bit when the system clock frequency is 4 MHz or more.

Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats are described below.

① 7-bit addressing format

To adapt the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (S1D) to "0". The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C address register (S0D). At the time of this comparison, address comparison of the RWB bit of the I²C address register (S0D) is not performed. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 42, (1) and (2).

② 10-bit addressing format

To adapt the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (S1D) to "1". An address comparison is performed between the first-byte address data transmitted from the master and the 8-bit slave address stored in the I²C address register (S0). At the time of this comparison, an address comparison between the RWB bit of the I²C address register (S0) and the R/$\overline{W}$ bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the RWB bit which is the last bit of the address data not only specifies the direction of communication for control data, but also is processed as an address data bit.

When the first-byte address data agree with the slave address, the AAS bit of the I²C status register (S1) is set to "1". After the second-byte address data is stored into the I²C data shift register (S0), perform an address comparison between the second-byte data and the slave address by software. When the address data of the 2 bytes agree with the slave address, set the RWB bit of the I²C address register (S0D) to "1" by software. This processing can make the 7-bit slave address and R/$\overline{W}$ data agree, which are received after a RESTART condition is detected, with the value of the I²C address register (S0D). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 42, (3) and (4).

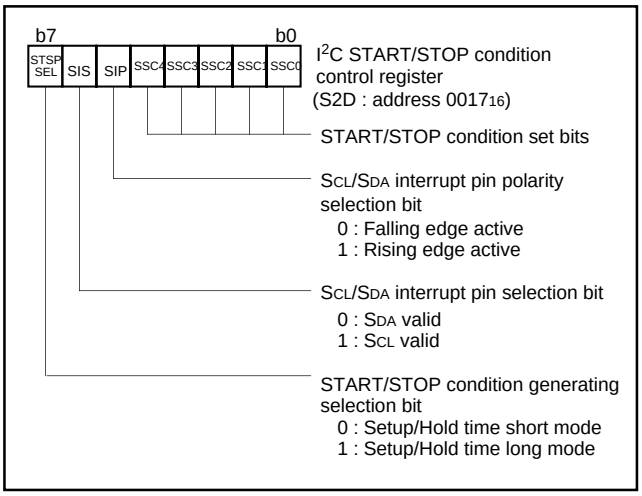


Fig. 41 Structure of I²C START/STOP condition control register

Table 15 Recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency

Oscillation frequency f(XIN) (MHz)	Main clock divide ratio	System clock ϕ (MHz)	START/STOP condition control register	SCL release time (μs)	Setup time (μs)	Hold time (μs)
8	2	4	XXX11010	6.75 μs (27 cycles)	3.5 μs (14 cycles)	3.25 μs (13 cycles)
8	8	1	XXX11000	6.25 μs (25 cycles)	3.25 μs (13 cycles)	3.0 μs (12 cycles)
			XXX00100	5.0 μs (5 cycles)	3.0 μs (3 cycles)	2.0 μs (2 cycles)
4	2	2	XXX01100	6.5 μs (13 cycles)	3.5 μs (7 cycles)	3.0 μs (6 cycles)
2	2	1	XXX01010	5.5 μs (11 cycles)	3.0 μs (6 cycles)	2.5 μs (5 cycles)
			XXX00100	5.0 μs (5 cycles)	3.0 μs (3 cycles)	2.0 μs (2 cycles)

Note: Do not set "00000₂" or an odd number to the START/STOP condition set bits (SSC4 to SSC0).

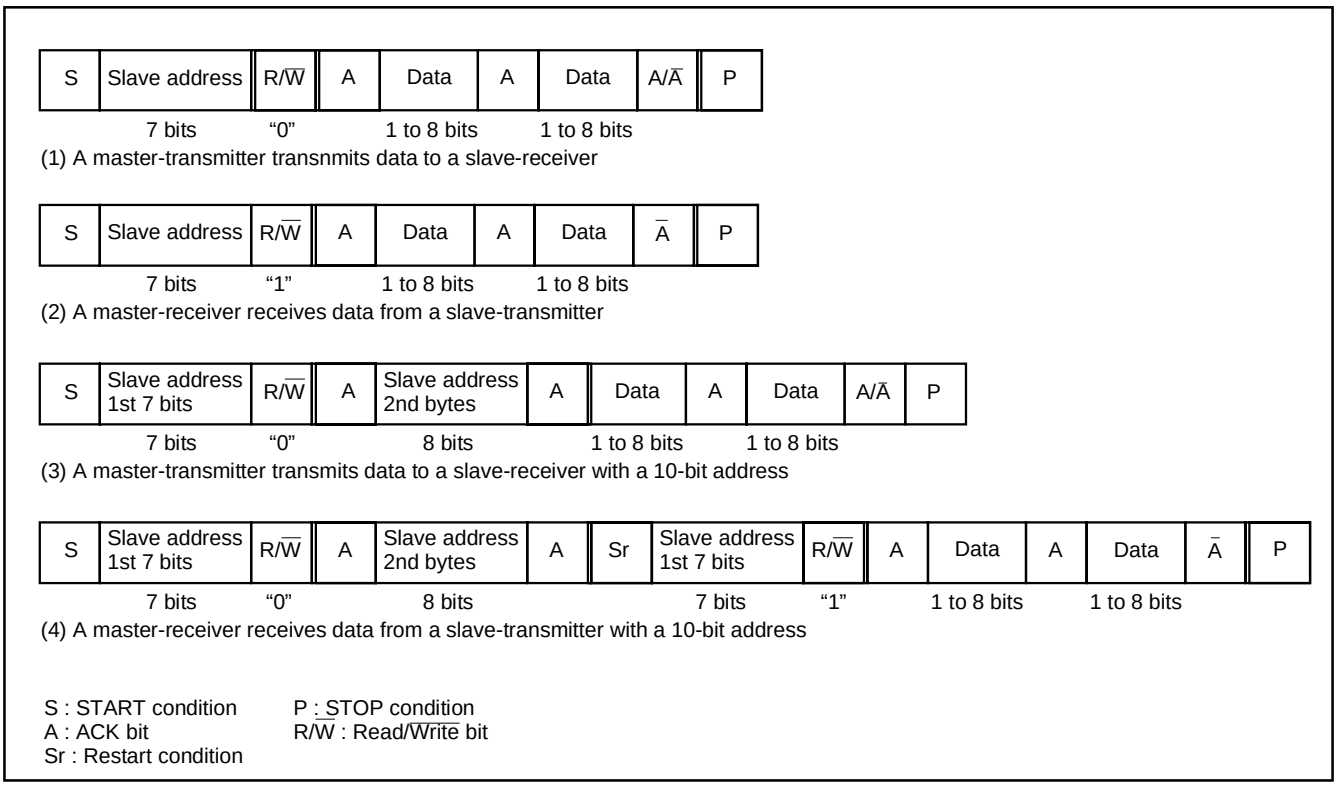


Fig. 42 Address data communication format

Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

(1) Set a slave address in the high-order 7 bits of the I^2C address register (S0D) and "0" into the RWB bit.
(2) Set the ACK return mode and SCL = 100 kHz by setting "85_{16}" in the I^2C clock control register (S2).
(3) Set "00_{16}" in the I^2C status register (S1) so that transmission/reception mode can become initializing condition.
(4) Set a communication enable status by setting "08_{16}" in the I^2C control register (S1D).
(5) Confirm the bus free condition by the BB flag of the I^2C status register (S1).
(6) Set the address data of the destination of transmission in the high-order 7 bits of the I^2C data shift register (S0) and set "0" in the least significant bit.
(7) Set "$F0_{16}$" in the I^2C status register (S1) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occur.
(8) Set transmit data in the I^2C data shift register (S0). At this time, an SCL and an ACK clock automatically occur.
(9) When transmitting control data of more than 1 byte, repeat step (8).
(10) Set "$D0_{16}$" in the I^2C status register (S1) to generate a STOP condition if ACK is not returned from slave reception side or transmission ends.

Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode and using the addressing format is shown below.

(1) Set a slave address in the high-order 7 bits of the I^2C address register (S0D) and "0" in the RWB bit.
(2) Set the no ACK clock mode and SCL = 400 kHz by setting "25_{16}" in the I^2C clock control register (S2).
(3) Set "00_{16}" in the I^2C status register (S1) so that transmission/reception mode can become initializing condition.
(4) Set a communication enable status by setting "08_{16}" in the I^2C control register (S1D).
(5) When a START condition is received, an address comparison is performed.
(6)•When all transmitted addresses are "0" (general call):
AD0 of the I^2C status register (S1) is set to "1" and an interrupt request signal occurs.
• When the transmitted address matches with the address set in (1):
ASS of the I^2C status register (S1) is set to "1" and an interrupt request signal occurs.
• In the cases other than the above AD0 and AAS of the I^2C status register (S1) are set to "0" and no interrupt request signal occurs.
(7) Set dummy data in the I^2C data shift register (S0).
(8) When receiving control data of more than 1 byte, repeat step (7).
(9) When a STOP condition is detected, the communication ends.

■Precautions when using multi-master I^2C-BUS interface

(1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I^2C-BUS interface are described below.

- I^2C data shift register (S0: address 0012_{16})
  When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.
- I^2C address register (S0D: address 0013_{16})
  When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because H/W changes the read/write bit (RWB) at the above timing.
- I^2C status register (S1: address 0014_{16})
  Do not execute the read-modify-write instruction for this register because all bits of this register are changed by H/W.
- I^2C control register (S1D: address 0015_{16})
  When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because H/W changes the bit counter (BC0-BC2) at the above timing.
- I^2C clock control register (S2: address 0016_{16})
  The read-modify-write instruction can be executed for this register.
- I^2C START/STOP condition control register (S2D: address 0017_{16})
  The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 5.

```
    ⋮
  LDA —                  (Taking out of slave address value)
  SEI                    (Interrupt disabled)
  BBS 5, S1, BUSBUSY     (BB flag confirming and branch pro
                          cess)
BUSFREE:
  STA S0                 (Writing of slave address value)
  LDM #$F0, S1           (Trigger of START condition generating)
  CLI                    (Interrupt enabled)
    ⋮
BUSBUSY:
  CLI                    (Interrupt enabled)
    ⋮
```

2. Use “Branch on Bit Set” of “BBS 5, $0014, –” for the BB flag confirming and branch process.
3. Use “STA $12, STX $12” or “STY $12” of the zero page addressing instruction for writing the slave address value to the I^2C data shift register.
4. Execute the branch instruction of above 2 and the store instruction of above 3 continuously shown the above procedure example.
5. Disable interrupts during the following three process steps:
   • BB flag confirming
   • Writing of slave address value
   • Trigger of START condition generating

   When the condition of the BB flag is bus busy, enable interrupts immediately.

(3) RESTART condition generating procedure

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 4.)
   Execute the following procedure when the PIN bit is “0”.

```
  LDM #$00, S1           (Select slave receive mode)
  LDA —                  (Taking out of slave address value)
  SEI                    (Interrupt disabled)
  STA S0                 (Writing of slave address value)
  LDM #$F0, S1           (Trigger of RESTART condition generating)
  CLI                    (Interrupt enabled)
```

2. Select the slave receive mode when the PIN bit is “0”. Do not write “1” to the PIN bit. Neither “0” nor “1” is specified for the writing to the BB bit.
   The TRX bit becomes “0” and the SDA pin is released.
3. The SCL pin is released by writing the slave address value to the I^2C data shift register.
4. Disable interrupts during the following two process steps:
   • Writing of slave address value
   • Trigger of RESTART condition generating

(4) Writing to I^2C status register

Do not execute an instruction to set the PIN bit to “1” from “0” and an instruction to set the MST and TRX bits to “0” from “1” simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to “0” from “1” simultaneously when the PIN bit is “1”. It is because it may become the same as above.

(5) Process of after STOP condition generating

Do not write data in the I^2C data shift register S0 and the I^2C status register S1 until the bus busy flag BB becomes “0” after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers do not have the problem.

(6) ES0 bit switch

In standard clock mode when SSC = “00010_2” or in high-speed clock mode, flag BB may switch to “1” if ES0 bit is set to “1” when SDA is “L”.

Countermeasure:

Set ES0 to “1” when SDA is “H”.

LPC INTERFACE

LPC interface function is base on Low Pin Count (LPC) Interface Specification, Revision 1.0. The 3885 supports only I/O read cycle and
I/O write cycle. There are two channels of bus buffers to the host.
The functions of Input Data Bus Buffer, Output Data Bus Buffer and Data Bus Buffer Status Register are the same as that of the 8042, 3880 group, 3881 group and 3886 group. It can be written in or read out from the host controller through LPC interface. LPC interface function block diagram is shown in Figure 43.
Functional input or output pins of LPC interface are shared with Port 8 ($P8_0$–$P8_6$). Setting the LPC interface enable bit (bit3 of LPCCON) to "1" enables LPC interface. Enabling channel i (i = 0, 1) of the data bus buffer is controlled by the data bus buffer i (i = 0, 1) enable bits (bit 4 or bit 5 of LPCCON).
The slave addresses of the data bus buffer channel i (i = 0, 1) are definable by setting LPCi (i = 0, 1) address register H/L (LPC0ADL, LPC0ADH, LPC1ADL, LPC1ADH). The bit 2 value of LPCi address register L is not decoded. This bit returns "0" when the internal CPU read. The bit 2 of slave address is latched to XA2i flag when the host controller writes the data.
The input buffer full (IBF) interrupt occurs when the host controller writes the data. The output buffer empty (OBE) interrupt is generated when the host controller reads out the data. The 3885 merges two input buffer full (IBF) interrupt requests and two output buffer empty (OBE) interrupt requests as shown in Figure 44.

Table 16 Function explanation of the control pin in LPC interface

Pin name	Input/ Output	Function
$P8_0$/LAD_0	I/O	These pins communicate address, control and data information between the host and the data bus buffer of the 3885.
$P8_1$/LAD_1	I/O	
$P8_2$/LAD_2	I/O	
$P8_3$/LAD_3	I/O	
$P8_4$/$\overline{LFRAME}$	I	Input the signal to indicate the start of new cycle and termination of abnormal communication cycles.
$P8_5$/$\overline{LRESET}$	I	Input the signal to reset the LPC interface function.
$P8_6$/LCLK	I	Input the LPC synchronous clock signal.

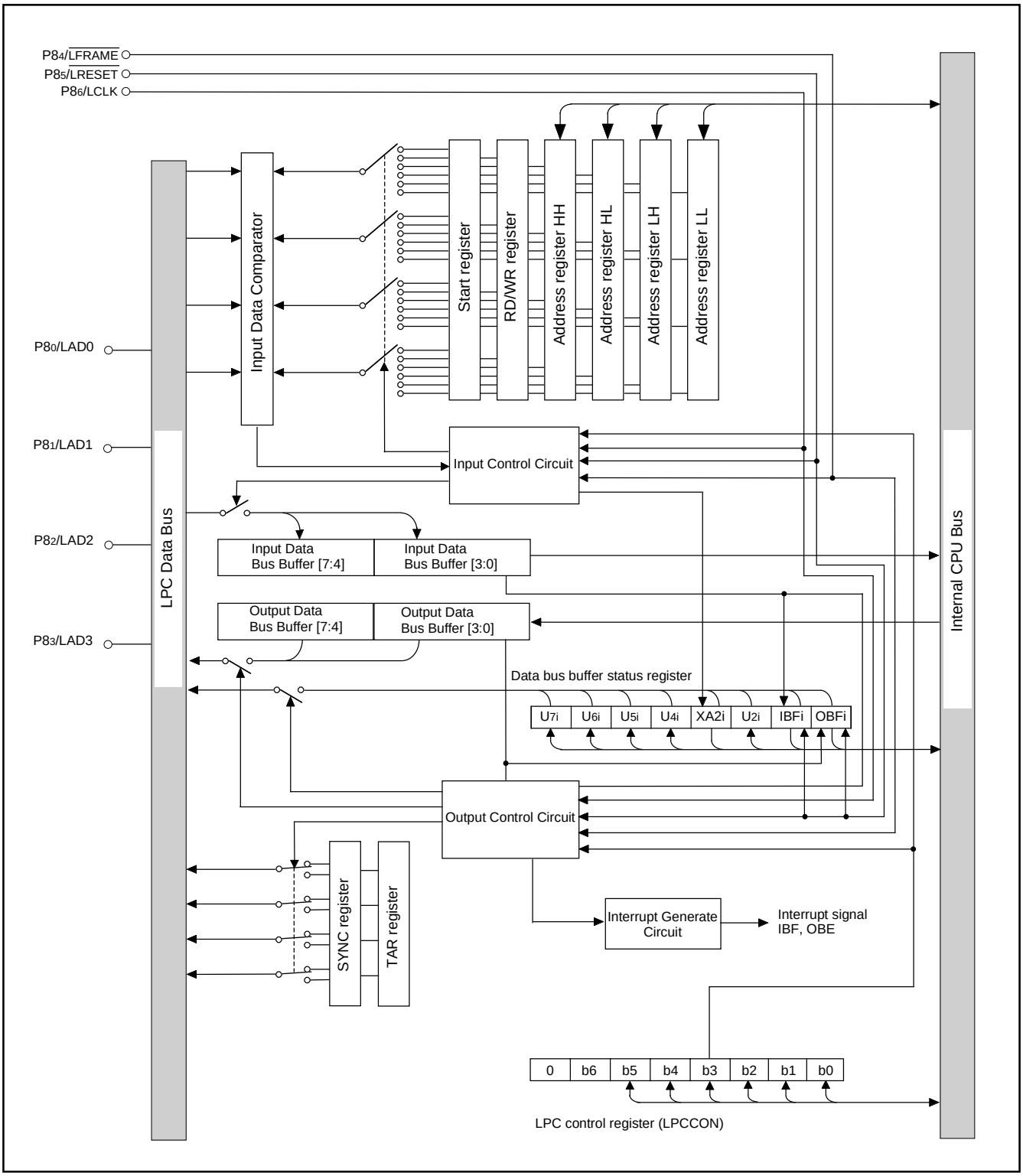


Fig. 43 Block diagram of LPC interface function (1ch)

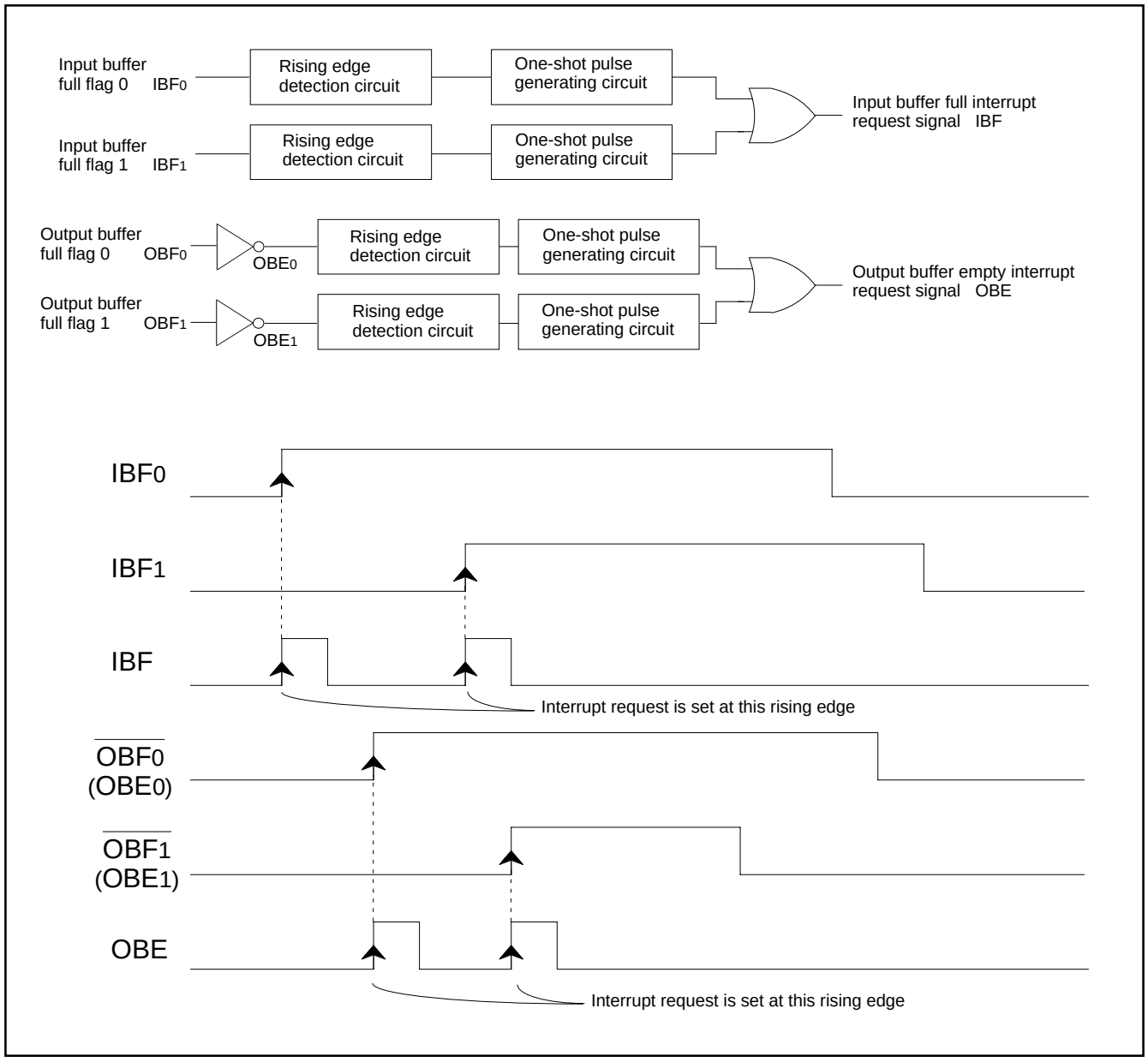


Fig. 44 Interrupt request circuit of data bus buffer

[LPC Control Register (LPCCON)] 002A16

• SYNC output select bit (SYNCSEL)
  "00": OK
  "01": LONG & OK
  "10": Err
  "11": LONG & Err
• LPC interface software reset bit (LPCSR)
  "0": Reset release (automatic)
  "1": Reset
• LPC interface enable bit (LPCBEN)
  "0": $P8_0$–$P8_6$ works as port
  "1": $P8_0$–$P8_6$ works as LPC interface
• Data bus buffer 0 enable bit (DBBEN0)
  "0": Data bus buffer 0 disable
  "1": Data bus buffer 0 enable
• Data bus buffer 1 enable bit (DBBEN1)
  "0": Data bus buffer 1 disable
  "1": Data bus buffer 1 enable

Bits 0 and 1 of the LPC control register (LPCCON) specify the SYNC code output.
Bit 2 of the LPC control register (LPCCON) enables the LPC interface to enter the reset state by software. When LPCSR is set to "1", LPC interface is initialized in the same manner as the external "L" input to $\overline{\text{LRESET}}$ pin (See Figure 50). Writing "0" to LPCSR the reset state will be released after 1.5 cycle of ϕ and this bit is cleared to "0".

[Data Bus Buffer Status Register i (i = 0, 1) (DBBSTS0, DBBSTS1)] 002916, 002C16

Bits 0, 1 and 3 are read-only bits and indicate the status of the data bus buffer. Bits 2, 4, 5, 6 and 7 are user definable flags which can be read and written by software. The data bus buffer status register can be read out by the host controller when bit 2 of the slave address (A2) is "1".

•Bit 0: Output buffer full flag i (OBFi)

This bit is set to "1" when a data is written into the output data bus buffer i and cleared to "0" when the host controller reads out the data from the output data bus buffer i.

•Bit 1: Input buffer full flag i (IBFi)

This bit is set to "1" when a data is written into the input data bus buffer i by the host controller, and cleared to "0" when the data is read out from the input data bus buffer i by the internal CPU.

•Bit 3: XA2 flag (XA2i)

The bit 2 of slave address is latched while a data is written into the input data bus buffer i.

[Input Data Bus Buffer i(i=0,1) (DBBIN0, DBBIN1)] 002816, 002B16

In I/O write cycle from the host controller, the data byte of the data phase is latched to DBBINi (i=0,1). The data of DBBINi can be read out form the data bus buffer registers (DBB0, DBB1) address in SFR area.

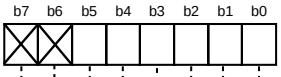
[Output Data Bus Buffer i (i = 0, 1) (DBBOUT0, DBBOUT1)] 002816, 002B16

Writing data to data bus buffer registers (DBB0 , DBB1) address from the internal CPU means writing to DBBOUTi (i = 0, 1). The data of DBBOUTi (i = 1, 0) is read out from the host controller when bit 2 of slave address (A2) is "0".

[LPCi address register H/L (LPC0ADL, LPC1ADL / LPC0ADH, LPC1ADH)] 0FF016 to 0FF316

The slave addresses of data bus buffer channel i(i=0,1) are definable by setting LPCi address registers H/L (LPC0ADL, LPC0ADH, LPC1ADL, LPC1ADH). These registers can be set and cleared any time. When the internal CPU reads LPCi address register L, the bit 2 (A2) is fixed to "0". The bit 2 of slave address (A2) is latched to XA2i flag when the host controller writes the data. The slave addresses, set in these registers, is used for comparing with the addresses from the host controller.

LPC control register



Symbol	Address	When reset
LPCCON	$002A_{16}$	00000000_2

Bit symbol	Bit name	Function	R	W
SYNCSEL	SYNC output select bit	00 : OK 01 : Long & OK 10 : Err 11 : Long & Err	○	○
LPCSR	LPC interface software reset bit	0 : Reset release(automatic) 1 : Reset	○	○
LPCEN	LPC interface enable bit	0 : $P8_0$ to $P8_6$ as port 1 : LPC interface enable	○	○
DBBEN0	Data bus buffer 0 enable bit	0 : Data bus buffer 0 disable 1 : Data bus buffer 0 enable	○	○
DBBEN1	Data bus buffer 1 enable bit	0 : Data bus buffer 1 disable 1 : Data bus buffer 1 enable	○	○
Cannot write to this bit. Returns “0” when read.			—	—

Fig. 45 LPC control register

Data bus buffer status register i (i = 0, 1)

Symbol	Address	When reset
DBBSTS0	0029_{16}	00000000_2
DBBSTS1	$002C_{16}$	00000000_2

Bit symbol	Bit name	Function	R	W
OBFi	Output buffer full flag	0 : Buffer empty 1 : Buffer full	○	×
IBFi	Input buffer full flag	0 : Buffer empty 1 : Buffer full	○	×
U2i	User definable flag	This flag can be freely defined by user.	○	○
XA2i	XA2i flag	This flag indicates the A2 status when IBFi flag is set.	○	×
U4i	User definable flag	This flag can be freely defined by user.	○	○
U5i			○	○
U6i			○	○
U7i			○	○

Fig. 46 Data bus buffer control register

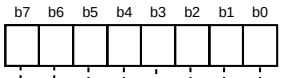
LPCi address register L (i=0,1) **(Note2)**

Symbol	Address	When reset
LPC0ADL	$0FF0_2$	00000000_2
LPC1ADL	$0FF2_2$	00000000_2

Bit symbol	Bit name	R	W
LPCSAD0	Slave address bit 0	○	○
LPCSAD1	Slave address bit 1	○	○
LPCSAD2	Slave address bit 2 **(Note 1)**	○	×
LPCSAD3	Slave address bit 3	○	○
LPCSAD4	Slave address bit 4	○	○
LPCSAD5	Slave address bit 5	○	○
LPCSAD6	Slave address bit 6	○	○
LPCSAD7	Slave address bit 7	○	○

Notes 1: Always returnes “0” when read , even if writing “1” to this bit.
2: Do not set the same 16-bit slave address to both channel 0 and channel 1.

LPCi address register H (i=0,1)



Symbol	Address	When reset
LPC0ADH	$0FF1_2$	00000000_2
LPC1ADH	$0FF3_2$	00000000_2

Bit symbol	Bit name	R	W
LPCSAD8	Slave address bit 8	○	○
LPCSAD9	Slave address bit 9	○	○
LPCSAD10	Slave address bit 10	○	○
LPCSAD11	Slave address bit 11	○	○
LPCSAD12	Slave address bit 12	○	○
LPCSAD13	Slave address bit 13	○	○
LPCSAD14	Slave address bit 14	○	○
LPCSAD15	Slave address bit 15	○	○

Fig. 47 LPC related registers

Basic Operation of LPC Interface

Set up steps for LPC interface is as below.

•Set the LPC interface enable bit (bit3 of LPCCON) to "1".

•Choose which data bus buffer channel use.

•Set the data bus buffer i enable bit (i = 0, 1) (bit 4 or 5 of LPCCON) to "1".

•Set the slave address to LPCi address register L and H (i = 0, 1) (LPC0ADL, LPC0ADH, LPC1ADL, LPC1ADH).

(1) Example of I/O write cycle

The I/O write cycle timing is shown in Figure 48. The standard transfer cycle number of I/O write cycle is 13. The communication starts from the falling edge of $\overline{\text{LFRAME}}$.

The data on LAD [3:0] is monitored at every rising edge of LCLK.

• 1st clock: The last clock when $\overline{\text{LFRAME}}$ is "Low". The host send "0000_2" on LAD [3:0] for communication start.

• 2nd clock: $\overline{\text{LFRAME}}$ is "High". The host send "$001X_2$" on LAD [3:0] to inform the cycle type as I/O write.

• From 3rd clock to 6th clock : In these four cycles , the host sends 16-bit slave address. The 3885 compares it with the LPCi address register H and L (i = 0, 1).
  - 3rd clock: The slave address bit [15:12].
  - 4th clock: The slave address bit [11:8].
  - 5th clock: The slave address bit [7:4].
  - 6th clock: The slave address bit [3:0].

• 7th clock and 8th clock are used for one data byte transfer. The data is written to the input data bus buffer (DBBINi, i = 0, 1)
  - 7th clock: The host sends the data bit [3:0].
  - 8th clock: The host sends the data bit [7:4].

• 9th clock and 10th clock are for turning the communication direction from the host→the peripheral to the slave→the host.
  - 9th clock: The host outputs "1111_2" on LAD [3:0].
  - 10th clock: The LAD [3:0] is set to tri-state by the host to turn the communication direction.

• 11th clock: The 3885 outputs "0000_2" (SYNC OK) to LAD [3:0] for acknowledgment.

• 12th clock: The 3885 outputs "1111_2" to LAD [3:0]. In this timing the address bit 2 is latched to XA2i (bit3 of DBBSTSi), IBFi (bit 1 of DBBSTSi) is set to "1" and IBF interrupt signal is generated.

• 13th clock: The LAD [3:0] is set to tri-state by the host to turn the communication direction.

(2) Example for I/O read cycle

The I/O read cycle timing is shown in Figure 49. The standard transfer cycle number of I/O read cycle is 13. The data on LAD [3:0] is monitored at every rising edge of LCLK. The communication starts from the falling edge of $\overline{\text{LFRAME}}$.

•1st clock: The last clock when $\overline{\text{LFRAME}}$ is "Low". The host sends "0000_2" on LAD [3:0] for communication start.

•2nd clock: $\overline{\text{LFRAME}}$ is "High". The host sends "$000X_2$" on LAD [3:0] to inform the cycle type as I/O read.

• From 3rd clock to 6th clock: In these four cycles , the host sends 16-bit slave address. The 3885 compares it with the LPCi address register H or L (i = 0, 1).
  - 3rd clock: The slave address bit [15:12].
  - 4th clock: The slave address bit [11:8].
  - 5th clock: The slave address bit [7:4].
  - 6th clock: The slave address bit [3:0].

• 7thclock and 8thclock are used for turning the communication direction from the host→the peripheral to the peripheral→the host.
  - 7th clock: The host outputs "1111_2" on LAD [3:0].
  - 8th clock: The LAD [3:0] is set to tri-state by the host to turn the communication direction.

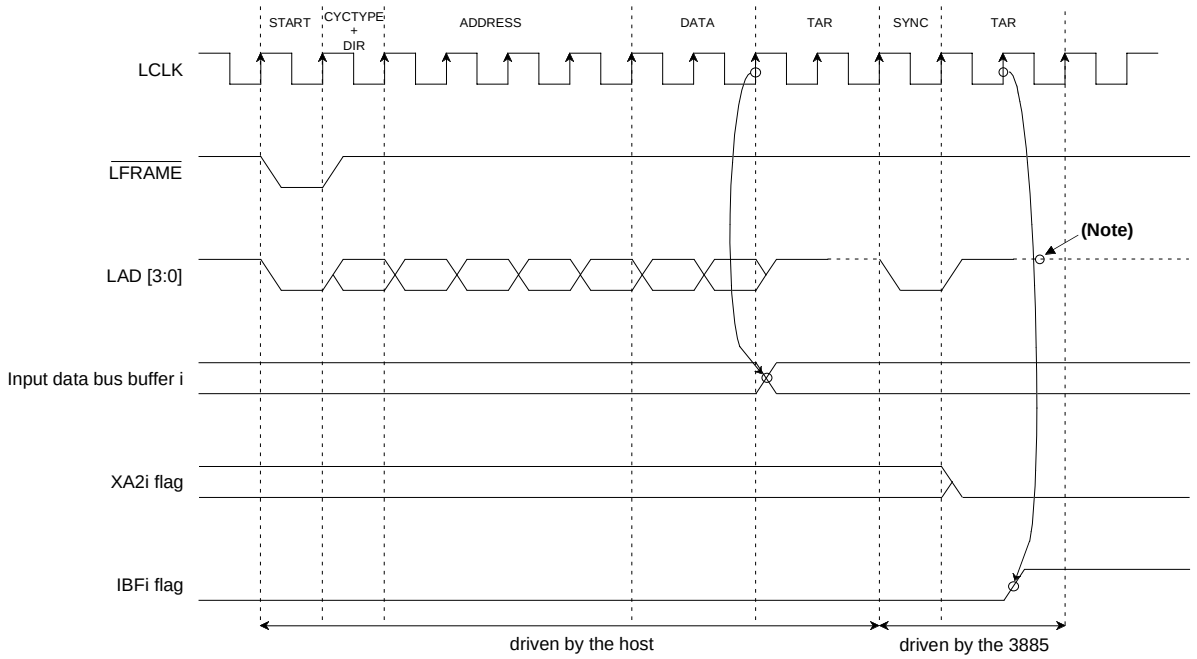
• 9th clock: The 3885 outputs "0000_2" (SYNC OK) to LAD [3:0] for acknowledgment.

• 10th clock and 11th clock are used for one data byte transfer from the output data bus buffer i (DBBOUTi) or data bus buffer status register i (DBBSTSi).
  - 10th clock: The 3885 sends the data bit [3:0].
  - 11th clock: The 3885 sends the data bit [7:4].

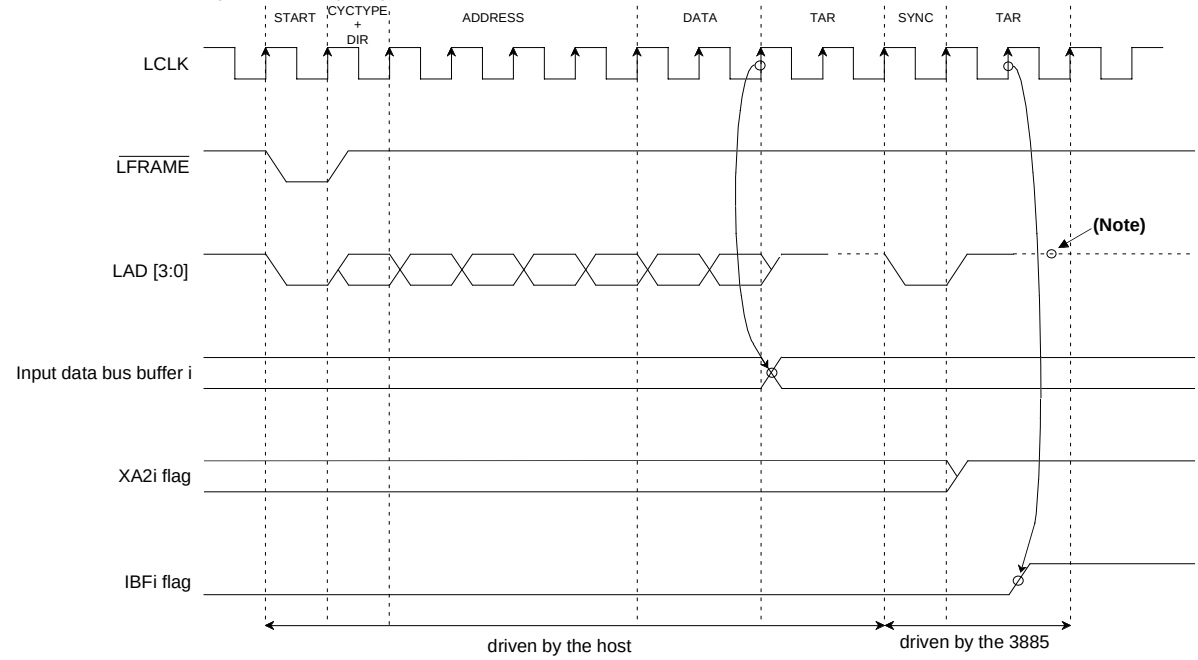
• 12th clock: The 3885 outputs "1111_2" to LAD [3:0]. In this timing OBFi (bit 2 of DBBSTSi) is cleared to "0" and OBE interrupt signal is generated.

• 13th clock: The LAD [3:0] is set to tri-state by the host to turn the communication direction.

● Data write (I/O write cycle)



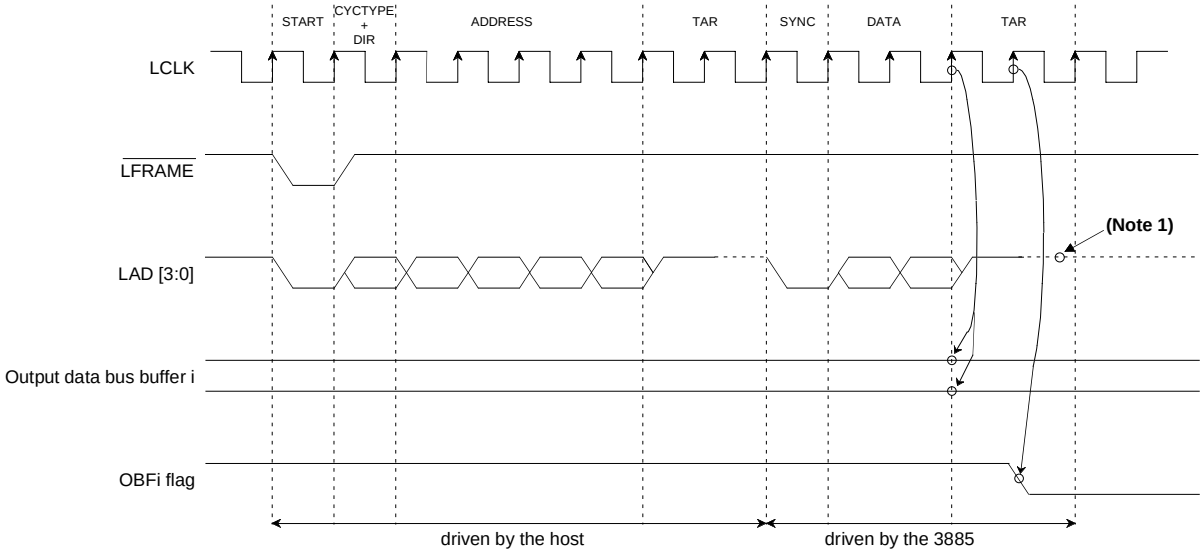
● Command write (I/O write cycle)



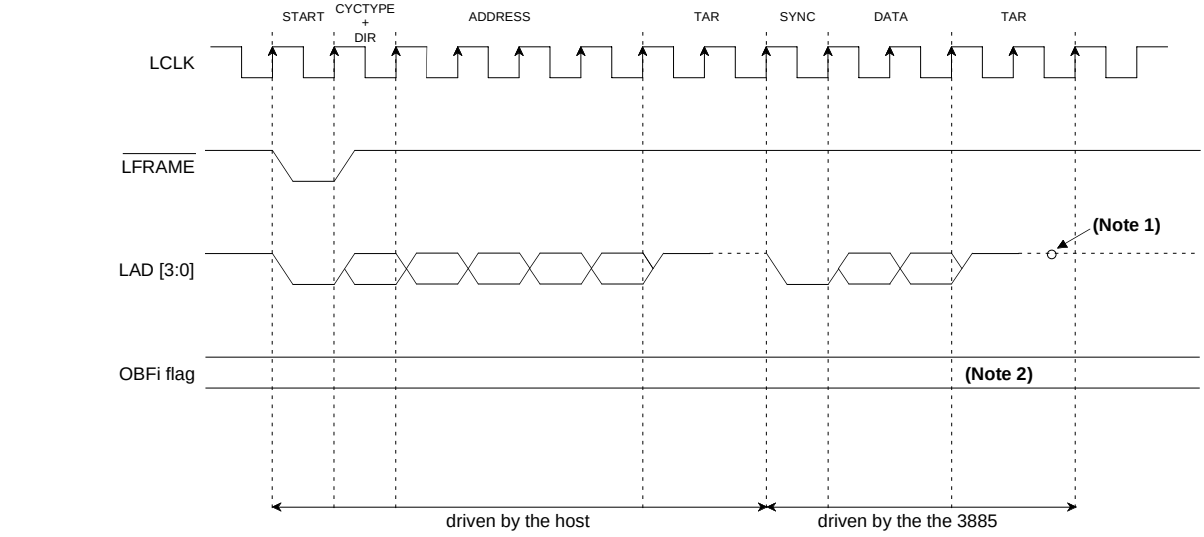
Note: LAD_0 to LAD_3 pins remain tri-state after transfer completion.

Fig. 48 Data and command write timing

● Data Read (I/O read cycle)



● Status Read (I/O read cycle)



Notes 1: LAD_0 to LAD_3 pins remain tri-state after transfer completion.
2: OBFi flag does not change.

Fig. 49 Data and status read timing

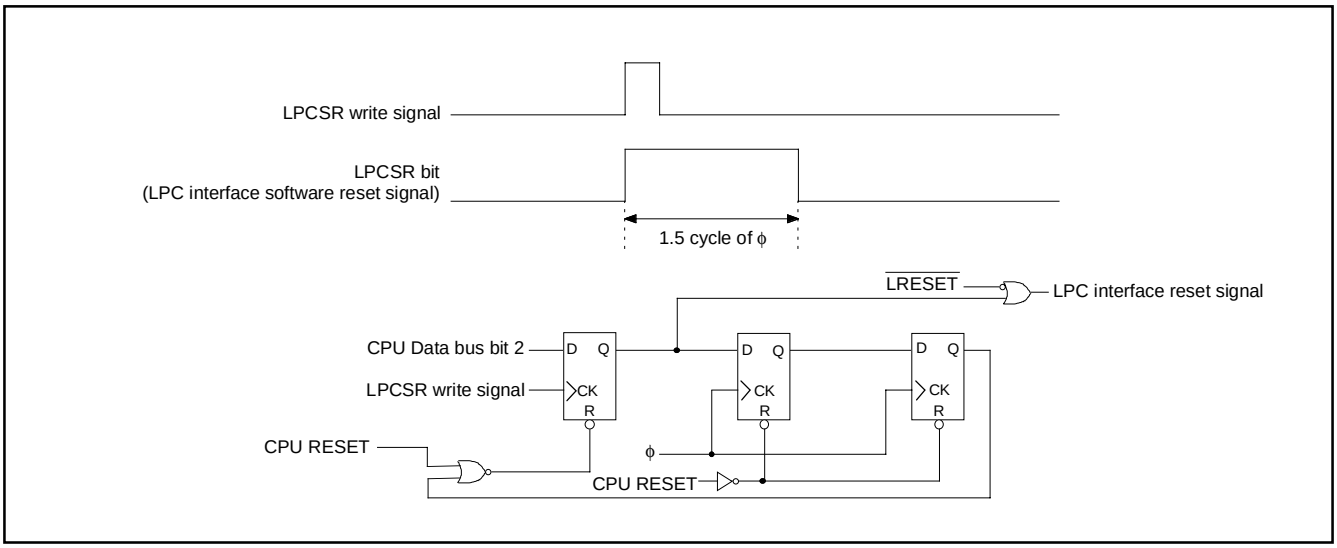


Fig. 50 Reset timing and block

Table 17 Reset conditions of LPC interface function

	Pin name / Internal register	LRESET = "L"	Note
Pin	P80/LAD0	Tri-state	
	P81/LAD1		
	P82/LAD2		
	P83/LAD3		
	P84/$\overline{\text{LFRAME}}$	Input	
	P85/$\overline{\text{LRESET}}$	LPC bus interface function	
	P86/LCLK	Input	
Internal register	Input data bus buffer registeri	Keep same value before $\overline{\text{LRESET}}$ goes "L".	
	Output data bus buffer registeri		
	Uxi flag 7, 6, 5, 4, 2		
	XA2i flag	Initialization to "0".	
	IBFi flag	Initialization to "0".	There is possibility to generate IBF interrupt request.
	OBFi flag	Initialization to "0".	There is possibility to generate OBE interrupt request.
	LPCi address register	Keep same value before $\overline{\text{LRESET}}$ goes "L".	
	LPCCON		

SERIALIZED INTERRUPT

The serialized IRQ circuit communicates the interrupt status to the host controller based on the Serialized IRQ Support for PCI System, Version 6.0.
Table 18 shows the summary of serialized interrupt of 3885.

Table 18 Smmary of serialized IRQ function

Item	Function
The factors of serialized IRQ	The numbers of serialized IRQ factor that can output simultaneously are 3. • Channel 0 (IRQ1,IRQ2) ① Setting Software IRQi (i = 1, 12) request bit (bits 0, 1 of SERIRQ) to “1”. ② The “1” of OBF0 and Hardware IRQi (i=1, 12) request bit (bits 3, 4 of SERCON) to “1”. • Channel 1 (IRQx ; user selectable) ① Setting the IRQx request bit (bit 7 of SERIRQ) to “1”. ② The “1” of OBF1 and Hardware IRQx request bit to “1”.
The number of frame	• Channel 0 (IRQ1, IRQ12) ① Setting Software IRQ1 request bit (bit 0 of SERIRQ) to “1” or detecting “1” of OBF0 with “1” of Hardware IRQ1 request bit (bit 4 of SERCON) selects IRQ1 Frame . ② Setting IRQ12 Software request bit (bit 1 of SERIRQ) to “1” or detecting “1” of OBF0 with “1” of Hardware IRQ1 request bit (bit 4 of SERCON) selects IRQ12 Frame. • Channel 1 (IRQx ; user selectable) Setting IRQx frame select bit (bit 2-6 of SERIRQ) selects IRQ 1–15 frame or extend frame 0–10.
Operation clock	Synchronized with LCLK (Max. 33 MHz).
Clock restart	LPC clock restart enable bit (bit 1 of SERCON) enables restart owing to “L” output of $\overline{\text{CLKRUN}}$ with the interrupt when the LPC clock has stopped or slowed down.
Clock stop inhibition	LPC clock stop inhibition bit (bit 2 of SERCON) enables the inhibition of clock stop control during the IRQSER cycle when the clock tends to stop or slow down.

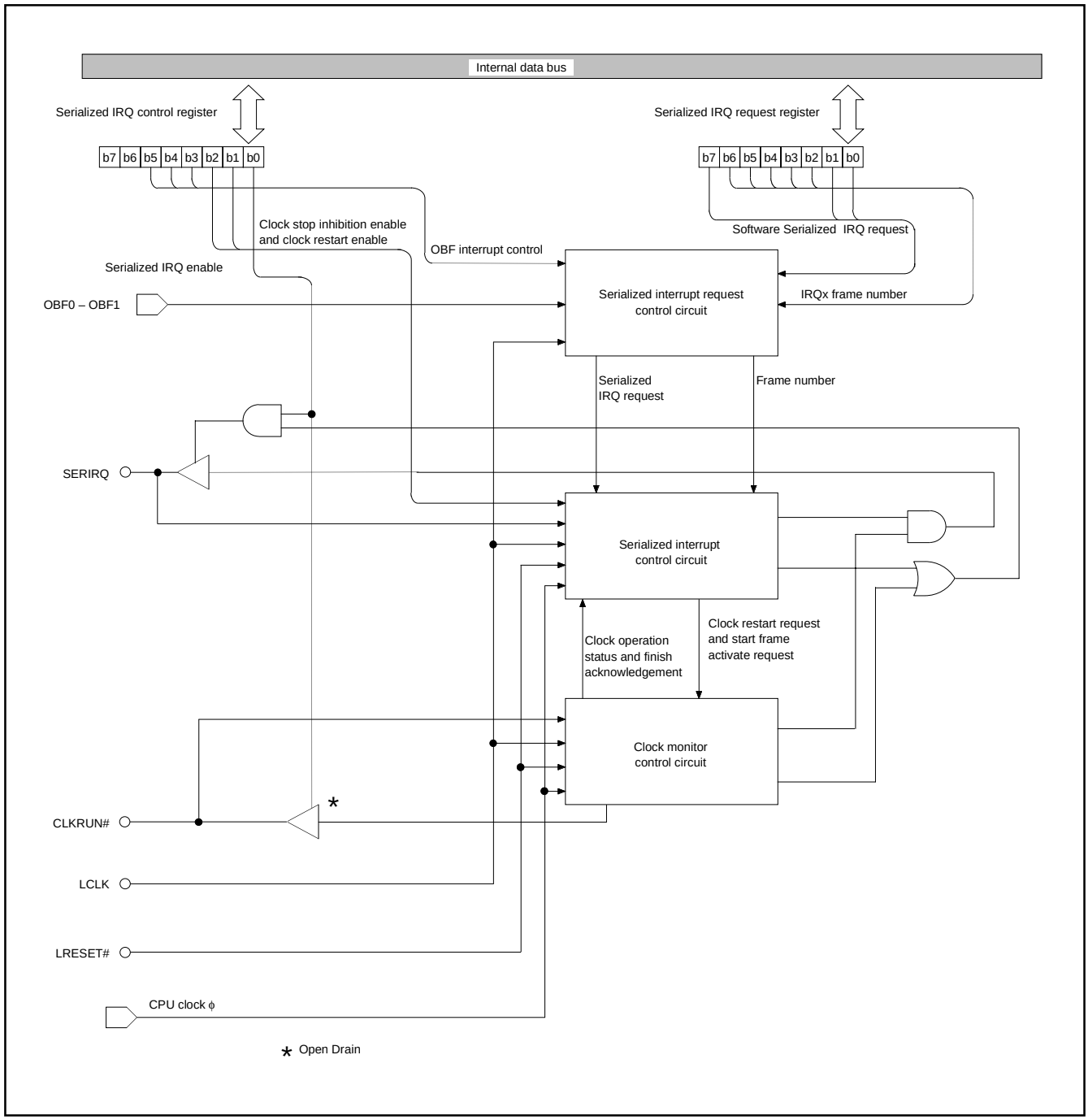


Fig. 51 Block diagram of serialized interrupt

Register Explanation

The serialized IRQ function is configured and controlled by the serialized IRQ request register (SERIRQ) and the serialized IRQ control register (SERCON).

[Serialized IRQ control register (SERCON)] 001D16

Bit 0 : Serialized IRQ enable bit (SIRQEN)
This bit enables/disables the serialized IRQ interface. When this bit is "1", use of serialized IRQ is enabled. Then P87 functions as IRQ/Data line (SERIRQ) and P47 functions as CLKRUN.
Output structure of CLKRUN pin becomes N-channel open drain.

Bit 1 : LPC clock restart enable bit (RUNEN)
Setting this bit to "1" enables clock restart with "L" output of CLKRUN.

Bit 2 : LPC clock stop inhibition bit (SUPEN)
Setting this bit to "1" makes CLKRUN output change to "L" for inhibiting the clock stop.

Bit 3 : Hardware IRQ1 request bit (SEIR1)
When this bit is "1", OBF_0 status is directly connected to the IRQ_1 frame.

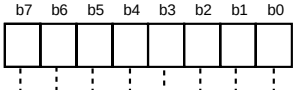
Bit 4 : Hardware IRQ12 request bit (SEIR12)
When this bit is "1", OBF_0 status is directly connected to IRQ12 frame.

Bit 5 : Hardware IRQx request bit (SEIRx)
When this bit is "1", OBF_1 status is directly connected to the IRQ_x frame.

Bit 6 : IRQ1/IRQ12 disable bit (SCH0EN)
This bit controls whether the serialized IRQ channel 0 transfers the IRQ1 and IRQ12 frame to the host or not.

Bit 7 : IRQx output polarity bit (SCH1POL)
This bit selects IRx frame output level.

Serialized IRQ control register



Symbol: SERCON | Address: $001D_{16}$ | When reset: 00000000_2

Bit symbol	Bit name	Function	R	W
SIRQEN	Serialized IRQ enable bit	0 : Serialized IRQ disable 1 : Serialized IRQ enable	○	○
RUNEN	LPC clock restart enable bit	0 : Clock restart disable 1 : Clock restart enable	○	○
SUPEN	LPC clock stop inhibition bit	0 : Stop inhibition control disable 1 : Stop inhibition control enable	○	○
SEIR1	Hardware IRQ1 request bit	0 : No IRQ1 request 1 : OBF_0 synchronized IRQ1 request	○	○
SEIR12	Hardware IRQ12 request bit	0 : No IRQ12 request 1 : OBF_0 synchronized IRQ12 request	○	○
SEIRx	Hardware IRQx request bit	0 : No IRQx request 1 : OBF_1 synchronized IRQx request	○	○
SCH0EN	IRQ1/IRQ12 disable bit	0 : IRQ1/IRQ12 output enable 1 : IRQ1/IRQ12 output disable	○	○
SCH1POL	IRQx output polarity bit	0 : -Request Hiz-Hiz-Hiz -No request L-H-Hiz 1 : -Request L-H-Hiz -No request Hiz-Hiz-Hiz	○	○

Fig. 52 Configuration of serialized IRQ control register

[Serialized IRQ request register (SERIRQ)] 001F16

The interrupt source is definable by this register.

Bit 0 : Software IRQ1 request bit (IR1)
SERIRQ line shows IR1 value at the sample phase of IRQ1 frame, when the SCH0EN is “1”.

Bit 1 : Software IRQ12 request bit (IR12)
SERIRQ line shows IR12 value at the sample phase of IRQ12 frame, when the SCH0EN is “1”.

Bits 2-6 : IRQx frame select bits (ISi, i = 0–4)
These bits select the active IRQ frame of serial IRQ channel 1. When these bit are “000002”, the serial IRQ channel 1 is disabled.

Bit 7 : Software IRQx request bit (IRx)
SERIRQ line shows IRx value at the sample phase of IRQx frame which is selected by bits 2 to 6 of SERIRQ. Output level is selectable by the IRQx output polarity bit (SCH1POL).

Serialized IRQ request register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol: SERIRQ
Address: 001F16
When reset: 000000002

Bit symbol	Bit name	Function	R	W
IR1	Software IRQ1 request bit	0: No IRQ1 request 1: IRQ1 request	○	○
IR12	Software IRQ12 request bit	0: No IRQ12 request 1: IRQ12 request	○	○
IS0	IRQx frame select bit	b6b5b4b3b2 0 0 0 0 0 : Disable serial IRQ channel 1 0 0 0 0 1 : IRQ1 Frame 0 0 0 1 0 : IRQ2 Frame 0 0 0 1 1 : IRQ3 Frame 0 0 1 0 0 : IRQ4 Frame 0 0 1 0 1 : IRQ5 Frame 0 0 1 1 0 : IRQ6 Frame 0 0 1 1 1 : IRQ7 Frame 0 1 0 0 0 : IRQ8 Frame 0 1 0 0 1 : IRQ9 Frame 0 1 0 1 0 : IRQ10 Frame 0 1 0 1 1 : IRQ11 Frame 0 1 1 0 0 : IRQ12 Frame 0 1 1 0 1 : IRQ13 Frame 0 1 1 1 0 : IRQ14 Frame 0 1 1 1 1 : IRQ15 Frame 1 0 0 0 0 : Do not select 1 0 0 0 1 : Do not select 1 0 0 1 0 : Do not select 1 0 0 1 1 : Do not select 1 0 1 0 0 : Do not select 1 0 1 0 1 : Extend Frame 0 1 0 1 1 0 : Extend Frame 1 1 0 1 1 1 : Extend Frame 2 1 1 0 0 0 : Extend Frame 3 1 1 0 0 1 : Extend Frame 4 1 1 0 1 0 : Extend Frame 5 1 1 0 1 1 : Extend Frame 6 1 1 1 0 0 : Extend Frame 7 1 1 1 0 1 : Extend Frame 8 1 1 1 1 0 : Extend Frame 9 1 1 1 1 1 : Extend Frame 10	○	○
IS1				
IS2				
IS3				
IS4				
IRx	Software IRQx request bit	0: No IRQx request 1: IRQx request	○	○

Fig. 53 Structure of serialized IRQ request register

Operation of Serialized IRQ

A cycle operation of serialized IRQ starts with Start Frame and finishes with Stop Frame. There are two modes of operation : Continuous (Idle) mode and Quiet (Active) mode. The next operation mode is determined by monitoring the stop frame pulse width.

●Timing of serialized IRQ cycle

Figure 54 shows the timing diagram of serialized IRQ cycle.

(1) Start Frame

The Start Frame is detected when the SERIRQ line remains “L” in 4 to 8 clocks.

(2) IRQ/Data Frame

Each IRQ/Data Frame is three clocks. When the IRQi (i = 0, 1, x) request is “0”, then the SERIRQ line is driven to “L” during the Sample phase (1st clock) of the corresponding IRQ/Data frame, to “H” during the Recovery phase (2nd clock), to tri-state during the Turn-around phase (3rd clock). When the IRQi request is “1”, then the SERIRQ line is tri-state in all phases (3 clocks period).

(3) Stop Frame

The Stop Frame is detected when the SERIRQ line remains “L” in 2 or 3 clocks. The next operation mode is Quiet mode when the pulse width of “L” is 2 clocks. The next operation mode is the Continuous mode when the pulse width is 3 clocks.

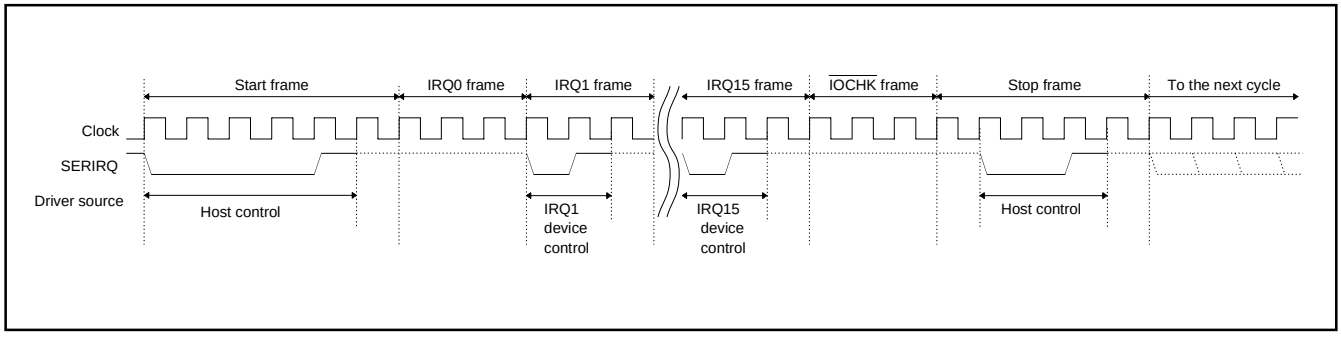


Fig. 54 Timing diagram of serialized IRQ cycle

Operation Mode

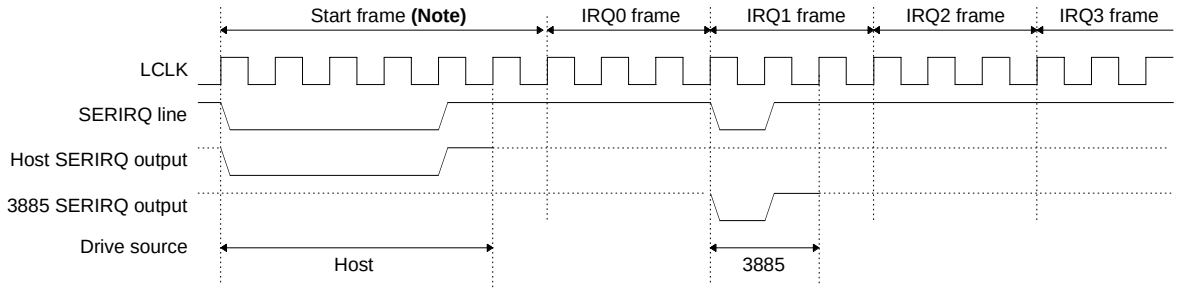
Figure 55 shows the timing of continuous mode; Figure 56 shows that of Quiet mode.

(1) Continuous mode

Serialized IRQ cycles starts in Continuous mode after CPU reset in the case of $\overline{\text{LRESET}}$ = "L" and the previous stop frame being 3 clocks.

After receiving the start frame; the IRQ1 Frame, IRQ12 Frame or IRQx frame is asserted.

Note : If the pulse width of "L" is less than 4 clocks, or 9 clocks or more; the start frame is not detected and the next start (the falling edge of SERIRQ) is waited.



Note: The start frame count is 4 clocks as exemple.

Fig. 55 Timing diagram of Continuous mode

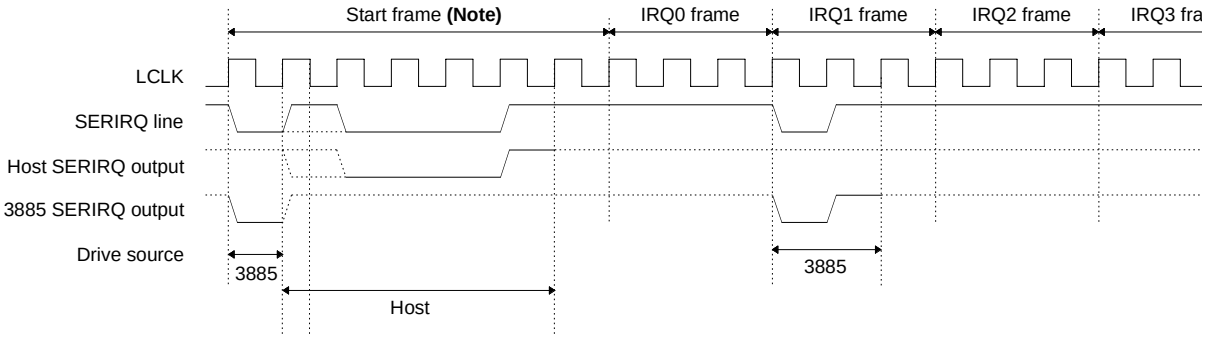
(2) Quiet mode

At clock stop, clock slow down or the pulse width of the last stop frame being 2 clocks, it is the Quiet mode.

In this mode the 3885 drives the SERIRQ line to "L" in the 1st clock. After that the host drives the rest start frame (Note). The IRQ1 frame, IRQ12 frame or IRQx frame is asserted.

Note: When the sum of pulse width of "L" driven by the 3885 in the 1st clock and driven by the host in the rest clocks is within 4 to 8-clock cycles, the start frame is detected.

If the sum of pulse width of "L" is less than 4 clocks, or 9 clocks or more; the start frame is not detected and the next start (the falling edge of SERIRQ) is waited.



Note: The start frame count is 4 clocks as exemple

Fig. 56 Timing diagram of Quiet mode

Clock Restart/Stop Inhibition Request

Asserting the CLKRUN signal can request the host to restart for clocks stopped or slowed down, or maintain the clock tending to stop or slow down.

Figure 57 shows the timing diagram of clock restart request; Figure 58 shows an example of timing of clock stop inhibition request.

(1) Clock restart operation

In case the LPC clock restart enable bit (bit 1 of SERCON) is “1” and the CLKRUN (BUS) is “H”, when the serialized interrupt request occurs, the 3885 drives CLKRUN to “L” for requesting the PCI clock generator to restart the LCLK if the clock is slowed down or stopped.

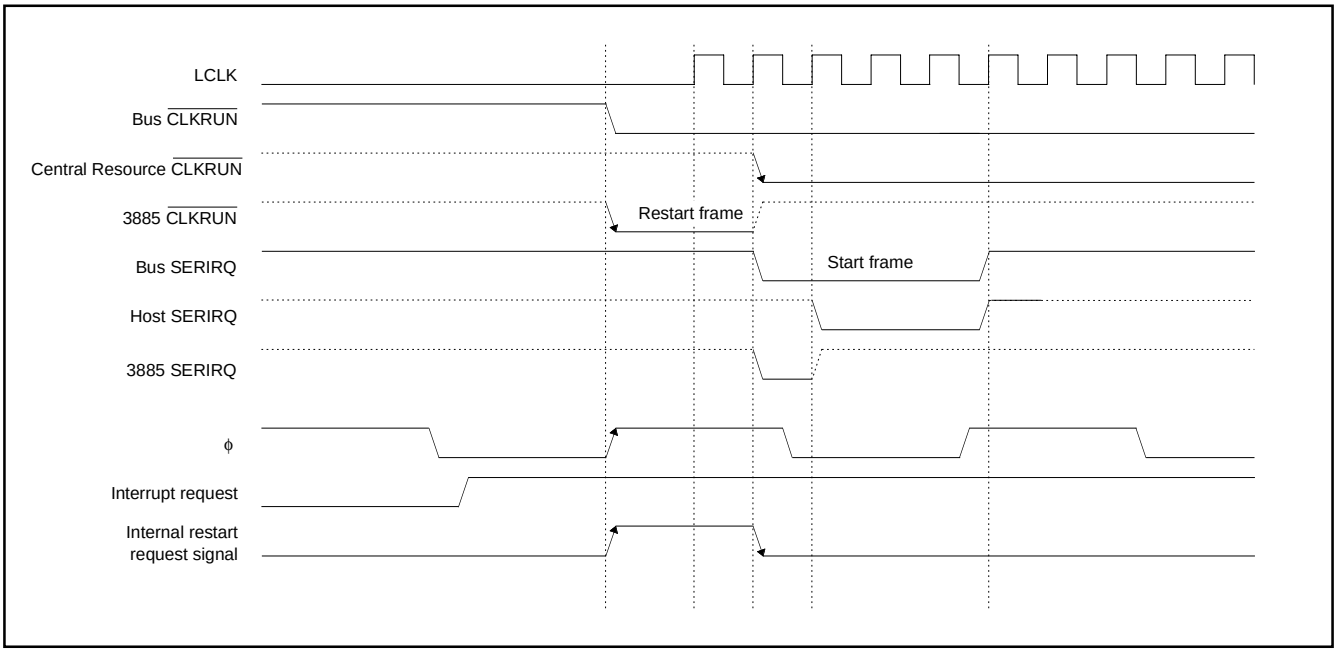


Fig. 57 Timing diagram of clock restart request

(2) Clock stop inhibition request

In case the LPC clock stop inhibition bit (bit 2 of SERCON) is “1” and the serialized interrupt request is held, if the LCLK tends to stop, the 3885 drives CLKRUN to “L” for requesting the PCI clock generator not to stop LCLK.

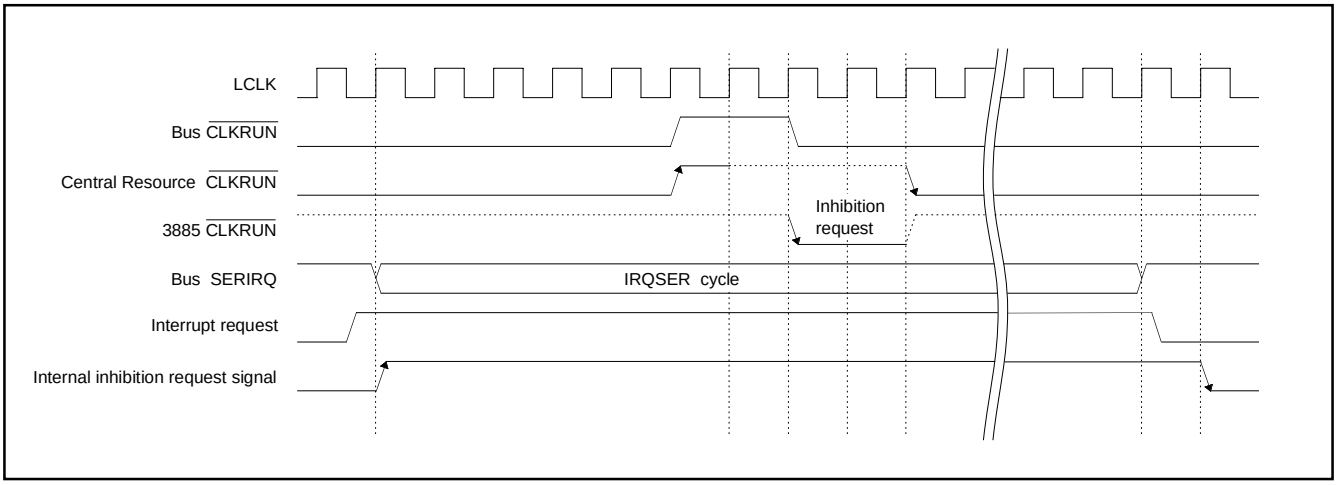


Fig. 58 Timing diagram of clock stop inhibition request

A-D CONVERTER
[A-D Conversion Register 1,2 (AD1, AD2)] 003516, 003816

The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

Bit 7 of the A-D conversion register 2 is the conversion mode selection bit. When this bit is set to "0," the A-D converter becomes the 10-bit A-D mode. When this bit is set to "1," that becomes the 8-bit A-D mode. The conversion result of the 8-bit A-D mode is stored in the A-D conversion register 1. As for 10-bit A-D mode, 10-bit reading or 8-bit reading can be performed by selecting the reading procedure of the A-D conversion register 1, 2 after A-D conversion is completed (in Figure 60).

The A-D conversion register 1 performs the 8-bit reading inclined to MSB after reset, the A-D conversion is started, or reading of the A-D converter register 1 is generated; and the register becomes the 8-bit reading inclined to LSB after the A-D converter register 2 is generated.

[AD/DA Control Register (ADCON)] 003416

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} into 1024, and outputs the divided voltages in the 10-bit A-D mode (256 division in 8-bit A-D mode).

The A-D converter successively compares the comparison voltage V_{ref} in each mode, dividing the V_{REF} (see below), with the input voltage.

- 10-bit A-D mode (10-bit reading)

$$V_{ref} = \frac{V_{REF}}{1024} \times n \quad (n = 0–1023)$$

- 10-bit A-D mode (8-bit reading)

$$V_{ref} = \frac{V_{REF}}{256} \times n \quad (n = 0–255)$$

- 8-bit A-D mode

$$V_{ref} = \frac{V_{REF}}{256} \times (n–0.5) \quad (n = 1–255)$$
$$= 0 \quad (n = 0)$$

Channel Selector

The channel selector selects one of ports $P6_0/AN_0$ to $P6_7/AN_7$, and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the A-D conversion registers 1, 2. When an A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set $f(X_{IN})$ to 500 kHz or more during an A-D conversion.

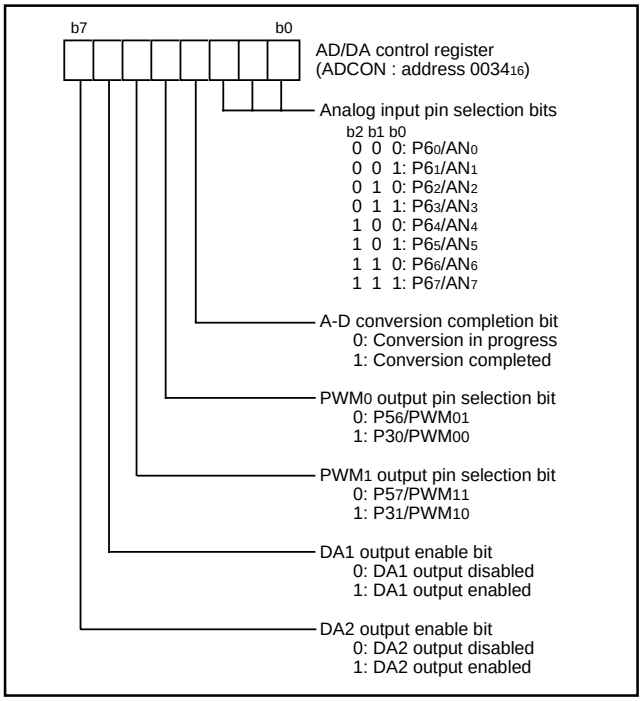


Fig. 59 Structure of AD/DA control register

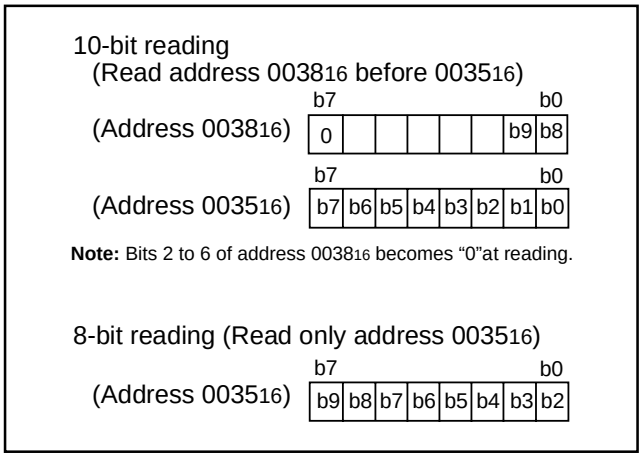


Fig. 60 Structure of 10-bit A-D mode reading

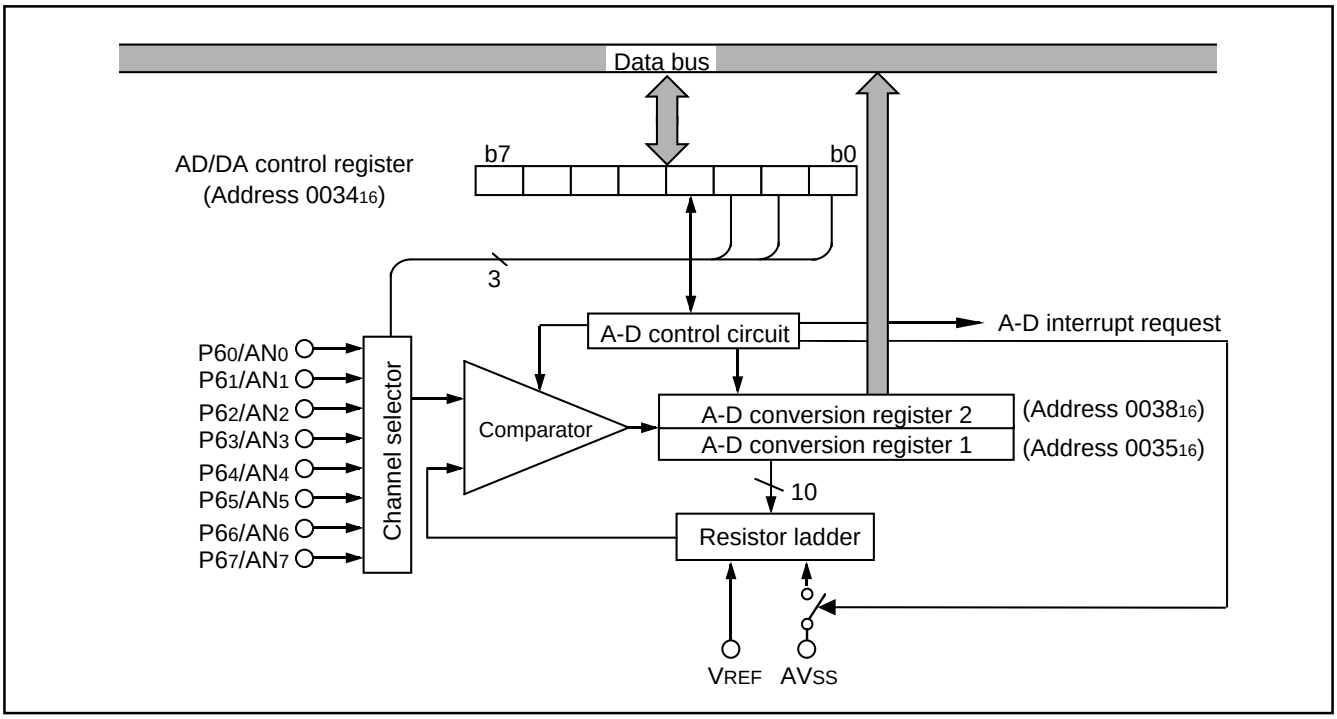


Fig. 61 Block diagram of A-D converter

D-A CONVERTER

The 3885 group has two internal D-A converters (DA_1 and DA_2) with 8-bit resolution.

The D-A converter is performed by setting the value in each D-A conversion register. The result of D-A conversion is output from the DA_1 or DA_2 pin by setting the DA output enable bit to "1".

When using the D-A converter, the corresponding port direction register bit ($P5_6$ for DA_1 or $P5_7$ for DA_2) must be set to "0" (input status).

The output analog voltage V is determined by the value n (decimal notation) in the D-A conversion register as follows:

$V = V_{REF} \times n/256$ (n = 0 to 255)

Where V_{REF} is the reference voltage.

At reset, the D-A conversion registers are cleared to "00_{16}", the DA output enable bits are cleared to "0", and the $P5_6/DA_1/PWM_{01}$ and $P5_7/DA_2/PWM_{11}$ pins become high impedance.

The DA output does not have buffers. Accordingly, connect an external buffer when driving a low-impedance load.

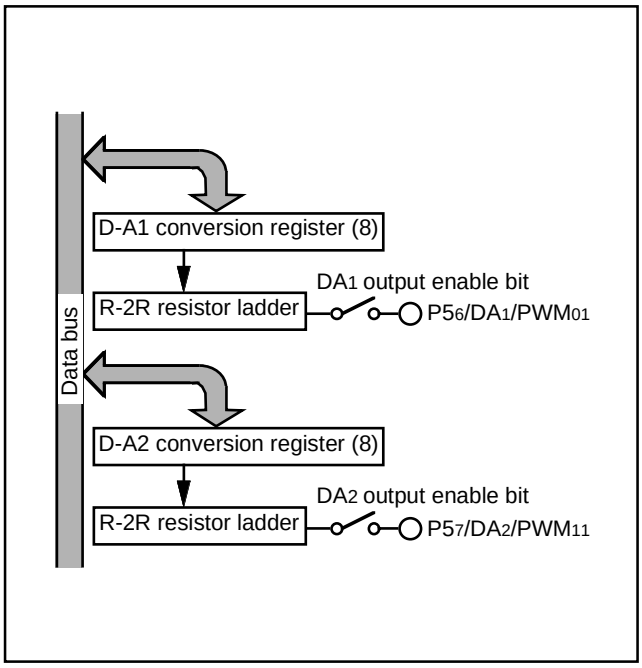


Fig. 62 Block diagram of D-A converter

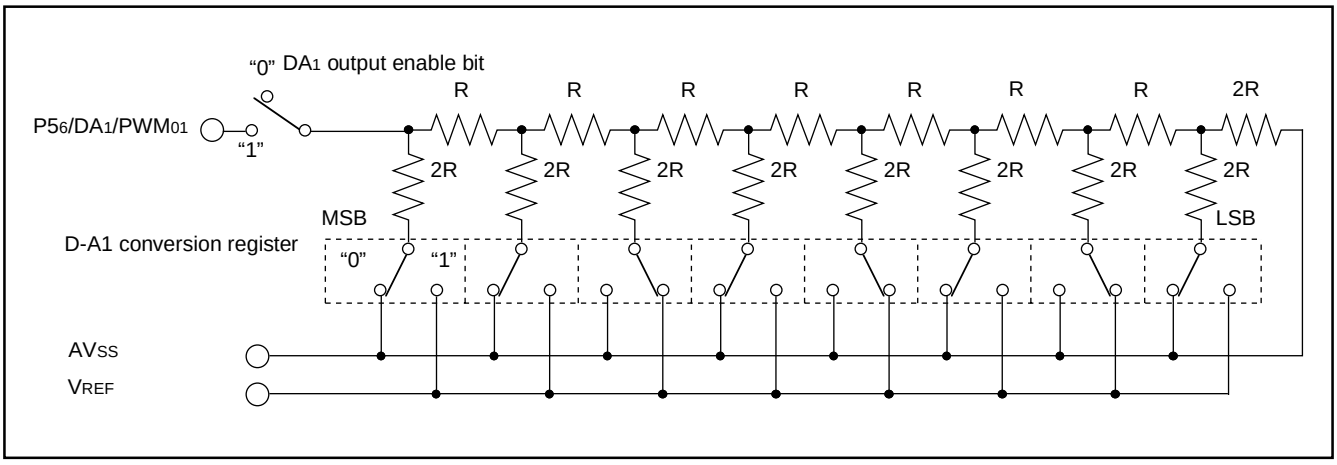


Fig. 63 Equivalent connection circuit of D-A converter (DA1)

COMPARATOR CIRCUIT

Comparator Configuration

The comparator circuit consists of the ladder resistors, the analog comparators, a comparator control circuit, the comparator reference input selection bit (bit 7 of PCTL2), a comparator data register (CMPD), the comparator reference power source input pin ($P2_0$/CMP_{REF}) and analog input pins ($P3_0$–$P3_7$). The analog input pin ($P3_0$–$P3_7$) also functions as an ordinary digital port.

Comparator Operation

To activate the comparator circuit, first set port P3 to input mode by setting the corresponding direction register (P3D) to "0" to use port P3 as an analog voltage input pin. The internal fixed analog voltage (V_{CC} × 29/32) can be generated by setting "1" to the comparator reference input selection bit (bit 7 of PCTL2). The internal fixed analog voltage becomes about 2.99 V at V_{CC} = 3.3 V. When setting "0" to the comparator reference input selection bit, the $P2_0$/CMP_{REF} pin becomes the comparator reference power source input pin and it is possible to input the comparator reference power source optionally from the external. The voltage comparison is immediately performed by the writing operation to the comparator data register (CMPD). After 14 cycles of the internal system clock ϕ (the time required for the comparison), the comparison result is stored in the comparator data register (CMPD).

If the analog input voltage is greater than the internal reference voltage, each bit of this register is "1"; if it is less than the internal reference voltage, each bit of this register is "0". To perform another comparison, the voltage comparison must be performed again by writing to the comparator data register (CMPD).

Read the result when 14 cycles of ϕ or more have passed after the comparator operation starts. The ladder resistor is turned on during 14 cycles of ϕ , which is required for the comparison, and the reference voltage is generated. An unnecessary current is not consumed because the ladder resistor is turned off while the comparator operation is not performed. Since the comparator consists of capacitor coupling, the electric charge may lost if the clock frequency is low.

Keep the clock frequency more than 1 MHz during the comparator operation. Do not execute the STP, WIT, or port P3 I/O instruction.

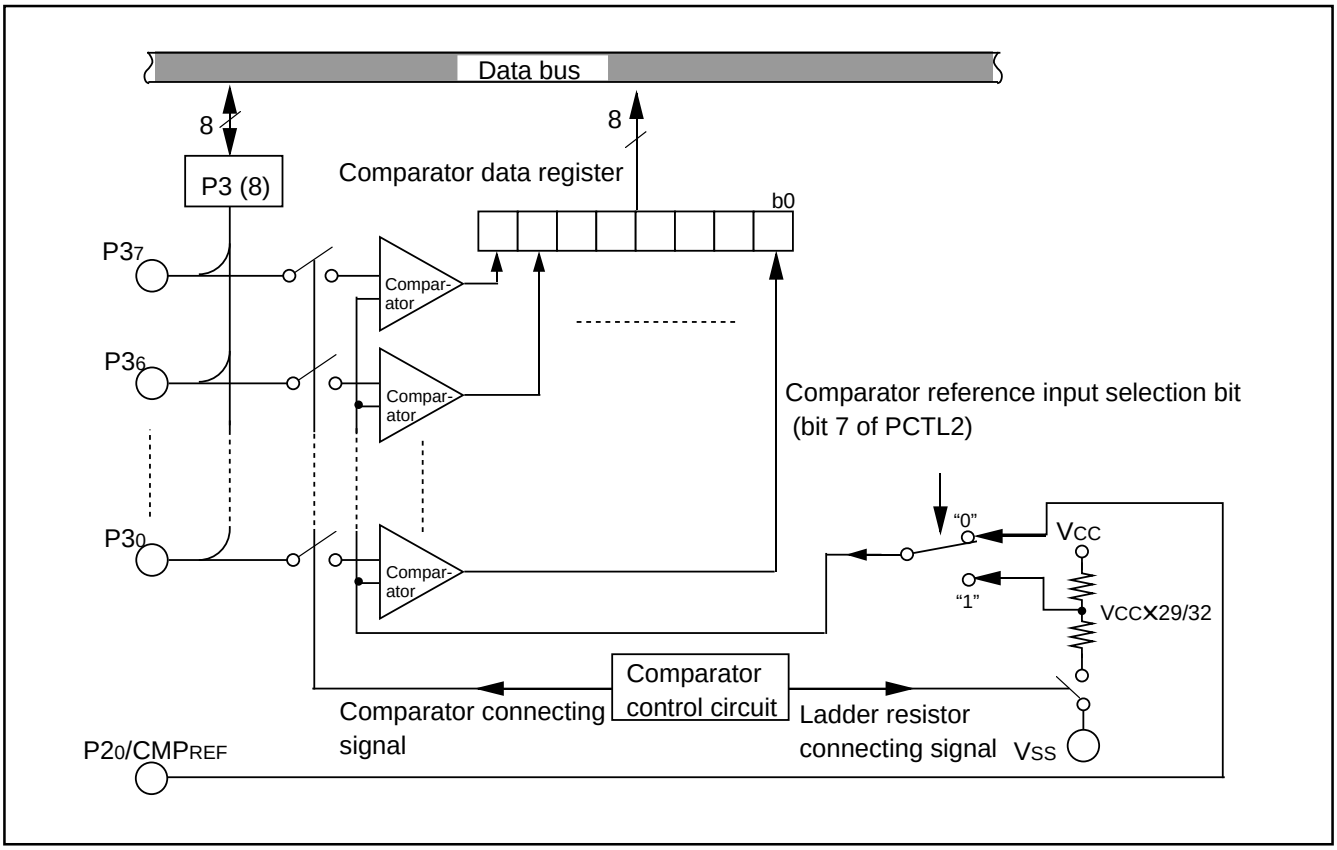


Fig. 64 Comparator circuit

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 16 X_{IN} cycle or more. (When the power source voltage should be between 3.3V ± 0.3V and the oscillation should be stable.) Then the $\overline{\text{RESET}}$ pin set to “H”, the reset state is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.6 V for V_{CC} of 3.0 V.

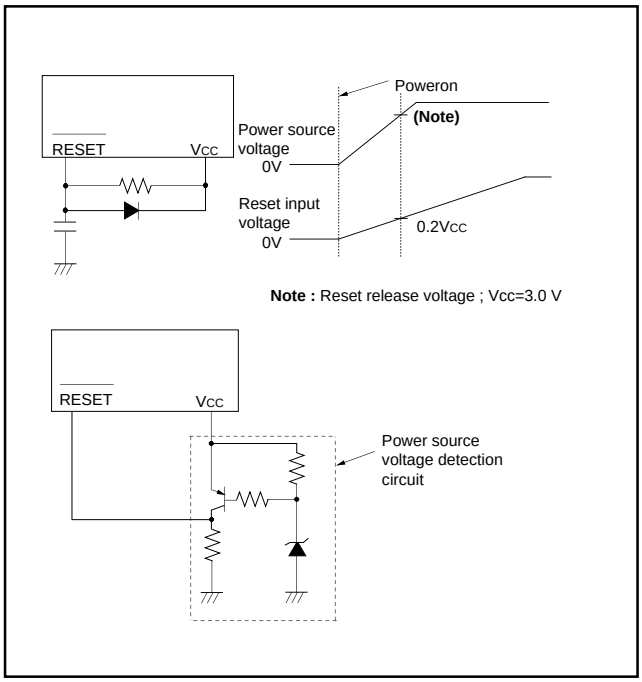


Fig. 65 Reset circuit example

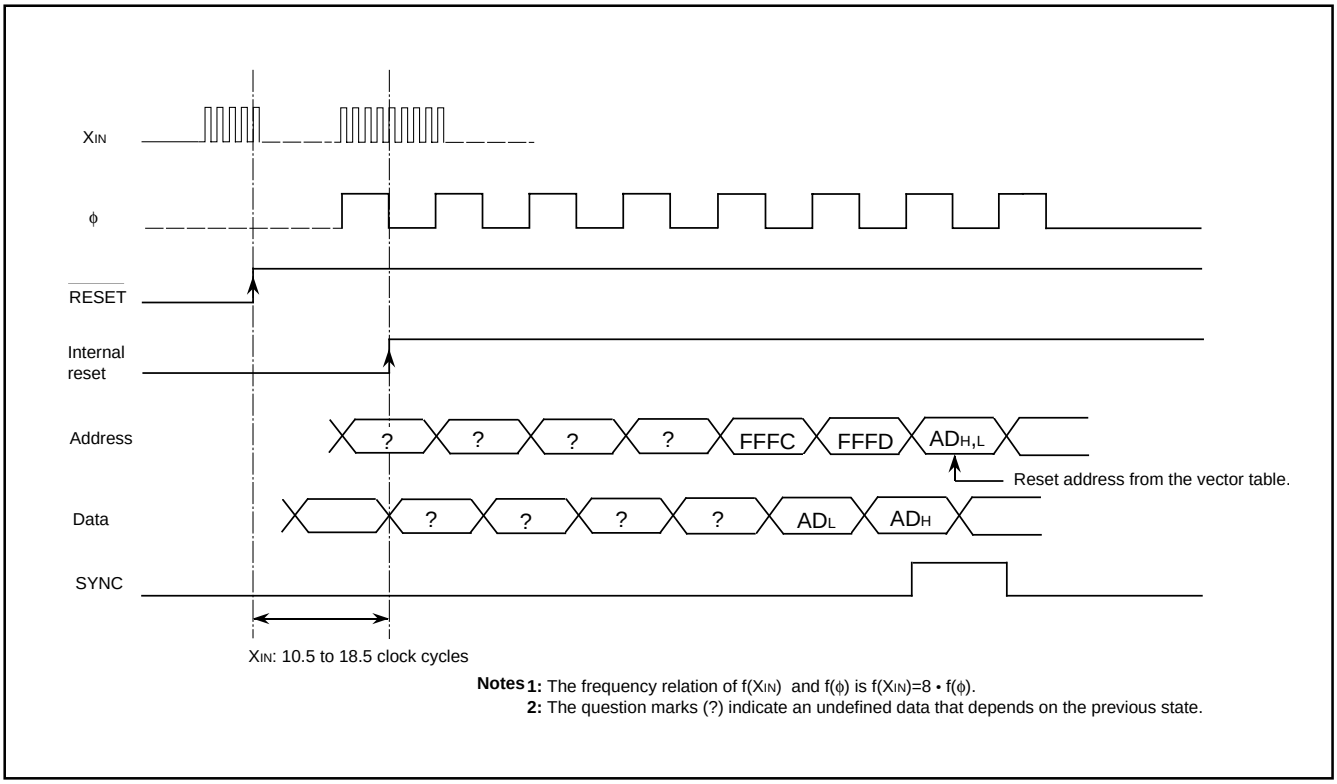


Fig. 66 Reset sequence

		Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Port P5 (P5)	$000A_{16}$	00_{16}
(12)	Port P5 direction register (P5D)	$000B_{16}$	00_{16}
(13)	Port P6 (P6)	$000C_{16}$	00_{16}
(14)	Port P6 direction register (P6D)	$000D_{16}$	00_{16}
(15)	Port P7 (P7)	$000E_{16}$	00_{16}
(16)	Port P7 direction register (P7D)	$000F_{16}$	00_{16}
(17)	Port P8 (P8)	0010_{16}	00_{16}
(18)	Port P8 direction register (P8D)	0011_{16}	00_{16}
(19)	I^2C data shift register (S0)	0012_{16}	X X X X X X X X
(20)	I^2C address register (S0D)	0013_{16}	00_{16}
(21)	I^2C status register (S1)	0014_{16}	0 0 0 1 0 0 0 X
(22)	I^2C control register (S1D)	0015_{16}	00_{16}
(23)	I^2C clock control register (S2)	0016_{16}	00_{16}
(24)	I^2C start/stop condition control register (S2D)	0017_{16}	0 0 0 1 1 0 1 0
(25)	Transmit/Receive buffer register (TB/RB)	0018_{16}	X X X X X X X X
(26)	Serial I/O status register (SIOSTS)	0019_{16}	1 0 0 0 0 0 0 0
(27)	Serial I/O control register (SIOCON)	$001A_{16}$	00_{16}
(28)	UART control register (UARTCON)	$001B_{16}$	1 1 1 0 0 0 0 0
(29)	Baud rate generator (BRG)	$001C_{16}$	X X X X X X X X
(30)	Serialized IRQ control register (SERCON)	$001D_{16}$	00_{16}
(31)	Watchdog timer control register (WDTCON)	$001E_{16}$	0 0 1 1 1 1 1 1
(32)	Serialized IRQ request register (SERIRQ)	$001F_{16}$	X X X X X X X X
(33)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(34)	Timer 1 (T1)	0021_{16}	01_{16}
(35)	Timer 2 (T2)	0022_{16}	FF_{16}
(36)	Timer XY mode register (TM)	0023_{16}	00_{16}
(37)	Prescaler X (PREX)	0024_{16}	FF_{16}
(38)	Timer X (TX)	0025_{16}	FF_{16}
(39)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(40)	Timer Y (TY)	0027_{16}	FF_{16}
(41)	Data bus buffer register 0 (DBB0)	0028_{16}	X X X X X X X X
(42)	Data bus buffer status register 0 (DBBSTS0)	0029_{16}	00_{16}
(43)	LPC control register (LPCCON)	$002A_{16}$	00_{16}
(44)	Data bus buffer register 1 (DBB1)	$002B_{16}$	X X X X X X X X
(45)	Data bus buffer status register 1 (DBBSTS1)	$002C_{16}$	00_{16}
(46)	Comparator data register (CMPD)	$002D_{16}$	00_{16}
(47)	Port control register 1 (PCTL1)	$002E_{16}$	00_{16}
(48)	Port control register 2 (PCTL2)	$002F_{16}$	00_{16}
(49)	PWM0H register (PWM0H)	0030_{16}	X X X X X X X X
(50)	PWM0L register (PWM0L)	0031_{16}	X 0 X X X X X X
(51)	PWM1H register (PWM1H)	0032_{16}	X X X X X X X X
(52)	PWM1L register (PWM1L)	0033_{16}	X 0 X X X X X X
(53)	AD/DA control register (ADCON)	0034_{16}	0 0 0 0 1 0 0 0
(54)	A-D conversion register 1 (AD1)	0035_{16}	X X X X X X X X
(55)	D-A1 conversion register (DA1)	0036_{16}	00_{16}
(56)	D-A2 conversion register (DA2)	0037_{16}	00_{16}
(57)	A-D conversion register 2 (AD2)	0038_{16}	0 0 0 0 0 0 X X
(58)	Interrupt source selection register (INTSEL)	0039_{16}	00_{16}
(59)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(60)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(61)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(62)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(63)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(64)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(65)	LPC0 address register L (LPC0ADL)	$0FF0_{16}$	00_{16}
(66)	LPC0 address register H (LPC0ADH)	$0FF1_{16}$	00_{16}
(67)	LPC1 address register L (LPC1ADL)	$0FF2_{16}$	00_{16}
(68)	LPC1 address register H (LPC1ADH)	$0FF3_{16}$	00_{16}
(69)	Port P5 input register (P5I)	$0FF8_{16}$	00_{16}
(70)	Port control register 3 (PCTL3)	$0FF9_{16}$	00_{16}
(71)	Flash memory control register (FMCR)	$0FFE_{16}$	X X X 0 0 0 0 1
(72)	Processor status register	(PS)	X X X X 1 X X
(73)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X : Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 67 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3885 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3f(XCIN).

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

Oscillation Control
(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116". When the oscillation stabilizing time set after STP instruction released bit is "1", set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

Either XIN or XCIN divided by 16 is input to the prescaler 12 as count source, and the output of the prescaler 12 is connected to timer 1. Set the timer 1 interrupt enable bit to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. Therefore make sure not to set the timer 1 interrupt request bit to "1" before the STP instruction stops the oscillator. When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

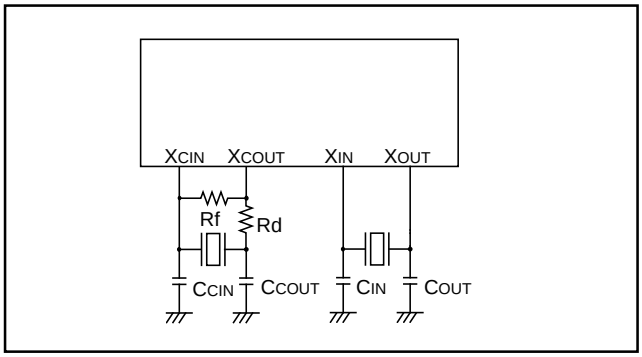


Fig. 68 Ceramic resonator circuit

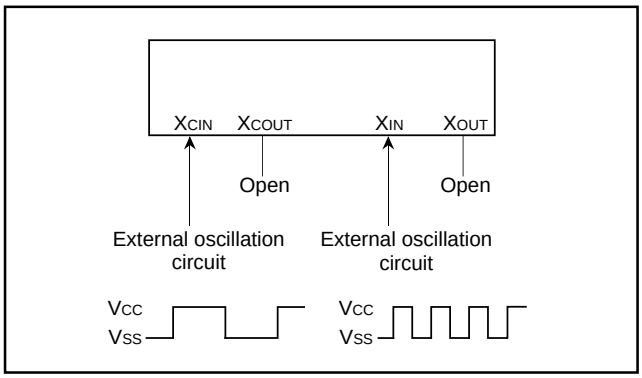
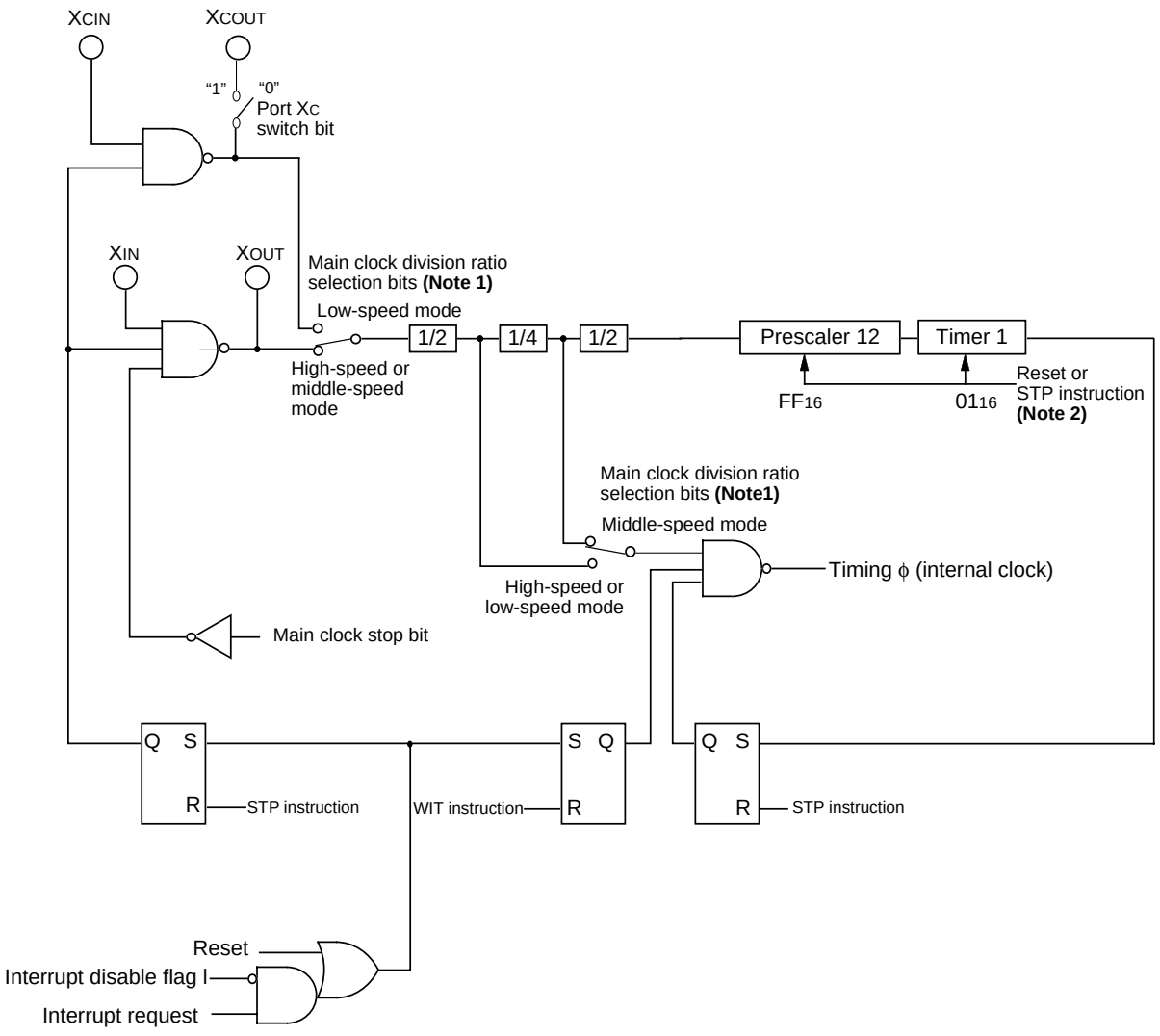


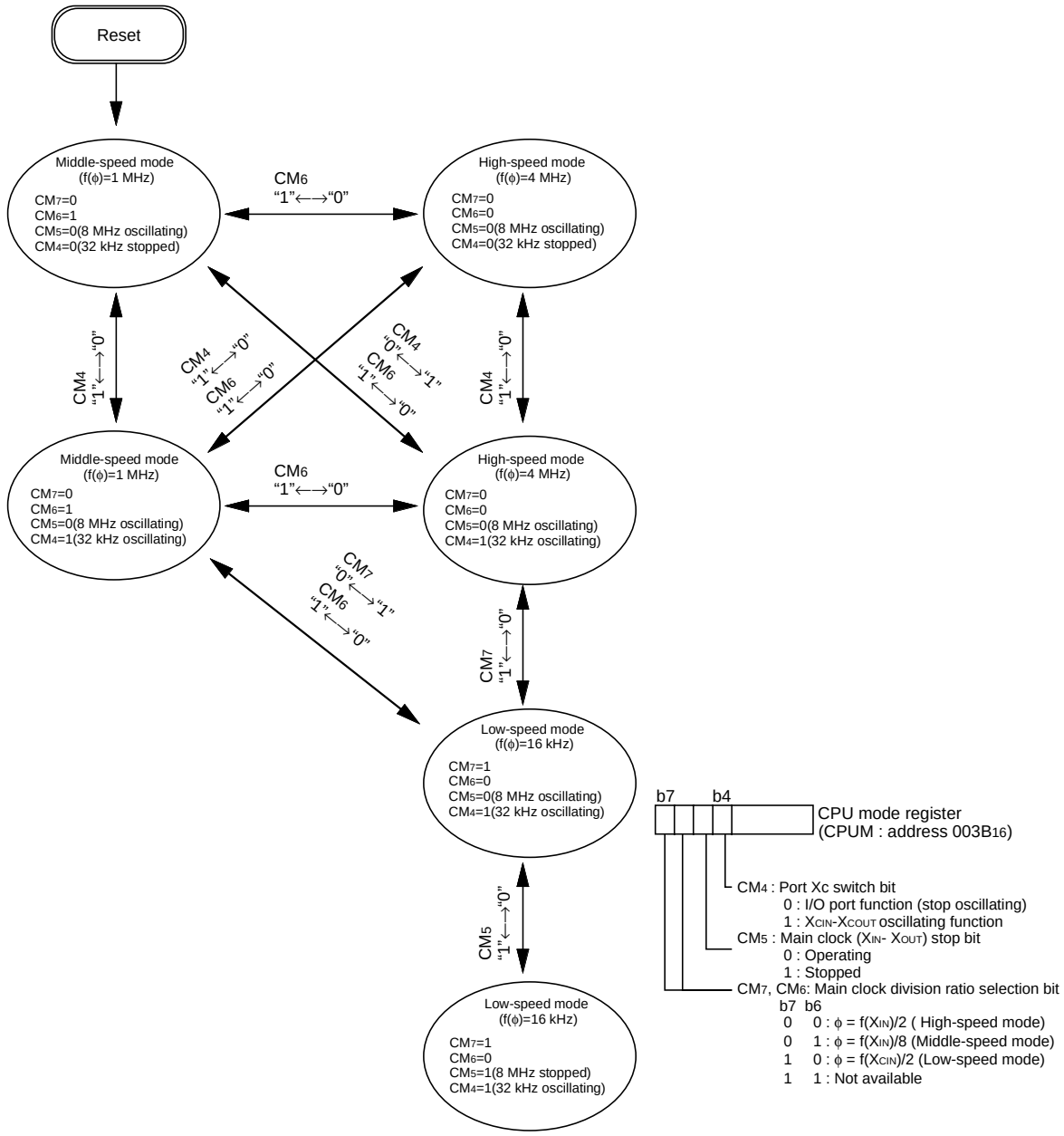
Fig. 69 External clock input circuit



Notes 1: Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register. When low-speed mode is selected, set port Xc switch bit (b4) to "1".

2: f(X_{IN})/16 is supplied as the count source to the Prescaler 12 at reset. When exciting STP instruction, the count source does not change either f(X_{IN}))/16 or f(X_{CIN}))/16 after releasing stop mode. Oscillation stabilizing time is not fixed "01FF$_{16}$" when the bit 6 of PCTL2 is "1".

Fig. 70 System clock generating circuit block diagram (Single-chip mode)



Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3 : Timer operates in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs by connecting prescaler 12 and Timer 1 in middle/high-speed mode.
5 : When the stop mode is ended, a delay of approximately 0.25 s occurs by Timer 1 and Timer 2 in low-speed mode.
6 : Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle/high-speed mode.
7 : The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.

Fig. 71 State transitions of system clock

FLASH MEMORY MODE

The 3885 (flash memory version) has an internal new DINOR flash memory that can be reprogrammed with 2 power sources when V_{CC} is 3.3 V.

For this flash memory , two flash memory modes are available in which to read, program, and erase: parallel I/O and a CPU reprogram mode in which the flash memory can be manipulated by the Central Processing Unit (CPU). Each mode is detailed in the pages to follow.

The flash memory of the 3885 is divided into User ROM area and Boot ROM area as shown in Figure 72.

In addition to the ordinary user ROM area to store a microcomputer operation control program, 3885 program has a Boot ROM area that is used to store a program to control reprogramming in CPU reprogram mode. The user can store a reprogram control software in this area that suits the user's application system. This Boot ROM area can be reprogrammed in only parallel I/O mode.

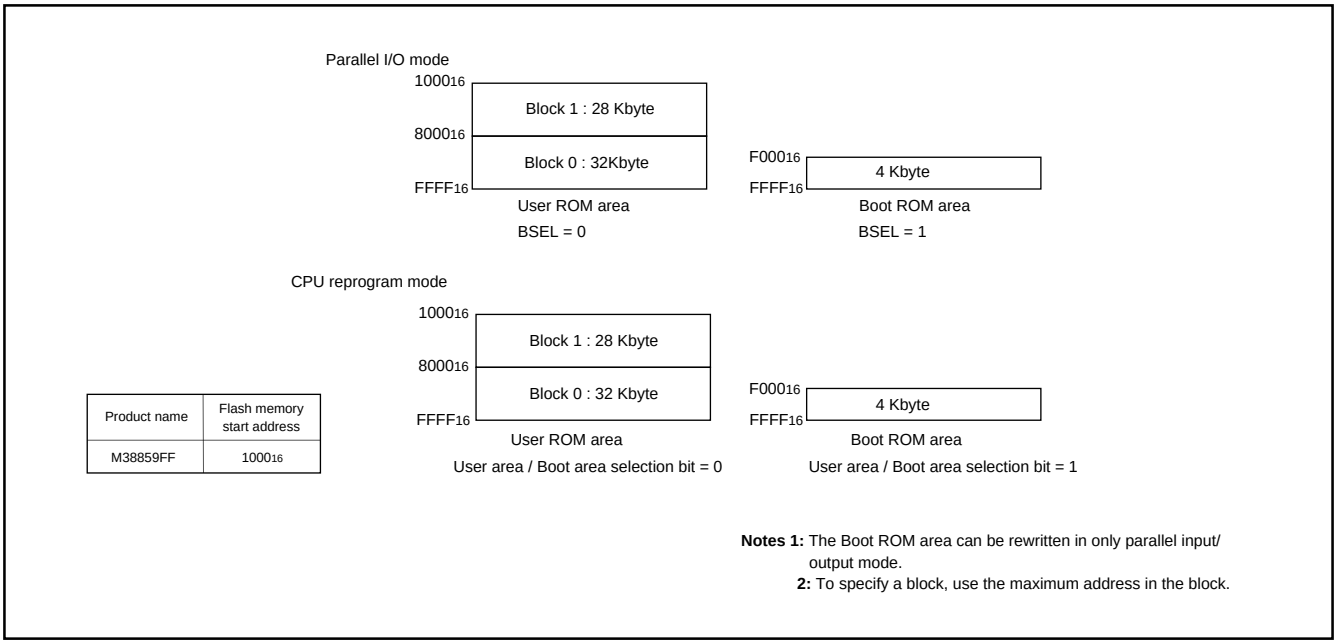


Fig. 72 Block diagram of flash memory version

Parallel I/O Mode

The parallel I/O mode is entered by making connections shown in Figures 73 and then turning the Vcc power supply on.

Address

The user ROM is divided into two blocks as shown in Figure 72. The block address referred to in this data sheet is the maximum address value of each block.

User ROM and Boot ROM Areas

In parallel I/O mode, the user ROM and boot ROM areas shown in Figure 72 can be rewritten. The BSEL pin is used to choose between these two areas. The user ROM area is selected by pulling the BSEL input low; the boot ROM area is selected by driving the BSEL input high. Both areas of flash memory can be operated on in the same way.

Program and block erase operations can be performed in the user ROM area. The user ROM area and its blocks are shown in Figure 72.

The user ROM area is 60 Kbytes in size. In parallel I/O mode, it is located at addresses 1000_{16} through $FFFF_{16}$. The boot ROM area is 4 Kbytes in size. In parallel I/O mode, it is located at addresses $F000_{16}$ through $FFFF_{16}$. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)

In the Boot ROM area, an erase block operation is applied to only one 4 Kbyte block.

Functional Outline (Parallel I/O Mode)

In parallel I/O mode, bus operation modes—Read, Output Disable, Standby, Write, and Deep Power Down—are selected by the status of the $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, and $\overline{RP}$ input pins.

The contents of erase, program, and other operations are selected by writing a software command. The data, status register, etc. in memory can only be read out by a read after software command input.

Program and erase operations are controlled using software commands.

The following explains about bus operation modes, software commands, and status register.

Bus Operation Modes

Read

The Read mode is entered by pulling the $\overline{OE}$ pin low when the $\overline{CE}$ pin is low and the $\overline{WE}$ and $\overline{RP}$ pins are high. There are two read modes: array, and status register, which are selected by software command input. In read mode, the data corresponding to each software command entered is output from the data I/O pins D_0–D_7. The read array mode is automatically selected when the device is powered on or after it exits deep power down mode.

Output Disable

The output disable mode is entered by pulling the $\overline{CE}$ pin low and the $\overline{WE}$, $\overline{OE}$, and $\overline{RP}$ pins high. Also, the data I/O pins are placed in the high-impedance state.

Standby

The standby mode is entered by driving the $\overline{CE}$ pin high when the $\overline{RP}$ pin is high. Also, the data I/O pins are placed in the high-impedance state. However, if the $\overline{CE}$ pin is set high during erase or program operation, the internal control circuit does not halt immediately and normal power consumption is required until the operation under way is completed.

Write

The write mode is entered by pulling the $\overline{WE}$ pin low when the $\overline{CE}$ pin is low and the $\overline{OE}$ and $\overline{RP}$ pins are high. In this mode, the device accepts the software commands or write data entered from the data I/O pins. A program, erase, or some other operation is initiated depending on the content of the software command entered here. The input data such as address and software command is latched at the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs earlier.

Deep Power Down

The deep power down is entered by pulling the $\overline{RP}$ pin low. Also, the data I/O pins are placed in the high-impedance state. When the device is freed from deep power down mode, the read array mode is selected and the content of the status register is set to "80_{16}." If the $\overline{RP}$ pin is pulled low during erase or program operation, the operation under way is canceled and the data in the relevant block becomes invalid.

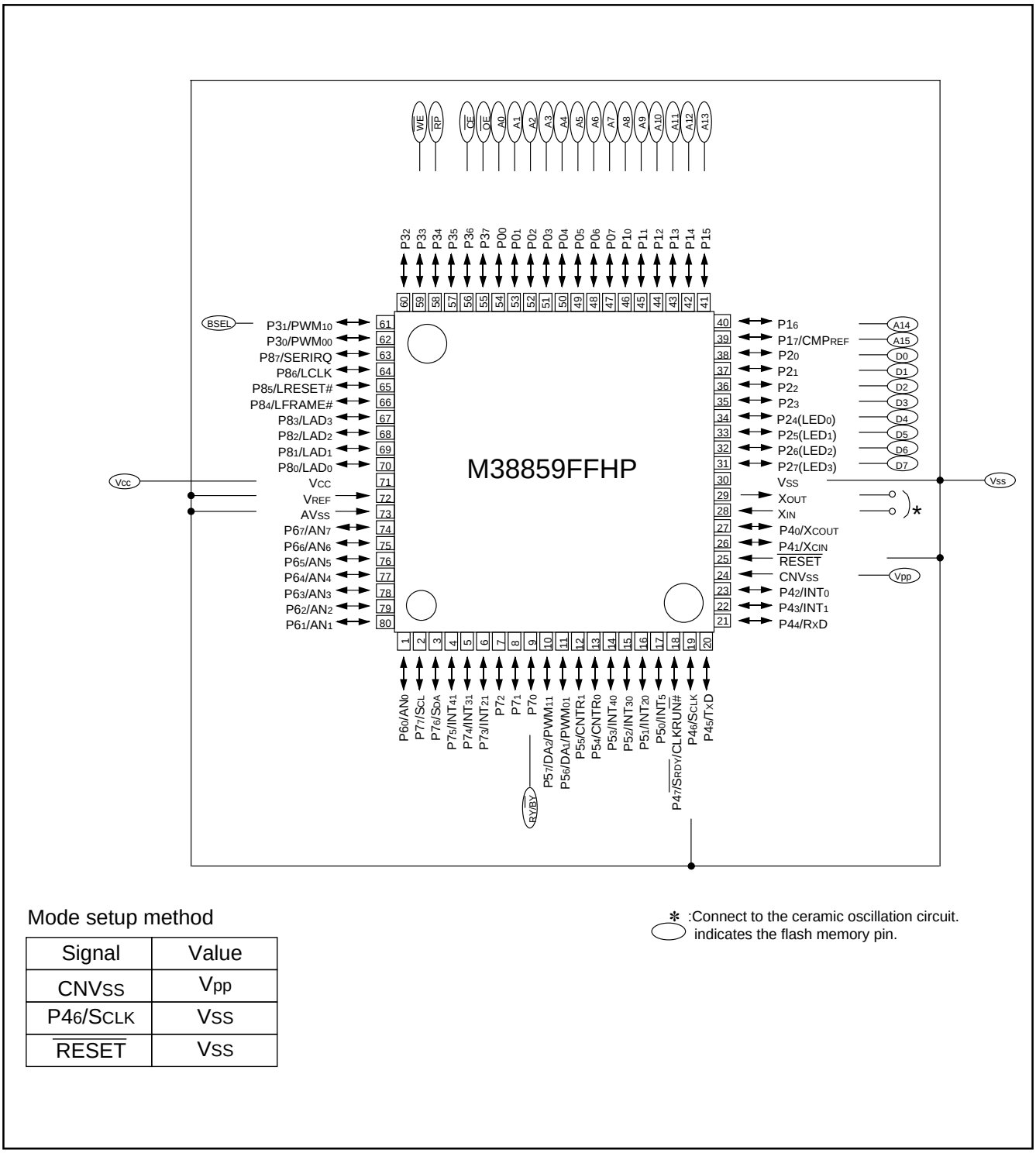
Table 19 Relationship between control signals and bus operation modes

Mode \ Pin name		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RP}$	D_0 to D_7
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data output
	Status register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Status register data output
Output disabled		V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-z
Stand by		V_{IH}	X	X	V_{IH}	Hi-z
Write	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command/data input
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command input
	Other	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command input
Deep power down		X	X	X	V_{IL}	Hi-z

Note : X can be V_{IL} or V_{IH}.

Table 20 Description of Pin Function (Flash Memory Parallel I/O Mode)

Pin name	Signal name	I/O	Function
V_{CC},V_{SS}	Power supply input	I	Apply 3.0 ± 0.3 V to the Vcc pin and 0 V to the Vss pin.
CNV_{SS}	Power suppy input	I	Connect to V_{pp} = 5V ± 0.5V.
$\overline{RESET}$	Reset input	I	Input “L” level.
X_{IN}	Clock input	I	Connect a ceramic or crystal resonator between the X_{IN} and X_{OUT} pins. When entering an externally derived clock, enter it from X_{IN} and leave X_{OUT} open.
X_{OUT}	Clock output	O	
AV_{SS}	Analog power supply input	I	Connect to Vss.
V_{REF}	Reference voltage input	I	Connect to Vss.
$P0_0$ to $P0_7$	Address input A_0 to A_7	I	This is address A_0–A_7 input pins.
$P1_0$ to $P1_7$	Address input A_8 to A_{15}	I	These are address A_8–A_{15} input pins.
$P2_0$ to $P2_7$	Data I/O D_0 to D_7	I/O	These are data D_0–D_7 input/output pins.
$P3_0$	Input $P3_0$	I	Input “H” or “L” or keep open.
$P3_1$	BSEL input	I	This is a BSEL input pin.
$P3_2$	Input $P3_2$	I	Input “H” or “L” or keep open.
$P3_3$	$\overline{WE}$ input	I	This is a $\overline{WE}$ input pin.
$P3_4$	$\overline{RP}$ input	I	This is a $\overline{RP}$ input pin.
$P3_5$	RY/$\overline{BY}$ output	O	This is a RY/$\overline{BY}$ output pin.
$P3_6$	$\overline{CE}$ input	I	This is a $\overline{CE}$ input pin.
$P3_7$	$\overline{OE}$ input	I	This is a $\overline{OE}$ input pin.
$P4_0$ to $P4_5$	Input $P4_0$ to $P4_5$	I	Input “H” or “L” or keep open.
$P4_6$	Flash mode Input	I	Connect “L” for Pallarel I/O mode.
$P4_7$	Input $P4_7$	I	Input “H” or “L” or keep open.
$P5_0$ to $P5_7$	Input P5	I	Input “H” or “L” or keep open.
$P6_0$ to $P6_7$	Input P6	I	Input “H” or “L” or keep open.
$P7_0$ to $P7_7$	Input P7	I	Input “H” or “L” or keep open.
$P8_0$ to $P8_7$	Input P8	I	Input “H” or “L” or keep open.



Mode setup method

Signal	Value
CNVSS	Vpp
P46/SCLK	VSS
$\overline{\text{RESET}}$	VSS

* :Connect to the ceramic oscillation circuit.
indicates the flash memory pin.

Fig. 73 Pin connection diagram in parallel I/O mode

Software Commands

Table 21 lists the software commands. By entering a software command from the data I/O pins (D_0–D_7) in Write mode, specify the content of the operation, such as erase or program operation, to be performed.

The following explains the content of each software command.

Read Array Command (FF_{16})

The read array mode is entered by writing the command code "FF_{16}" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the content of the specified address is output from the data I/O pins (D_0–D_7).

The read array mode is retained intact until another command is written.

The read array mode is also selected automatically when the device is powered on and after it exits deep power down mode.

Read Status Register Command (70_{16})

When the command code "70_{16}" is written in the first bus cycle, the content of the status register is output from the data I/O pins (D_0–D_7) by a read in the second bus cycle. Since the content of the status register is updated at the falling edge of $\overline{OE}$ or $\overline{CE}$, the $\overline{OE}$ or $\overline{CE}$ signal must be asserted each time the status is read. The status register is explained in the next section.

Clear Status Register Command (50_{16})

This command is used to clear the bits SR4,SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "50_{16}" in the first bus cycle.

Table 21 Software command list (parallel I/O mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D_0 to D_7)	Mode	Address	Data (D_0 to D_7)
Read array	1	Write	X(Note 4)	FF_{16}			
Read status register	2	Write	X	70_{16}	Read	X	SRD(Note 1)
Clear status register	1	Write	X	50_{16}			
Program	2	Write	X	40_{16}	Write	WA(Note 2)	WD(Note 2)
Block erase	2	Write	X	20_{16}	Write	BA(Note 3)	$D0_{16}$

Notes 1: SRD = Status Register Data

2: WA = Write Address, WD = Write Data

3: BA = Block Address (Enter the maximum address of each block)

4: X denotes a given address in the user ROM area or boot ROM area.

Program Command (40$_{16}$)

The program operation starts when the command code "40$_{16}$" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.

Whether the write operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ signal status. When the program starts, the read status register mode is accessed automatically and the content of the status register can be read out from the data bus (D_0–D_7). The status register bit 7 (SR7) is set to "0" at the same time the write operation starts and is returned to "1" upon completion of the write operation. In this case, the read status register mode remains active until the read array command (FF$_{16}$) is written.

The RY/$\overline{BY}$ pin is "L" during write operation and "H" when the write operation is completed as is the status register bit 7.

At program end, program results can be checked by reading the status register.

Block Erase Command (20$_{16}$/D0$_{16}$)

By writing the command code "20$_{16}$" in the first bus cycle and the confirmation command code "D0$_{16}$" in the second bus cycle that follows to the block address of a flash memory block, the system initiates a block erase (erase and erase verify) operation.

Whether the block erase operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ signal. At the same time the block erase operation starts, the read status register mode is automatically entered, so the content of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF$_{16}$) is written.

The RY/$\overline{BY}$ pin is "L" during block erase operation and "H" when the block erase operation is completed as is the status register bit 7.

After the block erase operation is completed, the status register can be read out to know the result of the block erase operation. For details, refer to the section where the status register is detailed.

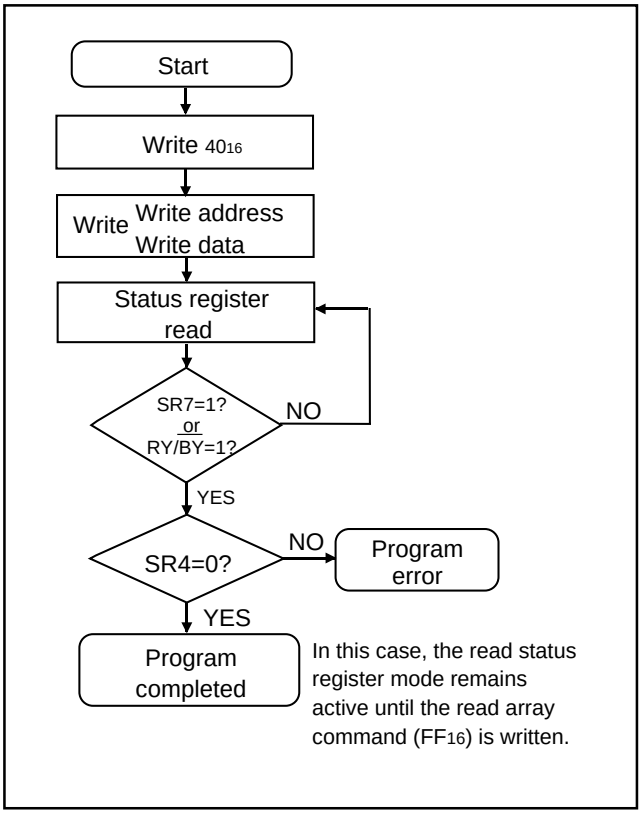


Fig. 74 Page program flowchart

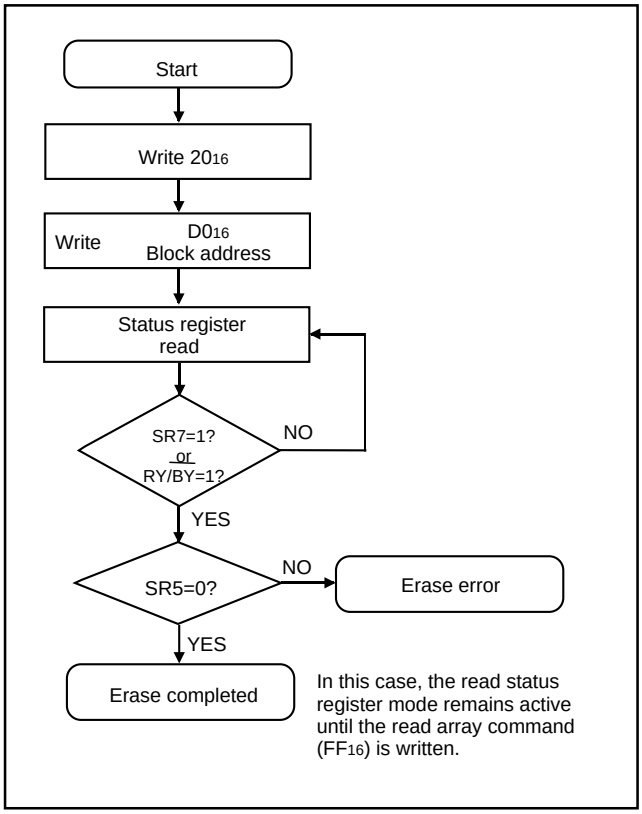


Fig. 75 Block erase flowchart

Status Register

The status register indicates status such as whether an erase operation or a program ended successfully or in error. It can be read under the following conditions.

(1) In the read array mode when the read status register command (70_{16}) is written and the block address is subsequently read.
(2) In the period from when the program write or auto erase starts to when the read array command (FF_{16})

The status register is cleared in the following situations.

(1) By writing the clear status register command (50_{16})
(2) In the deep power down mode
(3) In the power supply off state

Table 22 gives the definition of each status register bit. When power is turned on or returning from the deep power down mode, the status register outputs "80_{16}".

Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory. When power is turned on or returning from the deep power down mode, "1" is set for it. This bit is "0" (busy) during the write or erase operations and becomes "1" when these operations ends.

Erase Status (SR5)

The erase status reports the operating status of the erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

Program Status (SR4)

The program status reports the operating status of the write operation. If a write error occurs, it is set to "1". When the program status is cleared, it is set to "0".

If "1" is written for any of the SR5, SR4 bits, the program erase all blocks, block erase, commands are not accepted. Before executing these commands, execute the clear status register command (50_{16}) and clear the status register.

Also, any commands are not correct, both SR5 and SR4 are set to "1".

Full Status Check

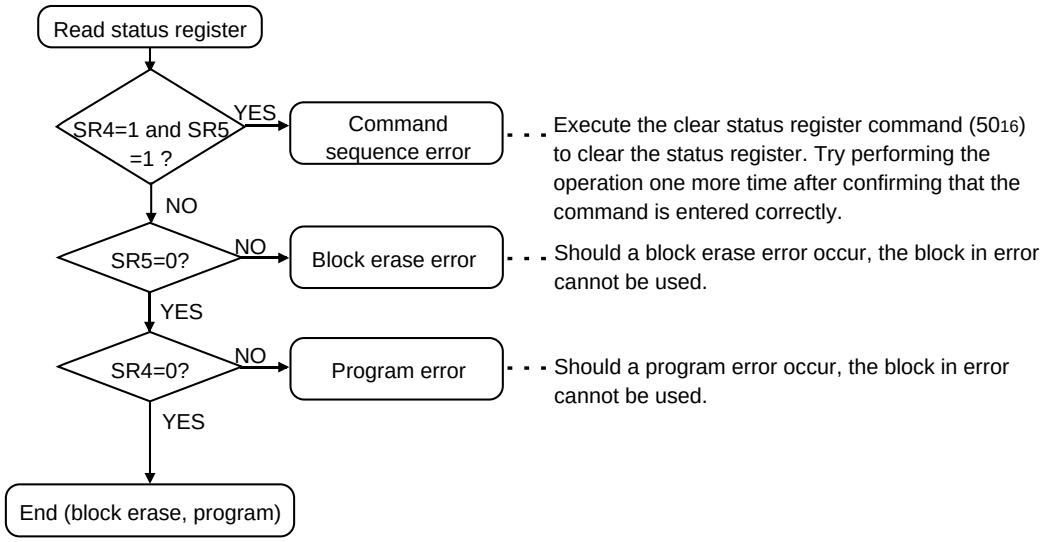
Results from executed erase and program operations can be known by running a full status check. Figure 76 shows a flowchart of the full status check and explains how to remedy errors which occur.

Ready/Busy (RY/$\overline{BY}$) pin

The RY/$\overline{BY}$ pin is an output pin (N-chanel open drain output) which, like the sequencer status (SR7), indicates the operating status of the flash memory. It is "L" level during auto program or auto erase operations and becomes to the high impedance state (ready state) when these operations end. The RY/$\overline{BY}$ pin requires an external pull-up.

Table 22 Status register

Each bit of SRD0 bits	Status name	Definition	
		"1"	"0"
SR7 (D_7)	Sequencer status	Ready	Busy
SR6 (D_6)	Reserved	-	-
SR5 (D_5)	Erase status	Ended in error	Ended successfully
SR4 (D_4)	Program status	Ended in error	Ended successfully
SR3 (D_3)	Reserved	-	-
SR2 (D_2)	Reserved	-	-
SR1 (D_1)	Reserved	-	-
SR0 (D_0)	Reserved	-	-



Note: When one of SR5 to SR4 is set to “1” , none of the program, all blocks erase, or block erase is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 76 Full status check flowchart and remedial procedure for errors

CPU Reprogram Mode

In CPU reprogram mode, the on-chip flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).

In CPU reprogram mode, only the user ROM area shown in Figure 72 can be reprogrammed; the Boot ROM area cannot be reprogrammed. Make sure the program and block erase commands are issued for only the user ROM area.

The control program for CPU reprogram mode can be stored in either user ROM or Boot ROM area. In the CPU reprogram mode, because the flash memory cannot be read from the CPU, the reprogram control software must be transferred to internal RAM area before it can be executed.

Microcomputer Mode and Boot Mode

The control software for CPU reprogram mode must be programed into the user ROM or Boot ROM area in parallel I/O mode beforehand. (If the control software is programed into the Boot ROM area, the standard serial I/O mode becomes unusable.)

See Figure 72 for details about the Boot ROM area.

Normal microcomputer mode is entered when the microcomputer is released from reset with pulling CNVSS pin low. In this case, the CPU starts operating using the control software in the user ROM area.

When the microcomputer is released from reset by pulling the P46/SCLK pin high, the CNVSS pin high, the CPU starts operating using the control software in the Boot ROM area (program start address should be stored FFFC16, FFFD16). This mode is called the "boot mode".

Block Address

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command. In case of the M38859FF, these are two block.

Outline Performance (CPU Reprogram Mode)

In the CPU reprogram mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. This reprogram control software must be transferred to internal RAM before it can be executed.

The CPU reprogram mode is accessed by applying 5V ± 10% to the CNVSS pin and writing "1" for the CPU reprogram mode select bit (bit 1 in address 0FFE16). Software commands are accepted once the mode is accessed.

Use software commands to control software and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 77 shows the flash memory control register.

Bit 0 is the RY/$\overline{BY}$ status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is "0". Otherwise, it is "1".

Bit 1 is the CPU reprogram mode select bit. When this bit is set to "1" and 5V ± 10% are applied to the CNVSS pin, the M38859FF enters the CPU reprogram mode. Software commands are accepted once the mode is accessed. In CPU reprogram mode, the CPU becomes unable to access the internal flash memory. Therefore, use the control software in RAM for write to bit 1. To set this bit to "1", it is necessary to write "0" and then write "1" in succession. The bit can be set to "0" by only writing a "0".

Bit 2 is the CPU reprogram mode entry flag. This bit can be read to check whether the CPU reprogram mode has been entered or not.

Bit 3 is the flash memory reset bit used to reset the control circuit of the internal flash memory. This bit is used when exiting CPU reprogram mode and when flash memory access has failed. When the CPU reprogram mode select bit is "1", writing "1" for this bit resets the control circuit. To release the reset, it is necessary to set this bit to "0".

Bit 4 is the User area/Boot area selection bit. When this bit is set to "1", Boot ROM area is accessed, and CPU reprogram mode in Boot ROM area is available. In boot mode, this bit is set "1" automatically. To set and clear this bit must be operated in RAM area.

Figure 78 shows a flowchart for setting/releasing the CPU reprogram mode.

Notes on CPU Reprogram Mode

Described below are the precautions to be observed when reprogram the flash memory in CPU reprogram mode.

(1) Operation speed

During CPU reprogram mode, set the internal clock φ frequency 4MHz or less using the main clock division ratio selection bits (bit 6,7 at 003B16).

(2) Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU reprogram mode .

(3) Interrupts inhibited against use

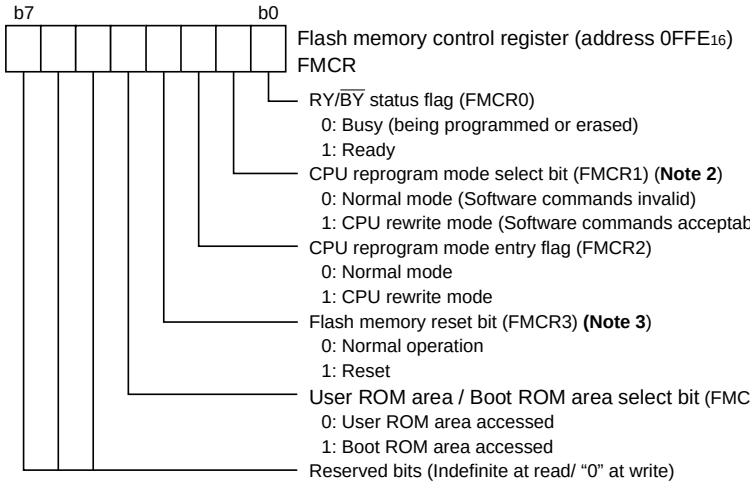
The interrupts cannot be used during CPU reprogram mode because they refer to the internal data of the flash memory.

(4) Watchdog timer

In case of the watchdog timer has been running already, the internal reset generated by watchdog timer underflow does not happen, because of watchdog timer is always clearing during program or erase operation.

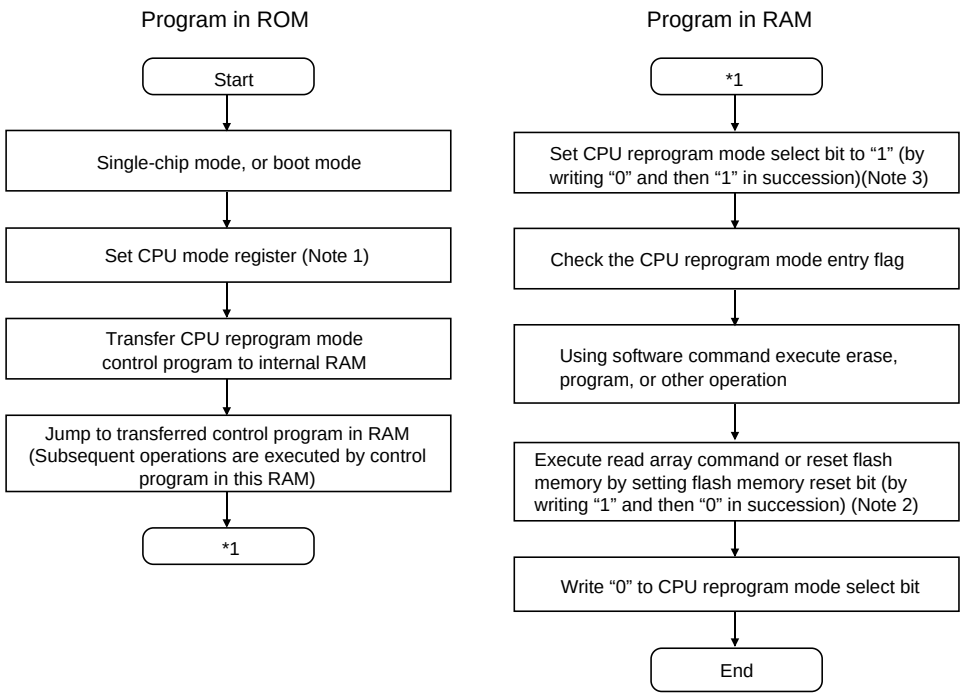
(5) Reset

Reset is always valid. In case of CNVSS = "H" when reset is released, boot mode is active. So the program starts from the address contained in address FFFC16 and FFFD16 in boot ROM area.



Notes 1: The contents of flash memory control register are "XXX00001" just after reset release.
2: For this bit to be set to "1", the user needs to write "0" and then "1" to it in succession. If it is not this procedure, this bit will not be set to "1". Additionally, it is required to ensure that no interrupt will be generated during that interval.
Use the control program in the area except the built-in flash memory for write to this bit.
3: This bit is valid when the CPU rewrite mode select bit is "1". Set this bit 3 to "0" subsequently after setting bit 3 to "1".
4: Use the control program in the area except the built-in flash memory for write to this bit.

Fig. 77 Flash memory control registers



Notes 1: Set bit 6,7 (Main clock division ratio selection bits) at CPU mode register (003B16).
2: Before exiting the CPU reprogram mode after completing erase or program operation, always be sure to execute a read array command or reset the flash memory.

Fig. 78 CPU rewrite mode set/reset flowchart

Software Commands

Table 23 lists the software commands.
After setting the CPU reprogram mode select bit to "1", write a software command to specify an erase or program operation.
The content of each software command is explained below.

Read Array Command (FF_{16})

The read array mode is entered by writing the command code "FF_{16}" in the first bus cycle. When an address to be read is input in next bus cycles, the content of the specified address is read out at the data bus (D_0–D_7).
The read array mode is retained intact until another command is written. And after power on and after recover from deep power down mode, this mode is selected also.

Read Status Register Command (70_{16})

When the command code "70_{16}" is written in the first bus cycle, the content of the status register is read out at the data bus (D_0–D_7) by a read in the second bus cycle.
The status register is explained in the next section.

Clear Status Register Command (50_{16})

This command is used to clear the bits SR1,SR4 and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "50_{16}" in the first bus cycle.

Table 23 List of software commands (CPU rewrite mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D_0 to D_7)	Mode	Address	Data (D_0 to D_7)
Read array	1	Write	X (Note 4)	FF_{16}			
Read status register	2	Write	X	70_{16}	Read	X	SRD (Note 1)
Clear status register	1	Write	X	50_{16}			
Program	2	Write	X	40_{16}	Write	WA (Note 2)	WD (Note 2)
Block erase	2	Write	X	20_{16}	Write	BA (Note 3)	$D0_{16}$

Note 1: SRD = Status Register Data
2: WA = Write Address, WD = Write Data
3: BA = Block Address (Enter the maximum address of each block.)
4: X denotes a given address in the user ROM area .

Program Command (40$_{16}$)

Program operation starts when the command code "40$_{16}$" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.

Whether the program operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ status flag. When the program starts, the read status register mode is accessed automatically and the content of the status register is read into the data bus (D0–D7). The status register bit 7 (SR7) is set to "0" at the same time the program operation starts and is returned to "1" upon completion of the program operation. In this case, the read status register mode remains active until the read array command (FF$_{16}$) is written.

The RY/$\overline{BY}$ status flag is "0" during program operation and "1" when the program operation is completed as is the status register bit 7.

At program end, program results can be checked by reading the status register.

Block Erase Command (20$_{16}$/D0$_{16}$)

By writing the command code "20$_{16}$" in the first bus cycle and the confirmation command code "D0$_{16}$" in the second bus cycle that follows to the block address of a flash memory block, the system initiates a block erase (erase and erase verify) operation.

Whether the block erase operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ status flag. At the same time the block erase operation starts, the read status register mode is automatically entered, so the content of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF$_{16}$) is written.

The RY/$\overline{BY}$ status flag is "0" during block erase operation and "1" when the block erase operation is completed as is the status register bit 7.

After the block erase operation is completed, the status register can be read out to know the result of the block erase operation. For details, refer to the section where the status register is detailed.

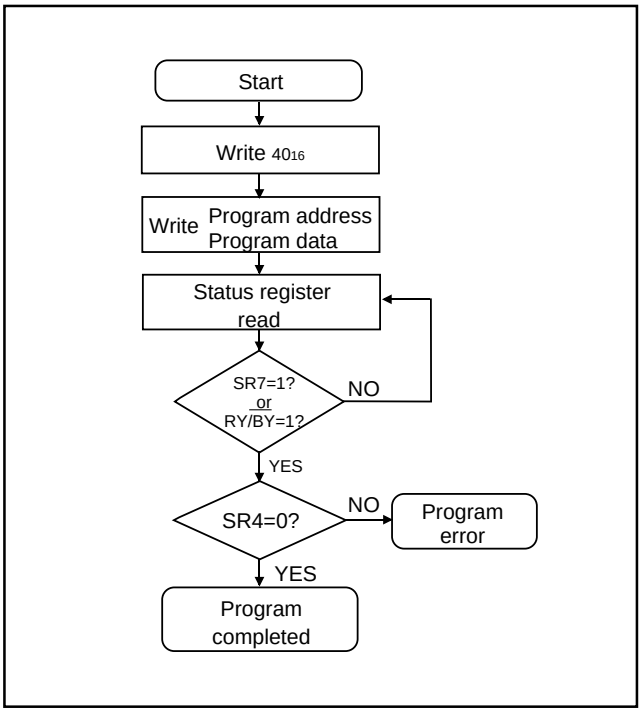


Fig. 79 Program flowchart

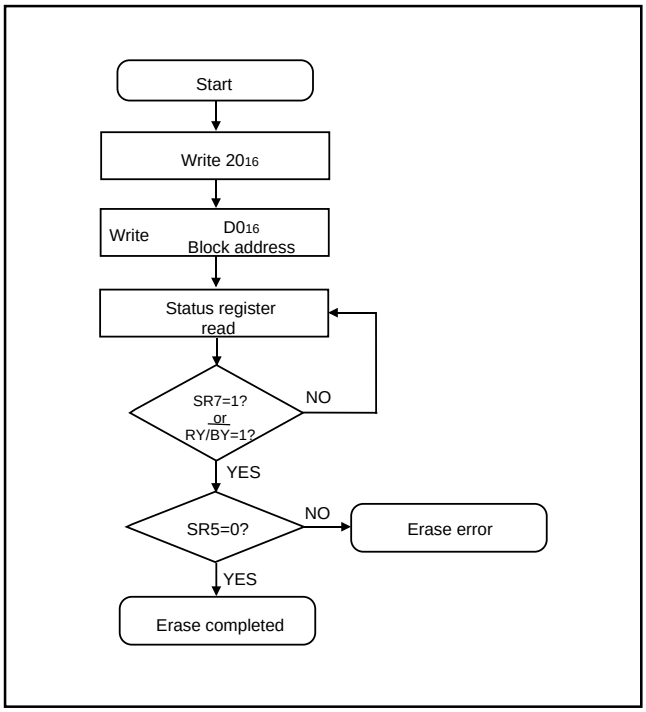


Fig. 80 Erase flowchart

Status Register

The status register shows the operating state of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways.

(1) By reading an arbitrary address from the user ROM area after writing the read status register command (70_{16})
(2) By reading an arbitrary address from the user ROM area in the period from when the program starts or erase operation starts to when the read array command (FF_{16}) is input

Table 24 shows the status register.
Also, the status register can be cleared in the following way.
(1) By writing the clear status register command (50_{16})
(2) In the deep power down mode
(3) In the power supply off state
After a reset, the status register is set to "80_{16}".
Each bit in this register is explained below.

Sequencer status (SR7)

After power-on, and after recover from deep power down mode, the sequencer status is set to "1"(ready).
The sequencer status indicates the operating status of the device. This status bit is set to "0" (busy) during program or erase operation and is set to "1" upon completion of these operations.

Erase status (SR5)

The erase status informs the operating status of erase operation to the CPU. When an erase error occurs, it is set to "1".
The erase status is reset to "0" when cleared.

Program status (SR4)

The program status informs the operating status of write operation to the CPU. When a write error occurs, it is set to "1".
The program status is reset to "0" when cleared.

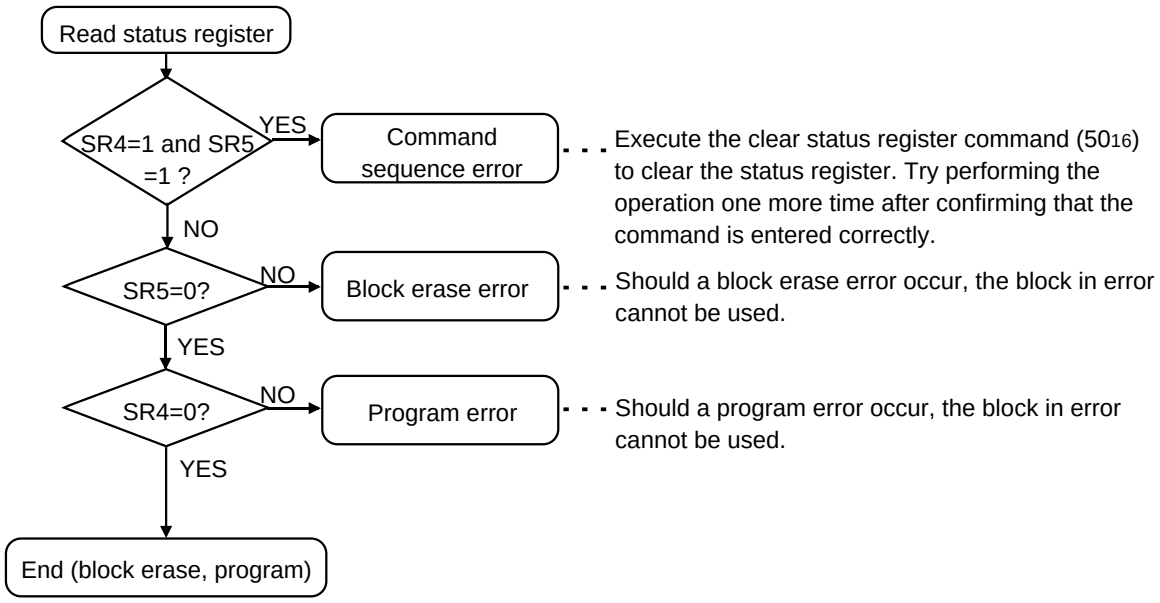
If "1" is set for any of the SR5 or SR4 bits, the program, erase all blocks, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50_{16}) and clear the status register.
Also, any commands are not correct, both SR5 and SR4 are set to "1".

Table 24 Definition of each bit in status register

Each bit of SRD0 bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 81 shows a full status check flowchart and the action to be taken when each error occurs.



Note: When one of SR5 to SR4 is set to “1” , none of the program, erase all blocks, and block erase commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 81 Full status check flowchart and remedial procedure for errors

Functions To Inhibit Rewriting Flash Memory

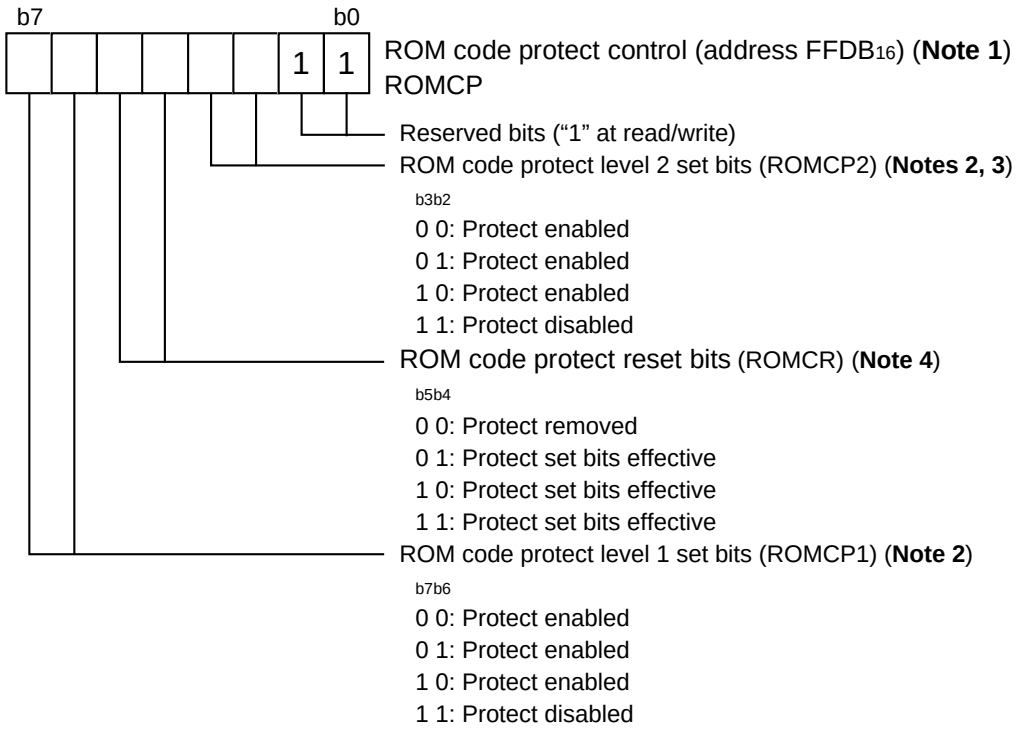
To prevent the contents of the flash memory data from being read out or rewritten easily, the device incorporates a ROM code protect function for use in parallel I/O mode.

ROM code protect function

The ROM code protect function is the function inhibit reading out or modifying the contents of the flash memory version by using the ROM code protect control address ($FFDB_{16}$) during parallel I/O mode. Figure 82 shows the ROM code protect control address ($FFDB_{16}$). (This address exists in the user ROM area.)

If one of the pair of ROM code protect bits is set to "0", ROM code protect is turned on, so that the contents of the flash memory data are protected against readout and reprogram. ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a manufactures inspection test also. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM code protect reset bits are set to "00", ROM code protect is turned off, so that the contents of the flash memory data can be read out or reprogram. Once ROM code protect is turned on, the contents of the ROM code protect reset bits cannot be modified in parallel I/O mode. Use CPU reprogram mode to reprogram the contents of the ROM code protect reset bits.



Notes 1: The contents of ROM code protect control register are "FF_{16}" just after reset release. This area is on the ROM in the mask ROM version.

2: When ROM code protect is turned on, the internal flash memory is protected against readout or modification in parallel I/O mode.

3: When ROM code protect level 2 is turned on, ROM code readout by a shipment inspection LSI tester, etc. also is inhibited.

4: The ROM code protect reset bits can be used to turn off ROM code protect level 1 and ROM code protect level 2. However, since these bits cannot be modified in parallel I/O mode, they need to be rewritten in standard serial I/O mode or CPU rewrite mode.

Fig. 82 ROM code protect control address

Flash Memory Electrical Characteristics

Table 25 Flash memory mode Electrical characteristics
(Ta = 25°C, Vcc = 3.3 ± 0.3V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{PP1}	V_{PP} power source current (read)				100	μA
I_{PP2}	V_{PP} power source current (program)				60	mA
I_{PP3}	V_{PP} power source current (erase)				30	mA
V_{IL}	"L" input voltage (Note)		0		0.8	V
V_{IH}	"H" input voltage (Note)		2.0		V_{CC}	V
V_{PP}	V_{PP} power source voltage		4.5		5.5	V

Note: Input pins for parallel I/O mode.

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The instruction with the addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the SRDY signal, set the transmit enable bit, the receive enable bit, and the SRDY output enable bit to "1".

Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

In clock-synchronous mode, an external clock is used as synchronous clock, write transmission data to the transmit buffer register during transfer clock is "H".

A-D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that f(XIN) is at least on 500 kHz during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

D-A Converter

When a D-A converter is not used, set all values of D-Ai conversion registers (i=1, 2) to "00$_{16}$".

Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The period of the internal clock ϕ is twice of the XIN period in high-speed mode.

NOTES ON USAGE

Handling of Power Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin), between power source pin (V_{CC} pin) and analog power source input pin (AV_{SS} pin), and between program power source pin (CNV_{SS}/V_{PP}) and GND pin for flash memory version when on-board reprogramming is executed. Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF–0.1 µF is recommended.

Flash Memory Version

The CNV_{SS} pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.
To improve the noise reduction, connect a track between CNV_{SS} pin and V_{SS} pin with 1 to 10 kΩ resistance.
For the mask ROM version, there is no operational interference even if CNV_{SS} pin is connected to Vss pin via a resistor.

Electric Characteristic Differences Between Mask ROM and Flash Memory Version MCUs

There are differences in electric characteristics, operation margin, noise immunity, and noise radiation between Mask ROM and Flash Memory version MCUs due to the difference in the manufacturing processes.
When manufacturing an application system with the Flash Memory version and then switching to use of the Mask ROM version, please perform sufficient evaluations for the commercial samples of the Mask ROM version.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

For the mask ROM confirmation and the mark specifications, refer to the “Mitsubishi MCU Technical Information” Homepage:
http://www.infomicom.maec.co.jp/indexe.htm

ELECTRICAL CHARACTERISTICS

Table 26 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltages	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 4.6	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$, V_{REF}, $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P7_0$–$P7_7$		–0.3 to 5.8	V
V_I	Input voltage CNV_{SS} **(Note 1)**		–0.3 to 6.5	V
V_I	Input voltage CNV_{SS} **(Note 2)**		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P7_0$–$P7_7$		–0.3 to 5.8	V
P_d	Power dissipation	T_a = 25 °C	500	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Notes 1: Flash memory version
2: Mask ROM version

Table 27 Recommended operating conditions
(V_{CC} = 3.3 V ± 0.3V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage		3.0	3.3	3.6	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage	when A-D converter is used	2.0		V_{CC}	V
		when D-A converter is used	2.7		V_{CC}	
AV_{SS}	Analog power source voltage			0		V
V_{IA}	A-D converter input voltage AN_0–AN_7		AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$, RESET, CNV_{SS}		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $P7_0$–$P7_7$		0.8V_{CC}		5.5	V
V_{IH}	“H” input voltage (when TTL input level is selected) $P7_0$–$P7_5$		2.0		5.5	V
V_{IH}	“H” input voltage (when I^2C-BUS input level is selected) S_{DA}, S_{CL}		0.7V_{CC}		5.5	V
V_{IH}	“H” input voltage (when SMBUS input level is selected) S_{DA}, S_{CL}		1.4		5.5	V
V_{IH}	“H” input voltage X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, RESET, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	“L” input voltage (when TTL input level is selected) $P7_0$–$P7_5$		0		0.8	V
V_{IL}	“L” input voltage (when I^2C-BUS input level is selected) S_{DA}, S_{CL}		0		0.3V_{CC}	V
V_{IL}	“L” input voltage (when SMBUS input level is selected) S_{DA}, S_{CL}		0		0.6	V
V_{IL}	“L” input voltage X_{IN}, X_{CIN}		0		0.16V_{CC}	V

Table 28 Recommended operating conditions
(V_{CC} = 3.3 V ± 0.3V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P2_4$–$P2_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P2_4$–$P2_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$			40	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 29 Recommended operating conditions
(V_{CC} = 3.3 V ± 0.3V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ **(Note 1)**			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ **(Note 1)**			10	mA
$I_{OL(peak)}$	"L" peak output current	$P2_4$–$P2_7$ **(Note 1)**			20	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ **(Note 2)**			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ **(Note 2)**			5	mA
$I_{OL(avg)}$	"L" peak output current	$P2_4$–$P2_7$ **(Note 2)**			15	mA
f(X_{IN})	Main clock input oscillation frequency **(Note 3)**				8	MHz
f(X_{CIN})	Sub-clock input oscillation frequency **(Notes 3, 4)**			32.768	50	kHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50%.
4: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that f(X_{CIN}) < f(X_{IN})/3.

Table 30 Electrical characteristics
(V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P8_0$–$P8_7$ **(Note)**	I_{OH} = –5 mA	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	I_{OL} = 5 mA			1.0	V
		I_{OL} = 1.6 mA			0.4	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0, INT_1 INT_{20}–INT_{40}, INT_{21}–INT_{41}, INT_5 $P3_0$–$P3_7$, RxD, S_{CLK}, $\overline{LRESET}$ $\overline{LFRAME}$, LCLK, SERIRQ			0.4		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ $\overline{RESET}$, CNV_{SS}	V_I = V_{CC} (Pin floating. Pull-up transistors "off")			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		3		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ $\overline{RESET}$,CNV_{SS}	V_I = V_{SS} (Pin floating. Pull-up transistors "off")			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–3	–100	µA
I_{IL}	"L" input current $P3_0$–$P3_7$ (at Pull-up)	V_I = V_{SS}	–13	–50	3.6	µA
V_{RAM}	RAM hold voltage	When clock stopped	2.0			V

Note: $P0_0$–$P0_3$ are measured when the $P0_0$–$P0_3$ output structure selection bit (bit 0 of PCTL1) is "0".
$P0_4$–$P0_7$ are measured when the $P0_4$–$P0_7$ output structure selection bit (bit 1 of PCTL1) is "0".
$P1_0$–$P1_3$ are measured when the $P1_0$–$P1_3$ output structure selection bit (bit 2 of PCTL1) is "0".
$P1_4$–$P1_7$ are measured when the $P1_4$–$P1_7$ output structure selection bit (bit 3 of PCTL1) is "0".
$P4_2$, $P4_3$, $P4_4$, and $P4_6$ are measured when the P4 output structure selection bit (bit 2 of PCTL2) is "0".
$P4_5$ is measured when the $P4_5$/TxD P-channel output disable bit (bit 4 of UARTCON) is "0".

Table 31 Electrical characteristics
(V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V, T_a = –20 to 85 °C, Mask ROM version unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			2.5	7	mA
		High-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			0.8	2	mA
		Middle-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = stopped Output transistors “off”			1.5	4	mA
		Middle-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”			0.6	1.5	mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			15	40	µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			10	20	µA
		Additional current when A-D converter works $f(X_{IN})$ = 8 MHz			500		µA
		Additional current when LPC I/F functions LCLK = 33 MHz			1.5		mA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Table 32 Electrical characteristics
(V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V, T_a = –20 to 85 °C, Flash memory version, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			6.0	13	mA
		High-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			0.8	2	mA
		Middle-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = stopped Output transistors “off”			2.0	7	mA
		Middle-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”			0.6	1.5	mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			100	200	µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			10	20	µA
		Additional current when A-D converter works $f(X_{IN})$ = 8 MHz			500		µA
		Additional current when LPC I/F functions LCLK = 33 MHz			1.5		mA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Table 33 A-D converter characteristics (1)
(V_{CC} = 3.3 V ± 0.3V, V_{REF} = 2.0 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)
10-bit A-D mode (when conversion mode selection bit (bit 7 of AD2) is "0")

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					10	bit
–	Absolute accuracy (excluding quantization error)		V_{CC} = V_{REF} = 3.3 V			±4	LSB
t_{CONV}	Conversion time					61	2tc(X_{IN})
R_{LADDER}	Ladder resistor			12	35	100	kΩ
I_{VREF}	Reference power source input current	at A-D converter operated	V_{REF} = 3.3 V	50	150	200	µA
		at A-D converter stopped	V_{REF} = 3.3 V			5	µA
$I_{I(AD)}$	A-D port input current					5.0	µA

Table 34 A-D converter characteristics (2)
(V_{CC} = 3.3 V ± 0.3V, V_{REF} = 2.0 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)
8-bit A-D mode (when conversion mode selection bit (bit 7 of AD2) is "1")

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					8	bit
–	Absolute accuracy (excluding quantization error)		V_{CC} = V_{REF} = 3.3 V			±2	LSB
t_{CONV}	Conversion time					50	2tc(X_{IN})
R_{LADDER}	Ladder resistor			12	35	100	kΩ
I_{VREF}	Reference power source input current	at A-D converter operated	V_{REF} = 3.3 V	50	150	200	µA
		at A-D converter stopped	V_{REF} = 3.3 V			5	µA
$I_{I(AD)}$	A-D port input current					5.0	µA

Table 35 D-A converter characteristics
(V_{CC} = 3.3 V ± 0.3V, V_{REF} = 2.7 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setting time				3	µs
RO	Output resistor		2	3.5	5	kΩ
I_{VREF}	Reference power source input current				2.1	mA

Table 36 Comparator characteristics
(V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Absolute accuracy	1LSB = V_{CC}/16			1/2	LSB
T_{CONV}	Conversion time	at 8 MHz operating			3.5	µs
		at 4 MHz operating			7	µs
V_{IA}	Analog input voltage		0		V_{CC}	V
I_{IA}	Analog input current				5.0	µA
R_{LADDER}	Ladder resistor		20	40	50	kΩ
CMP_{REF}	Internal reference voltage			29V_{CC}/32		V
	External reference input voltage		V_{CC}/32		V_{CC}	V

Table 37 Timing requirements
(V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	16			$t_{C(XIN)}$
$t_{C(XIN)}$	Main clock input cycle time	125			ns
$t_{WH(XIN)}$	Main clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	Main clock input “L” pulse width	50			ns
$t_{C(XCIN)}$	Sub-clock input cycle time	20			µs
$t_{WH(XCIN)}$	Sub-clock input “H” pulse width	5			µs
$t_{WL(XCIN)}$	Sub-clock input “L” pulse width	5			µs
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	80			ns
$t_{WH(INT)}$	INT_0, INT_1, INT_{20}, INT_{30}, INT_{40}, INT_{21}, INT_{31}, INT_{41} input “H” pulse width	80			ns
$t_{WL(INT)}$	INT_0, INT_1, INT_{20}, INT_{30}, INT_{40}, INT_{21}, INT_{31}, INT_{41} input “L” pulse width	80			ns
$t_{C(SCLK1)}$	Serial I/O clock input cycle time **(Note)**	800			ns
$t_{WH(SCLK1)}$	Serial I/O clock input “H” pulse width **(Note)**	370			ns
$t_{WL(SCLK1)}$	Serial I/O clock input “L” pulse width **(Note)**	370			ns
$t_{su(RxD-SCLK1)}$	Serial I/O input setup time	220			ns
$t_{h(SCLK1-RxD)}$	Serial I/O input hold time	100			ns

Note : When bit 6 of SIOCON is “1” (clock synchronous).
Divide this value by four when bit 6 of SIOCON is “0” (UART).

Table 38 Switching characteristics
(V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WH} (S_{CLK})	Serial I/O clock output “H” pulse width	Fig. 90	$t_{C(SCLK)}$/2–30			ns
t_{WL} (S_{CLK})	Serial I/O clock output “L” pulse width		$t_{C(SCLK)}$/2–30			ns
t_d (S_{CLK}-TxD)	Serial I/O output delay time **(Note 1)**				140	ns
t_v (S_{CLK}-TxD)	Serial I/O output valid time **(Note 1)**		–30			ns
t_r (S_{CLK})	Serial I/O clock output rising time				30	ns
t_f (S_{CLK})	Serial I/O clock output falling time				30	ns
t_r (CMOS)	CMOS output rising time **(Note 2)**			10	30	ns
t_f (CMOS)	CMOS output falling time **(Note 2)**			10	30	ns

Notes 1: When the $P4_5$/TxD P-channel output disable bit (bit 4 of UARTCON) is “0”.
2: The X_{OUT} pin is excluded.

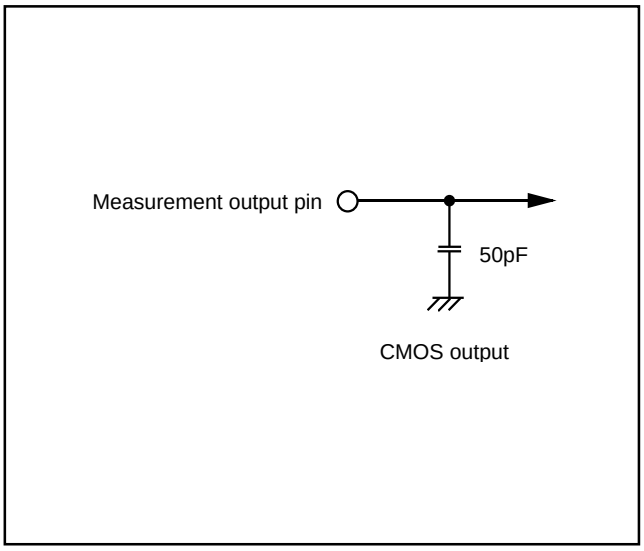


Fig. 83 Circuit for measuring output switching characteristics

Timing diagram

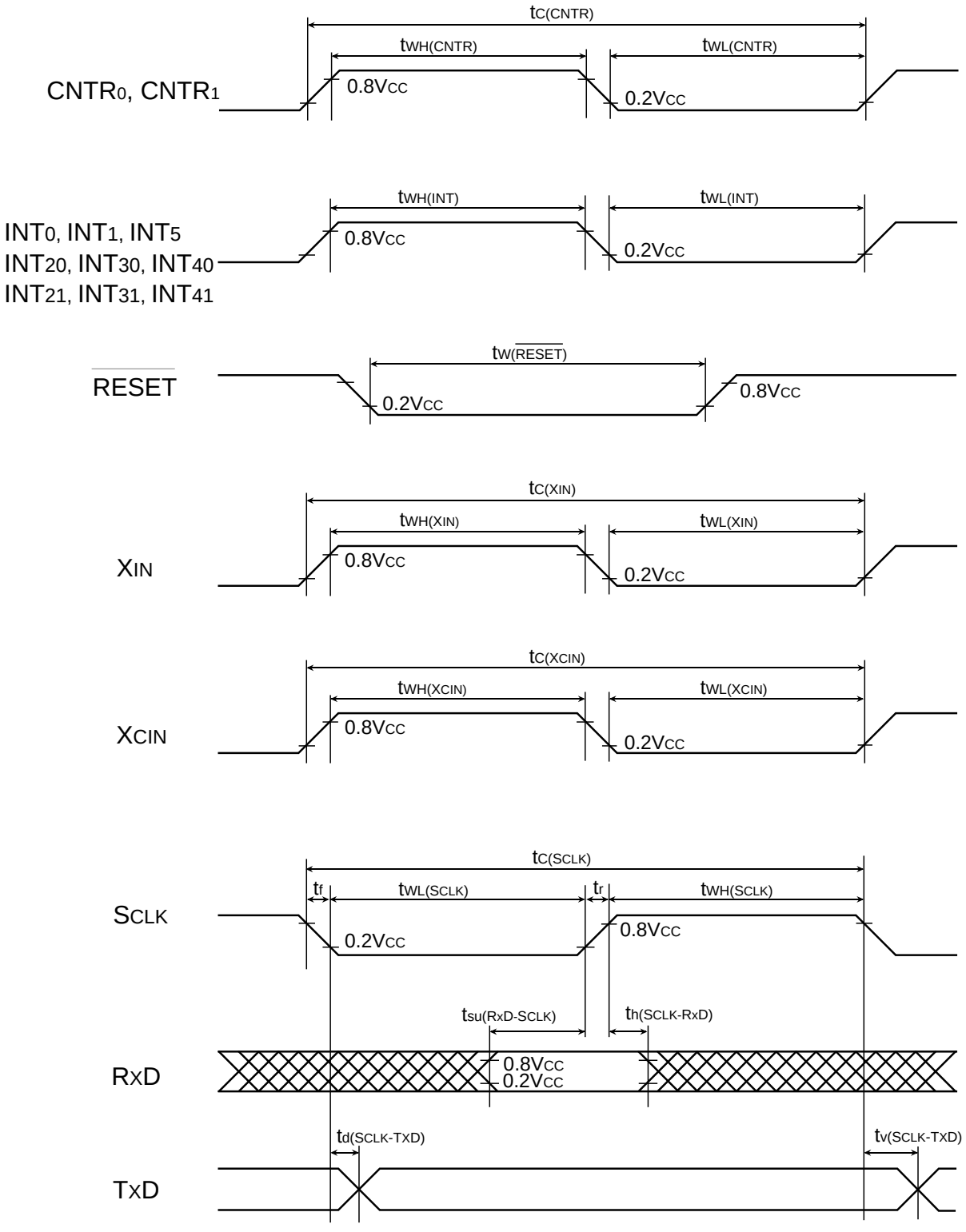


Fig. 84 Timing diagram

Table 39 Multi-master I²C-BUS bus line characteristics

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time for START condition	4.0		0.6		µs
t_{LOW}	Hold time for SCL clock = “0”	4.7		1.3		µs
t_R	Rising time of both SCL and SDA signals		1000	20+0.1Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time for SCL clock = “1”	4.0		0.6		µs
t_F	Falling time of both SCL and SDA signals		300	20+0.1Cb	300	ns
$t_{SU;DAT}$	Data setup time	250		100		ns
$t_{SU;STA}$	Setup time for repeated START condition	4.7		0.6		µs
$t_{SU;STO}$	Setup time for STOP condition	4.0		0.6		µs

Note: Cb = total capacitance of 1 bus line

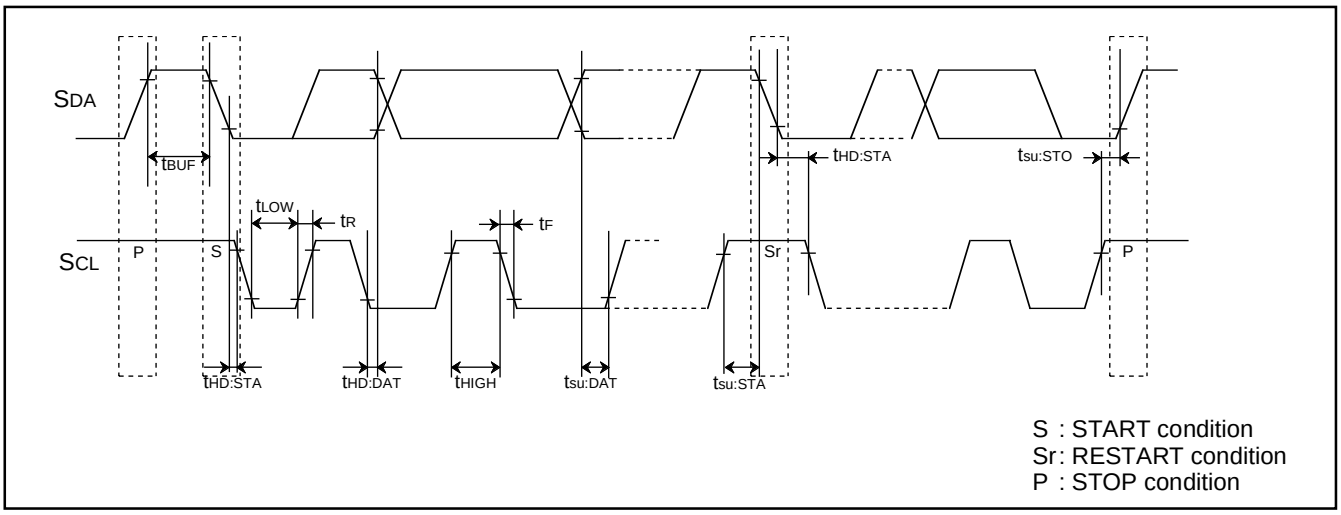


Fig. 85 Timing diagram of multi-master I²C-BUS

Table 40 Timing requirements and switching characteristics
(V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$t_{C(CLK)}$	LCLK clock input cycle time		30			ns
$t_{WH(CLK)}$	LCLK clock input “H” pulse width		11			ns
$t_{WL(CLK)}$	LCLK clock input “L” pulse width		11			ns
$t_{su(D-C)}$	input set up time	LAD_3 to LAD_0,	13			ns
		SERIRQ, $\overline{CLKRUN}$, $\overline{LFRAME}$	7			
$t_{h(C-D)}$	input hold time	LAD_3 to LAD_0, $\overline{CLKRUN}$, $\overline{LFRAME}$	0			ns
		SERIRQ,	2			
$t_{V(C-D)}$	LAD_3 to LAD_0, SERIRQ, $\overline{CLKRUN}$ valid delay time		2		15	ns
$t_{off(A-F)}$	LAD_3 to LAD_0,SERIRQ,$\overline{CLKRUN}$ floating output delay time				28	ns

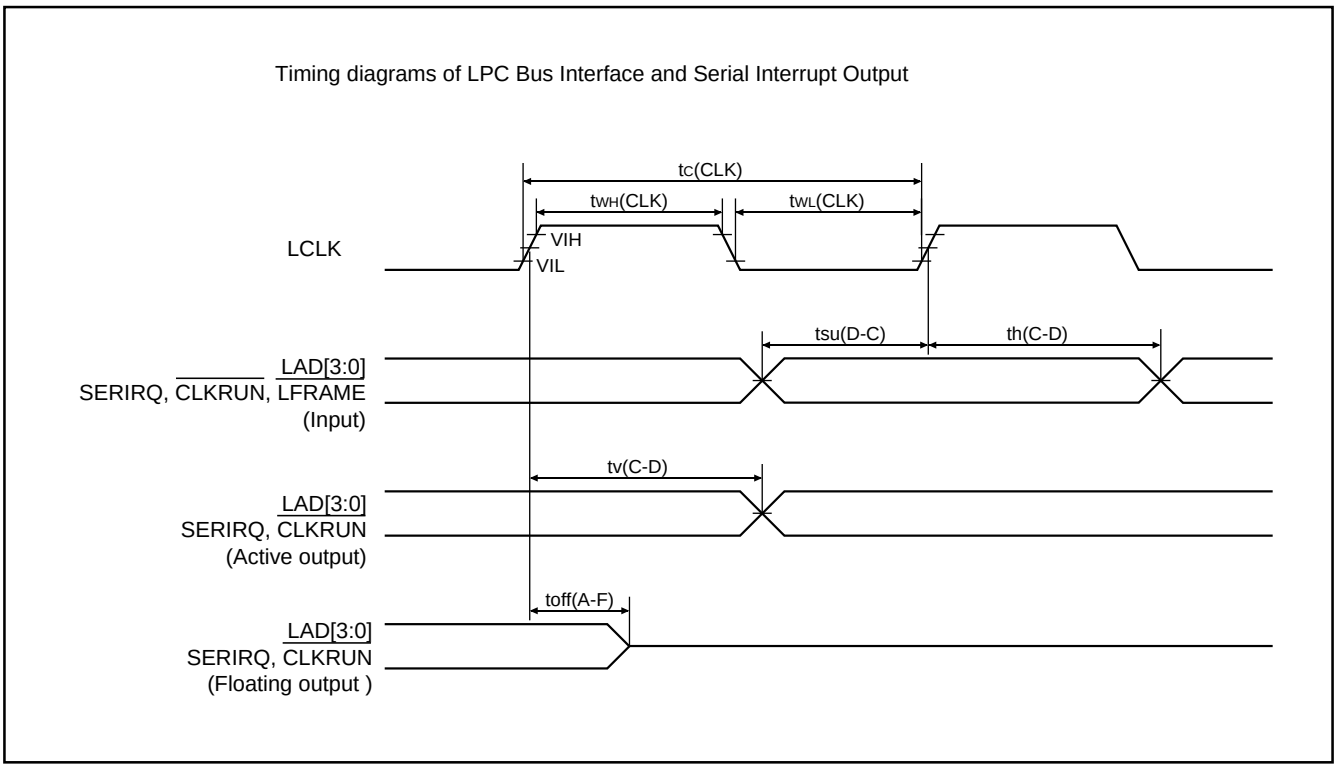


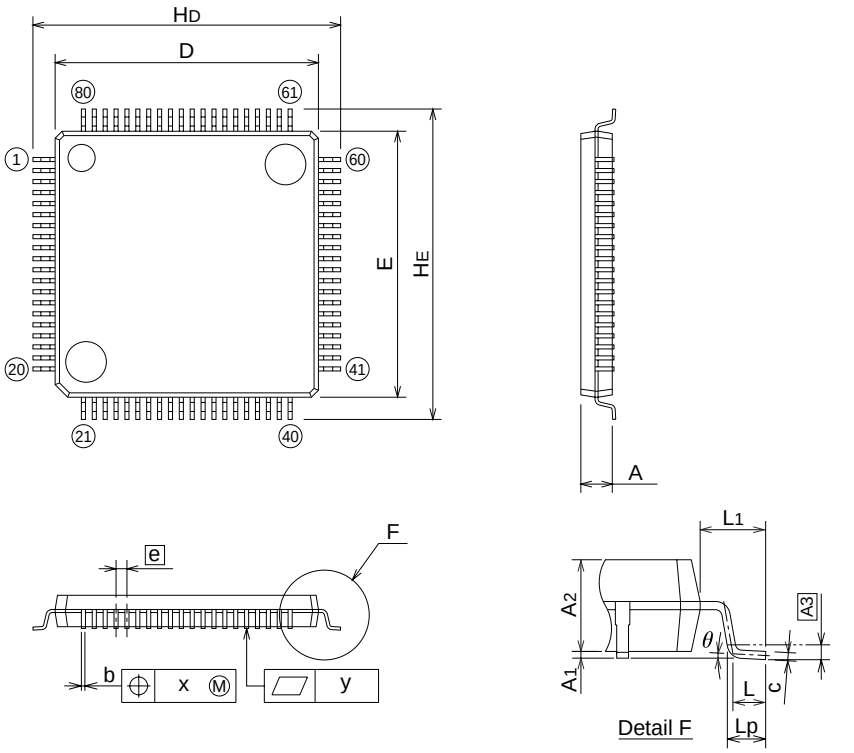
Fig. 86 Timing diagram of LPC Interface and Serialized IRQ

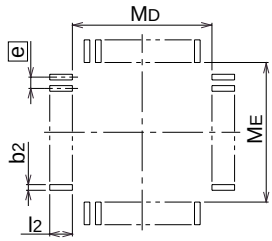
PACKAGE OUTLINE

80P6Q-A (MMP)

Plastic 80pin 12X12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	–	0.47	Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
L	0.3	0.5	0.7
L_1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	0.9	–	–
M_D	–	12.4	–
M_E	–	12.4	–

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REVISION HISTORY	3885 GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
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