# PLL102-05

## Low Skew Output Buffer

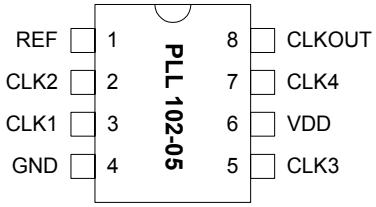
## FEATURES

- Frequency range 25 ~ 60MHz.
- Internal phase locked loop will allow spread spectrum modulation on reference clock to pass to the outputs (up to 100kHz SST modulation).
- Zero input - output delay.
- Less than 700 ps device - device skew.
- Less than 250 ps skew between outputs.
- Less than 150 ps cycle - cycle jitter.
- Output Enable function tri-state outputs.
- 3.3V operation.
- Available in 8-Pin 150mil SOIC.

## DESCRIPTION

The PLL102-05 is a high performance, low skew, low jitter zero delay buffer designed to distribute high speed clocks and is available in 8-pin SOIC package. It has four outputs that are synchronized with the input. The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than ±350 ps, the device acts as a zero delay buffer.

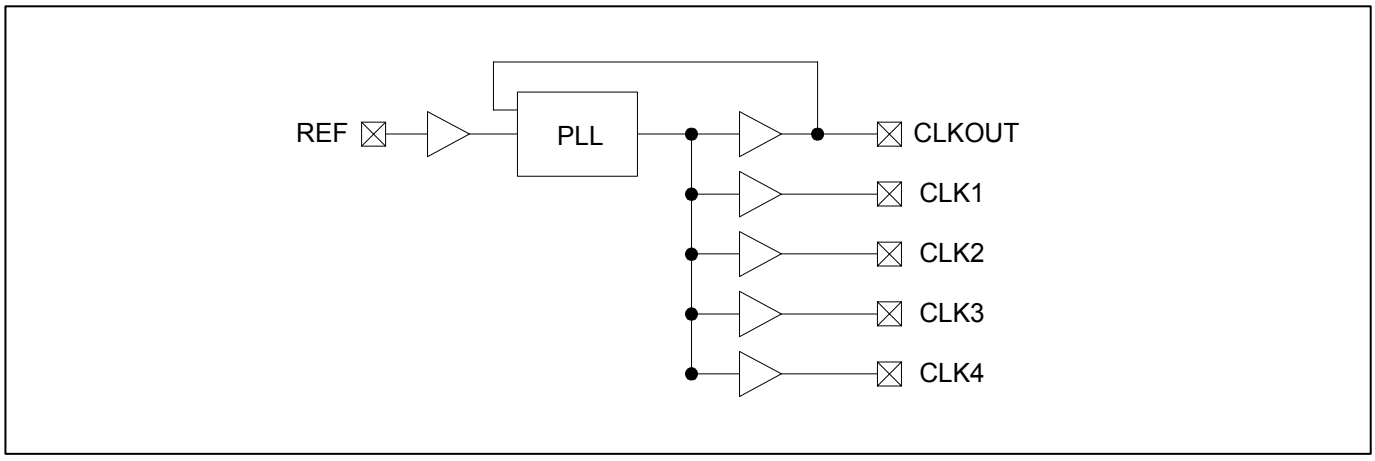
## PIN CONFIGURATION




### Remark

If REF clock is stopped for more than 10us after it has already been provided to the chip, and after power-up, the output clocks will disappear. In that instance, a full power-up reset is required in order to reactivate the output clocks.

## BLOCK DIAGRAM



## PIN DESCRIPTIONS

| Name | Number | Type | Description |
|---|---|---|---|
| REF[1] | 1 | I | Input reference frequency. Spread spectrum modulation on this signal will be passed to the output (up to 100kHz SST modulation). |
| CLK2[2] | 2 | O | Buffered clock output. |
| CLK1[2] | 3 | O | Buffered clock output. |
| GND | 4 | P | Ground. |
| CLK3[2] | 5 | O | Buffered clock output. |
| VDD | 6 | P | 3.3V Power Supply. |
| CLK4[2] | 7 | O | Buffered clock output. |
| CLKOUT[2] | 8 | O | Buffered clock output. Internal feed back on this pin. |

**Notes:** 1: Weak pull-down. 2: Weak pull-down on all outputs.

## ELECTRICAL SPECIFICATIONS

### 1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 4.6 | V |
| Input Voltage, dc | $V_I$ | -0.5 | $V_{DD}$+0.5 | V |
| Output Voltage, dc | $V_O$ | -0.5 | $V_{DD}$+0.5 | V |
| Storage Temperature | $T_S$ | -65 | 150 | °C |
| Ambient Operating Temperature* | $T_A$ | -40 | 85 | °C |
| Junction Temperature | $T_J$ | | 125 | °C |
| Lead Temperature (soldering, 10s) | | | 260 | °C |
| ESD Protection, Human Body Model | | | 2 | kV |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

### 2. Electrical Characteristics

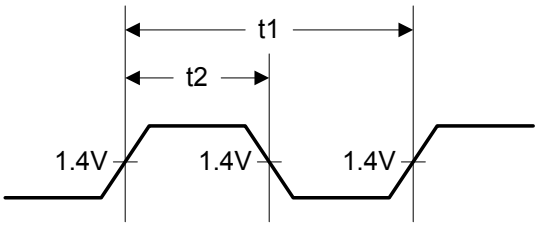
| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 2.97 | | 3.63 | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input High Voltage | $V_{IH}$ | | 2.0 | | | V |
| Input Low Current | $I_{IL}$ | $V_{IN}$ = 0V | | 19 | 50.0 | µA |
| Input High Current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | | 0.10 | 100.0 | µA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 50mA | | 0.25 | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = 50mA | 2.4 | 2.9 | | V |
| Power Down Supply Current | $I_{DD}$ | REF = 0MHz | | 0.3 | 50.0 | µA |
| Supply Current | $I_{DD}$ | Unloaded outputs at 133MHz, SEL inputs at $V_{DD}$ or GND | | 35 | 45 | mA |

## 3. Switching Characteristics

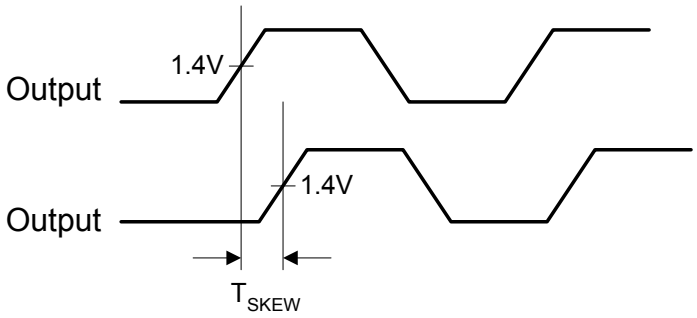
| PARAMETERS | SYMBOL | DESCRIPTION | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Output Frequency | t1 | | 25 | | 60 | MHz |
| Duty Cycle ( t2 ÷ t1 ) | Dt1 | Measured at 1.4V, $C_L$=30pF, $F_{out}$ = 60MHz | 40.0 | 50.0 | 60.0 | % |
| Duty Cycle ( t2 ÷ t1 ) | Dt2 | Measured at 1.4V | 45.0 | 50.0 | 55.0 | % |
| Rise Time | $T_r$ | Measured between 0.8V and 2.0V, $C_L$=30pF | | 1.2 | 1.5 | ns |
| Fall Time | $T_f$ | Measured between 2.0V and 0.8V, $C_L$=30pF | | 1.2 | 1.5 | ns |
| Output to Output Skew | $T_{skew}$ | All outputs equally loaded, $C_L$=20pF | | | 250 | ps |
| Delay, REF Rising Edge to CLKOUT Rising Edge | $T_{delay}$ | Measured at 1.4V | | 0 | ±350 | ps |
| Device to Device Skew | $T_{dsk-dsk}$ | Measured at $V_{DD}$/2 on the CLKOUT pins of devices | | 0 | 700 | ps |
| Cycle to Cycle Jitter | $T_{cyc-cyc}$ | Loaded outputs | | | 150 | ps |
| PLL Lock Time | $T_{lock}$ | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |
| Jitter; Absolute Jitter | $T_{jabs}$ | At 10,000 cycles, $C_L$=30pF | | 70 | 100 | ps |
| Jitter; 1-sima | $T_{j1-s}$ | At 10,000 cycles, $C_L$=30pF | | 10 | 20 | ps |

## SWITCHING WAVEFORMS

### Duty Cycle Timing

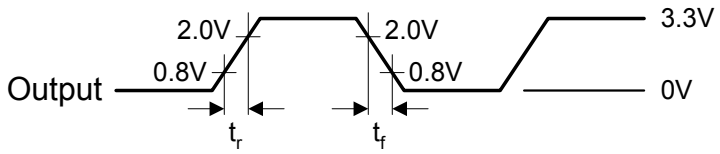



### Output - Output Skew

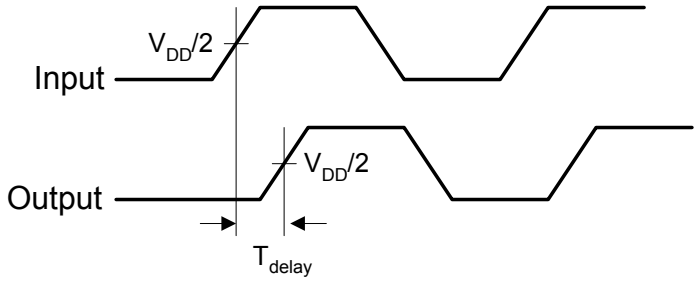


## SWITCHING WAVE FORMS

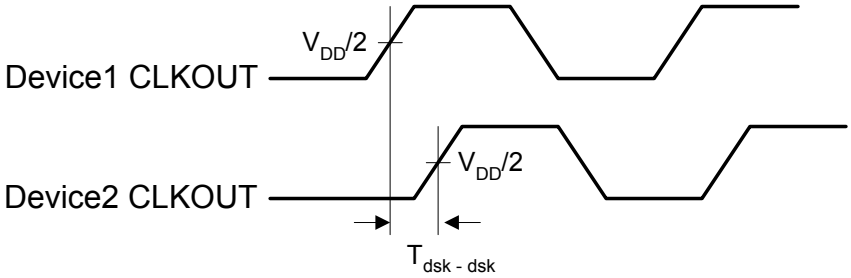
All Outputs Rise/Fall Time




Input to Output Propagation Delay




Device to Device Skew



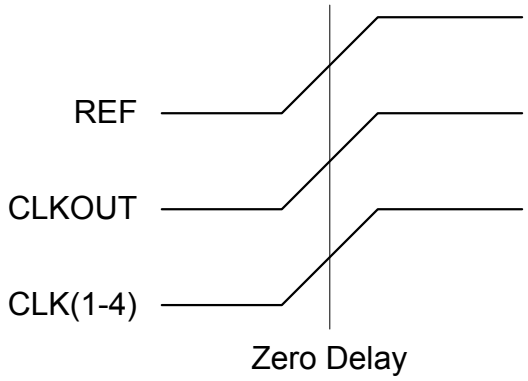
### Output-Output Skew

The skew between CLKOUT and the CLK(1-4) outputs is not dynamically adjusted by the PLL. Since CLKOUT is one of the inputs to the PLL, zero phase difference is maintained from REF to CLKOUT. If all outputs are equally loaded, zero phase difference will maintained from REF to all outputs.

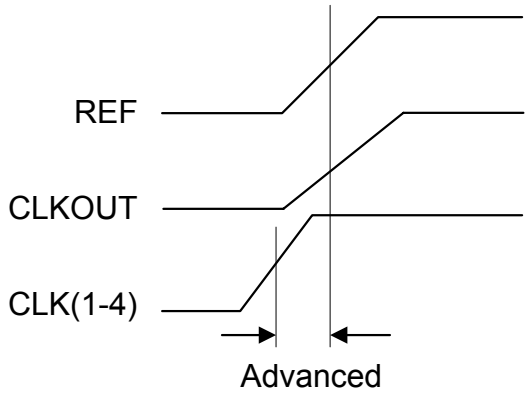
If applications requiring zero output-output skew, all the outputs must equally loaded.

If the CLK(1-4) outputs are less loaded than CLKOUT, CLK(1-4) outputs will lead it; if the CLK(0-4) is more loaded than CLKOUT, CLK(1-4) will lag the CLKOUT.

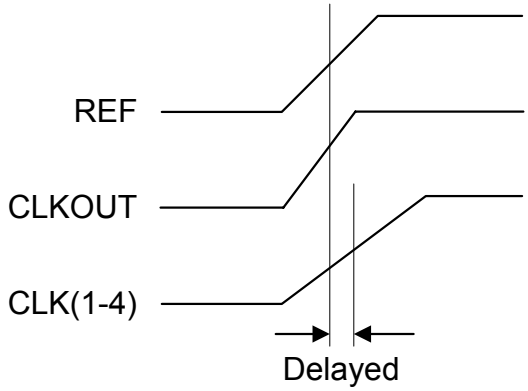
Since the CLKOUT and the CLK(1-4) outputs are identical, they all start at the same time, but difference loads cause them to have different rise times and different times crossing the measurement thresholds.




REF input and all outputs loaded equally




REF input and CLK(1-4) outputs loaded equally, with CLK(1-4) less loaded than CLKOUT.

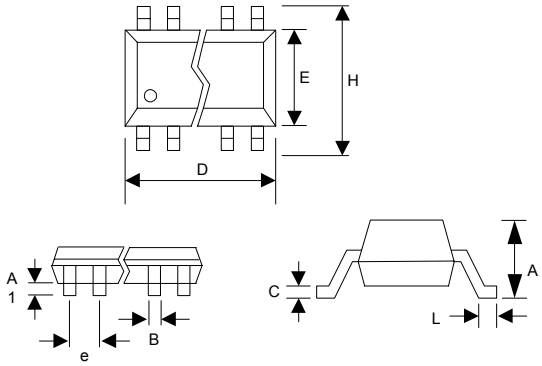



REF input and CLK(1-4) outputs loaded equally, with CLK(1-4) more loaded than CLKOUT.

## PACKAGE INFORMATION

8 PIN Narrow SOIC ( mm )

| | SOIC | |
|---|---|---|
| Symbol | Min. | Max. |
| A | 1.55 | 1.73 |
| A1 | 0.15 | 0.18 |
| B | 0.35 | 0.49 |
| C | 0.19 | 0.25 |
| D | 4.80 | 4.98 |
| E | 3.81 | 3.99 |
| H | 5.84 | 6.20 |
| L | 0.41 | 0.89 |
| e | 1.27 BSC | |




## ORDERING INFORMATION

***For part ordering, please contact our Sales Department:***
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

***PART NUMBER***

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

**PLL102-05 X X X X**

*PART NUMBER*

NONE= TUBE
R=TAPE AND REEL

NONE=NORMAL PACKAGE
L=GREEN PACKAGE

PACKAGE TYPE
S=SOIC

TEMPERATURE
C=COMMERCIAL,
I=INDUSTRIAL

| Part / Order Number | Marking | Package Option | Temperature |
|---|---|---|---|
| PLL102-05SC-R | P102-05SC | SOIC - Tape and Reel | 0 to +70° C |
| PLL102-05SC | P102-05SC | SOIC – Tube | 0 to +70° C |
| PLL102-05SCL-R | P102-05SCL | SOIC - Tape and Reel | 0 to +70° C |
| PLL102-05SCL | P102-05SCL | SOIC – Tube | 0 to +70° C |

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