



**PRELIMINARY**

**CY7C1061G/CY7C1061GE**

**16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC)**

**Features**

- High speed
  - $t_{AA} = 10 \text{ ns}/15 \text{ ns}$
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
  - $I_{CC} = 90\text{-mA}$  typical at 100 MHz
  - $I_{SB2} = 20\text{-mA}$  typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages

**Functional Description**

CY7C1061G and CY7C1061GE are high-performance CMOS fast static RAM devices with embedded ECC<sup>[1]</sup>. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY7C1061GE device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access devices with a single chip enable input, assert the chip enable (CE) input LOW. To access dual chip enable devices, assert both chip enable inputs – CE<sub>1</sub> as LOW and CE<sub>2</sub> as HIGH.

To perform data writes, assert the Write Enable ( $\overline{WE}$ ) input LOW, and provide the data and address on the device data pins (I/O<sub>0</sub> through I/O<sub>15</sub>) and address pins (A<sub>0</sub> through A<sub>19</sub>) respectively. The Byte High and Byte Low Enable (BHE, BLE) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. BHE controls I/O<sub>8</sub> through I/O<sub>15</sub> and BLE controls I/O<sub>0</sub> through I/O<sub>7</sub>.

To perform data reads, assert the Output Enable ( $\overline{OE}$ ) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O<sub>0</sub> through I/O<sub>15</sub>). You can perform byte accesses by asserting the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected (CE HIGH for a single chip enable device and CE<sub>1</sub> HIGH / CE<sub>2</sub> LOW for a dual chip enable device), or control signals are de-asserted ( $\overline{OE}$ , BLE, BHE).

On the CY7C1061GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the [Truth Table on page 16](#) for a complete description of read and write modes.

The logic block diagrams are on page 2.

The CY7C1061G and CY7C1061GE devices are available in 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages.

For a complete list of related documentation, click [here](#).

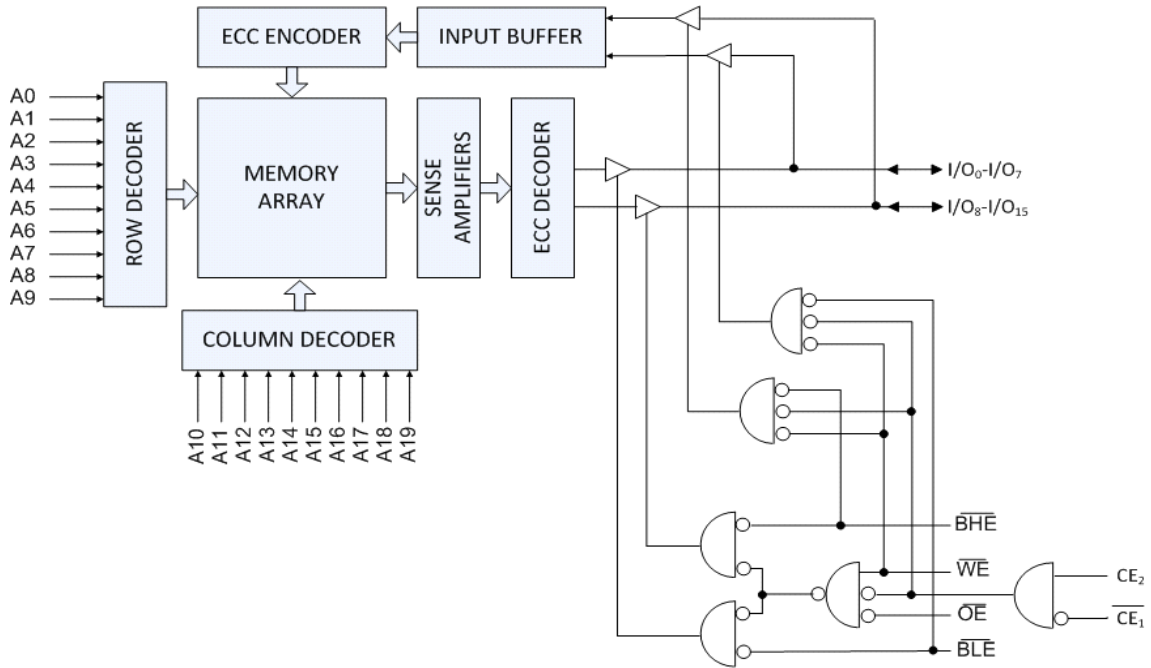
**Product Portfolio**

Product	Features and Options (see the Pin Configurations section)	Range	V <sub>CC</sub> Range (V)	Speed (ns) 10/15	Current Consumption			
					Operating I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (mA)	
					f = f <sub>max</sub>			
					Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY7C1061G18	Single or dual chip enables  Optional ERR pins  Address MSB A <sub>19</sub> pin placement options compatible with Cypress and other vendors	Industrial	1.65 V–2.2 V	15	70	80	20	30
CY7C1061G(E)30			2.2 V–3.6 V	10	90	110		
CY7C1061G			4.5 V–5.5 V	10	90	110		

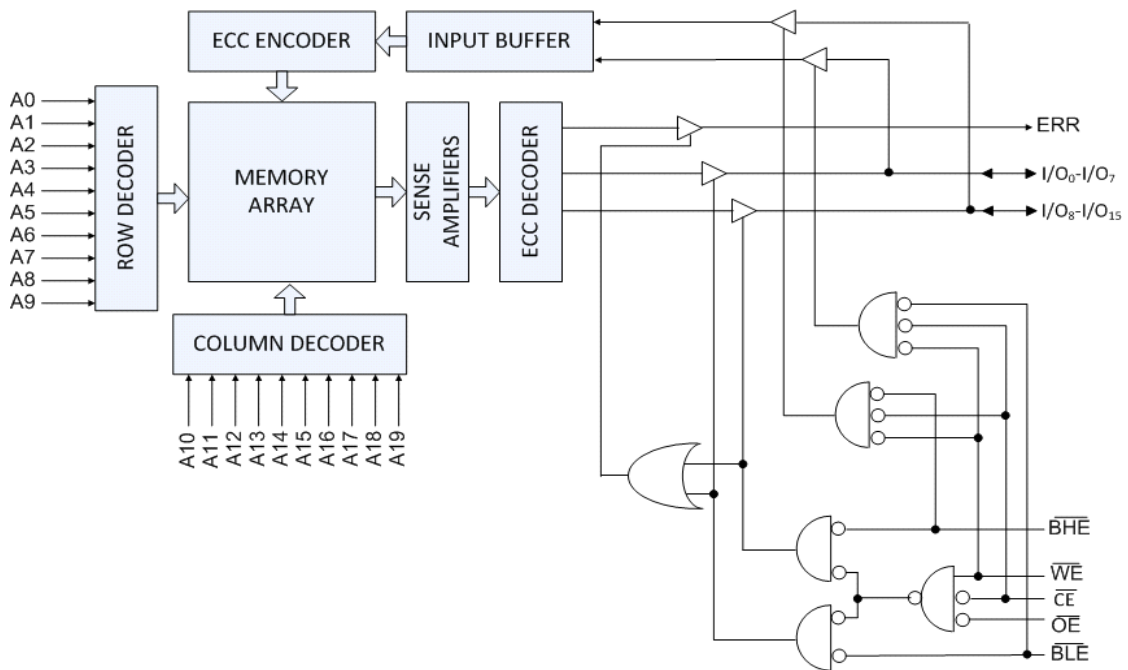
**Notes**

1. This device does not support automatic write-back on error detection.
2. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for a V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for a V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for a V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

**Logic Block Diagram – CY7C1061G**



**Logic Block Diagram – CY7C1061GE**

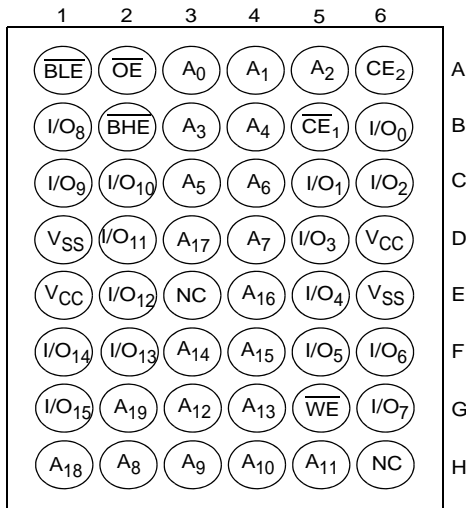


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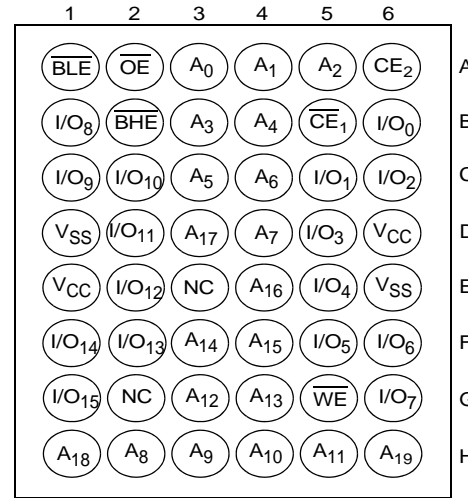
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**Pin Configurations**

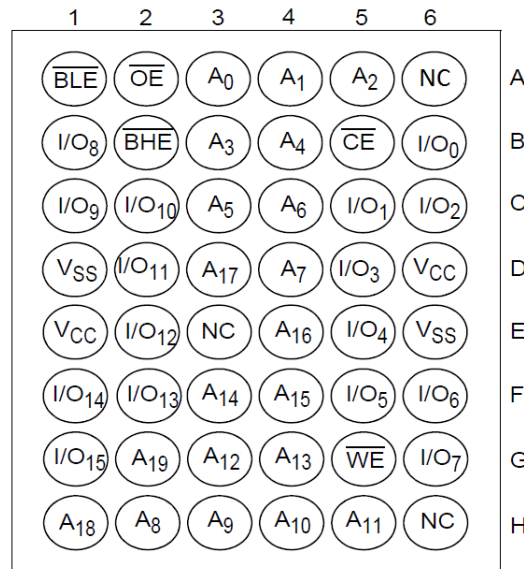
**Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm)**  
 Dual Chip Enable without ERR, Address MSB A19 at Ball G2,  
 CY7C1061G<sup>[3]</sup> Package/Grade ID: BVJXI



**Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm)**  
 Dual Chip Enable without ERR, Address MSB A19 at Ball H6,  
 CY7C1061G<sup>[3]</sup> Package/Grade ID: BVXI



**Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G<sup>[3]</sup>**  
 Package/Grade ID: BV1XI

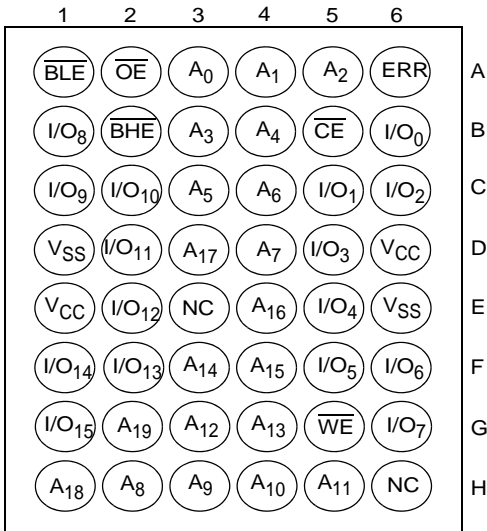


**Note**

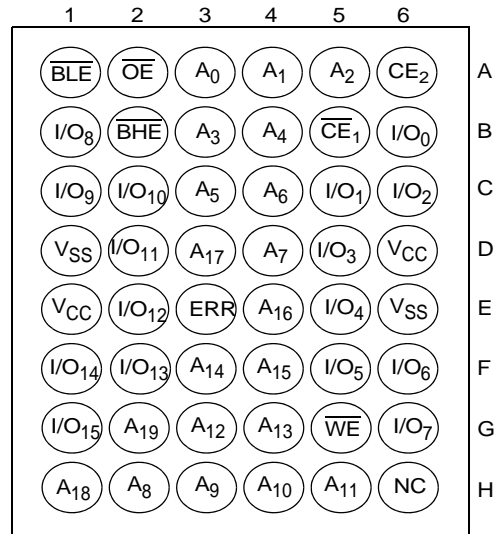
3. NC pins are not connected internally to the die.

**Pin Configurations** (continued)

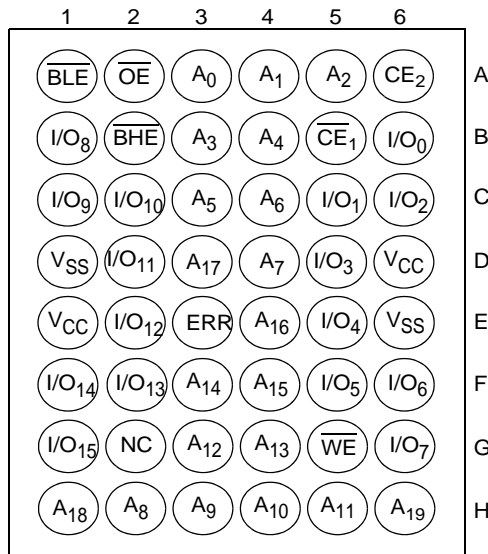
**Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm)**  
**Single Chip Enable with ERR, Address MSB A19 at Ball G2**  
**CY7C1061GE<sup>[4, 5]</sup> Package/Grade ID: BV1XI**



**Figure 5. 48-ball VFBGA (6 × 8 × 1.0 mm)**  
**Dual Chip Enable with ERR, Address MSB A19 at Ball G2**  
**CY7C1061GE<sup>[4, 5]</sup> Package/Grade ID: BVJXI**



**Figure 6. 48-ball VFBGA (6 × 8 × 1.0 mm) Dual Chip Enable with ERR, Address MSB A19 at Ball H6**  
**CY7C1061GE<sup>[4, 5]</sup> Package/Grade ID: BVXI**



**Notes**

- 4. NC pins are not connected internally to the die.
- 5. ERR is an Output pin. If not used, this pin should be left floating.



**Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

- Storage temperature ..... -65 °C to +150 °C
- Ambient temperature with power applied ..... -55 °C to +125 °C
- Supply voltage on  $V_{CC}$  relative to GND ..... -0.5 V to +6.0 V
- DC voltage applied to outputs in High Z State <sup>[8]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

- DC input voltage<sup>[8]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V
- Current into outputs (LOW) ..... 20 mA
- Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V
- Latch-up current ..... > 140 mA

**Operating Range**

Grade	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

**DC Electrical Characteristics**

Over the operating range of -40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit	
			Min	Typ <sup>[10]</sup>	Max		
$V_{OH}$	Output HIGH voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	1.4	-	-	V	
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.0	-	-		
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.2	-	-		
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	-		
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	$V_{CC} - 0.4$ <sup>[11]</sup>	-	-		
$V_{OL}$	Output LOW voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	-	-	0.2	V	
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$	-	-	0.4		
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	-	-	0.4		
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	-	-	0.4		
$V_{IH}$ <sup>[8]</sup>	Input HIGH voltage	1.65 V to 2.2 V	1.4	-	$V_{CC} + 0.2$	V	
		2.2 V to 2.7 V	2.0	-	$V_{CC} + 0.3$		
		2.7 V to 3.6 V	2.0	-	$V_{CC} + 0.3$		
		4.5 V to 5.5 V	2.2	-	$V_{CC} + 0.5$		
$V_{IL}$ <sup>[8]</sup>	Input LOW voltage	1.65 V to 2.2 V	-0.2	-	0.4	V	
		2.2 V to 2.7 V	-0.3	-	0.6		
		2.7 V to 3.6 V	-0.3	-	0.8		
		4.5 V to 5.5 V	-0.5	-	0.8		
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1.0	-	+1.0	$\mu\text{A}$	
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1.0	-	+1.0	$\mu\text{A}$	
$I_{CC}$	Operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}$ , CMOS levels	f = 100 MHz	-	90.0	110.0	mA
			f = 66.7 MHz	-	70.0	80.0	
$I_{SB1}$	Automatic CE power down current – TTL inputs	$\text{Max } V_{CC}, \overline{CE} \geq V_{IH}$ <sup>[9]</sup> , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , f = $f_{MAX}$	-	-	40.0	mA	
$I_{SB2}$	Automatic CE power down current – CMOS inputs	$\text{Max } V_{CC}, \overline{CE} \geq V_{CC} - 0.2 \text{ V}$ <sup>[9]</sup> , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ , f = 0	-	20.0	30.0	mA	

**Notes**

8.  $V_{IL(\text{min})} = -2.0 \text{ V}$  and  $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$  for pulse durations of less than 2 ns.
9. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
10. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8 \text{ V}$  (for a  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3 \text{ V}$  (for a  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC} = 5 \text{ V}$  (for a  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25 \text{ }^\circ\text{C}$ .
11. This parameter is guaranteed by design and is not tested

### Capacitance

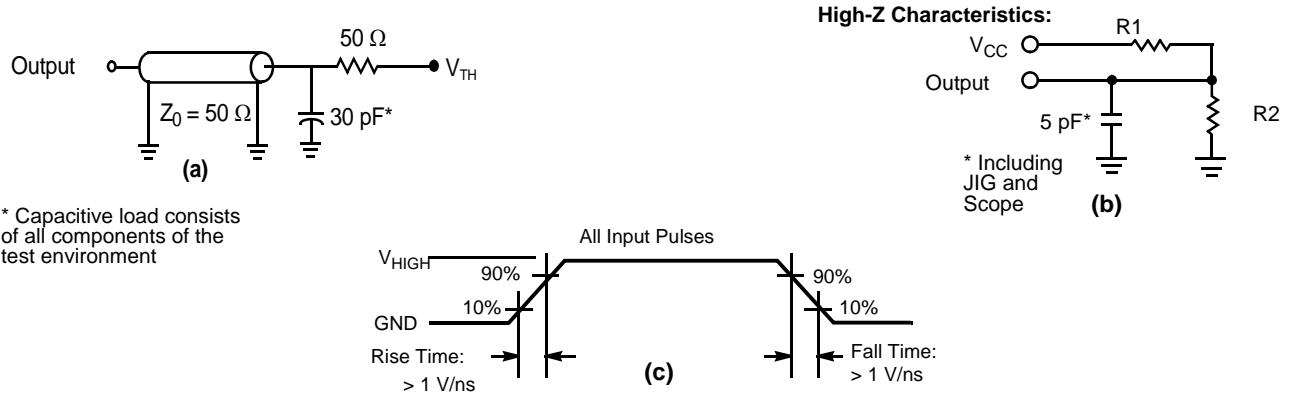
Parameter <sup>[12]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	10	10	pF
C <sub>OUT</sub>	I/O capacitance		10	10	10	pF

### Thermal Resistance

Parameter <sup>[12]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	93.63	31.50	57.99	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		21.58	15.75	13.42	°C/W

### AC Test Loads and Waveforms

Figure 11. AC Test Loads and Waveforms<sup>[13]</sup>



\* Capacitive load consists of all components of the test environment

Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V <sub>TH</sub>	0.9	1.5	1.5	V
V <sub>HIGH</sub>	1.8	3	3	V

#### Notes

12. Tested initially and after any design or process changes that may affect these parameters.

13. Full-device AC operation assumes a 100-μs ramp time from 0 to V<sub>CC</sub> (min) and 100-μs wait time after V<sub>CC</sub> stabilizes to its operational value.



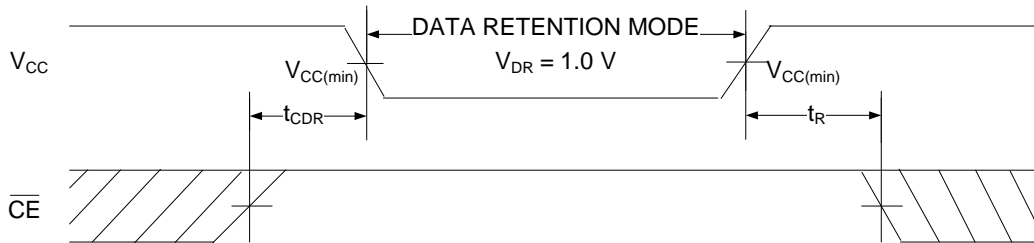
### Data Retention Characteristics

Over the operating range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}^{[14]}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	30.0	mA
$t_{CDR}^{[15]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[15, 16]}$	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10.0	–	ns
		$V_{CC} < 2.2\text{ V}$	15.0	–	ns

### Data Retention Waveform

**Figure 12. Data Retention Waveform** <sup>[14]</sup>



**Notes**

- 14. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 15. This parameter is guaranteed by design and is not tested
- 16. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$ .

## AC Switching Characteristics

Over the operating range of -40 °C to 85 °C

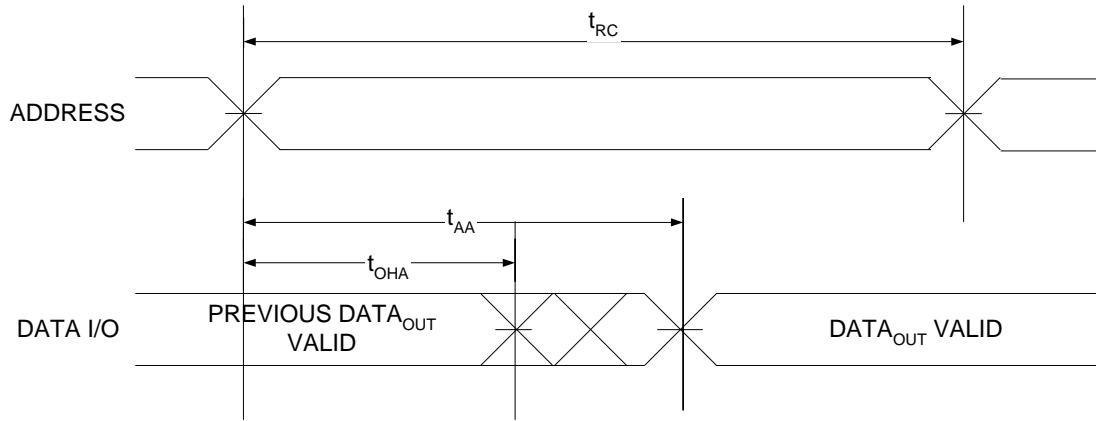
Parameter <sup>[17]</sup>	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
t <sub>POWER</sub>	V <sub>CC</sub> (stable) to the first access <sup>[18, 19]</sup>	100.0	–	100.0	–	µs
t <sub>RC</sub>	Read cycle time	10.0	–	15.0	–	ns
t <sub>AA</sub>	Address to data / ERR valid	–	10.0	–	15.0	ns
t <sub>OHA</sub>	Data / ERR hold from address change	3.0	–	3.0	–	ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to data / ERR valid <sup>[20]</sup>	–	10.0	–	15.0	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data / ERR valid	–	5.0	–	8.0	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to low Z <sup>[21, 22, 23]</sup>	0	–	1.0	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to high Z <sup>[21, 22, 23]</sup>	–	5.0	–	8.0	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to low Z <sup>[20, 21, 22, 23]</sup>	3.0	–	3.0	–	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to high Z <sup>[20, 21, 22, 23]</sup>	–	5.0	–	8.0	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to power-up <sup>[19, 20]</sup>	0	–	0	–	ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to power-down <sup>[19, 20]</sup>	–	10.0	–	15.0	ns
t <sub>DBE</sub>	Byte enable to data valid	–	5.0	–	8.0	ns
t <sub>LZBE</sub>	Byte enable to low Z <sup>[21, 22]</sup>	0	–	1.0	–	ns
t <sub>HZBE</sub>	Byte disable to high Z <sup>[21, 22]</sup>	–	6.0	–	8.0	ns
<b>Write Cycle <sup>[24, 25]</sup></b>						
t <sub>WC</sub>	Write cycle time	10.0	–	15.0	–	ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to write end <sup>[20]</sup>	7.0	–	12.0	–	ns
t <sub>AW</sub>	Address setup to write end	7.0	–	12.0	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	7.0	–	12.0	–	ns
t <sub>SD</sub>	Data setup to write end	5.0	–	8.0	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	0	–	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to low Z <sup>[21, 22, 23]</sup>	3.0	–	3.0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to high Z <sup>[21, 22, 23]</sup>	–	5.0	–	8.0	ns
t <sub>BW</sub>	Byte Enable to write end	7.0	–	12.0	–	ns

### Notes

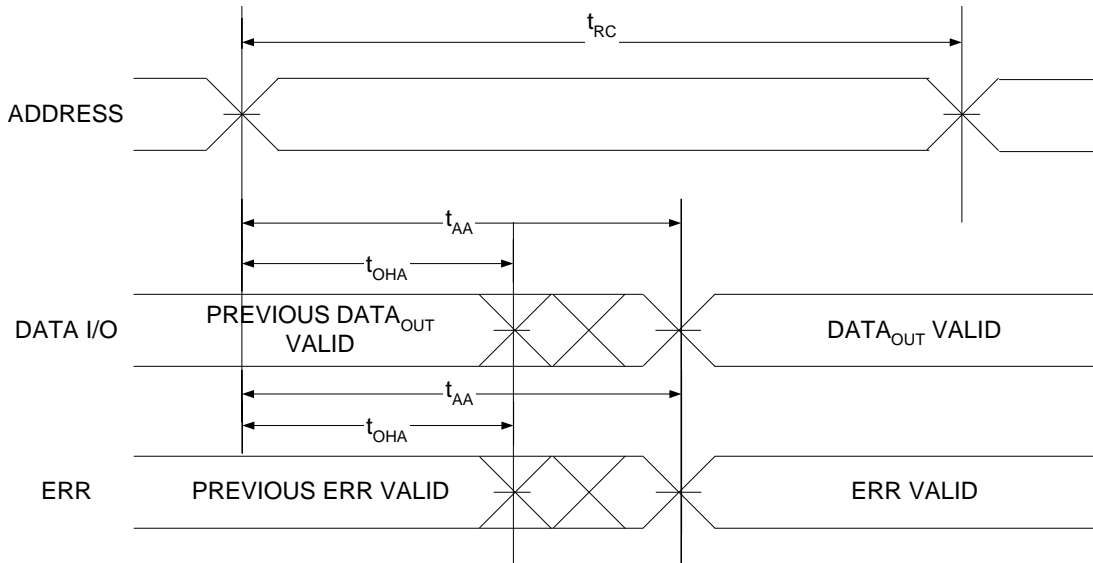
17. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for V<sub>CC</sub> ≥ 3 V) and V<sub>CC</sub>/2 (for V<sub>CC</sub> < 3 V), and input pulse levels of 0 to 3 V (for V<sub>CC</sub> ≥ 3 V) and 0 to V<sub>CC</sub> (for V<sub>CC</sub> < 3 V). Test conditions for the read cycle use the output loading, shown in part (a) of Figure 11 on page 8, unless specified otherwise.
18. t<sub>POWER</sub> gives the minimum amount of time that the power supply is at stable V<sub>CC</sub> until the first memory access is performed.
19. These parameters are guaranteed by design and are not tested.
20. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and CE<sub>2</sub>. When  $\overline{CE}_1$  is LOW and CE<sub>2</sub> is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or CE<sub>2</sub> is LOW,  $\overline{CE}$  is HIGH.
21. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZWE</sub>, and t<sub>HZBE</sub> are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 11 on page 8. Hi-Z, Lo-Z transition is measured ±200 mV from steady state voltage.
22. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
23. Tested initially and after any design or process changes that may affect these parameters.
24. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ , and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
25. The minimum write pulse width for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Switching Waveforms**

**Figure 13. Read Cycle No. 1 of CY7C1061G (Address Transition Controlled)** [26, 27]



**Figure 14. Read Cycle No. 2 of CY7C1061GE (Address Transition Controlled)** [26, 27]

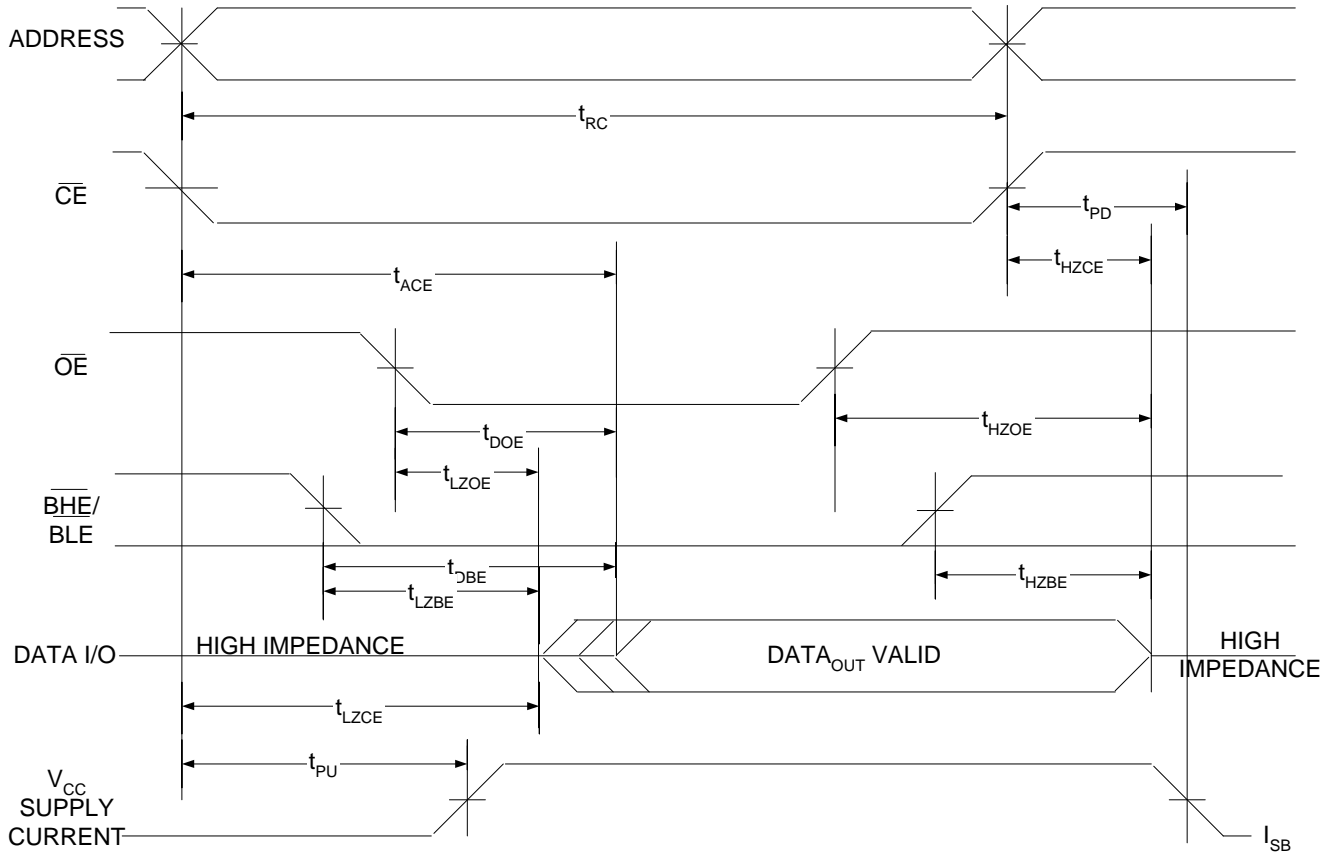


**Notes**

- 26. The device is continuously selected,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ .
- 27.  $\overline{WE}$  is HIGH for read cycle.

Switching Waveforms (continued)

Figure 15. Read Cycle No. 3 ( $\overline{OE}$  Controlled) [28, 29, 30]



Notes

- 28. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 29.  $\overline{WE}$  is HIGH for read cycle.
- 30. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.

Switching Waveforms (continued)

Figure 16. Write Cycle No. 1 ( $\overline{CE}$  Controlled) [31, 32, 33]

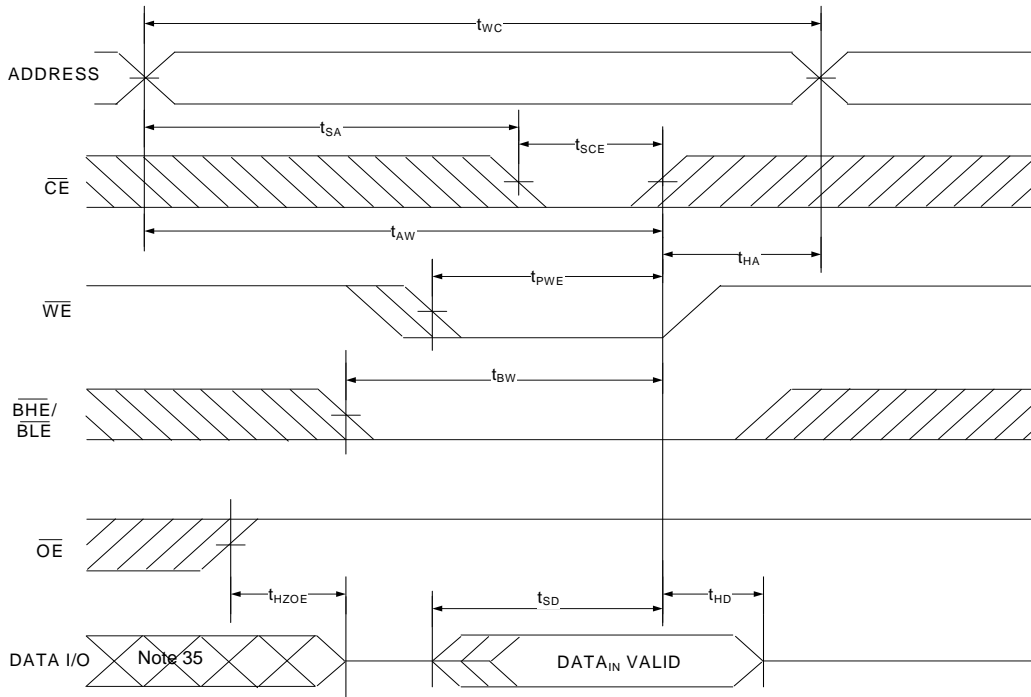
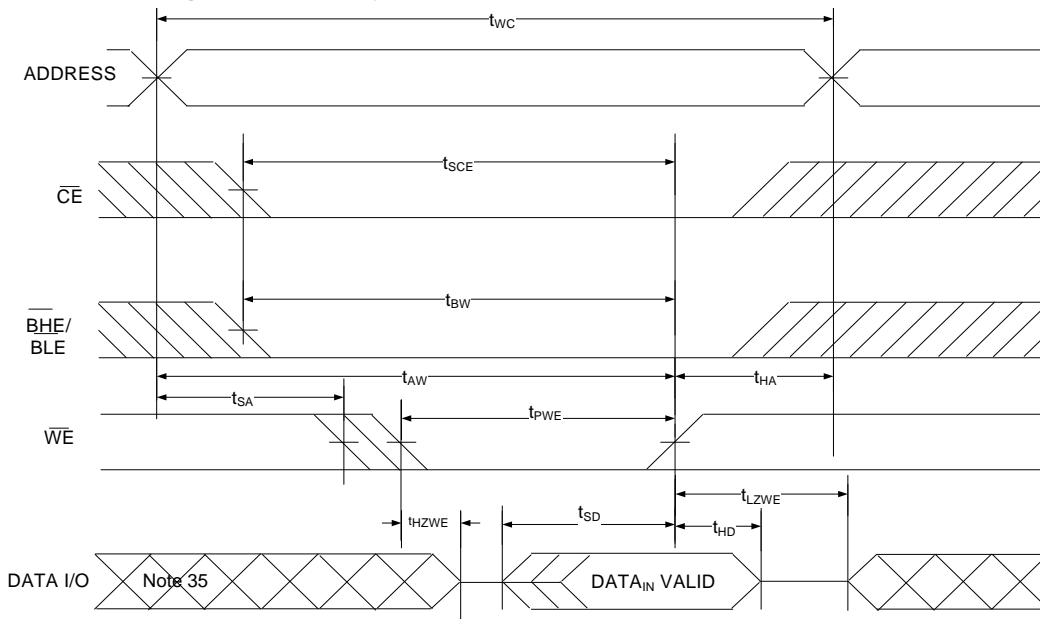


Figure 17. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [31, 32, 33, 34]

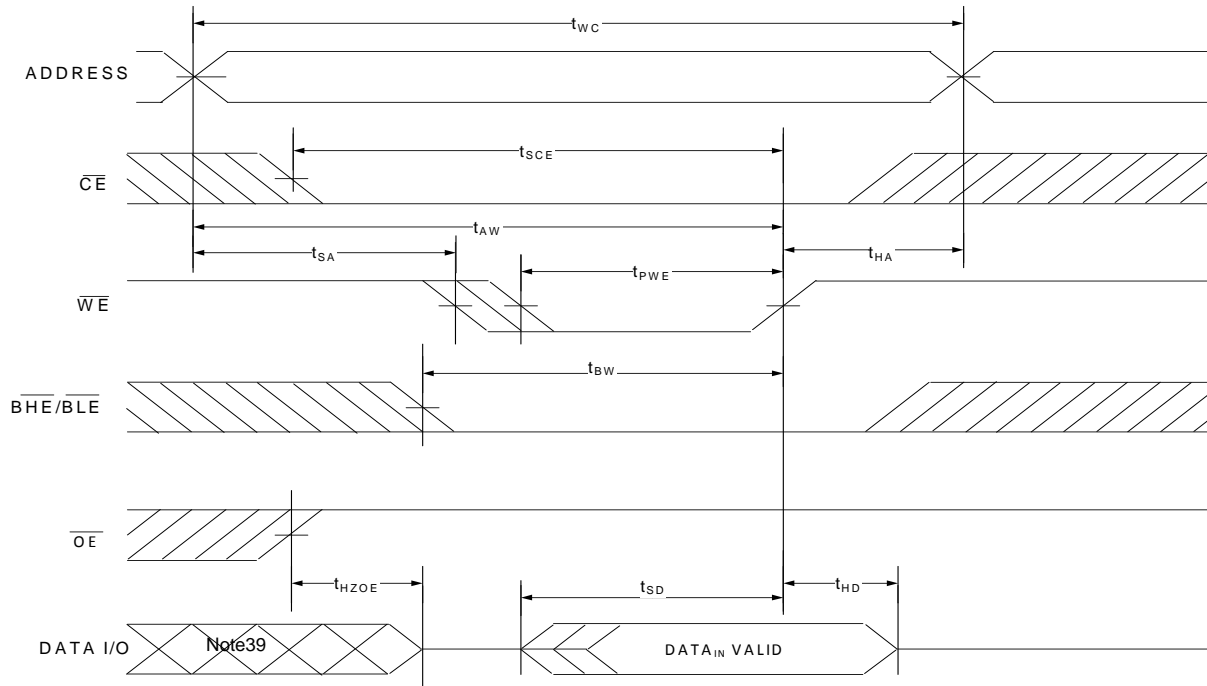


Notes

- 31. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 32. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 33. Data I/O is in high impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
- 34. The minimum write cycle pulse width should be equal to sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 35. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 18. Write Cycle No. 3 ( $\overline{WE}$  controlled)<sup>[36, 37, 38]</sup>

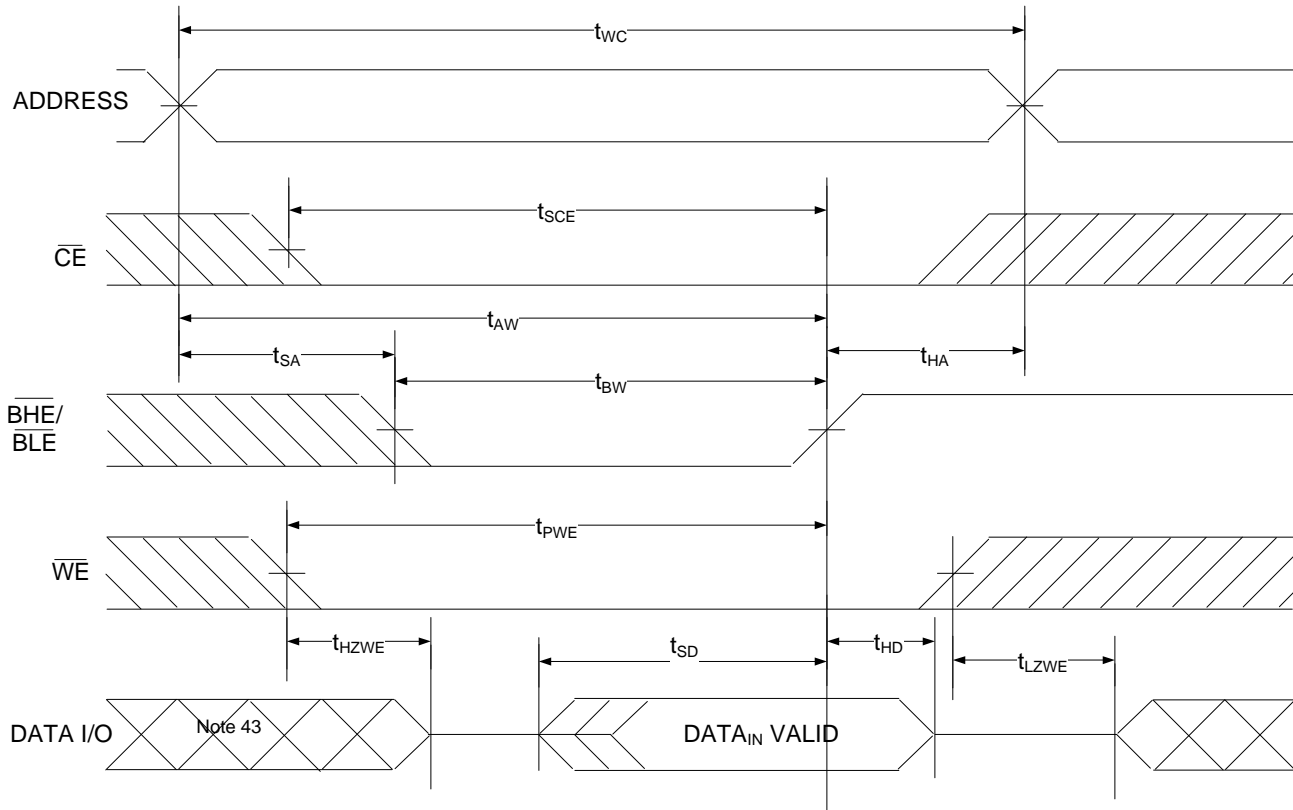


Notes

- 36. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 37. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 38. Data I/O is in high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
- 39. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 19. Write Cycle No. 4 (BLE or BHE Controlled) [40, 41, 42]



Notes

- 40. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 41. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 42. Data I/O is in high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
- 43. During this period, the I/Os are in output state. Do not apply input signals.

**Truth Table**

$\overline{CE}$ [44]	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X <sup>[45]</sup>	X <sup>[45]</sup>	X <sup>[45]</sup>	X <sup>[45]</sup>	High-Z	High-Z	Power down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data out	High-Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	H	H	L	High-Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data in	High-Z	Write lower bits only	Active (I <sub>CC</sub> )
L	X	L	H	L	High-Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

**ERR Output – CY7C1061GE**

Output [46]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected or outputs disabled or Write operation

**Notes**

44. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

45. The input voltage levels on these pins should be either at  $V_{IH}$  or  $V_{IL}$ .

46. ERR is an Output pin. If not used, this pin should be left floating.

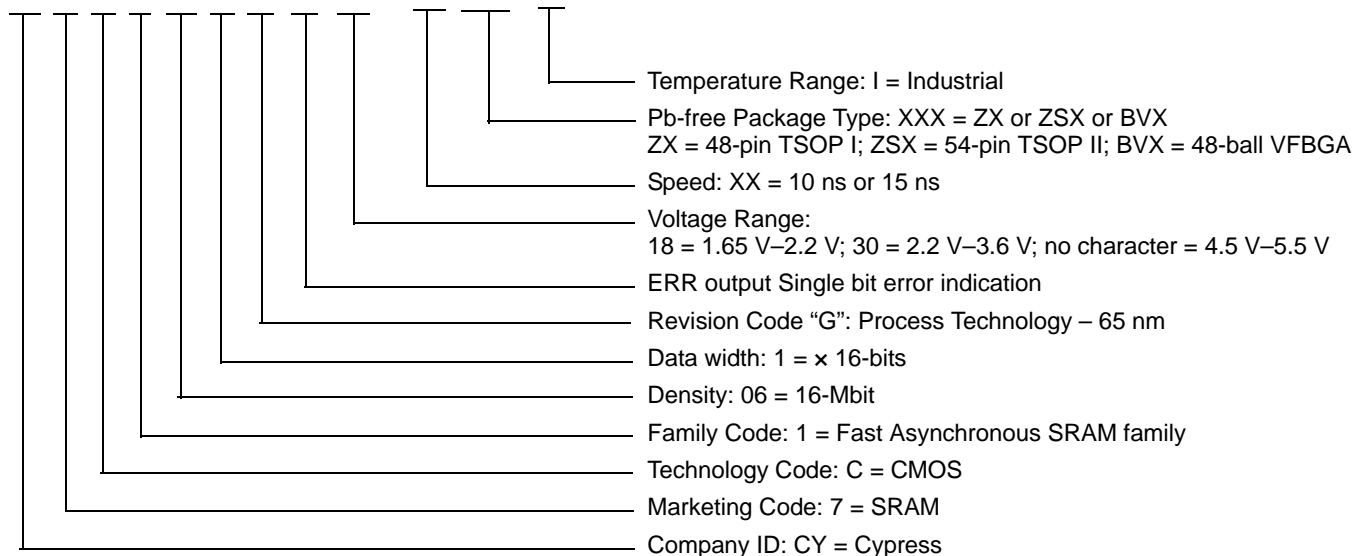


**Ordering Information**

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Key Features / Differentiators	Operating Range
10	2.2 V–3.6 V	CY7C1061G30-10ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1.0 mm)	Single Chip Enable without ERR	Industrial
		CY7C1061GE30-10ZXI			Single Chip Enable with ERR output at pin 6	
		CY7C1061G30-10ZSXI	51-85160	54-pin TSOP II (22.4 × 11.84 × 1.0 mm)	Dual Chip Enable without ERR	
		CY7C1061GE30-10ZSXI			Dual Chip Enable with ERR output at pin 43	
		CY7C1061G30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free)	Dual Chip Enable without ERR Address MSB A <sub>19</sub> at ball H6	
		CY7C1061GE30-10BVXI			Dual Chip Enable with ERR output at ball E3 Address MSB A <sub>19</sub> at ball H6	
		CY7C1061G30-10BV1XI			Single Chip Enable without ERR Address MSB A <sub>19</sub> at ball G2	
		CY7C1061G30-10BVJXI			Dual Chip Enable without ERR Address MSB A <sub>19</sub> at ball G2	
15	1.65 V–2.2 V	CY7C1061G18-15BV1XI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free)	Single Chip Enable without ERR Address MSB A <sub>19</sub> at ball G2	

**Ordering Code Definitions**

CY 7 C 1 06 1 G E XX - XX XXX I

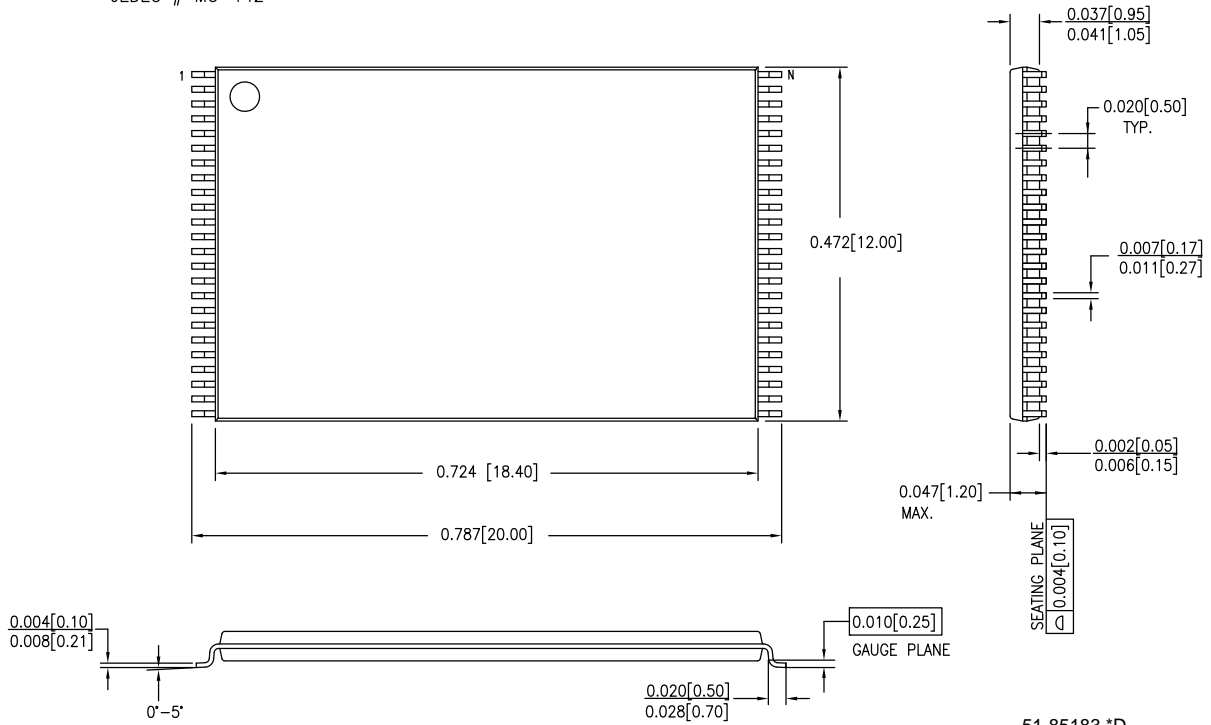


**Package Diagrams**

**Figure 20. 48-pin TSOP I (12 x 18.4 x 1.0 mm) Z48A Package Outline, 51-85183**

DIMENSIONS IN INCHES[MM]  $\frac{\text{MIN.}}{\text{MAX.}}$

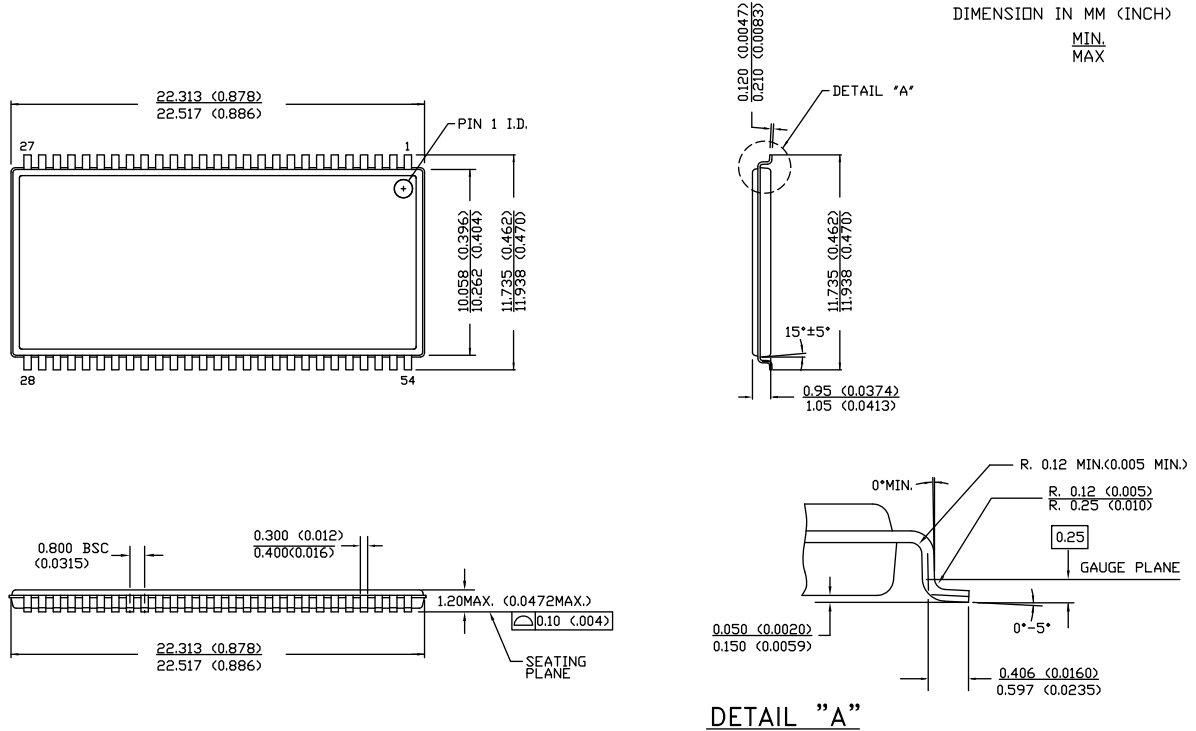
JEDEC # MO-142



51-85183 \*D

**Package Diagrams** (continued)

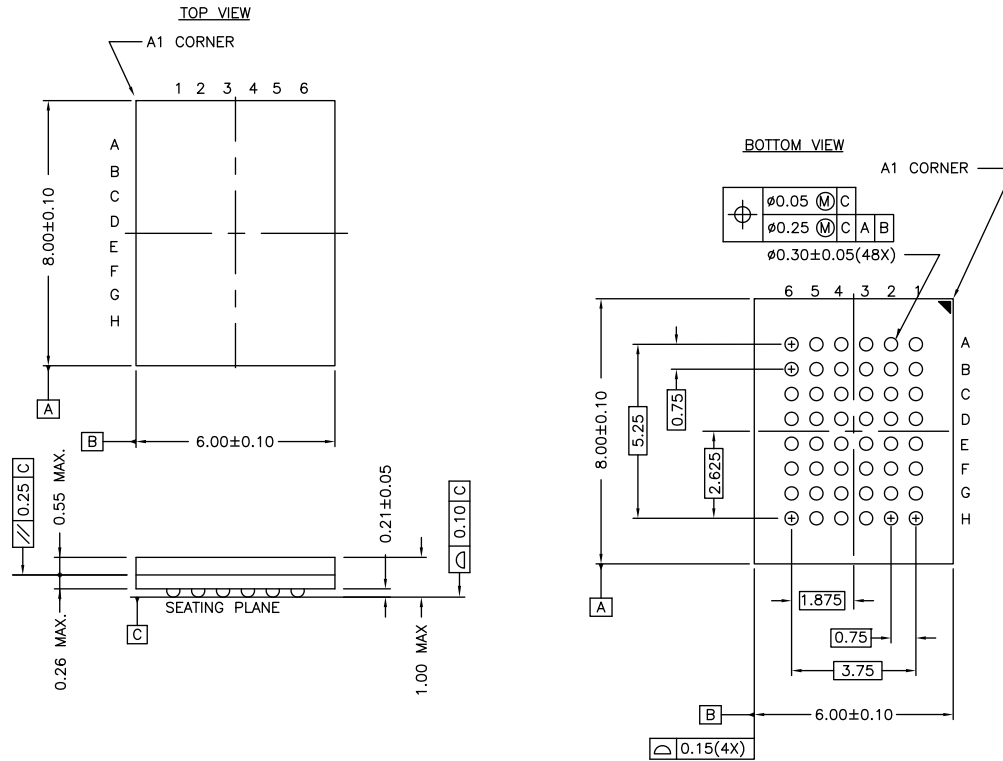
**Figure 21. 54-pin TSOP II (22.4 x 11.84 x 1.0 mm) Z54-II Package Outline, 51-85160**



51-85160 \*E

**Package Diagrams** (continued)

**Figure 22. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



NOTE:  
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H

**Acronyms**

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
$\overline{\text{OE}}$	Output Enable
SRAM	Static random access memory
TSOP	Thin small outline package
TTL	Transistor-transistor logic
VFBGA	Very fine-pitch ball grid array
$\overline{\text{WE}}$	Write Enable

**Document Conventions**

**Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

**Document History Page**

Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1 M words x 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3690091	TAVA	07/27/2012	New data sheet.
*A	3776318	AJU	10/30/2012	<p>Updated Document title to “CY7C1061G/CY7C1061GE, 16-Mbit (1 M words x 16 bit) Static RAM with Error-Correcting Code (ECC)”.</p> <p>Updated <a href="#">Features</a> (highlighted typical I<sub>CC</sub>, included ECC feature).</p> <p>Updated <a href="#">Functional Description</a> (Corrected typos, included 48-pin TSOP I information).</p> <p>Removed Selection Guide.</p> <p>Added 48-ball VFBGA pinouts (<a href="#">Figure 2</a>, <a href="#">Figure 5</a>, and <a href="#">Figure 6</a>), added 48-pin TSOP I (<a href="#">Figure 7</a>), and 54-pin TSOP II (<a href="#">Figure 10</a>).</p> <p>Updated <a href="#">Product Portfolio</a> to list all product options and added typical values for I<sub>CC</sub> and I<sub>SB2</sub> parameters.</p> <p>Changed latch up current limit from 200 to 140 mA (per JEDEC limits).</p> <p>Updated <a href="#">DC Electrical Characteristics</a>:</p> <p>Changed maximum value of I<sub>CC</sub> parameter from 100 mA to 110 mA for the Test Condition f = 100 MHz.</p> <p>Changed maximum value of I<sub>SB1</sub> parameter from 30 mA to 40 mA.</p> <p>Changed maximum value of I<sub>SB2</sub> parameter from 25 mA to 30 mA. Updated I<sub>SB2</sub> test conditions to reflect correct CMOS input levels.</p> <p>Added <a href="#">Note 9</a> and referred the same note in Test Conditions of I<sub>SB1</sub>, I<sub>SB2</sub> parameters.</p> <p>Changed C<sub>IN</sub> and C<sub>OUT</sub> values for 54 TSOP and 48 BGA packages from 6/8 pF to 10 pF.</p> <p>Included 48-pin TSOP I information in <a href="#">Capacitance</a> and <a href="#">Thermal Resistance</a>.</p> <p>Updated <a href="#">Data Retention Characteristics</a></p> <p>Changed maximum value of I<sub>CCDR</sub> parameter from 25 mA to 30 mA.</p> <p>Added <a href="#">Note 14</a> and referred the same note in Test Conditions of I<sub>CCDR</sub> parameter and <a href="#">Figure 12</a>.</p> <p>Updated <a href="#">AC Switching Characteristics</a>:</p> <p>Removed redundant t<sub>POWER</sub> parameter and associated footnote (captured in <a href="#">Note 13</a>).</p> <p>Updated <a href="#">Note 17</a> to include difference in input levels for V<sub>CC</sub> operation of less than 3 V.</p> <p>Added <a href="#">Note 20</a>.</p> <p>Updated <a href="#">Note 24</a> for better clarity.</p> <p>Removed the <a href="#">Note</a> “The minimum write cycle time for Write Cycle No. 2 (<math>\overline{WE}</math> controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.” and its references.</p> <p>Updated <a href="#">Switching Waveforms</a>:</p> <p>Updated <a href="#">Note 26</a> for better clarity.</p> <p>Updated <a href="#">Figure 15</a> to make it applicable to both CY7C1061G and CY7C1061GE.</p> <p>Updated <a href="#">Note 28</a> for better clarity.</p> <p>Updated <a href="#">Note 30</a> to correct typos.</p> <p>Referred <a href="#">Notes 31</a> and <a href="#">32</a> in <a href="#">Figure 16</a> and <a href="#">Figure 17</a>.</p> <p>Referred <a href="#">Notes 40</a> and <a href="#">41</a> in <a href="#">Figure 19</a>.</p> <p>Updated <a href="#">Notes 33</a> and <a href="#">42</a> for better clarity.</p> <p>Removed the <a href="#">Note</a> “If <math>\overline{CE}</math> goes HIGH simultaneously with <math>\overline{WE}</math> going HIGH, the output remains in a high-impedance state.” and its references (captured in <a href="#">Note 33</a> and <a href="#">Note 42</a>).</p> <p>Updated <a href="#">Truth Table</a> (Referred <a href="#">Note 44</a> in <math>\overline{CE}</math> column and added footnote 33).</p> <p>Updated <a href="#">Ordering Information</a>.</p> <p>Updated <a href="#">Package Diagrams</a> with the updated revisions.</p>
*B	4003550	AJU	05/17/2013	No technical updates.

**Document History Page** (continued)

Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1 M words x 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*C	4042263	AJU	06/27/2013	Updated <a href="#">Data Retention Characteristics</a> : Changed minimum value of $V_{DR}$ parameter from 1.5 V to 1 V. Updated <a href="#">AC Switching Characteristics</a> : Changed maximum value of $t_{HZBE}$ parameter from 5 ns to 6 ns for 10 ns speed bin. Changed minimum value of $t_{SD}$ parameter from 5.5 ns to 5 ns for 10 ns speed bin.
*D	4120023	MEMJ	09/11/2013	Updated <a href="#">Features</a> : Changed typical value of $I_{SB2}$ from 10 mA to 20 mA. Replaced "1.5-V data retention" with "1.0 V data retention". Updated <a href="#">Data Retention Waveform</a> : Changed value of $V_{DR}$ from 1.5 V to 1 V. Updated <a href="#">AC Switching Characteristics</a> : Changed minimum value of $t_{LZOE}$ parameter from 1 ns to 0 ns for 10 ns speed bin. Changed minimum value of $t_{LZBE}$ parameter from 1 ns to 0 ns for 10 ns speed bin. Updated <a href="#">Ordering Information</a> (Updated part numbers). Added Errata. Updated in new template.
*E	4163557	MEMJ	10/29/2013	Updated <a href="#">Pin Configurations</a> : Added <a href="#">Figure 3</a> . Updated <a href="#">DC Electrical Characteristics</a> : Added minimum value of $I_{SB2}$ parameter. Added Note 10 and referred the same note in minimum value of $I_{SB2}$ parameter. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated details in "Key Features / Differentiators" column corresponding to MPN "CY7C1061GE30-10BVXI" (Corrected ERR output location from ball G2 to ball E3).
*F	4272659	MEMJ	02/05/2014	Updated <a href="#">AC Switching Characteristics</a> : Added Note 22 and referred the same note in description of $t_{LZOE}$ , $t_{HZOE}$ , $t_{LZCE}$ , $t_{HZCE}$ , $t_{LZBE}$ , $t_{HZBE}$ , $t_{LZWE}$ , $t_{HZWE}$ parameters.

**Document History Page** (continued)

Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1 M words x 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*G	4292074	MEMJ / VINI	03/07/2014	Updated <a href="#">Features</a> section Introduced 15-ns speed bin Mentioned frequency for I <sub>CC</sub> typical measurement Changed "an error detection" to "a single-bit error detection" Updated <a href="#">DC Electrical Characteristics</a> : Added column for Typical values Moved reference to Note 10 from I <sub>SB2</sub> (Typical) to the "Typ" column heading Updated <a href="#">AC Switching Characteristics</a> : Added t <sub>POWER</sub> and associated Note 18. Added Note 25 and referred to Write Cycle timings Referred Note 21 to t <sub>HZBE</sub> and t <sub>LZBE</sub> Added Note 34 in <a href="#">Figure 17</a> . Added <a href="#">Figure 18</a> (WE controlled write) Added Note 35 in <a href="#">Figure 16</a> and <a href="#">Figure 17</a> , Note 39 in <a href="#">Figure 18</a> , and Note 43 in <a href="#">Figure 19</a> to indicate output state. Added condition to place outputs in disable state by making both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ HIGH in <a href="#">Truth Table</a> . Corrected ERR table by replacing "no error in stored data" with "no single bit error in stored data" Clarified different ordering options with respect to with or without ERR, location of ERR, and address MSB A <sub>19</sub> in <a href="#">Ordering Information</a> . Updated Errata Fix status
*H	4330547	AJU	04/02/2014	No technical updates.
*I	4375287	AJU	05/09/2014	Updated Errata: Updated FAST SRAM[47] Errata Summary: Updated date in "Fix Status" column in table and also "Fix Status" in bulleted points below the table. Completing Sunset Review.
*J	4397546	VINI	06/03/2014	Updated footnote 19 - removed tLZOE, tLZCE, tLZWE, and tLZBE, and added Hi-Z, Lo-Z transition.
*K	4469360	NILE	09/18/2014	Updated <a href="#">Package Diagrams</a> : spec 51-85160 – Changed revision from *D to *E.
*L	4545705	VINI	10/28/2014	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated Errata: Updated FAST SRAM[47] Errata Summary: Updated details in "Fix Status" column in table and also "Fix Status" in bulleted points below the table.
*M	4576640	VINI	11/21/2014	No technical updates.
*N	4604885	VINI	12/23/2014	Updated <a href="#">Functional Description</a> : Added related documentation hyperlink at the end. Updated <a href="#">Ordering Information</a> : Removed prune part number CY7C1061G18-15ZXI. Updated <a href="#">Package Diagrams</a> : spec 51-85183 – Changed revision from *C to *D.



**Document History Page** (continued)

Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1 M words x 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*O	4654020	NILE	02/10/2015	<p>Updated <a href="#">Pin Configurations</a>: Updated Note 5 (Added "If not used, this pin should be left floating." at the end). Updated Note 7 (Added "If not used, this pin should be left floating." at the end).</p> <p>Updated <a href="#">DC Electrical Characteristics</a>: Added details of <math>V_{OH}</math> parameter corresponding to voltage range "4.5 V to 5.5 V" and test condition "<math>V_{CC} = \text{Min}</math>, <math>I_{OH} = -0.1 \text{ mA}</math>". Added Note 11 and referred the same note in minimum value of <math>V_{OH}</math> parameter corresponding to voltage range "4.5 V to 5.5 V" and test condition "<math>V_{CC} = \text{Min}</math>, <math>I_{OH} = -0.1 \text{ mA}</math>".</p> <p>Updated <a href="#">AC Switching Characteristics</a>: Referred Note 19 in description of <math>t_{POWER}</math> parameter. Added Note 23 and referred the same note in description of <math>t_{LZOE}</math>, <math>t_{HZOE}</math>, <math>t_{LZCE}</math>, <math>t_{HZCE}</math>, <math>t_{LZWE}</math>, <math>t_{HZWE}</math> parameters.</p> <p>Updated <a href="#">ERR Output – CY7C1061GE</a>: Added Note 46 and referred the same note in "Output" column.</p> <p>Removed "Errata". All Errata for this product have been fixed and fixed samples are available since May 12, 2014.</p>

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Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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