Data Sheet | April 18, 2007 | FN3555.7

Serial I/O Filter

The Serial I/O Filter is a high performance filter engine that is ideal for off loading the burden of filter processing from a DSP microprocessor. It supports a variety of multistage filter configurations based on a user programmable filter and fixed coefficient halfband filters. These configurations include a programmable FIR filter of up to 256 taps, a cascade of from one to five halfband filters, or a cascade of halfband filters followed by a programmable FIR. The half band filters each decimate by a factor of two, and the FIR filter decimates from one to eight. When all six filters are selected, a maximum decimation of 256 is provided.

For digital tuning applications, a separate multiplier is provided which allows the incoming data stream to be multiplied, or mixed, by a user supplied mix factor. A two pin interface is provided for serially loading the mix factor from an external source or selecting the mix factor from an on-board ROM. The on-board ROM contains samples of a sinusoid capable of spectrally shifting the input data by one quarter of the sample rate, $F_S/4$. This allows the chip to function as a digital down converter when the filter stages are configured as a low-pass filter.

The serial interface for *3-* input and output data is compatible with the serial ports of common DSP microprocessors. Coefficients and configuration data are loaded over a bidirectional eight bit interface.

Features

- 45MHz Clock Rate
- 256 Tap Programmable FIR Filter
- 24-Bit Data, 32-Bit Coefficients
- Cascade of up to 5 Half Band Filters
- Decimation from 1 to 256
- Two Pin Interface for Down Conversion by $F_S/4$
- Multiplier for Mixing or Scaling Input with an External Source
- Serial I/O Compatible with Most DSP Microprocessors
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

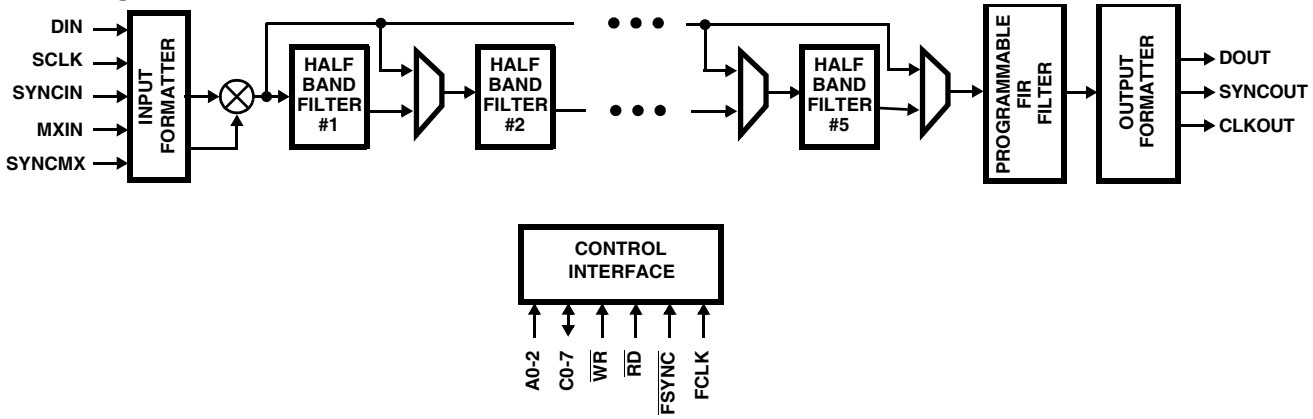
- Low Cost FIR Filter
- Filter Co-Processor
- Digital Tuner

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP43124SC-45	HSP43124SC-45	0 to +70	28 Ld SOIC (300 mil)	M28.3
HSP43124SC-45Z (Note)	HSP43124SC-45Z	0 to +70	28 Ld SOIC (300 mil, Pb-free)	M28.3

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

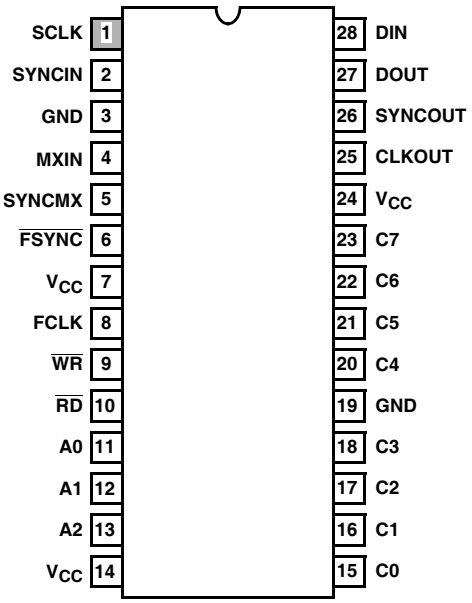
Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright Intersil Americas Inc. 1999, 2007. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

Pinout

HSP43124
(28 LD PDIP, SOIC)
TOP VIEW



Pin Description

NAME	TYPE	DESCRIPTION
V_{CC}	-	+5V Power Supply
GND	-	Ground
DIN	I	Serial Data Input. The bit value present on this input is sampled on the rising edge of SCLK. A “HIGH” on this input represents a “1”, and a low on this input represents “0”. The word format and operation of serial interface are contained in the Data Input Section.
SYNCIN	I	Data Sync. The HSP43124 is synchronized to the beginning of a new data word on DIN when SCLK samples SYNCIN “HIGH” one SCLK before the first bit of the new word. ***NOTE: SYNCIN should not maintain a “HIGH” state for longer than one SCLK cycle.***
SCLK	I	Serial Input CLK. The rising edge of SCLK clocks data on DIN and MXIN into the part. The following signals are synchronous to this clock: DIN, SYNCIN, MXIN, SYNCMX.
MXIN	I	Mix Factor Input. MXIN is the serial input for the mix factor. It is sampled on the rising edge of SCLK. A “HIGH” on this input represents a “1”, and a low on this input represents “0”. Also used to specify the Weaver Modulator ROM output as a part of the two pin $F_S/4$ down conversion interface. Details on word format and operation are contained in the Mix Factor Section.
SYNCMX	I	Mix Factor Sync. The HSP43124 is synchronized to the beginning of a serially input mix factor when SCLK samples SYNCMX “HIGH” one SCLK before the first bit of the new mix factor. ***NOTE: SYNCMX should only pulse “HIGH” for one SCLK cycle. Also used to specify Weaver Modulator ROM output as a part of the two pin $F_S/4$ down conversion interface.***
FCLK	I	Filter Clock. The filter clock determines the processing speed of the Filter Compute Engine. Clock rate requirements on FCLK for particular filter configurations is discussed in the Filter Compute Engine Section. This clock may be asynchronous to the serial input clock (SCLK). $\overline{FSYNC}$ is synchronous to this clock.
$\overline{FSYNC}$	I	Filter Sync. This input, when sampled low by the rising edge of FCLK, resets the filter compute engine so that the data sample following the next SYNCIN cycle is the first data sample into the filter structure. If a data stream is currently being input, the current sum of products and the input data are “canceled” and the DIN pin is ignored until the next SYNCIN cycle occurs.
$\overline{WR}$	I	Write. The falling edge of $\overline{WR}$ loads data present on C0-7 into the configuration or coefficient register specified by the address on A0-2. The $\overline{WR}$ signal is asynchronous to all other clocks. ***NOTE: $\overline{WR}$ should not be low when $\overline{RD}$ is low.***
$\overline{RD}$	I	Read. The falling edge of $\overline{RD}$ accesses the control registers or coefficient RAM addressed by A0-2 and places the contents of that memory location on C0-7. When $\overline{RD}$ returns “HIGH” the C0-7 bus functions as an input bus. The $\overline{RD}$ pin is asynchronous to all other clocks. ***NOTE: $\overline{RD}$ should not be low when $\overline{WR}$ is low.***
A0-2	I	Address Bus. The A0-2 inputs are decoded on the falling edge of both $\overline{RD}$ and $\overline{WR}$. Table 1 shows the address map for the control registers.
C0-7	I/O	Control and Coefficient bus. This bidirectional bus is used to access the control registers and coefficient RAM.
CLKOUT	O	Output Clock. Programmable bit clock for serial output. ***NOTE: Assertion of $\overline{FSYNC}$ initializes CLKOUT to a high state.***
SYNCOUT	O	Output Data Sync. SYNYOUT is asserted HIGH for one CLKOUT cycle before the first bit of a new output sample is available on DOUT.
DOUT	O	Serial Data Output. The bit stream is synchronous to the rising edge of CLKOUT. (See the Serial Output Formatter section for additional details.)

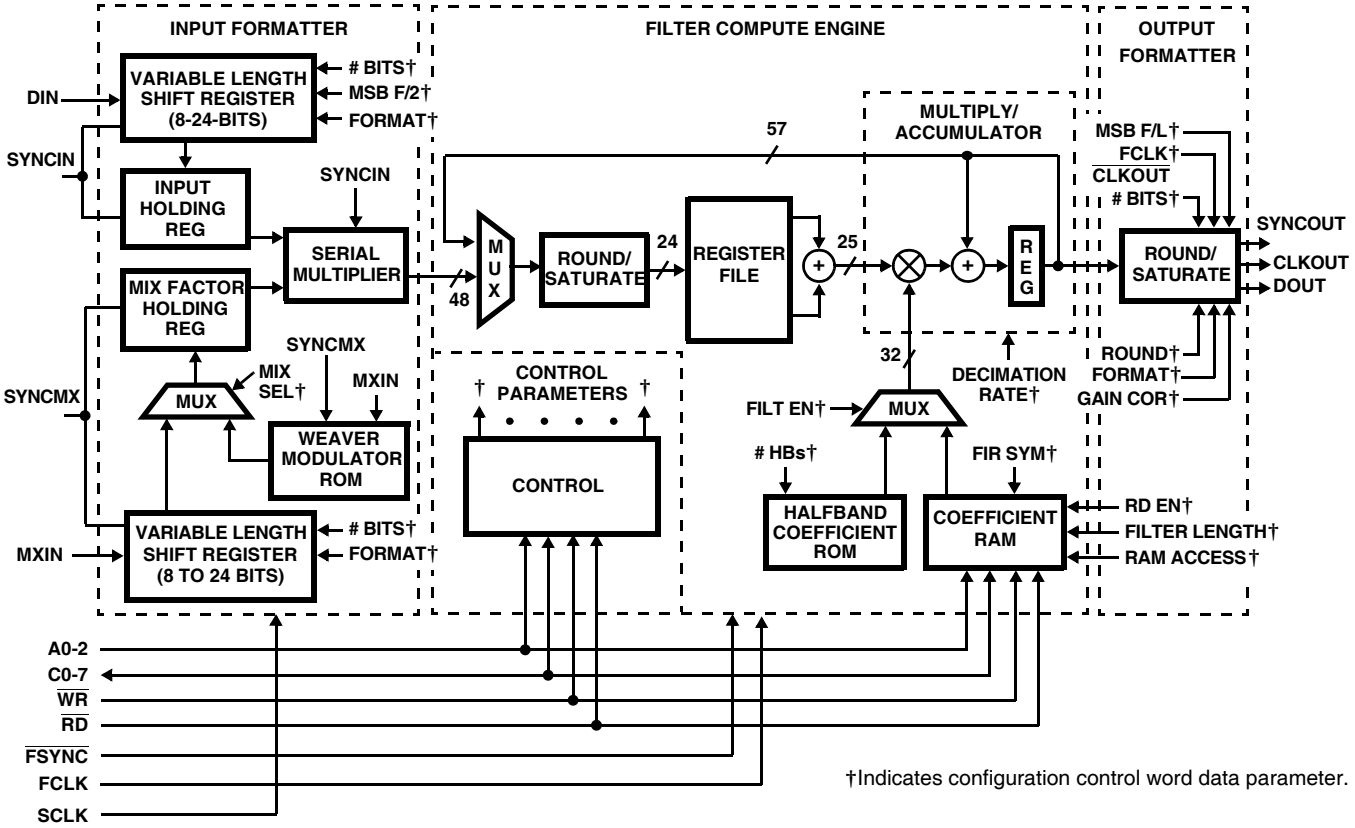


FIGURE 1. SERIAL FILTER BLOCK DIAGRAM

Functional Descriptions

The HSP43124 is a high performance digital filter designed to process a serial input data stream. A second serial interface is provided for mix factor inputs, which are multiplied by the input samples as shown in Figure 1. The multiplier result is passed to the Filter Compute Engine for processing.

The Filter Compute Engine centers around a single multiply/accumulator (MAC). The MAC performs the sum-of-products required by a particular filter configuration. The processing rate of the MAC is determined by the filter clock, FCLK. Increasing FCLK relative to the input sample rate increases the length of filter that can be realized.

The filtered results are passed to the Output Formatter where they are rounded or truncated to a user defined bit width. The Output Formatter then generates the timing and synchronization signals required to serially transmit the data to an external device.

Filter Configuration

The HSP43124 is configured for operation by loading a set of eight control registers. These registers are written through a bidirectional interface which is also used for reading the control registers. The interface consists of an 8-bit data bus, C0-7, a 3-bit address bus, A0-2, and read/write lines, RD and WR. The address map for the control registers is shown in Table 1.

Data is written to the configuration control registers on the falling edge of the $\overline{WR}$ input. This requires that the address, A0-2, and data, C0-7, be stable and valid on the falling edge of the $\overline{WR}$, as shown in Figure 2. ***NOTE: $\overline{WR}$ should not be active low when $\overline{RD}$ is active low.***

Data is read from the configuration control registers on the falling edge of the $\overline{RD}$ input. The contents of a particular register are accessed by setting up an address, A0-2, to the falling edge of RD as shown in Figure 2. The data is output on C0-7. The data on C0-7 remains valid until RD returns HIGH, at which point the C0-7 bus is Three-Stated and functions as an input. For proper operation, the address on A0-2 must be held until RD returns “high” as shown in Figure 2. ***NOTE: RD should not be active low when WR is active low.***

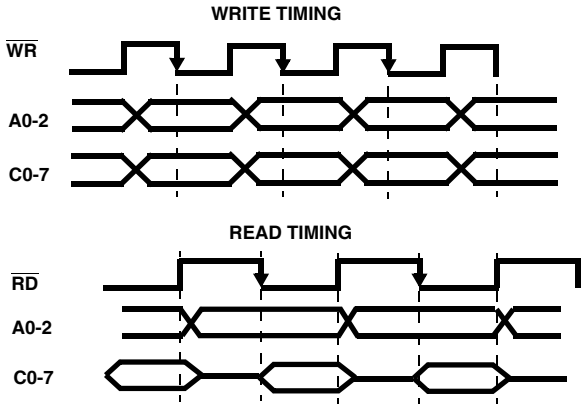


FIGURE 2. READ/WRITE TIMING

TABLE 1. CONFIGURATION CONTROL REGISTER FUNCTIONAL DESCRIPTION

ADDRESS	REGISTER DESCRIPTION	BIT POSITIONS	BIT FUNCTION
000	Filter Configuration	2-0	Specifies the number of halfbands to use. Number ranges from 0 to 5. Other values are invalid.
		3	Filter Enable bit. 1 = Enable. 0 = Minimum filter bypass (either the FIR or HBF must be enabled to get an output).
		4	Coefficient read enable. When set to 1, enables reading and disables writing of coefficient RAM. ***NOTE: This bit must be set to 0 prior to writing the Coefficient RAM.***
		7-5	FIR Decimation Rate. Range is 1-8 (8 = 000).
001	Programmable FIR Filter Length	7-0	Number of Taps in the Programmable FIR Filter. For even or odd symmetric filters, values range from 4- 256, 1 to 3 are invalid, and 0000000 = 256. For asymmetric filters, the value loaded in this register must be two times the actual number of coefficients.
010	Coefficient RAM Access	7-0	Coefficient RAM is loaded by multiple writes to this address. (See Writing Coefficients section for additional details.)
011	Input Format	4-0	Number of bits in input data word, from 8 (01000) to 24 (11000). Values outside the range of 8 - 24 are invalid.
		5	Number System. 0 = Two's Complement, 1 = Offset Binary.
		6	Serial Format. 1 = MSB First, 0 = LSB First.
		7	Unused
100	Output Timing	4-0	Number of FCLKS per CLKOUT. Range 1 to 32. (00000 = 32 FCLKS)
		5	1 = MSB First, 0 = LSB First.
		6-7	Unused
101	Output Format	4-0	Number of bits in output data word, from 8 to 32. A value of 32 is represented by 00000, and values from 1 to 7 are invalid.
		5	Round Select. 1 = Round to Selected Number of Bits, 0 = Truncate.
		6	Number System. 0 = Two's Complement, 1 = Offset Binary.
		7	Gain Correction. 1 = Apply scale factor of 2 to data. 0 = No Scaling.
110	Filter Symmetry	1-0	00 = Even Symmetric FIR Coefficients 01 = Non-Symmetric Coefficients 10 = Odd Symmetric FIR
		7-2	Reserved: Must be 0.
111	Mix Factor Format	4-0	Number of bits in mix factor, from 8 (01000) to 24 (11000). Values outside the range of 8 - 24 are invalid.
		5	Serial Format. 1 = MSB First, 0 = LSB First.
		6	Mix Factor Select. 1 = Serial Input, 0 = Weaver modulator look-up-table.
		7	Unused

Writing Coefficients

The HSP43124 provides a register bank to store filter coefficients for configurations which use the programmable filter. The register bank consists of 128 thirty-two-bit registers. Each register is loaded by 4 one byte writes to the bidirectional interface used for loading the configuration registers. The coefficients are loaded in order from least significant byte (LSB) to most significant byte (MSB).

The coefficient registers are loaded by first setting the coefficient read enable bit to "0" (bit 4 of the Filter Configuration Register). Next, coefficients are loaded by setting the A2-0 address to 010 (binary) and writing one byte at a time as shown in Figure 3. The down loaded bytes are stored in a holding register until the 4th write cycle. On completion of the fourth write cycle, the contents of the holding register are loaded into the Coefficient RAM, and the write pointer is incremented to the next register. If the user attempts to write more than 128 coefficients, the pointer

halts at the 128th register location, and writing is disabled. The coefficient address pointer is reset when any other configuration register is written or read. ***NOTE: A new coefficient set may be loaded during a filter calculation at the risk of corrupting output data until the load is complete.***

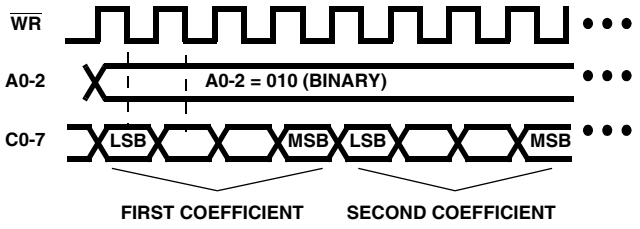
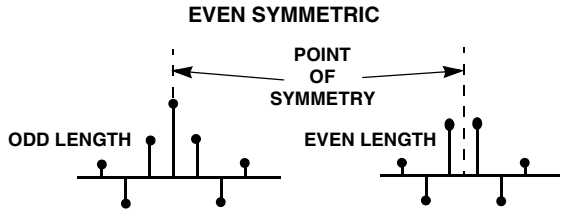
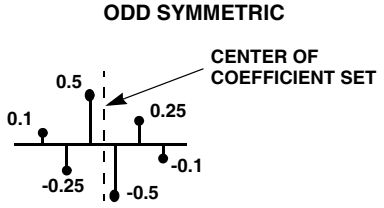


FIGURE 3. COEFFICIENT LOADING

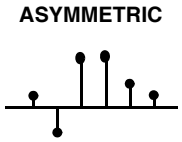
The number of coefficients that must be loaded is dependent on whether the coefficient set exhibits even symmetry, odd symmetry, or asymmetry (see Figure 4).



NOTE: Filters with even symmetric coefficients exhibit symmetry about the center of the coefficient set. Most FIR filters have coefficients which are symmetric in nature.



NOTE: Odd symmetric coefficients have a coefficient envelope which has the characteristics of an odd function (i.e. coefficients which are equidistant from the center of the coefficient set are equal in magnitude but opposite in sign). Coefficients designed to function as a differentiator or Hilbert Transform exhibit these characteristics.



NOTE: Asymmetric Coefficient sets exhibit no symmetry.

FIGURE 4. COEFFICIENT CHARACTERISTICS

For filters that exhibit either even or odd symmetry, only the unique half of the coefficient set must be loaded. The coefficients are loaded in order starting with the first filter tap and ending with the center tap. The coefficient associated with the first tap is the first to be multiplied by an incoming data sample as shown in Figure 5. For even/odd symmetric filters of length N, N/2 coefficients must be loaded if the filter length is even, and (N+1)/2 coefficients must be loaded if the filter length is odd. For example, a 17 tap symmetric filter would require the loading of 9 coefficients. Enough storage is provided for a 256 tap symmetric filter.

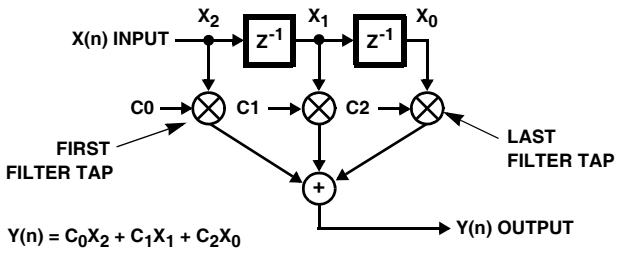


FIGURE 5. THREE TAP TRANSVERSAL FILTER ARCHITECTURE

For asymmetric filters the entire coefficient set must be loaded. The coefficients are loaded in order starting with the first tap and ending with the final filter tap (see Figure 5 for tap/coefficient association). Enough storage is provided for a 128 tap asymmetric filter. For asymmetric filters the value loaded into the Programmable Filter Length Register addressed must be twice the actual number of coefficients.

Reading Coefficients

The coefficients are read from the storage registers one byte at a time via C0-7 as shown in Figure 6. To read the coefficients, the user first sets the Coefficient Read Enable bit to 1 (bit 4 of Filter Configuration Control Register). Setting this bit resets the RAM read pointer and disables the RAM from being written. Next, with A2-0 = 010, multiple “high” to “low” transitions of $\overline{RD}$, output the coefficients on C0-7, one byte at a time, in the order they were written. ***NOTE: $\overline{RD}$ should not be “low” when $\overline{WR}$ is “low”***.

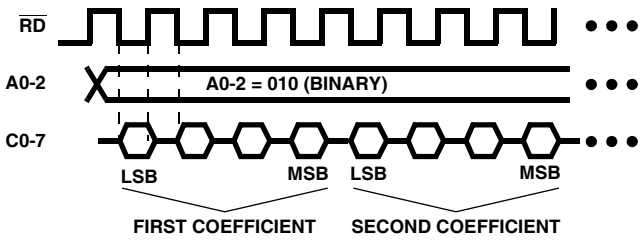


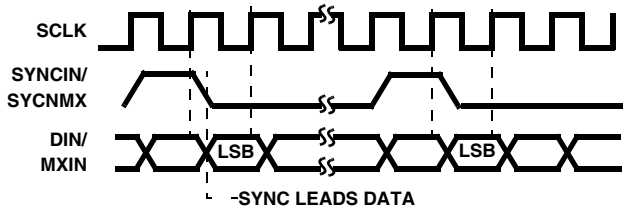
FIGURE 6. COEFFICIENT READING

Data Input

Data is serially input to the HSP43124 through the DIN input. On the rising edge of SCLK, the bit value present at DIN is clocked into the Variable Length Shift Register. The beginning of a serial data word is designated by asserting SYNCIN “high” one SCLK prior to the first data bit as shown

in Figure 7. On the following SCLK, the first data bit is clocked into the Variable Length Shift Register. Data bits are clocked into the shift register until the data word, of user programmable length (8 to 24 bits), is complete. At this point, the shifting of data into the register is disabled and its contents are held until SYNCIN is asserted on the rising edge of SCLK. When this occurs, the contents of the Variable Length Shift Register are transferred to the Input Holding Register, and the shift register is enabled to accept serial data on the following SCLK. The serial data word may be two's complement or offset binary and may be input most significant bit (MSB) first or least significant bit (LSB) first as defined in the Input Format Register (see Table 1). If a data word is specified to be less than 24 bits, the least significant bits of the Input Holding Register are zeroed.

NOTE: SYNCIN should not be "high" for longer than one SCLK cycle.



NOTE: Assumes data is being loaded LSB first.

FIGURE 7. SERIAL INPUT TIMING FOR EITHER DIN OR MXIN INPUTS

Mix Factor

The HSP43124 provides a second serial interface for loading values which are multiplied by the input samples in the serial multiplier. These values, or mix factors, are input using the MXIN and SYNCMX pins. Aside from being used as a serial input, this interface can also be used to select mix factors from the Weaver Modulator ROM. The mix factor source is specified in the Mix Factor Format Register (see Table 1). ***NOTE: Data is passed unmodified through the serial multiplier by selecting the Weaver Modulation ROM as the mix factor source and tying both SYNCMX and MXIN "high".***

The procedure for loading serial mix factors is similar to that for the loading of data via the DIN input. The bit value present on MXIN is clocked into the Variable Length Shift register by the rising edge of SCLK. The beginning of the serial word is designated by the assertion of SYNCMX one SCLK prior to the first bit of the serial word as shown in Figure 7. After the serial word has been clocked into the shift register, the shifting of bits into the register is disabled and its contents are held until the next assertion of SYNCMX. When SYNCMX is asserted on the rising edge of SCLK, the contents of the Variable Length Shift register are transferred into the Mix Factor Holding Register. The parallel output of the Mix Factor Holding Register feeds directly into the serial multiplier. The mix factor data word is programmable in length from 8 to 24 bits and may be input MSB or LSB first as specified in the Mix Factor Format Register. If a data word is specified to be less than 24 bits, the least significant bits of the Mix Factor Holding Register are zeroed.

The MXIN and SYNCMX inputs can function as two pin interfaces to Weaver Modulator ROM addresses. Used in proper sequence, down conversion by $F_S/4$ can be achieved. These inputs are latched on the rising edge of SCLK when SYNCIN is high as shown in Figure 9. The mapping of SYNCIN and MXIN to ROM outputs is given in Table 2. When SYNCIN is high on the rising edge of SCLK, the output of the ROM is transferred to the Mix Factor holding register, and the SYNCMX and MXIN inputs are decoded to produce a new ROM output. As a result, there is a latency of one SYNCIN cycle between when the SYNCMX and MXIN inputs are decoded and when the ROM output is loaded into the Mix Factor Holding register.

TABLE 2. WEAVER MODULATOR ROM DECODING

SYNCMX	MXIN	MIX FACTOR
0	0	0
0	1	-1
1	0	0
1	1	1

Serial Multiplier

The Serial Multiplier multiplies the Mix Factor Holding register by the contents of the Input Holding register. The multiplication cycle is initiated when SYNCIN is sampled high by the rising edge of SCLK. This transfers the contents of the Variable Length Shift register to the Input Holding Register, and loads the output of the Mix Factor Holding Register into the Serial Multiplier. On subsequent SCLKs, the contents of the Input Holding Register are shifted into the Serial Multiplier for processing. When the last data bit is shifted into the multiplier, the multiplication cycle is complete and the result is written to the Register File on the next rising edge of FCLK.

The synchronization between a data sample and the mix factor it is to be multiplied by is dependent on which mix factor source is specified. For mix factors which are input serially, the mix factor is loaded concurrently with the data sample to be multiplied (see Figure 8).

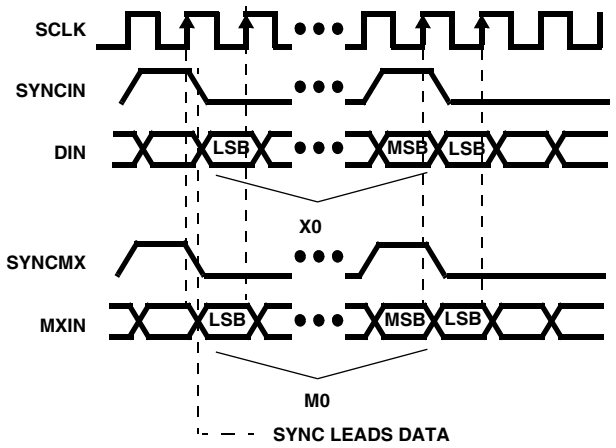


FIGURE 8. DATA/MIX FACTOR SYNCHRONIZATION FOR SERIALLY INPUT MIX FACTORS

NOTE: Figure 8 shows the loading of a data sample, X0, such that it will be multiplied by a mix factor designated by M0. For mix factor bit widths which are less than the input bit width, SYNCMX may be asserted before SYNCIN if desired.

If the mix factor is generated by the Weaver Modulator ROM, the mix factor must be specified on MXIN and SYNCMX one SYNCIN before that which precedes the target data word (see Figure 9).

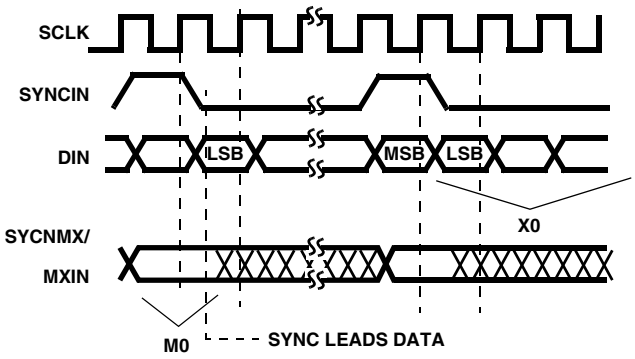


FIGURE 9. DATA/MIX FACTOR SYNCHRONIZATION WEAVER

Filter Compute Engine

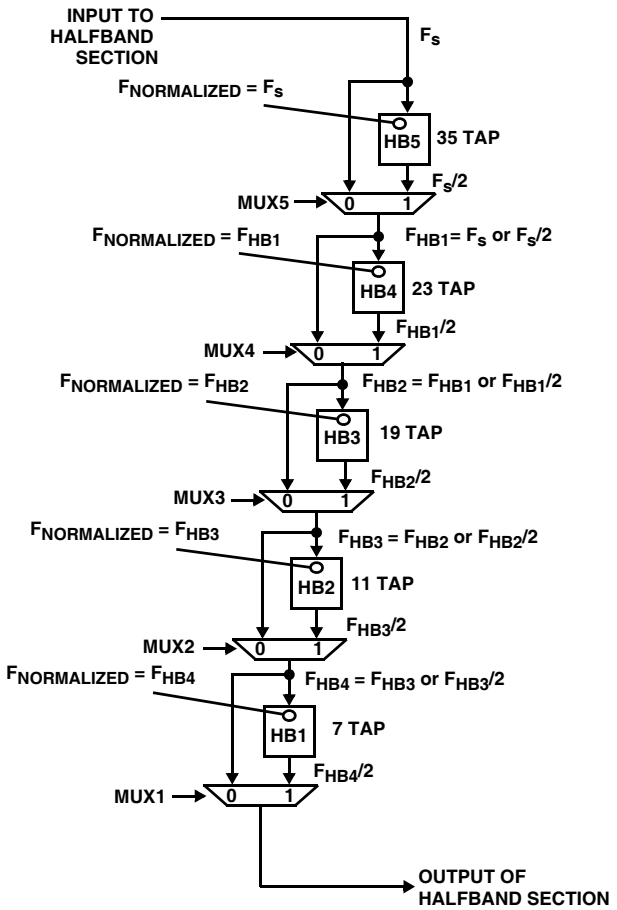
The Filter Compute Engine centers around a multiply accumulator which is used to perform the sum-of-products required for a variety of filtering configurations. These configurations include a cascade of up to 5 halfband filters, a single symmetric filter of up to 256 taps, a single asymmetric filter of up to 128 taps, or a cascade of halfband filters followed by a programmable filter. The filter configuration is specified by programming the Filter Configuration Register (see Table 1).

The cascade of up to five halfband filters is an efficient decimating filter structure. Each fixed coefficient filter in the chain introduces a decimation of two, and the aggregate decimation rate of the entire halfband filtering stage is given by:

$$DEC_{HB} = 2^{(\text{NUMBER OF HALFBAND FILTERS SELECTED})} \quad \text{(EQ. 1)}$$

Thus, a cascade of 3 halfband filters would decimate the input sample stream by a factor of 8.

Figure 10A is a block diagram of the halfband filter section. The normalized frequencies for each halfband stage is labeled. Figure 10B is an illustration of a cascaded filter composed of five halfband filters. The final stage filter output is clocked at FCLK/32. Since the output of each filter is at half the rate of the input, the five halfband filter passband characteristics can be viewed on a single plot whose X axis is normalized to the filter output clock rate. Notice that all halfband filters, by design, have 120dB passbands that are less than the output rate divided by 2. Since the alias profile is well below -120dB in the filter passband, alias concerns are eliminated. The frequency responses of the five filters are presented graphically in Figure 10C and in tabular form in Table 3. Notice that the 6dB passband bandwidth (F = 0.25) is identical for all five halfband filters. The width of the transition band, however, is different for each filter. The transition band for the fifth halfband filter, HB5, is the narrowest while that for the first halfband filter, HB1, is the widest. The cascade of the halfband filters always terminates with HB5 and is preceded by filters in order of increasing transition bandwidth. For example, if the HSP43124 is configured to operate with three halfbands, the chain of filters would consist of HB3 followed by HB4 and terminated with HB5. If only one halfband is selected, HB5 is used.



MULTIPLEXERS' DECODER TABLE AND EQUATIONS

BITS2-0	MUX1	MUX2	MUX3	MUX4	MUX5
000	0	0	0	0	0
001	0	0	0	0	1
010	0	0	0	1	1
011	0	0	1	1	1
100	0	1	1	1	1
101	1	1	1	1	1

MUX1 = (BIT2 AND BIT0) AND $\overline{BIT1}$

MUX2 = BIT2

MUX3 = (BIT1 AND BIT0) OR BIT2

MUX4 = BIT1 OR BIT2

MUX5 = BIT0 OR BIT1 OR BIT2

INVALID = BIT2 AND BIT1

FIGURE 10A. BLOCK DIAGRAM OF FIXED COEFFICIENT HALFBAND FILTERS

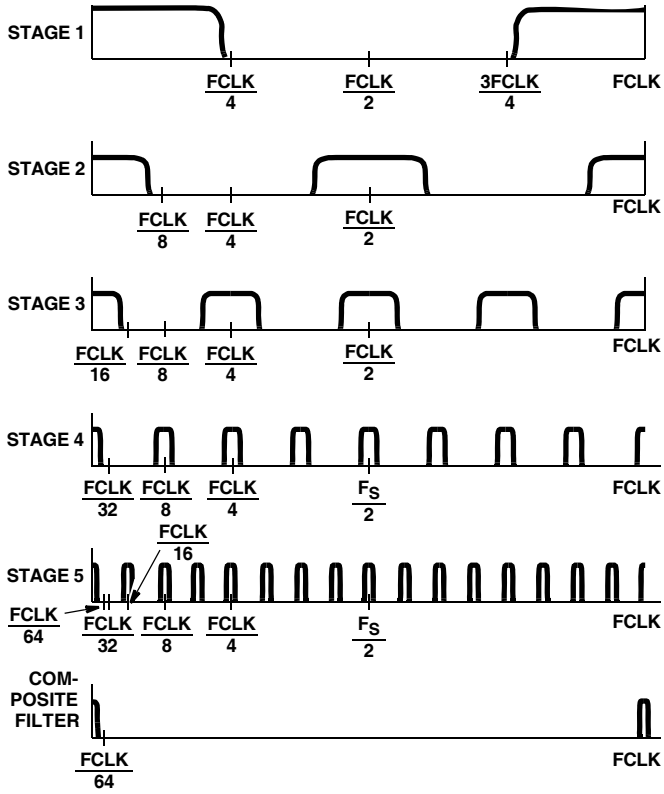


FIGURE 10B. SPECTRAL COMPOSITION OF FIVE CASCADED HALFBANDS

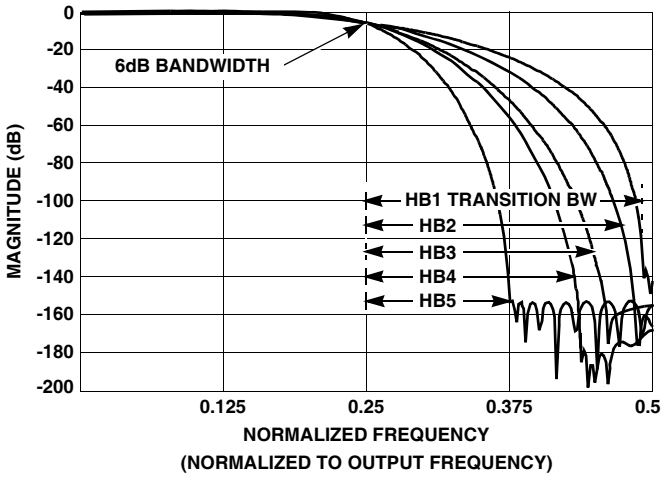


FIGURE 10C. COMPOSITE RESPONSE OF FIXED COEFFICIENT HALFBAND FILTERS WITH RESPECT TO THE NORMALIZED FREQUENCY SHOWN IN FIGURE 10A

The coefficient set for each of the halfband filters is given in Table 4. These values are the 32-bit, two's complement, integer representation of the filter coefficients. Scaling these values by 2^{-31} yields the fractional two's complement coefficients used to achieve unity gain in the Filter Processor.

If a specific frequency response is desired, a programmable FIR filter may be activated. The filter compute engine takes advantage of symmetry in FIR coefficients is by summing data samples sharing a common coefficient prior to multiplication. In this manner, two filter taps are calculated per multiply accumulate cycle. If an asymmetric filter is specified, only one tap per multiply accumulate cycle is calculated.

The processing rate of the Filter Compute Engine is proportional to FCLK. As a result, the frequency of FCLK must exceed a minimum value to insure that a filter calculation is complete before the result is required for output. In configurations which do not use decimation, one input sample period is available for filter calculation before an output is required. For configurations which employ decimation, up to 256 input sample periods may be available for filter calculation. The following equation specifies the minimum FCLK rate required for configurations which use the programmable filter as an FIR filter.

$$\text{Min FCLK} = \begin{cases} \frac{F_S}{DEC_{HB}}(TAPS/(2*DEC_{FIR}) + HB_{CLKS} + 1) \\ \text{or at least } 14F_S \text{ when Halfbands are used} \end{cases} \quad \text{(EQ. 2)}$$

In this equation F_S is the input sample rate (SCLK/# Bits in SER word), TAPS is the number of taps in the FIR filter (0 to 256), DEC_{FIR} is the decimation rate of the programmable FIR (1 to 8), HB_{CLKS} is a compute clock factor based on the number of halfband filters in the configuration (see Table 5), and DEC_{HB} is the aggregate decimation rate for the cascade of halfband filters (see Table 5). For example, if the input sample rate is 800kHz, a 128 tap FIR filter with no decimation is selected, and a cascade of 2 halfband filters is used, calculate the minimum FCLK rate as follows:

$$\text{Min FCLK} = \begin{cases} \left(\frac{800kHz}{4}\right)\left(\left(\frac{128}{2^1}\right) + 33 + 1\right) \\ (200kHz)[64 + 33 + 1] = 19.6MHz \\ \text{or at least } 14\ (800kHz) = 11.2MHz \end{cases} \quad \text{(EQ. 3)}$$

Thus, the Min FCLK is 19.6MHz.

NOTE: For configurations in which the halfband filters are used, the FCLK rate must exceed $14F_S$.

The longest length FIR filter realizable for a particular configuration is determined by solving the above equation for TAPS. The resulting expression is given below.

$$\text{Max TAPS} = 2DEC_{FIR}((FCLK/F_S)DEC_{HB} - HB_{CLKS} - 1) \quad \text{(EQ. 4)}$$

The maximum throughput sample rate may be specified by solving the above equation for F_S. The resulting equation is

$$\text{Max } F_S = FCLK*DEC_{HB}/(TAPS/(2*DEC_{FIR}) + HB_{CLKS} + 1). \quad \text{(EQ. 5)}$$

NOTE: For configurations using filters with asymmetric coefficients, the term TAPS in the above equations should be multiplied by two in order to determine the correct FCLK.

The Filter Compute Engine is synchronized with an incoming data stream by asserting the $\overline{\text{FSYNC}}$ input. When this input is sampled low by the rising edge of FCLK, the Compute Engine is reset, and the data word following the next assertion of SYNCIN is recognized as the first data sample input to the filter structure.

TABLE 3. FREQUENCY RESPONSE OF HALFBAND FILTERS

NORMALIZED FREQUENCY	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
0.000000	-0.000000	0.000000	0.000000	-0.000000	-0.000000
0.007812	0.000000	-0.000000	-0.000000	-0.000000	-0.000000
0.015625	-0.000113	-0.000000	-0.000000	-0.000000	-0.000000
0.023438	-0.000677	-0.000006	-0.000000	-0.000000	-0.000000
0.031250	-0.002243	-0.000052	-0.000000	-0.000000	-0.000000
0.039062	-0.005569	-0.000227	-0.000000	-0.000000	0.000000
0.046875	-0.011596	-0.000719	-0.000001	0.000000	-0.000000
0.054688	-0.021433	-0.001859	-0.000009	-0.000000	-0.000000
0.062500	-0.036333	-0.004165	-0.000041	-0.000000	-0.000000
0.070312	-0.057670	-0.008391	-0.000149	-0.000001	-0.000000
0.078125	-0.086916	-0.015557	-0.000448	-0.000012	-0.000000
0.085938	-0.125619	-0.026983	-0.001175	-0.000066	-0.000000
0.093750	-0.175382	-0.044301	-0.002767	-0.000258	-0.000000

TABLE 3. FREQUENCY RESPONSE OF HALFBAND FILTERS (Continued)

NORMALIZED FREQUENCY	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
0.101562	-0.237843	-0.069457	-0.005963	-0.000815	-0.000000
0.109375	-0.314663	-0.104701	-0.011924	-0.002208	-0.000000
0.117188	-0.407509	-0.152566	-0.022368	-0.005313	-0.000000
0.125000	-0.518045	-0.215834	-0.039695	-0.011613	-0.000000
0.132812	-0.647925	-0.297499	-0.067100	-0.023435	-0.000031
0.140625	-0.798791	-0.400727	-0.108640	-0.044186	-0.000287
0.148438	-0.972266	-0.528809	-0.169262	-0.078552	-0.001468
0.156250	-1.169959	-0.685131	-0.254777	-0.132639	-0.005427
0.164062	-1.393465	-0.873129	-0.371785	-0.214009	-0.016180
0.171875	-1.644372	-1.096269	-0.527552	-0.331613	-0.041152
0.179688	-1.924262	-1.358019	-0.729872	-0.495620	-0.092409
0.187500	-2.234728	-1.661842	-0.986908	-0.717181	-0.187497
0.195312	-2.577375	-2.011181	-1.307047	-1.008144	-0.349593
0.203125	-2.953834	-2.409468	-1.698769	-1.380771	-0.606862
0.210938	-3.365774	-2.860128	-2.170548	-1.847495	-0.991193
0.218750	-3.814917	-3.366593	-2.730783	-2.420719	-1.536664
0.226562	-4.303048	-3.932319	-3.387764	-3.112694	-2.278126
0.234375	-4.832037	-4.560817	-4.149669	-3.935463	-3.250174
0.242188	-5.403856	-5.255675	-5.024594	-4.900864	-4.486639
0.250000	-6.020599	-6.020600	-6.020600	-6.020600	-6.020600
0.257812	-6.684504	-6.859450	-7.145791	-7.306352	-7.884833
0.265625	-7.397981	-7.776287	-8.408404	-8.769932	-10.112627
0.273438	-8.163642	-8.775419	-9.816921	-10.423476	-12.738912
0.281250	-8.984339	-9.861469	-11.380193	-12.279667	-15.801714
0.289062	-9.863195	-11.039433	-13.107586	-14.352002	-19.344007
0.296875	-10.803663	-12.314765	-15.009147	-16.655094	-23.416153
0.304688	-11.809574	-13.693460	-17.095793	-19.205034	-28.079247
0.312500	-12.885208	-15.182171	-19.379534	-22.019831	-33.409992
0.320312	-14.035372	-16.788332	-21.873730	-25.119940	-39.508194
0.328125	-15.265501	-18.520315	-24.593418	-28.528942	-46.509052
0.335938	-16.581776	-20.387625	-27.555685	-32.274414	-54.604954
0.343750	-17.991278	-22.401131	-30.780161	-36.389088	-64.087959
0.351562	-19.502172	-24.573368	-34.289623	-40.912403	-75.444221
0.359375	-21.123947	-26.918915	-38.110786	-45.892738	-89.610390
0.367188	-22.867725	-29.454887	-42.275345	-51.390583	-108.973686
0.375000	-24.746664	-32.201569	-46.821358	-57.483341	-152.503693
0.382812	-26.776485	-35.183285	-51.795181	-64.272881	-153.443375
0.390625	-28.976198	-38.429543	-57.254162	-71.898048	-158.914017
0.398438	-31.369083	-41.976673	-63.270584	-80.556969	-156.960175
0.406250	-33.984089	-45.870125	-69.937607	-90.550629	-153.317627
0.414062	-36.857830	-50.167850	-77.378593	-102.379677	-161.115540
0.421875	-40.037594	-54.945438	-85.762718	-117.007339	-153.504684

TABLE 3. FREQUENCY RESPONSE OF HALFBAND FILTERS (Continued)

NORMALIZED FREQUENCY	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
0.429688	-43.585945	-60.304272	-95.332924	-136.890198	-158.650345
0.437500	-47.588165	-66.385063	-106.462181	-185.130432	-154.637756
0.445312	-52.164894	-73.392075	-119.793030	-187.297241	-153.870453
0.453125	-57.495132	-81.640152	-136.802948	-182.300125	-161.882385
0.460938	-63.861992	-91.658478	-175.030167	-203.460876	-152.278915
0.468750	-71.755898	-104.468010	-158.939362	-174.691895	-164.329758
0.476562	-82.156616	-122.641861	-157.095886	-174.737076	-153.535690
0.484375	-97.627930	-166.537369	-155.613434	-175.108841	-153.507477
0.492188	-139.751450	-165.699081	-154.708450	-169.966568	-167.665482

TABLE 4. HALFBAND FILTER COEFFICIENTS (32 BITS, UN-NORMALIZED)

COEFFICIENT	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
C0	-67230275	12724188	624169	-197705	23964
C1	0	0	0	0	0
C2	604101076	-105279784	-6983862	2303514	-242570
C3	1073741823	0	0	0	0
C4	604101076	629426509	38140187	-13225905	1306852
C5	0	1073741827	0	0	0
C6	-67230275	629426509	-145867861	51077176	-4942818
C7		0	0	0	0
C8		-105279784	650958284	-161054660	14717750
C9		0	1073741793	0	0
C10		12724188	650958284	657968488	-37027884
C11			0	1073741825	0
C12			-145867861	657968488	84032070
C13			0	0	0
C14			38140187	-161054660	-191585682
C15			0	0	0
C16			-6983862	51077176	670589251
C17			0	0	1073741824
C18			624169	-13225905	670589251
C19				0	0
C20				2303514	-191585682
C21				0	0
C22				-197705	84032070
C23					0
C24					-37027884
C25					0
C26					14717750
C27					0
C28					-4942818
C29					0

TABLE 4. HALFBAND FILTER COEFFICIENTS (32 BITS, UN-NORMALIZED) (Continued)

COEFFICIENT	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
C30					1306852
C31					0
C32					-242570
C33					0
C34					23964

TABLE 5. PERFORMANCE ENVELOPE PARAMETERS

NUMBER OF HALFBANDS	HB_{CLKS}	DEC_{HB}
0	0	1
1	13	2
2	33	4
3	69	8
4	125	16
5	221	32

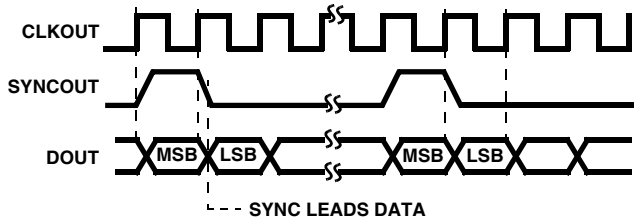
Serial Output Formatter

The Output Formatter serializes the parallel output of the filter compute engine and generates the timing and synchronization signals required to support a serial interface. The Formatter produces serial data words with programmable lengths from 8 to 32 bits. The data words may be organized with either most or least significant bit first. Also, the data word may be rounded or truncated to the desired length and the format of the output data may be specified as either two's complement or offset binary. To simplify applications where the Serial I/O Filter is used as a down converter, the output formatter can be configured to scale the output by a factor of 2. The above options are programmed via the Output Format and Output Timing Registers detailed in Table 1.

The HSP43124 outputs a bit stream through DOUT which is synchronous to a programmable clock signal output on CLKOUT. The output clock, CLKOUT, is derived from FCLK and has a programmable rate from 1 to $^1/_{32}$ times FCLK.

The duty cycle of CLKOUT is 50% for rates that have an even number of FCLKs per CLKOUT. For rates that have and odd number of FCLKs per CLKOUT the high portion of the CLKOUT waveform spans (n+1)/2 FCLKs and the low portion spans (n-1)/2 FCLKs where n is the number of FCLKs.

External devices synchronize to the beginning of an output data word by monitoring SYNCOUT. This output is asserted "high" one CLKOUT prior to the first bit of the next data word as shown in Figure 11.



NOTE: Assumes data is being output LSB first.

FIGURE 11. SERIAL OUTPUT TIMING

Input and Output Data Formats

The data formats for the input, output and coefficients are fractional two's complement. The bit weightings in the data words are given in Figure 12. Input or output data words programmed to have less than 24 bits, map to the most significant bit positions of the 24-bit word. For example, an input word defined to be 8 bits wide would map to the bit positions with weightings from -2^0 to 2^{-7}.

FRACTIONAL TWO'S COMPLEMENT FORMAT FOR 24-BIT INPUT AND OUTPUT

24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
-2^0.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

FRACTIONAL TWO'S COMPLEMENT FORMAT FOR 32-BIT COEFFICIENTS

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
-2^0.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}

NOTE: The negative sign on the MSB implies 2's complement formt.

FIGURE 12. DATA FORMATS

FCLK/SCLK Uncertainty Region

Figure 13 shows a clocking relationship for the HSP43124 Serial I/O filter that could result in an uncertainty at the output. For simplicity, the frequency of FCLK and SCLK are assumed to be equal to each other, and CLKOUT is assumed to be equal to FLCK. When the rising edge of FCLK lags behind the rising edge of SCLK by a small amount of time (T_{SCFC}), then the FCLK edge on which samples are read into the filter compute engine is determined by a race condition. In order to insure proper function for the HSP43124, T_{SCFC} must be greater than 3.8ns.

If exact timing (a particular clock edge for a specific data bit) then make SCLK and FCLK synchronous. If FCLK and SCLK are asynchronous, there will be jitter (a specific data bit will be output as 1 of 2 possible clock edges depending on the FCLK to SCLK phasing). For multiple part applications, use synchronous clocks or use separate syncs on what receives each data, as the outputs may vary by a clock cycle.

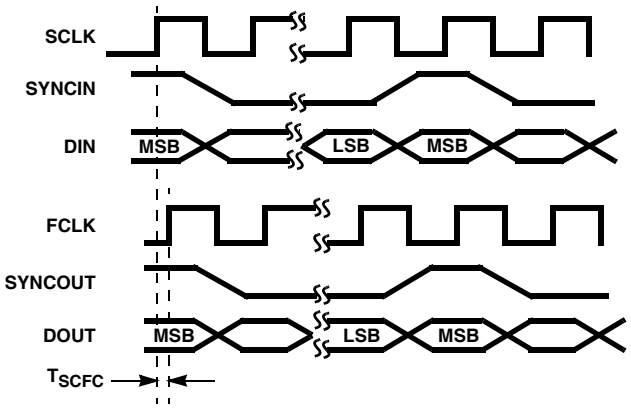


FIGURE 13. FCLK/SCLK UNCERTAINTY REGION

Asynchronous FCLK and SCLK

If FCLK and SCLK are asynchronous clocks, then the output sample rate (tracked by SYNCOUT) of the HSP43124 might jitter in a real time system. This jitter will be demonstrated using an SCLK with a period that is 3/2 times the period of FCLK (i.e., $F_{FCLK}/F_{SCLK} = 3/2$), as shown in Figure 14A and Figure 14B. If the LSB occurs when there are two FCLK edges in one SCLK period (see Figure 14A), then a null data bit will occur in the DOUT data stream. If the LSB occurs when there is one FCLK edge in one SCLK period for the LSB (see Figure 14B), then no null data bit will occur. Given the 3/2 period relationship between FCLK and SCLK, the user can see that the SYNCOUT jitters by one clock. For example, if the output data is represent by 16 bits, then the number of CLKOUT rising edges between SYNCOUT pulses should jitter between 15 and 16.

The SYNCOUT jitter demonstrated by the 3/2 frequency example can be generalized to other asynchronous F_{FCLK}/F_{SCLK} ratios. Setting the frequencies for FCLK and SCLK at integer multiples of one another eliminates timing jitter in the output sample rate.

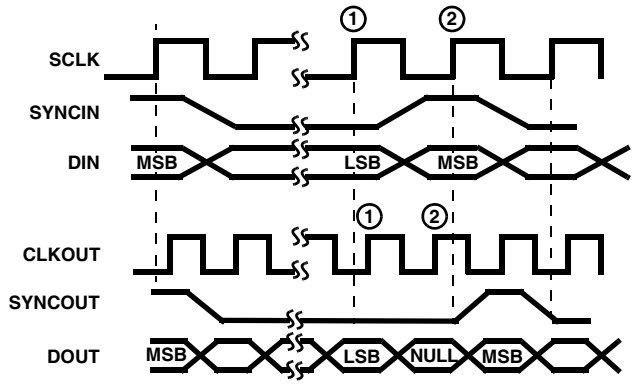


FIGURE 14A. NUMBER OF CLKOUT = NUMBER OF BITS + 1 FOR THE TIME PERIOD BETWEEN SYNCOUTS WHERE $F_{FCLK}/F_{SCLK} = 3/2$

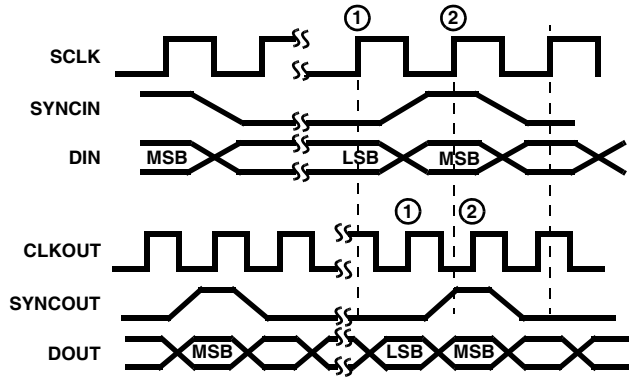


FIGURE 14B. NUMBER OF CLKOUT = NUMBER OF BITS FOR THE TIME PERIOD BETWEEN SYNCOUTS WHERE $F_{FCLK}/F_{SCLK} = 3/2$

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Rating . . . . . Class 1

Operating Conditions

Voltage Range (Commercial) . . . . . 4.75V to 5.25V
Voltage Range (Industrial) . . . . . 4.75V to 5.25V
Temperature Range (Commercial) . . . . . 0^oC to 70^oC
Temperature Range (Industrial) . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	65
PDIP Package	55

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

Die Characteristics

Gate Count 40,304

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5.0V $\pm$5%, T_A = 0^o to 70^oC Commercial, T_A = -40^o to 85^oC Industrial

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = Max, FCLK = SCLK = 45MHz Notes 2, 3	-	203	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	500	μA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	μA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	μA
Clock Input High	V_{IHC}	V_{CC} = Max, FCLK and SCLK	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = Min, FCLK and SCLK	-	0.8	V
Logical One Input Voltage	V_{IH}	V_{CC} = Max	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min	-	0.8	V
Logical One Output Voltage	V_{OH}	I_{OH} = -5mA, V_{CC} = Min	2.6	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 5mA, V_{CC} = Min	-	0.4	V
Input Capacitance	C_{IN}	FCLK = SCLK = 1MHz All Measurements Referenced to GND. T_A = 25^oC, Note 4	-	10	pF
Output Capacitance	C_{OUT}		-	10	pF

NOTES:

2. Power supply current is proportional to frequency. Typical rating is 4.5mA/MHz.
3. Output load per test circuit and C_L = 40pF.
4. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications

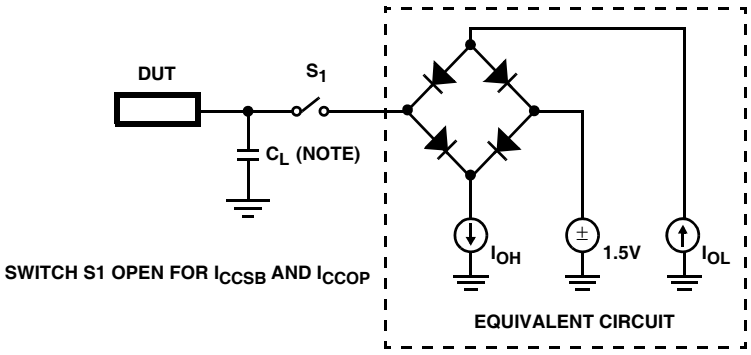
(Note 5) V_{CC} = +4.75V to +5.25V, T_A = 0°C to 70°C (Commercial)
V_{CC} = +4.75V to +5.25V, T_A = -40°C to 85°C (Industrial)

PARAMETER	SYMBOL	NOTES	45MHz		40MHz		33MHz		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
FCLK, SCLK Period	t_{CP}		22	-	25	-	30	-	ns
FCLK, SCLK High	t_{CH}		8	-	10	-	12	-	ns
FCLK, SCLK Low	t_{CL}		8	-	10	-	12	-	ns
Setup Time DIN, MXIN, SYNCIN, SYNCMX to SCLK	t_{DS}		8	-	8	-	9	-	ns
Hold Time DIN, MXIN, SYNCIN, SYNCMX from SCLK	t_{DH}		0	-	0	-	0	-	ns
Setup Time FSYNC to FCLK	t_{SS}		8	-	8	-	8	-	ns
Hold Time FSYNC from FCLK	t_{SH}		0	-	0	-	0	-	ns
Setup Time C0-7, A0-2 to Falling Edge of $\overline{WR}$	t_{WS}		10	-	10	-	10	-	ns
Hold Time C0-7, A0-2 from Falling Edge of $\overline{WR}$	t_{WH}		3	-	3	-	3	-	ns
Setup Time A0-2 to Falling Edge of $\overline{RD}$	t_{RS}		10	-	10	-	10	-	ns
Hold Time A0-2 from Rising Edge of $\overline{RD}$	t_{RH}		0	-	0	-	0	-	ns
$\overline{WR}$ High	t_{WRH}		10	-	10	-	12	-	ns
$\overline{WR}$ Low	t_{WRL}		10	-	10	-	12	-	ns
$\overline{RD}$ High	t_{RDH}		10	-	10	-	10	-	ns
$\overline{RD}$ Low to Data Valid	t_{RDO}		-	25	-	25	-	25	ns
$\overline{RD}$ High to Output Disable	t_{OD}		-	6	-	6	-	6	ns
FCLK to CLKOUT	t_{FOC}		-	12	-	13	-	14	ns
CLKOUT to SYNCOUT, DOUT	t_{DO}		-	8	-	9	-	10	ns
Output Rise, Fall Time	t_{RF}	Note 6	-	3	-	3	-	3	ns

NOTES:

5. AC tests performed with C_L = 40pF, I_{OL} = 5mA, and I_{OH} = -5mA. Input reference level for FCLK and SCLK is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V.
6. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

AC Test Load Circuit



NOTE: Test head capacitance.

Waveforms

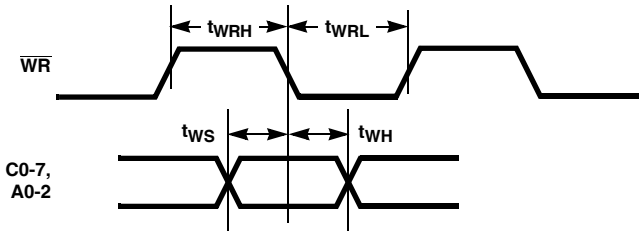


FIGURE 15. TIMING RELATIVE TO $\overline{WR}$

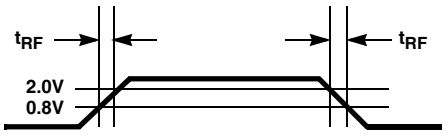


FIGURE 16. OUTPUT RISE AND FALL TIMES

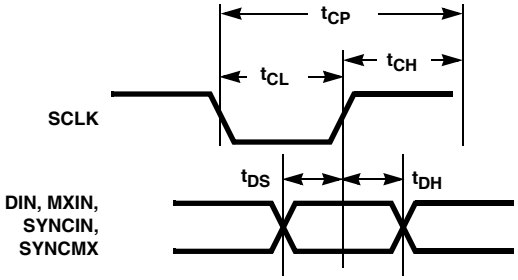


FIGURE 17. INPUT DATA TIMING

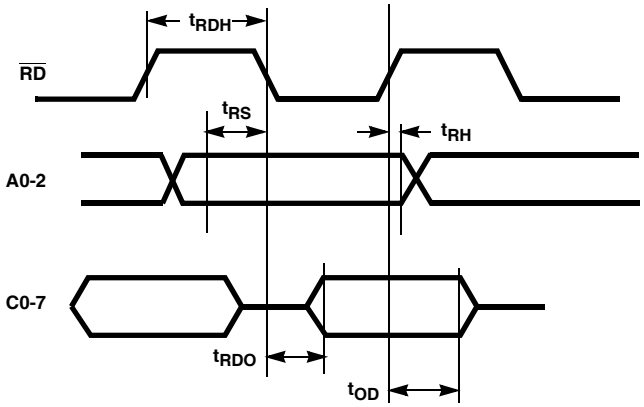


FIGURE 18. TIMING RELATIVE TO READ

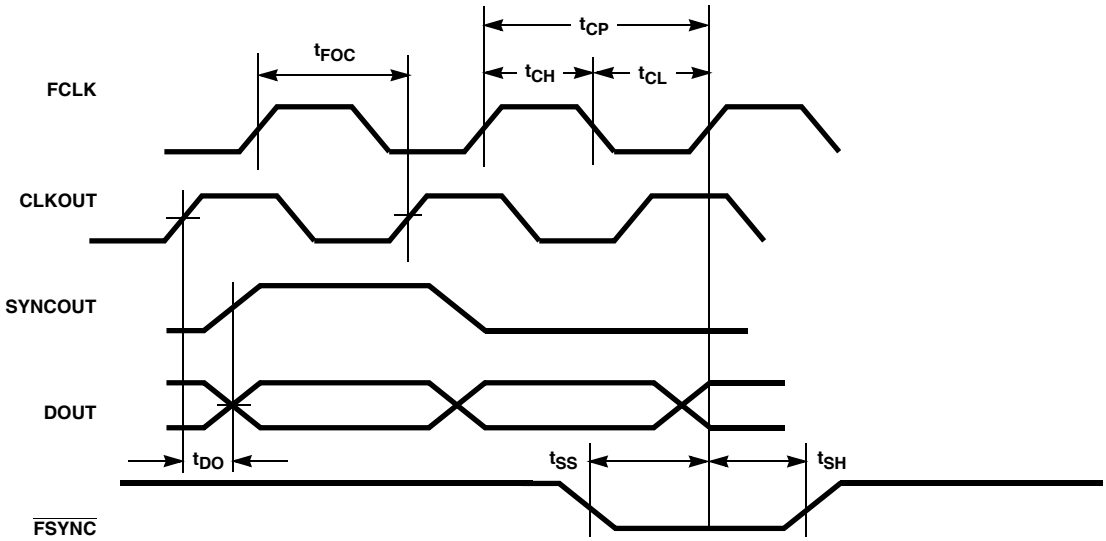
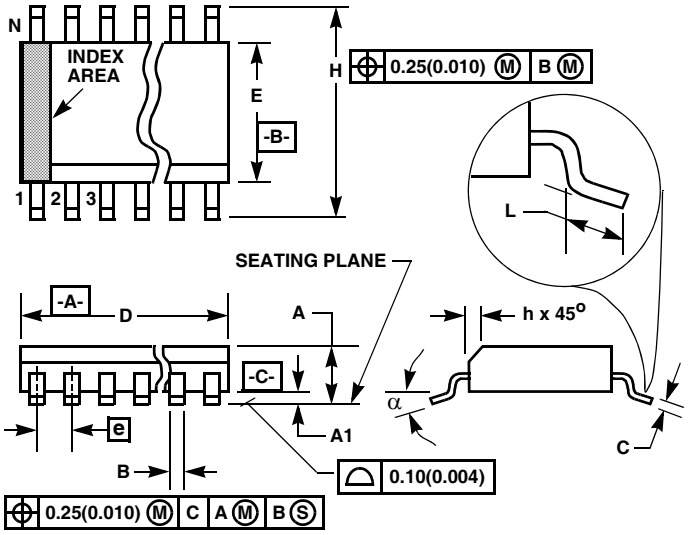


FIGURE 19. TIMING RELATIVE TO FLCK AND CLKOUT

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331