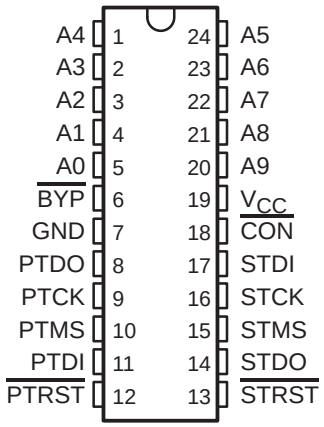
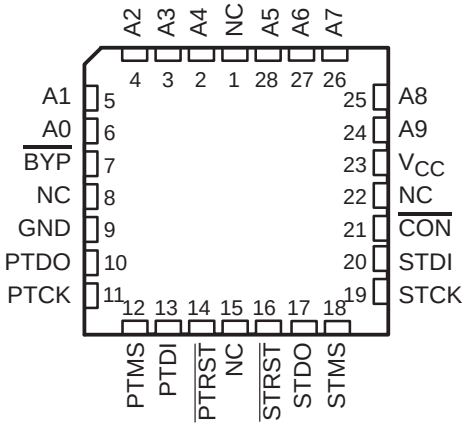
- **Members of Texas Instruments Broad Family of Testability Products Supporting IEEE Std 1149.1-1990 (JTAG) Test Access Port (TAP) and Boundary-Scan Architecture**
- **Extend Scan Access From Board Level to Higher Levels of System Integration**
- **Promote Reuse of Lower-Level (Chip/Board) Tests in System Environment**
- **Switch-Based Architecture Allows Direct Connect of Primary TAP to Secondary TAP**
- **Primary TAP Is Multidrop for Minimal Use of Backplane Wiring Channels**
- **Simple Addressing (Shadow) Protocol Is Received/Acknowledged on Primary TAP**
- **Shadow Protocols Can Occur in Any of Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR TAP States to Provide for Board-to-Board Test and Built-In Self-Test**
- **10-Bit Address Space Provides for Up to 1021 User-Specified Board Addresses**
- **Bypass ($\overline{BYP}$) Pin Forces Primary-to-Secondary Connection Without Use of Shadow Protocols**
- **Connect ($\overline{CON}$) Pin Provides Indication of Primary-to-Secondary Connection**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL}) Support Backplane Interface at Primary and High Fanout at Secondary**
- **Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (JT)**

SN54ABT8996 . . . JT PACKAGE
SN74ABT8996 . . . DW OR PW PACKAGE
(TOP VIEW)



SN54ABT8996 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’ABT8996 10-bit addressable scan ports (ASP) are members of the Texas Instruments (TI™) SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit assemblies. Unlike most SCOPE™ devices, the ASP is not a boundary-scannable device, rather, it applies TI’s addressable-shadow-port technology to the IEEE Standard 1149.1-1990 (JTAG) test access port (TAP) to extend scan access beyond the board level.

Conceptually, the ASP is a simple switch that can be used to directly connect a set of multidrop primary TAP signals to a set of secondary TAP signals – for example, to interface backplane TAP signals to a board-level TAP. The ASP provides all signal buffering that might be required at these two interfaces. When primary and secondary TAPs are connected, only a moderate propagation delay is introduced – no storage/retiming elements are inserted. This minimizes the need for reformatting board-level test vectors for in-system use.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SCOPE is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1999, Texas Instruments Incorporated

description (continued)

Most operations of the ASP are synchronous to the primary test clock (PTCK) input. This PTCK signal always is buffered directly onto the secondary test clock (STCK) output.

Upon power up of the device, the ASP assumes a condition in which the primary TAP is disconnected from the secondary TAP (unless the bypass signal is used, as below). This reset condition also can be entered by the assertion of the primary test reset ($\overline{\text{PTRST}}$) input or by use of shadow protocol. The $\overline{\text{PTRST}}$ signal is always buffered directly onto the secondary test reset ($\overline{\text{STRST}}$) output, ensuring that the ASP and its associated secondary TAP can be reset simultaneously.

When connected, the primary test data input (PTDI) and primary test mode select (PTMS) input are buffered onto the secondary test data output (STDO) and secondary test mode select (STMS) output, respectively, while the secondary test data input (STDI) is buffered onto the primary test data output (PTDO). When disconnected, STDO is at high impedance, while PTDO is at high impedance, except during acknowledgement of a shadow protocol. Upon disconnect of the secondary TAP, STMS holds its last low or high level, allowing the secondary TAP to be held in its last stable state. Upon reset of the ASP, STMS is high, allowing the secondary TAP to be synchronously reset to the Test-Logic-Reset state.

In system, primary-to-secondary connection is based on shadow protocols that are received and acknowledged on PTDI and PTDO, respectively. These protocols can occur in any of the stable TAP states other than Shift-DR or Shift-IR (i.e., Test-Logic-Reset, Run-Test/Idle, Pause-DR or Pause-IR). The essential nature of the protocols is to receive/transmit an address via a serial bit-pair signaling scheme. When an address is received serially at PTDI that matches that at the parallel address inputs (A9–A0), the ASP serially retransmits its address at PTDO as an acknowledgement and then assumes the connected (ON) status, as above. If the received address does not match that at the address inputs, the ASP immediately assumes the disconnected (OFF) status without acknowledgement.

The ASP also supports three dedicated addresses that can be received globally (that is, to which all ASPs respond) during shadow protocols. Receipt of the dedicated disconnect address (DSA) causes the ASP to disconnect in the same fashion as a non-matching address. Reservation of this address for global use ensures that at least one address is available to disconnect all receiving ASPs. The DSA is especially useful when the secondary TAPs of multiple ASPs are to be left in different stable states. Receipt of the reset address (RSA) causes the ASP to assume the reset condition, as above. Receipt of the test-synchronization address (TSA) causes the ASP to assume a connect status (MULTICAST) in which PTDO is at high impedance but the connections from PTMS to STMS and PTDI to STDO are maintained to allow simultaneous operation of the secondary TAPs of multiple ASPs. This is useful for multicast TAP-state movement, simultaneous test operation (such as in Run-Test/Idle state), and scanning of common test data into multiple like scan chains. The TSA is valid only when received in the Pause-DR or Pause-IR TAP states.

Alternatively, primary-to-secondary connection can be selected by assertion of a low level at the bypass ($\overline{\text{BYP}}$) input. This operation is asynchronous to PTCK and is independent of $\overline{\text{PTRST}}$ and/or power-up reset. This bypassing feature is especially useful in the board-test environment, since it allows the board-level automated test equipment (ATE) to treat the ASP as a simple transceiver. When the $\overline{\text{BYP}}$ input is high, the ASP is free to respond to shadow protocols. Otherwise, when $\overline{\text{BYP}}$ is low, shadow protocols are ignored.

Whether the connected status is achieved by use of shadow protocol or by use of $\overline{\text{BYP}}$, this status is indicated by a low level at the connect ($\overline{\text{CON}}$) output. Likewise, when the secondary TAP is disconnected from the primary TAP, the $\overline{\text{CON}}$ output is high.

The SN54ABT8996 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8996 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		SHADOW-PROTOCOL RESULT†	OUTPUTS						PRIMARY-TO-SECONDARY CONNECT STATUS
$\overline{BYP}$	$\overline{PTRST}$		$\overline{STRST}$	STCK	STMS	STDO	PTDO	$\overline{CON}$	
L	L	—	L	PTCK	H‡	PTDI	STDI	L	BYP/TRST‡
L	H	—	H	PTCK	PTMS	PTDI	STDI	L	BYP
H	L	—	L	PTCK	H	Z	Z	H	TRST
H	H	RESET	H	PTCK	H	Z	Z	H	RESET
H	H	MATCH	H	PTCK	PTMS	PTDI	STDI	L	ON
H	H	NO MATCH	H	PTCK	$STMS_0$§	Z	Z	H	OFF
H	H	HARD ERROR¶	H	PTCK	$STMS_0$§	Z	Z	H	OFF
H	H	DISCONNECT	H	PTCK	$STMS_0$§	Z	Z	H	OFF
H	H	TEST SYNCHRONIZATION	H	PTCK	PTMS	PTDI	Z	L	MULTICAST

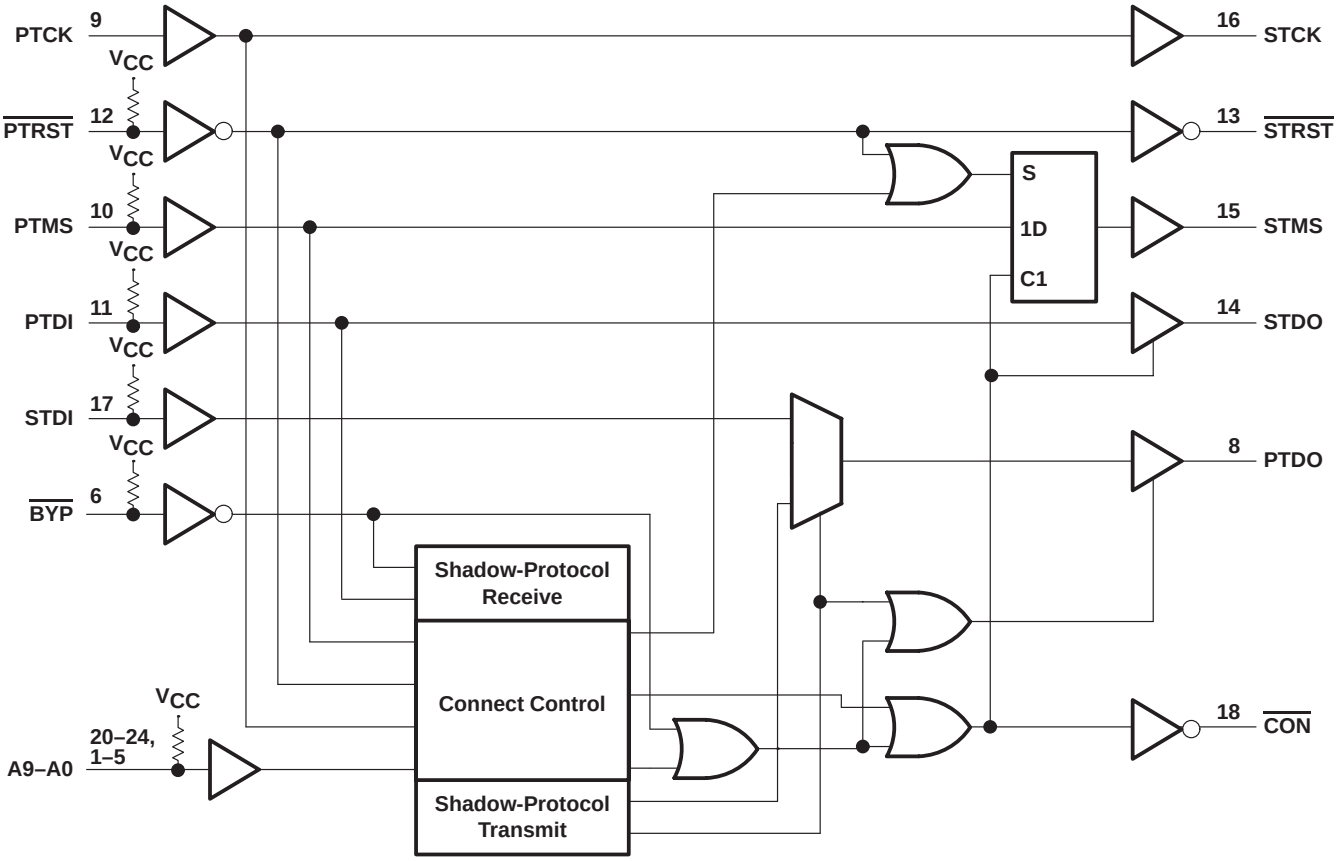
† Shadow protocols are received serially via PTCK and PTDI and acknowledged serially via PTCK and PTDO under certain conditions in which PTMS is static low or static high (see shadow protocol). The result shown here follows any required acknowledgement.

‡ In normal operation of IEEE Std 1149.1-compliant architectures, it is recommended that TMS be high prior to release of $\overline{TRST}$. The BYP/TRST connect status ensures that this condition is met at STMS regardless of the applied PTMS. Also, it is recommended that STMS be kept high for a minimum duration of 5 PTCK cycles following assertion of $\overline{PTRST}$, either by maintaining $\overline{PTRST}$ low or by setting PTMS high. This ensures that ICs both with and without $\overline{TRST}$ inputs are moved to their Test-Logic-Reset TAP states. It is expected that in normal application, this condition will only occur when $\overline{BYP}$ is fixed at the low state. In such case, upon release of $\overline{PTRST}$, the ASP immediately resumes the BYP connect status.

§ STMS level before indicated steady-state conditions were established

¶ The shadow protocol is well defined. Some variations in the protocol are tolerated (see protocol errors). Those that are not tolerated are considered hard errors and cause disconnect as indicated.

functional block diagram



Pin numbers shown are for the DW, JT, and PW packages.

Terminal Functions

TERMINAL NAME	DESCRIPTION
A9–A0	Address inputs. The ASP compares addresses received via shadow protocol against the value at A9–A0 to determine address match. The bit order is from most significant to least significant. An internal pullup at each A9–A0 terminal forces the terminal to a high level if it has no external connection.
$\overline{\text{BYP}}$	Bypass input. A low input at $\overline{\text{BYP}}$ forces the ASP into BYP or BYP/TRST status, depending on $\overline{\text{PTRST}}$ being high or low, respectively. While $\overline{\text{BYP}}$ is low, shadow protocols are ignored. Otherwise, while $\overline{\text{BYP}}$ is high, the ASP is free to respond to shadow protocols. An internal pullup forces $\overline{\text{BYP}}$ to a high level if it has no external connection.
$\overline{\text{CON}}$	Connect indicator (output). The ASP indicates secondary-scan-port activity (resulting from BYP, BYP/TRST, MULTICAST, or ON status) by forcing $\overline{\text{CON}}$ to be low. Inactivity (resulting from OFF, RESET, or TRST status) is indicated when $\overline{\text{CON}}$ is high.
GND	Ground
PTCK	Primary test clock. PTCK receives the TCK signal required by IEEE Standard 1149.1-1990. The ASP always buffers PTCK to STCK. Shadow protocols are received/acknowledged synchronously to PTCK and connect-status changes invoked by shadow protocol are made synchronously to PTCK.
PTDI	Primary test data input. PTDI receives the TDI signal required by IEEE Standard 1149.1-1990. During appropriate TAP states, the ASP monitors PTDI for shadow protocols. During shadow protocols, data at PTDI is captured on the rising edge of PTCK. When a valid shadow protocol is received in this fashion, the ASP compares the received address against the A9–A0 inputs. If the ASP detects a match, it outputs an acknowledgement and then connects its primary TAP terminals to its secondary TAP terminals. Under BYP, BYP/TRST, MULTICAST or ON status, the ASP buffers the PTDI signal to STDO. An internal pullup forces PTDI to a high level if it has no external connection.
PTDO	Primary test data output. PTDO transmits the TDO signal required by IEEE Standard 1149.1-1990. During shadow protocols, the ASP transmits any required acknowledgement via the PTDO. The acknowledgement data output at PTDO changes on the falling edge of PTCK. Under BYP, BYP/TRST, or ON status, the ASP buffers the PTDO signal from STDI. Under OFF, MULTICAST, RESET, or TRST status, PTDO is at high impedance.
PTMS	Primary test mode select. PTMS receives the TMS signal required by IEEE Standard 1149.1-1990. The ASP monitors the PTMS to determine the TAP-controller state. During stable TAP states other than Shift-DR or Shift-IR (i.e., Test-Logic-Reset, Run-Test-Idle, Pause-DR, Pause-IR) the ASP can respond to shadow protocols. Under BYP, MULTICAST, or ON status, the ASP buffers the PTMS signal to STMS. An internal pullup forces PTMS to a high level if it has no external connection.
$\overline{\text{PTRST}}$	Primary test reset. $\overline{\text{PTRST}}$ receives the $\overline{\text{TRST}}$ signal allowed by IEEE Standard 1149.1-1990. The ASP always buffers $\overline{\text{PTRST}}$ to $\overline{\text{STRST}}$. A low input at $\overline{\text{PTRST}}$ forces the ASP to assume TRST or BYP/TRST status, depending on $\overline{\text{BYP}}$ being high or low, respectively. Such operation also asynchronously resets the internal ASP state to its power-up condition. Otherwise, while $\overline{\text{PTRST}}$ is high, the ASP is free to respond to shadow protocols. An internal pullup forces $\overline{\text{PTRST}}$ to a high level if it has no external connection.
STCK	Secondary test clock. STCK retransmits the TCK signal required by IEEE Standard 1149.1-1990. The ASP always buffers STCK from PTCK.
STDI	Secondary test data input. STDI receives the TDI signal required by IEEE Standard 1149.1-1990. Under BYP, BYP/TRST, or ON status, the ASP buffers STDI to PTDO. An internal pullup forces STDI to a high level if it has no external connection.
STDO	Secondary test data output. STDO transmits the TDO signal required by IEEE Standard 1149.1-1990. Under BYP, BYP/TRST, MULTICAST, or ON status, the ASP buffers STDO from PTDI. Under OFF, RESET, or TRST status, STDO is at high impedance.
STMS	Secondary test mode select. STMS retransmits the TMS signal required by IEEE Standard 1149.1-1990. Under BYP, MULTICAST, or ON status, the ASP buffers STMS from PTMS. When disconnected (as a result of OFF status), STMS maintains its last valid state until the ASP assumes BYP/TRST, RESET, or TRST status (upon which it is forced high) or the ASP again assumes BYP, MULTICAST, or ON status.
$\overline{\text{STRST}}$	Secondary test reset. $\overline{\text{STRST}}$ retransmits the $\overline{\text{TRST}}$ signal allowed by IEEE Standard 1149.1-1990. The ASP always buffers $\overline{\text{STRST}}$ from $\overline{\text{PTRST}}$.
V_{CC}	Supply voltage

application information

In application, the ASP is used at each of several (serially-chained) groups of IEEE Std 1149.1-compliant devices. The ASP for each such group is assigned an address (via inputs A9–A0) that is unique from that assigned to ASPs for the remaining groups. Each ASP is wired at its primary TAP to common (multidrop) TAP signals (sourced from a central IEEE Std 1149.1 bus master) and fans out its secondary TAP signals to the specific group of IEEE Std 1149.1-compliant devices with which it is associated. An example is shown in Figure 1.

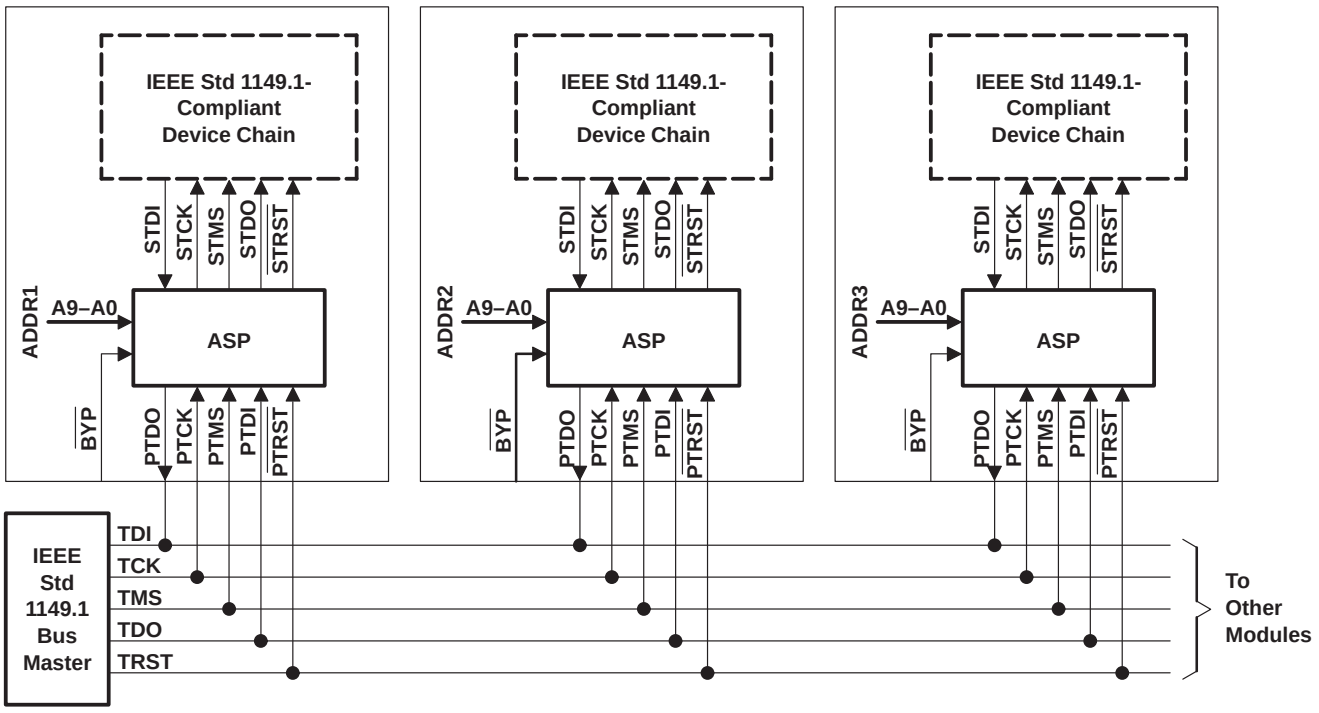


Figure 1. ASP Application

This application allows the ASP to be wired to a 4- or 5-wire multidrop test access bus, such as might be found on a backplane. Each ASP would then be located on a module, for example a printed-circuit board (PCB), which contains a serial chain of IEEE Std 1149.1-compliant devices and which would plug into the module-to-module bus (e.g., backplane). In the complete system, the ASP shadow protocols would allow the selection of the scan chain on a single module. The selected scan chain could then be controlled, via the multidrop TAP, as if it were the only scan chain in the system. Normal IR and DR scans can then be performed to accomplish the module test objectives.

Once scan operations to a given module are complete, another module can be selected in the same fashion, at which time the ASP-based connection to the first module is dissolved. This procedure can be continued progressively for each module to be tested. Finally, one of two global addresses can be issued to either leave all modules unselected (disconnect address, DSA) or to deselect and reset scan chains for all modules (reset address, RSA).

Additionally, in Pause-DR and Pause-IR TAP states, a third global address (test-synchronization address, TSA) can be invoked to allow simultaneous TAP-state changes and multicast scan-in operations to selected modules. This is especially useful in the former case, for allowing selected modules to be moved simultaneously to the Run-Test-Idle TAP state for module-level or module-to-module built-in self-test (BIST) functions, which operate synchronously to TCK in that TAP state, and in the latter case, for scanning common test setup/data into multiple like modules.

architecture

Conceptually, the ASP can be viewed as a bank of switches that can connect or isolate a module-level TAP to/from a higher-level (e.g., module-to-module) TAP. This is shown in Figure 2. The state of the switches (open versus closed) is based on shadow protocols, which are received on PTDI and are synchronous to PTCK.

The simple architecture of the ASP allows the system designer to overcome the limitations of IEEE Std 1149.1 *ring* and *star* configurations. Ring configurations (in which each module's TDO is chained to the next module's TDI) are of limited use in backplane environments, since removal of a module breaks the scan chain and prevents test of the remainder of the system. Star configurations (in which all module TDOs and TDIs are connected in parallel) are suited to the backplane environment, but, since each module must receive its own TMS, are costly in terms of backplane routing channels. By comparison, use of the ASP allows all five IEEE Std 1149.1 signals to be routed in multidrop fashion.

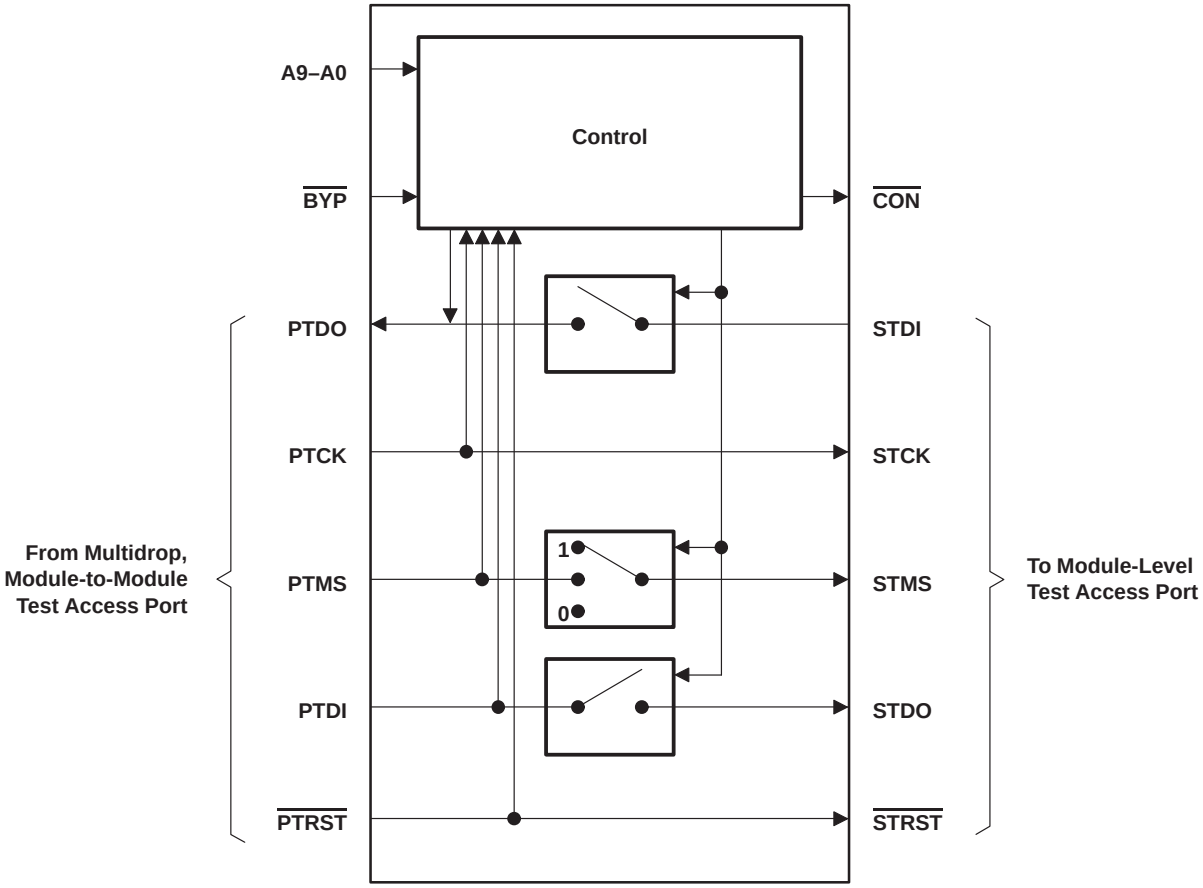


Figure 2. ASP Conceptual Model

As shown in the functional block diagram, the ASP comprises three major logic blocks. Blocks for shadow-protocol receive and shadow-protocol transmit are responsible for receipt of select protocol and transmission of acknowledge protocol, respectively. The connect-control block is responsible for TAP-state monitor and address matching.

Some additional logic is illustrated outside of these major blocks. This additional logic is responsible for controlling the activity of the ASP outputs based on the shadow-protocol result and/or protocol bypass [as selected by an active (low) $\overline{\text{BYP}}$ input].

shadow protocol

Addressing of an ASP in system is accomplished by shadow protocols, which are received at PTDI synchronously to PTCK. Shadow protocols can occur only in the following stable TAP states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR. Shadow protocols never occur in Shift-DR or Shift-IR states in order to prevent contention on the signal bus to which PTDO is wired. Additionally, the ASP PTMS must be held at a constant low or high level throughout a shadow protocol. If TAP-state changes occur in the midst of a shadow protocol, the shadow protocol is aborted and the select-protocol state machine returns to its initial state.

The shadow protocol is based on a serial bit-pair signaling scheme in which two bit-pair combinations (data one, data zero) are used to represent address data and the other two bit-pair combinations (select, idle) are used for framing – that is, to indicate where address data begins and ends.

These bit pairs are received serially at PTDI (or transmitted serially at PTDO) synchronously to PTCK as follows:

- The idle bit pair (I) is represented as two consecutive high signals.
- The select bit pair (S) is represented as two consecutive low signals.
- The data-one bit pair (D) is represented as a low signal followed by a high signal.
- The data-zero bit pair (D) is represented as a high signal followed by a low signal.

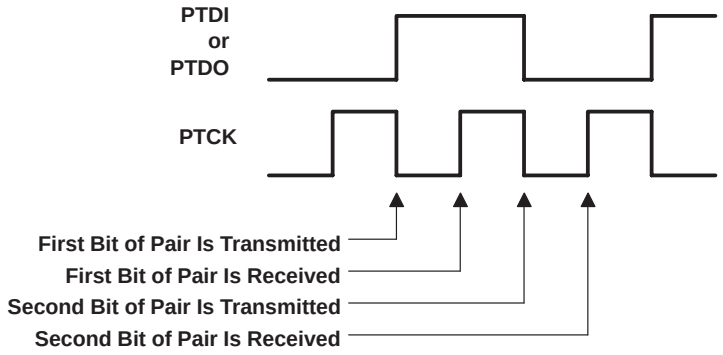


Figure 3. Bit-Pair Timing (Data Zero Shown)

A complete shadow protocol is composed of the receipt of a select protocol followed, if applicable, by the transmission of an acknowledge protocol (which is issued from PTDO only if the received address matches that at the A9–A0 inputs). Both of these subprotocols are composed of ten data bit pairs framed at the beginning by idle and select bit pairs and at the end by select and idle bit pairs. This is represented in an abbreviated fashion as follows: ISDDDDDDDDDSI. Figure 4 shows a complete shadow protocol (the symbol T is used to represent a high-impedance condition on the associated signal line – since the high-impedance state at PTDI is logically high due to pullup, it maps onto the idle bit pair).

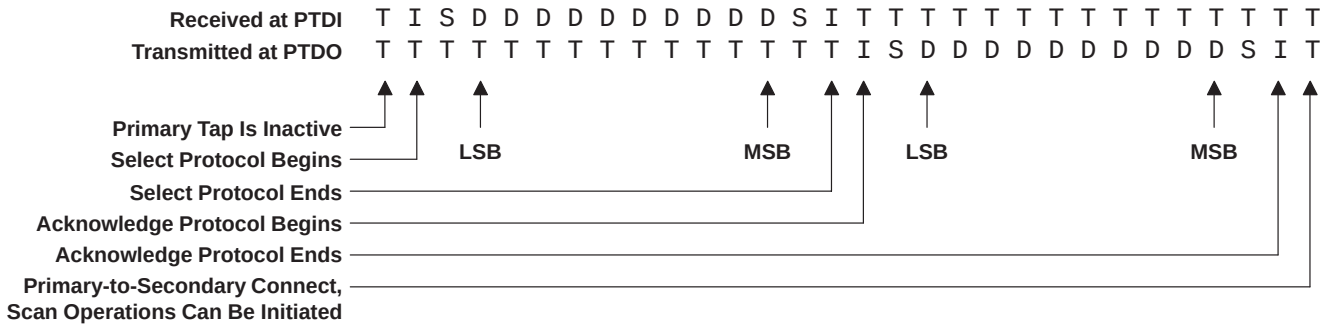


Figure 4. Complete Shadow Protocol

select protocol

The select protocol is the ASP's means of receiving (at PTDI) address information from an IEEE Std 1149.1 bus master. It follows the ISDDDDDDDDDDSI sequence described previously. A 10-bit address value is decoded from the received data-one and/or data-zero bit pairs. These bit pairs are interpreted in least-significant-bit-first order (that is, the first data bit pair received is considered to correspond to A0).

acknowledge protocol

Following the receipt of a complete select-protocol sequence, the protocol result provisionally is set to NO MATCH and the connect status set to OFF. The received address is then compared to that at the ASP address inputs (A9–A0). If these address values match, the ASP immediately (with no delay) responds with an acknowledge protocol transmitted from PTDO. This protocol follows the ISDDDDDDDDDDSI sequence described previously. The transmitted address represents the address of the selected ASP which, by definition, is the same address the ASP received in the select protocol. The 10-bit address value is encoded into data-one and/or data-zero bit pairs. The bit pairs are to be interpreted in least-significant-bit-first order (that is, the first data bit pair transmitted is to be considered to correspond to A0). If the received address does not match that at the A9–A0 inputs, no acknowledge protocol is transmitted and the shadow protocol is considered complete.

protocol errors

Protocol errors occur when bit pairs are received out of sequence. Some of these sequencing errors can be tolerated and are termed *soft* errors. No specific action occurs as the result of a soft error. Other errors represent cases where the addressing information could be incorrectly received and are termed *hard* errors. Hard errors are characterized by sequences in which at least one bit of address data has been properly transmitted followed by a sequencing error. When a hard error occurs, any connection to an ASP is dissolved.

Table 1 lists the bit-pair sequences that result in soft errors and hard errors. A hard error also results when the primary TAP state changes during select protocol following the proper transmission of at least one bit of address data. Figures 16 and 17 show shadow-protocol timing in case of protocol hard error while Figure 18 shows shadow-protocol timing in case of protocol soft error.

Table 1. Shadow-Protocol Errors†

SOFT ERRORS	HARD ERRORS
I(D)I	IS(D)I
I(D)(S)I	IS(D)S(D)I
I(D)(S)(D)I	IS(D)S(S)I
I(S)I	
IS(S)(D)I	
IS(S)(D)(S)I	

† A bit-pair token in parentheses represents one or more instances.

long address

Receipt of an address longer than ten bits is considered a hard error and the ASP assumes OFF status. The sole exceptions are when all data ones are received or all data zeros are received. In these special cases, the global addresses represented by these bit sequences are observed and appropriate action taken. That is, in the case that only data ones (ten or more) are received, the shadow-protocol result is TEST SYNCHRONIZATION (if the primary TAP state is Pause-DR or Pause-IR), and in the case that only data zeros (ten or more) are received, the shadow-protocol result is RESET (see test-synchronization address and reset address).

short address

In all cases, receipt of an address shorter than ten bits is considered a hard error and the ASP assumes OFF status.

connect control

The connect-control block monitors the primary TAP state to enable receipt/acknowledge of shadow protocols in appropriate states (namely, the stable, non-Shift TAP states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR). Upon receipt of a valid shadow protocol, this block performs the address matching required to compute the shadow-protocol result.

TAP-state monitor

The TAP-state monitor is a synchronous finite-state machine that monitors the primary TAP state. The state diagram is shown in Figure 5 and mirrors that specified by IEEE Standard 1149.1-1990. The TAP-state monitor proceeds through its states based on the level of PTMS at the rising edge of PTCK. Each state is described both in terms of its significance for ASP devices and for connected IEEE Std 1149.1-compliant devices (called targets). However, the monitor state (primary TAP) can be different from that of disconnected scan chains (secondary TAP).

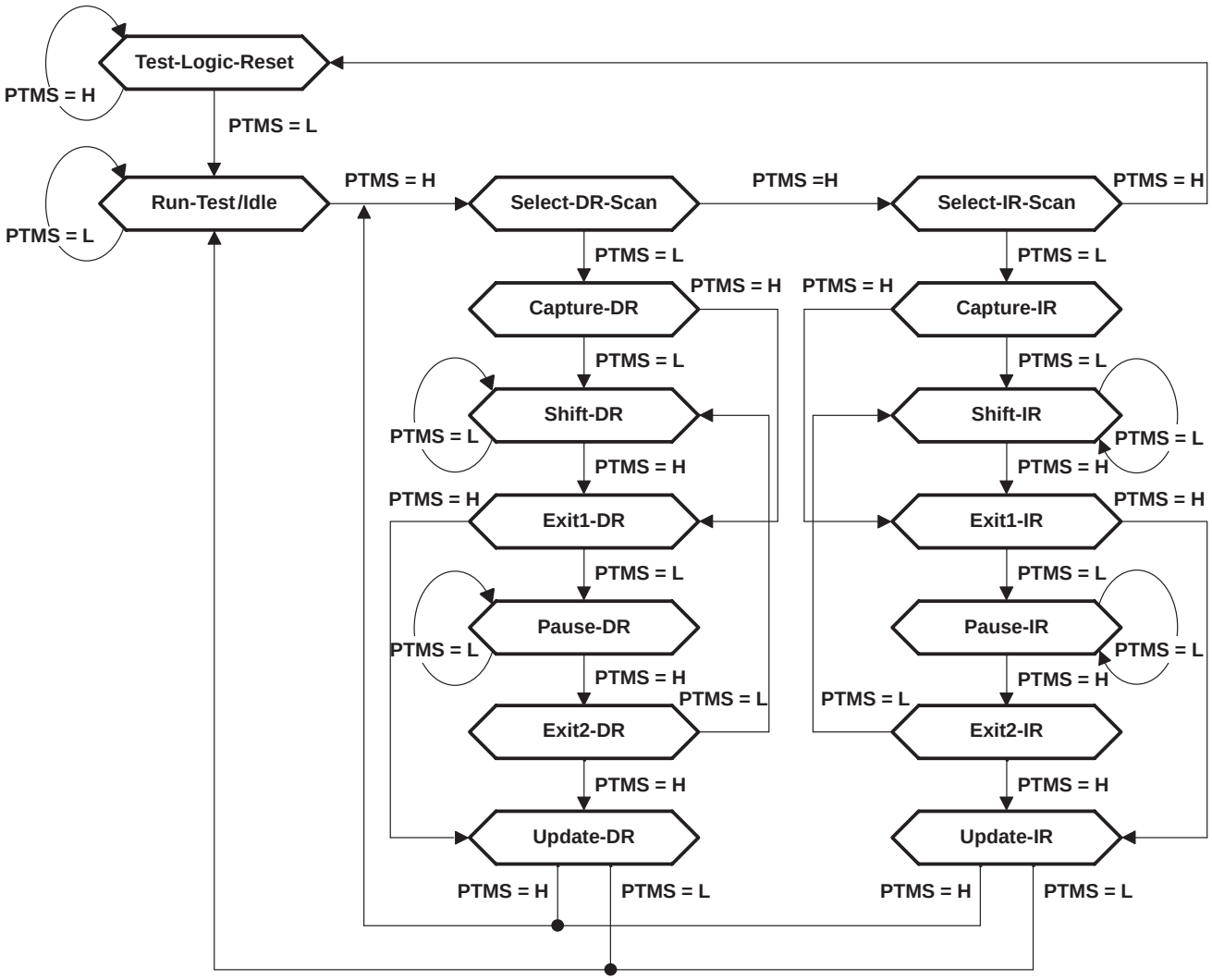


Figure 5. TAP-Monitor State Diagram

Test-Logic-Reset

The ASP TAP-state monitor powers up in the Test-Logic-Reset state. Alternatively, the ASP can be forced asynchronously to this state by assertion of its $\overline{\text{PTRST}}$ input. In the stable Test-Logic-Reset state, the ASP is enabled to receive and respond to shadow protocols. The ASP does not recognize the TSA in this state.

For a target device in the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

Run-Test/Idle

In the stable Run-Test/Idle state, the ASP is enabled to receive and respond to shadow protocols. The ASP does not recognize the TSA in this state.

For a target device, Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

Select-DR-Scan, Select-IR-Scan

The ASP is not enabled to receive and respond to shadow protocols in the Select-DR-Scan and Select-IR-Scan states.

For a target device, no specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

Capture-DR

The ASP is not enabled to receive and respond to shadow protocols in the Capture-DR state.

For a target device in the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the Capture-DR state is exited.

Shift-DR

The ASP is not enabled to receive and respond to shadow protocols in the Shift-DR state.

For a target device, upon entry to the Shift-DR state, the selected data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the selected data register. While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle.

Exit1-DR, Exit2-DR

The ASP is not enabled to receive and respond to shadow protocols in the Exit1-DR and Exit2-DR states.

For a target device, the Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

In the stable Pause-DR state, the ASP is enabled to receive and respond to shadow protocols. Additionally, the TSA can be recognized in this state.

For target devices, no specific function is performed in the stable Pause-DR state. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

Update-DR

The ASP is not enabled to receive and respond to shadow protocols in the Update-DR state.

For a target device, if the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

Capture-IR

The ASP is not enabled to receive and respond to shadow protocols in the Capture-IR state.

For a target device in the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the Capture-IR state is exited.

Shift-IR

The ASP is not enabled to receive and respond to shadow protocols in the Shift-IR state.

For a target device, upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the instruction register. While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle.

Exit1-IR, Exit2-IR

The ASP is not enabled to receive and respond to shadow protocols in the Exit1-IR and Exit2-IR states.

For target devices, the Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

In the stable Pause-IR state, the ASP is enabled to receive and respond to shadow protocols. Additionally, the TSA can be recognized in this state.

For target devices, no specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

Update-IR

The ASP is not enabled to receive and respond to shadow protocols in the Update-IR state.

For target devices, the current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

address matching

Connect status of the ASP is computed by a match of the address received in the last valid shadow protocol against that at the address inputs (A9–A0) as well as against the three dedicated addresses that are internal to the ASP (DSA, RSA, and TSA). The address map is shown in Table 2.

Table 2. Address Map

ADDRESS NAME	BINARY CODE	HEX CODE	SHADOW-PROTOCOL RESULT	RESULTANT PRIMARY-TO-SECONDARY CONNECT STATUS
Reset Address (RSA)	0000000000	000	RESET	RESET
Matching Address	A9–A0	A9–A0	MATCH	ON
Disconnect Address (DSA)	1111111110	3FE	DISCONNECT	OFF
Test Synchronization Address (TSA)	1111111111	3FF	TEST SYNCHRONIZATION	MULTICAST
All Other Addresses	All others	All others	NO MATCH	OFF

If the shadow-protocol address matches the address inputs (A9–A0), then the ASP responds by transmitting an acknowledge protocol. Following the complete transmission of the acknowledge protocol, the ASP assumes ON status (in which PTDI, PTDO, and PTMS are connected to STDO, STDI, and STMS, respectively). The ON status allows the scan chain associated with the ASP's secondary TAP to be controlled from the multidrop primary TAP as if it were directly wired as such. Figures 6 and 7 show the shadow-protocol timing for MATCH result when the prior ASP connect status is ON and OFF, respectively.

If the shadow-protocol address does not match the address inputs (A9–A0), then (unless the address is one of the three dedicated global addresses described below) the ASP responds immediately by assuming the OFF status (in which PTDO and STDO are high impedance and STMS is held at its last level). This has the effect of deselecting the scan chain associated with the ASP secondary TAP, but leaves the TAP state of the scan chain unchanged. No acknowledge protocol is sent. Figures 8 and 9 show the shadow-protocol timing for NO MATCH result when the prior ASP connect status is ON and OFF, respectively.

disconnect address

The disconnect address (DSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the DSA, it immediately responds by assuming the OFF status (in which PTDO and STDO are high impedance and STMS is held at its last level). This has the effect of deselecting the scan chain associated with the ASP secondary TAP, but leaves the TAP state of the scan chain unchanged. No acknowledge protocol is sent. Figures 10 and 11 show the shadow-protocol timing for DISCONNECT result when the prior ASP connect status is ON and OFF, respectively.

The same result occurs when a non-matching address is received. No specific action to disconnect an ASP is required, as a given ASP is disconnected by the address that connects another. The dedicated DSA ensures that at least one address is available for the purpose of disconnecting all receiving ASPs. It is especially useful when the currently selected scan chain is in a different TAP state than that to be selected. In such a case, the DSA is used to leave the former scan chain in the proper state, after which the primary TAP state is moved to that needed to select the latter scan chain.

reset address

The reset address (RSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the RSA, it immediately responds by assuming the RESET status (in which PTDO and STDO are high impedance and STMS is forced to the high level). This has the effect of deselecting and resetting (to Test-Logic-Reset state) the scan chain associated with the ASP secondary TAP. No acknowledge protocol is sent. Figures 12 and 13 show the shadow-protocol timing for RESET result when the prior ASP connect status is ON and OFF, respectively.

test synchronization address

The test synchronization address (TSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the TSA while its secondary TAP state is Pause-DR or Pause-IR, it immediately responds by assuming the MULTICAST status (in which PTDI and PTMS are connected to STDO and STMS respectively, while PTDO is high impedance). No acknowledge protocol is sent. The TSA is valid only when the TAP state of both primary and secondary is Pause-DR or Pause-IR. If the TSA is received when the TAP state of either primary or secondary is Test-Logic-Reset or Run-Test-Idle, the shadow-protocol result is considered to be DISCONNECT. Figures 14 and 15 show the shadow-protocol timing for TEST SYNCHRONIZATION result when the prior ASP connect status is ON and OFF, respectively.

The TSA allows simultaneous operation of the scan chains of all selected ASPs, either for global TAP-state movement or for scan input of common serial test data via PTDI. This is especially useful in the former case, to simultaneously move such scan chains into the Run-Test/Idle state in which module-level or module-to-module BIST operations can operate synchronous to TCK in that TAP state, and in the later case, to scan common test setup/data into multiple like modules.

protocol bypass

Protocol bypass is selected by a low $\overline{\text{BYP}}$ input. This protocol-bypass mode forces the ASP into BYP status (primary TAP signals are connected to secondary TAP signals) regardless of previous shadow-protocol results. The $\overline{\text{CON}}$ output is made active (low). Receipt of shadow protocols is disabled.

When $\overline{\text{BYP}}$ is taken low, the primary TAP serial data signals (PTDI, PTDO) are immediately (asynchronously to PTCK) connected to their respective secondary TAP signals (STDO, STDI). The primary TAP mode-select signal (PTMS) is also connected to its respective secondary TAP signal (STMS) unless $\overline{\text{PTRST}}$ is low, in which case STMS remains high until $\overline{\text{PTRST}}$ is released. Also, the shadow-protocol-receive block is reset to its power-up state and is held in this state such that select protocols appearing at the primary TAP are ignored.

When the $\overline{\text{BYP}}$ input is released (taken high), the ASP immediately (asynchronously to PTCK) resumes the connect status selected by the last valid shadow protocol. The shadow-protocol-receive block is again enabled to respond to select protocols.

Figures 19 and 20 show protocol-bypass timing when the ASP connect status before $\overline{\text{BYP}}$ active is ON and OFF, respectively.

asynchronous reset

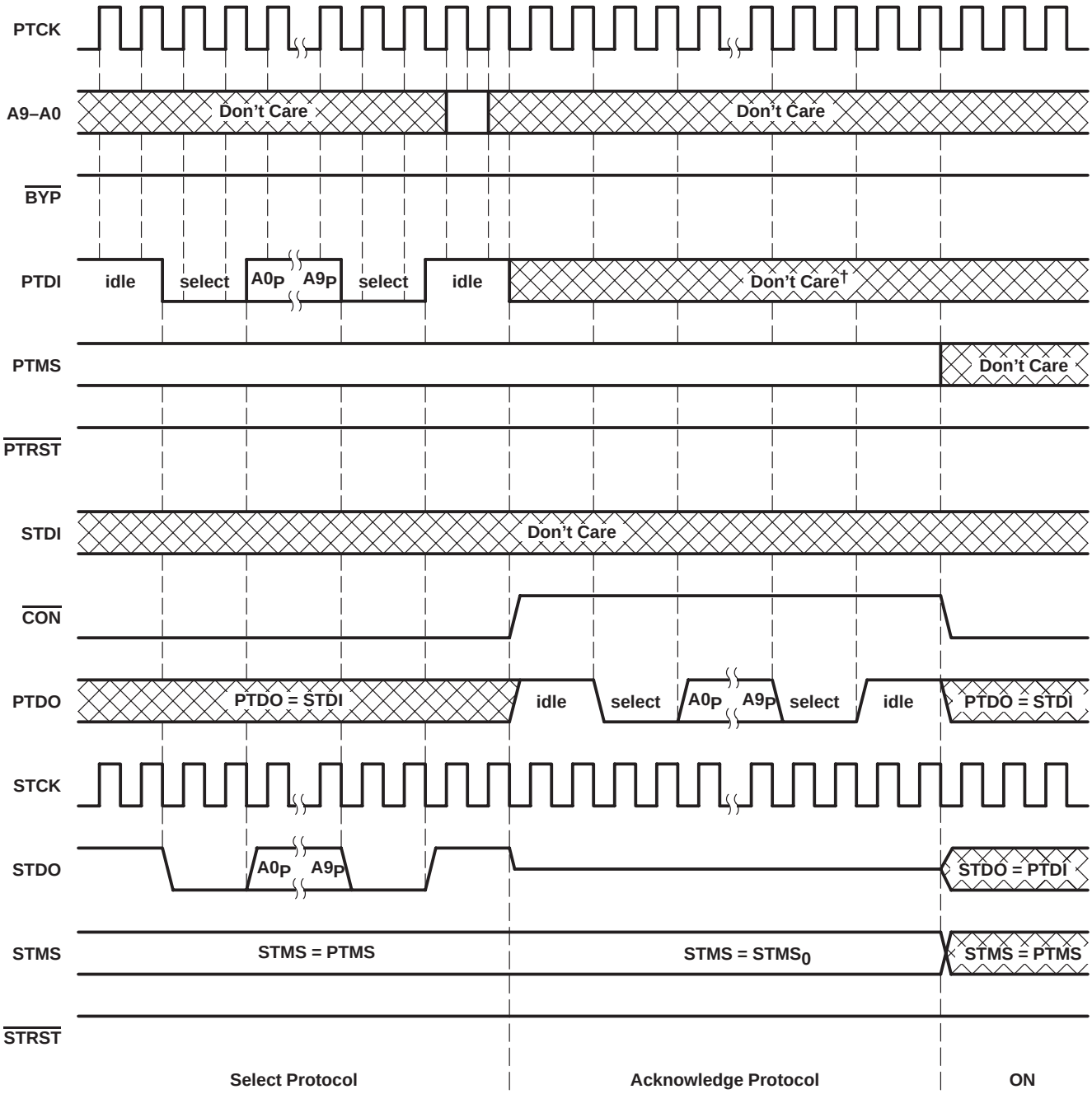
While the $\overline{\text{PTRST}}$ input is always buffered directly to the $\overline{\text{STRST}}$ output, it also serves as an asynchronous reset for the ASP. Given that $\overline{\text{BYP}}$ is high, when $\overline{\text{PTRST}}$ goes low, the ASP immediately assumes TRST status in which $\overline{\text{CON}}$ is high and PTDO and STDO are at high impedance. Otherwise, if $\overline{\text{BYP}}$ is low, the ASP assumes BYP/TRST status. In either case, STMS is set high so that connected IEEE Std 1149.1-compliant devices can be synchronously driven to their Test-Logic-Reset states. While $\overline{\text{PTRST}}$ is low, receipt of shadow protocols is disabled.

Figures 21 and 22 show asynchronous reset timing when the ASP connect status before $\overline{\text{PTRST}}$ active is ON and OFF, respectively. Figure 23 shows asynchronous reset timing when $\overline{\text{BYP}}$ is low.

connect indicator

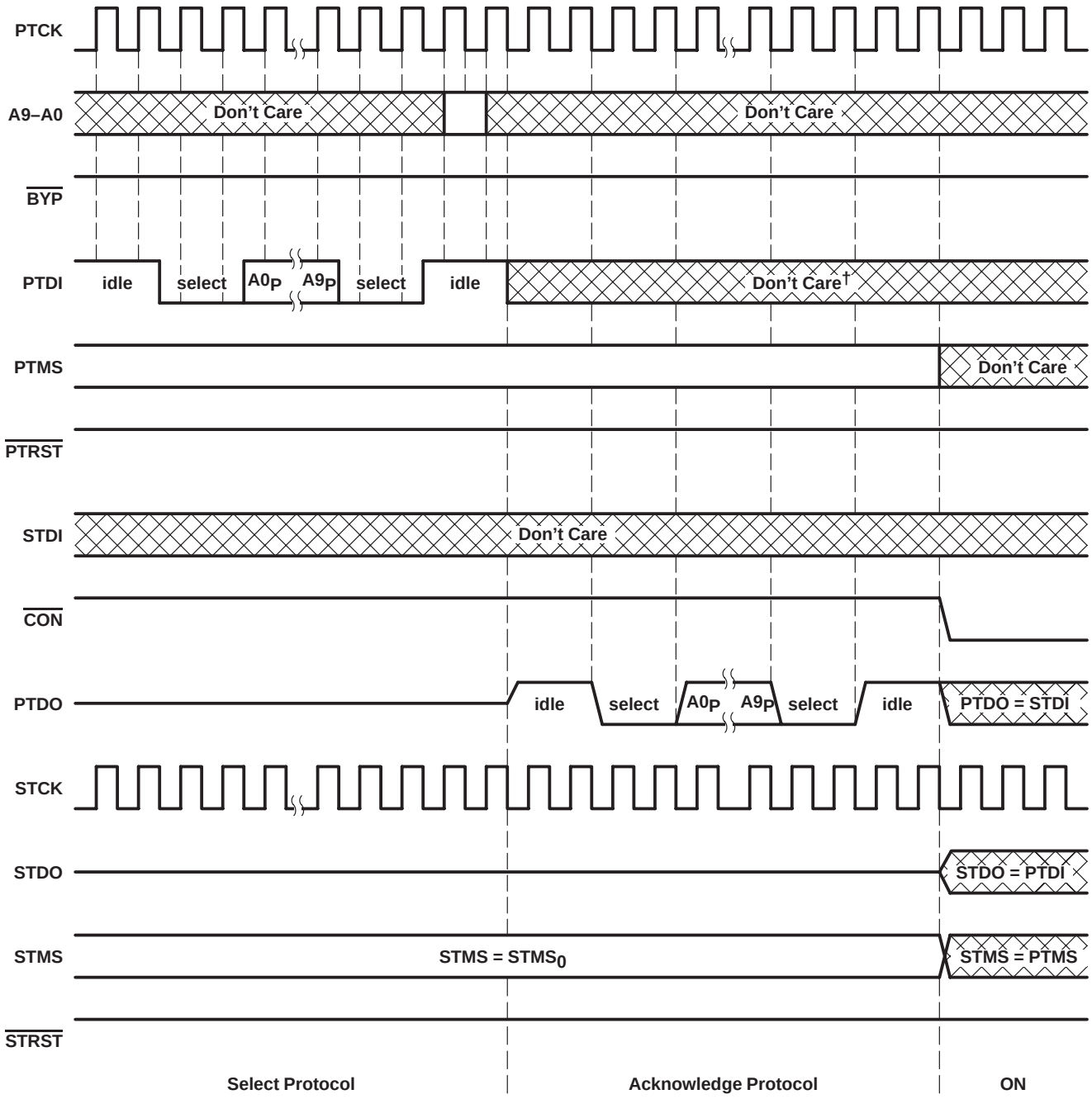
The $\overline{\text{CON}}$ output indicates secondary-scan-port activity (STDO, STMS active) regardless of whether such activity is achieved via protocol bypass or shadow protocol. If the $\overline{\text{BYP}}$ input is low, the $\overline{\text{CON}}$ output is low. Otherwise, if the $\overline{\text{BYP}}$ input is high, the $\overline{\text{CON}}$ output is low if the result of the last valid shadow protocol is MATCH or TEST SYNCHRONIZATION. In all other cases, and while acknowledge protocol is in progress, the $\overline{\text{CON}}$ output is high.

shadow-protocol timing



† The instantaneous value of PTDI during protocol acknowledge is "don't care" as long as the cumulative effect does not represent a protocol hard-error or another valid select protocol.

Figure 6. Shadow-Protocol Timing, Protocol Result = MATCH, Prior Connect Status = ON



† The instantaneous value of PTDI during protocol acknowledge is "don't care" as long as the cumulative effect does not represent a protocol hard-error or another valid select protocol.

Figure 7. Shadow-Protocol Timing, Protocol Result = MATCH, Prior Connect Status = OFF

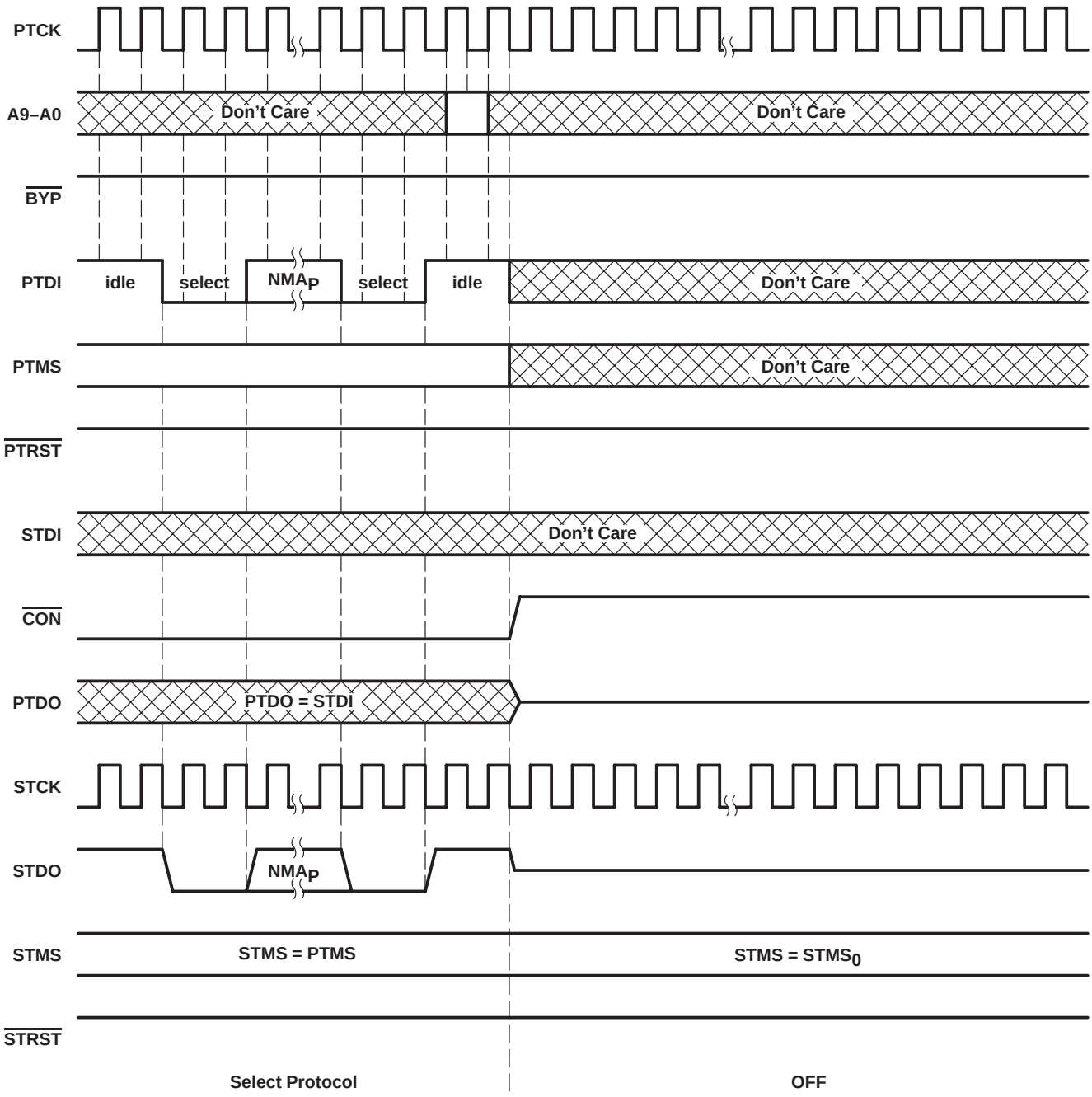


Figure 8. Shadow-Protocol Timing, Protocol Result = NO MATCH, Prior Connect Status = ON

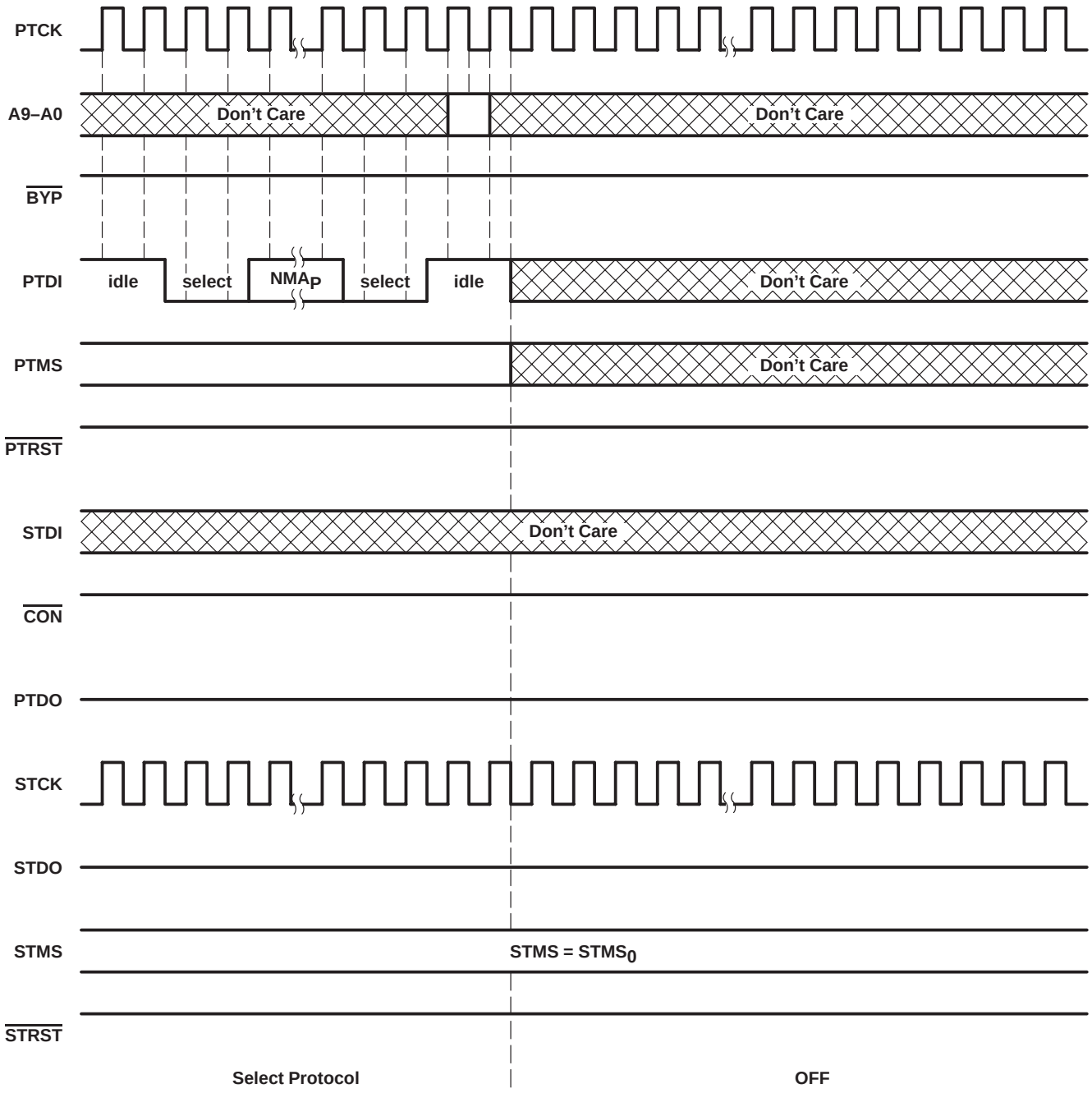


Figure 9. Shadow-Protocol Timing, Protocol Result = NO MATCH, Prior Connect Status = OFF

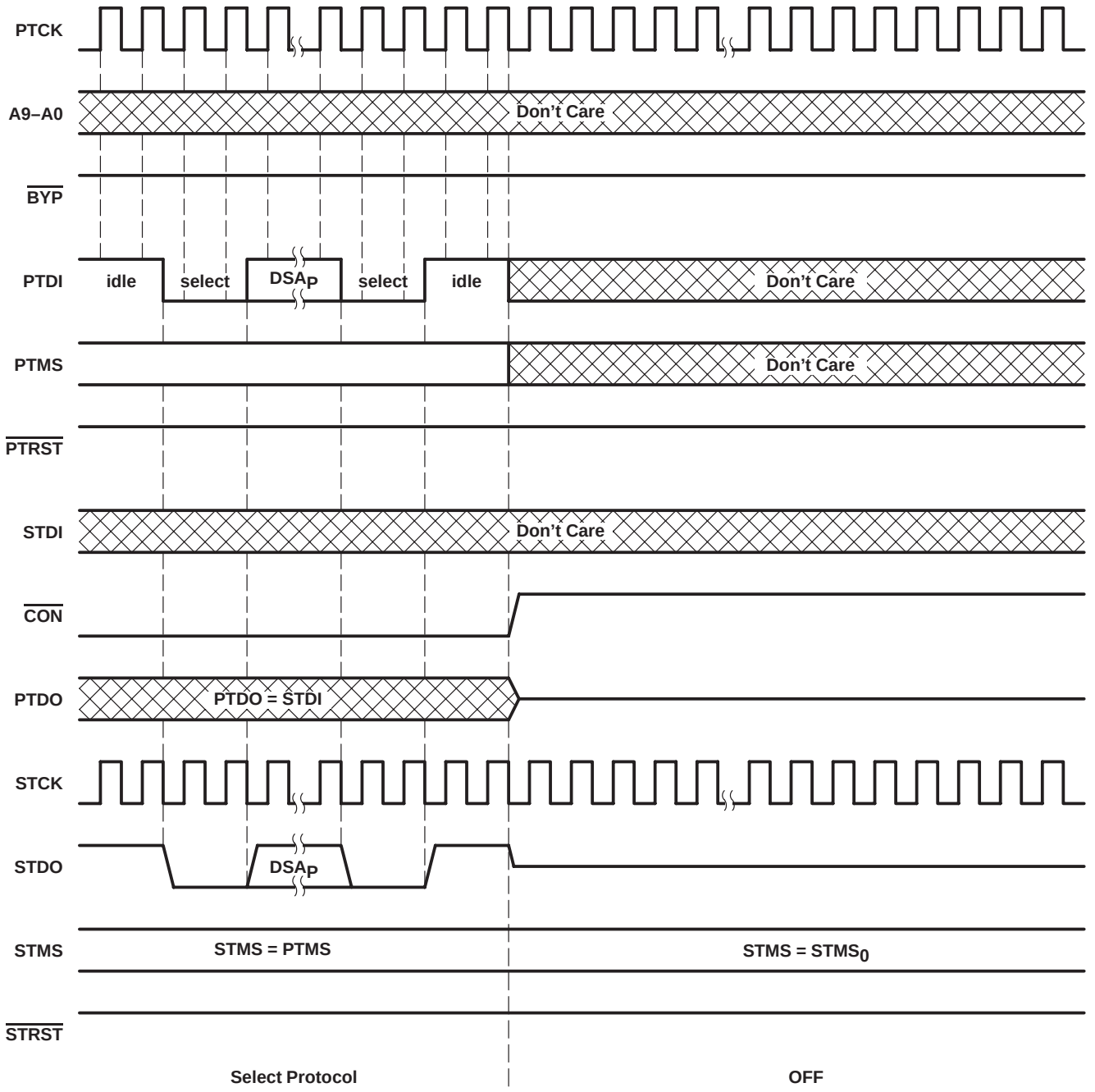


Figure 10. Shadow-Protocol Timing, Protocol Result = DISCONNECT, Prior Connect Status = ON

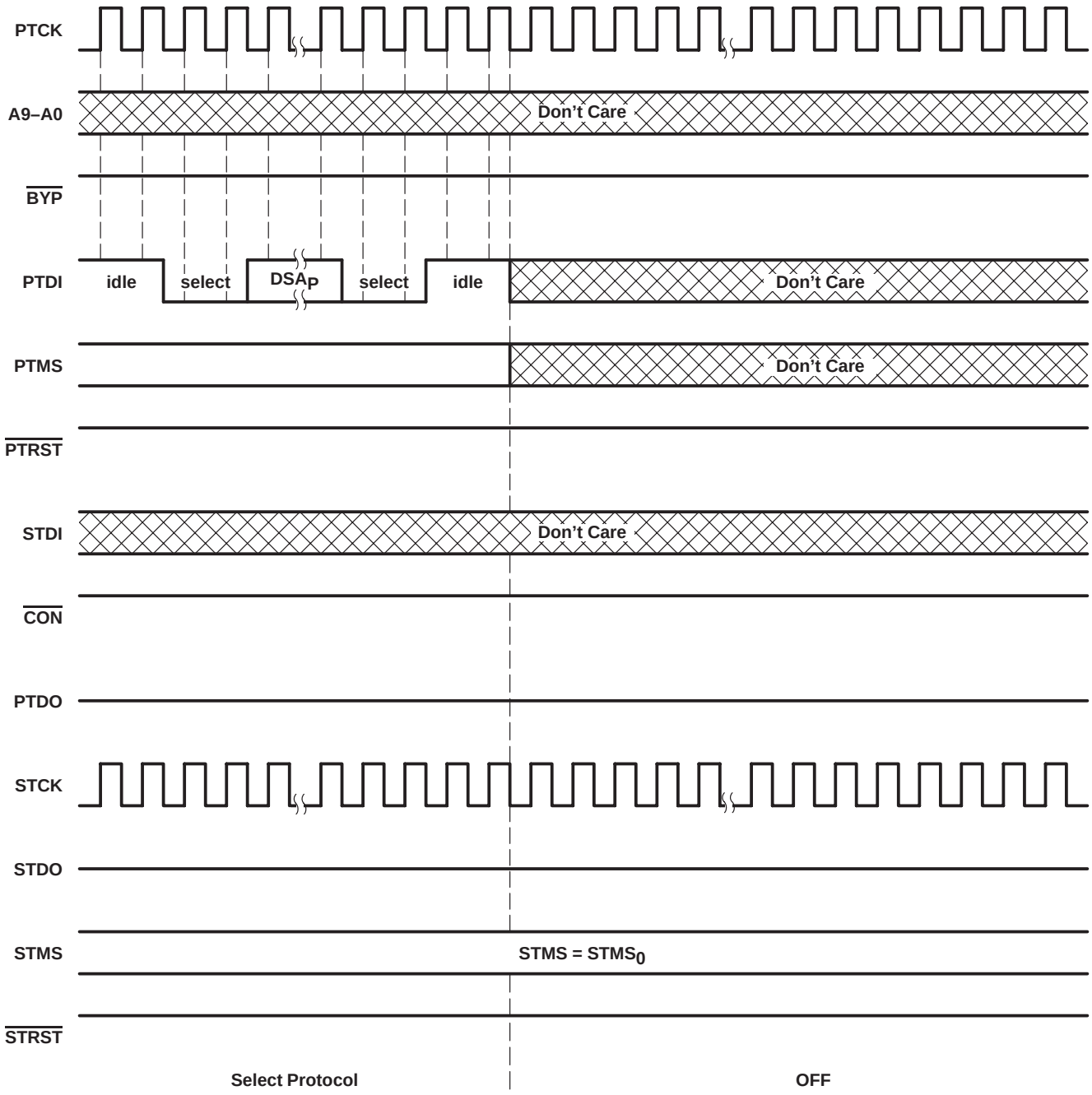


Figure 11. Shadow-Protocol Timing, Protocol Result = DISCONNECT, Prior Connect Status = OFF

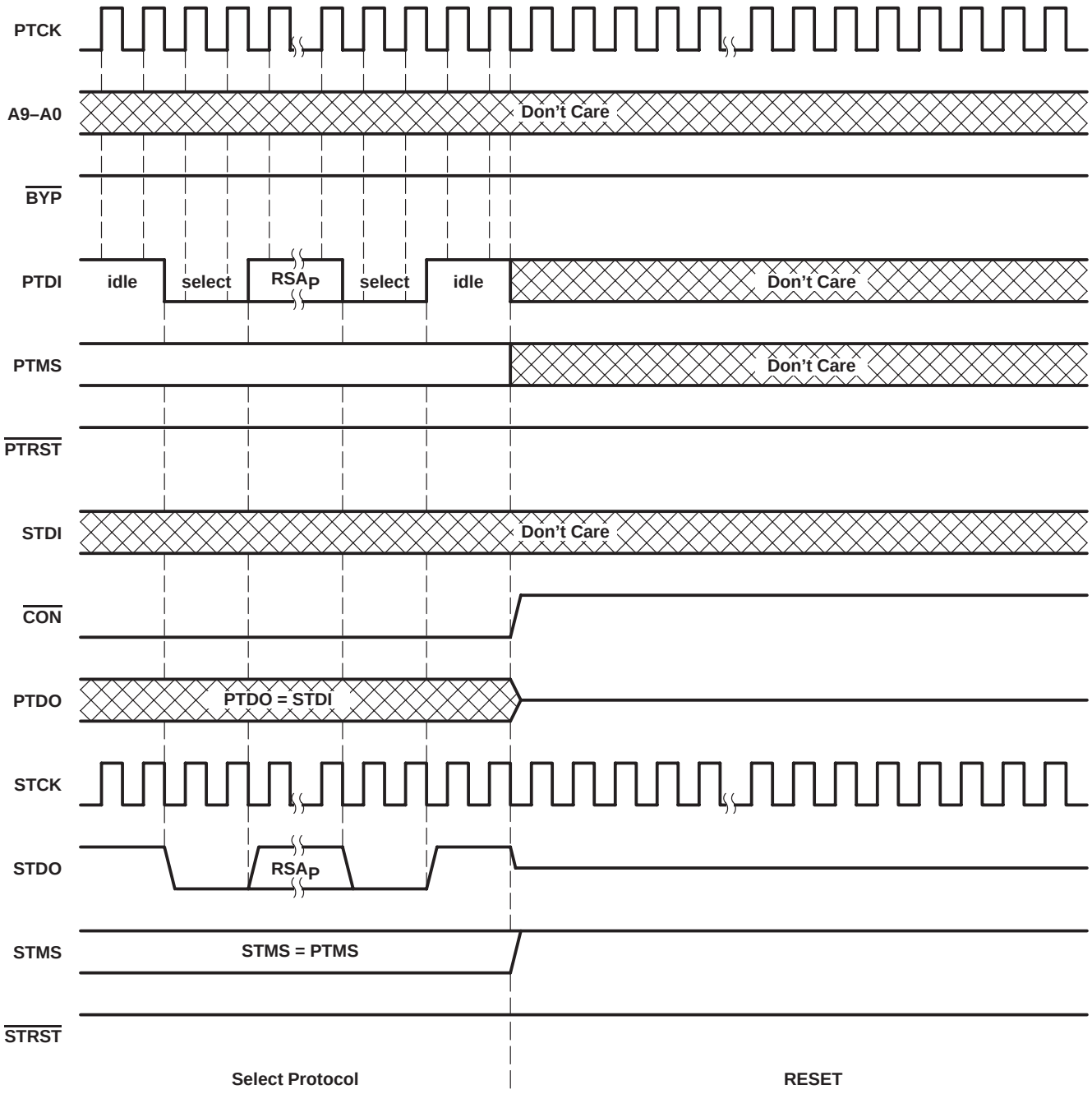


Figure 12. Shadow-Protocol Timing, Protocol Result = RESET, Prior Connect Status = ON

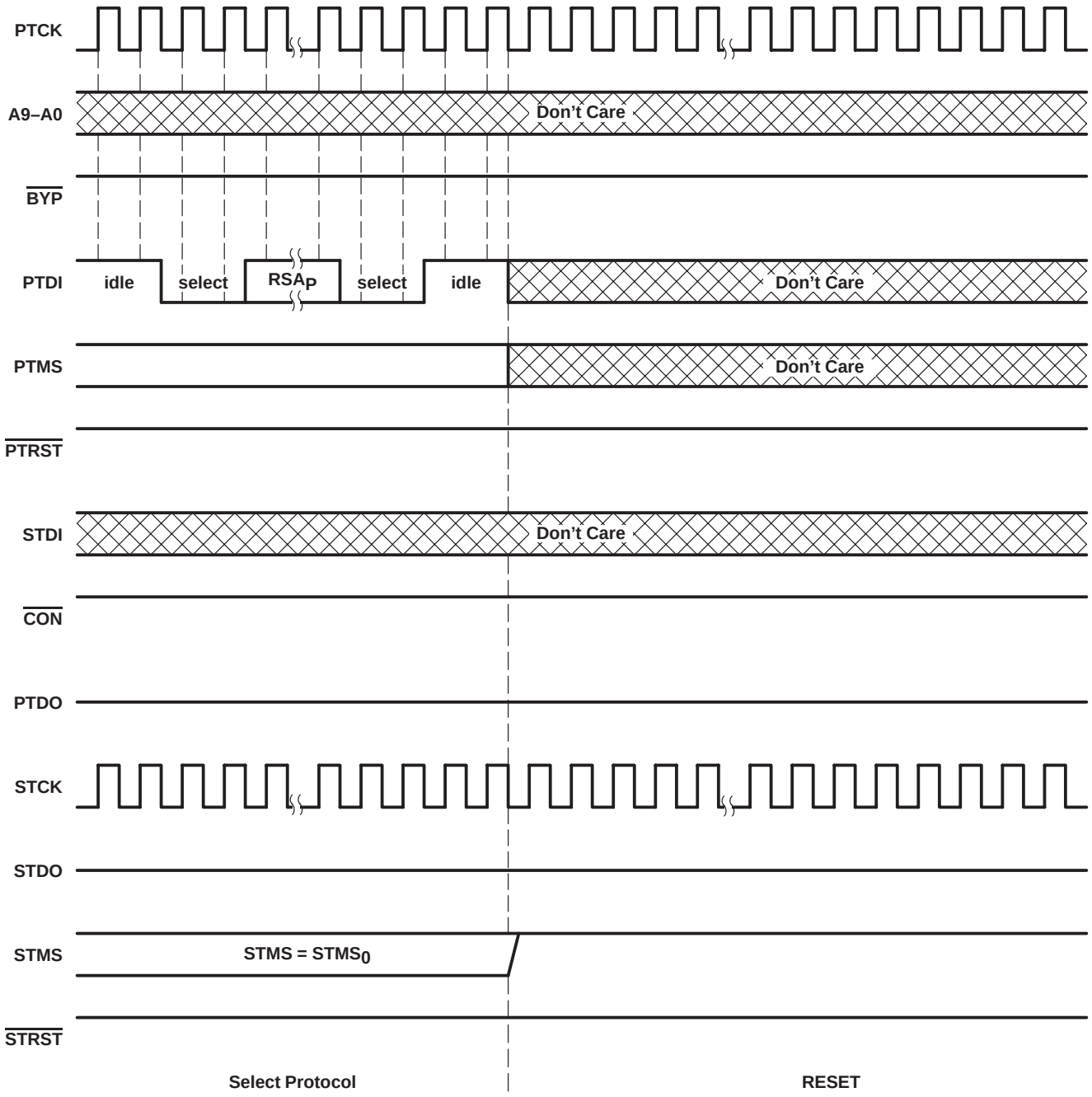


Figure 13. Shadow-Protocol Timing, Protocol Result = RESET, Prior Connect Status = OFF

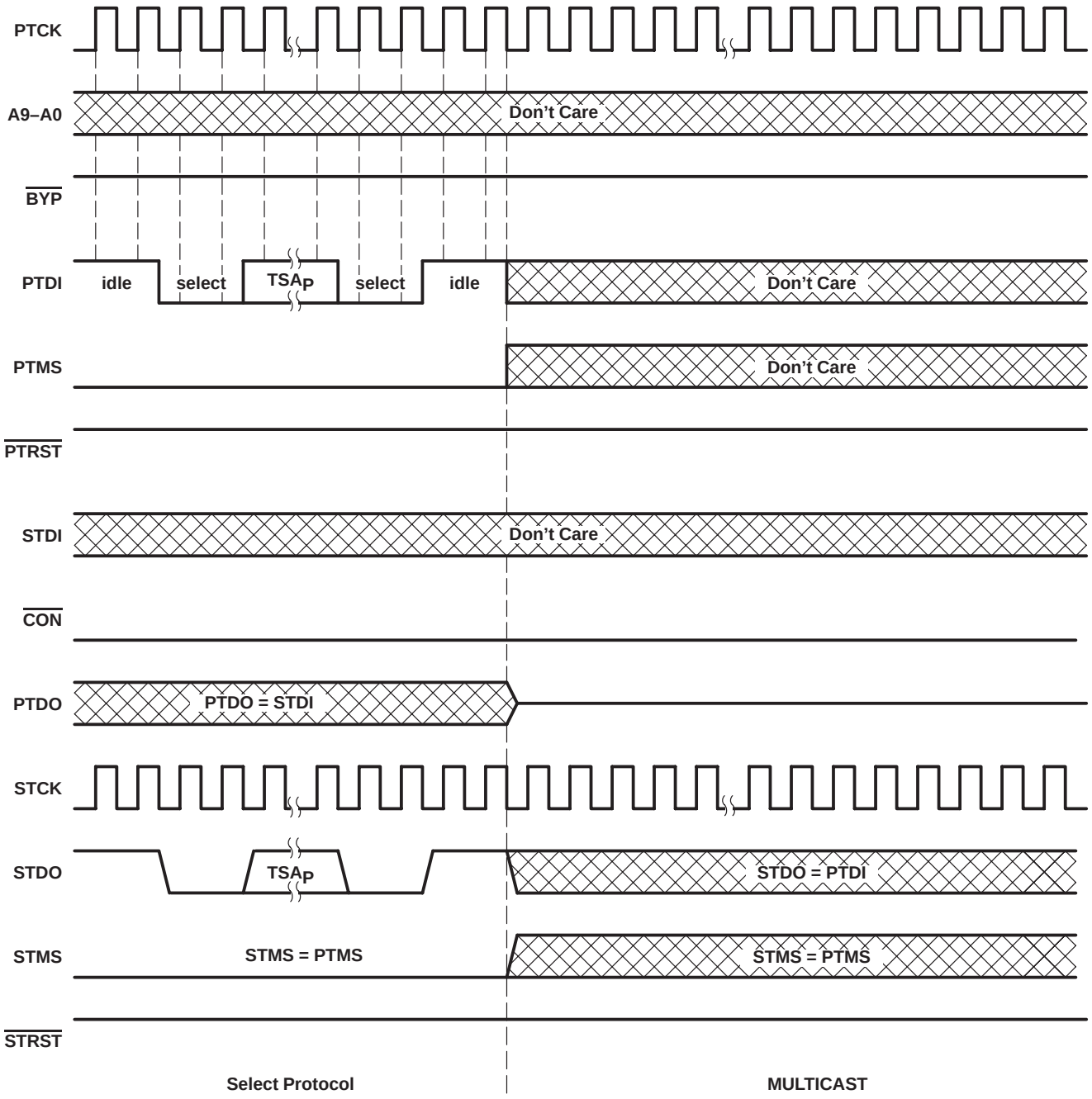


Figure 14. Shadow-Protocol Timing,
Protocol Result = TEST SYNCHRONIZATION, Prior Connect Status = ON

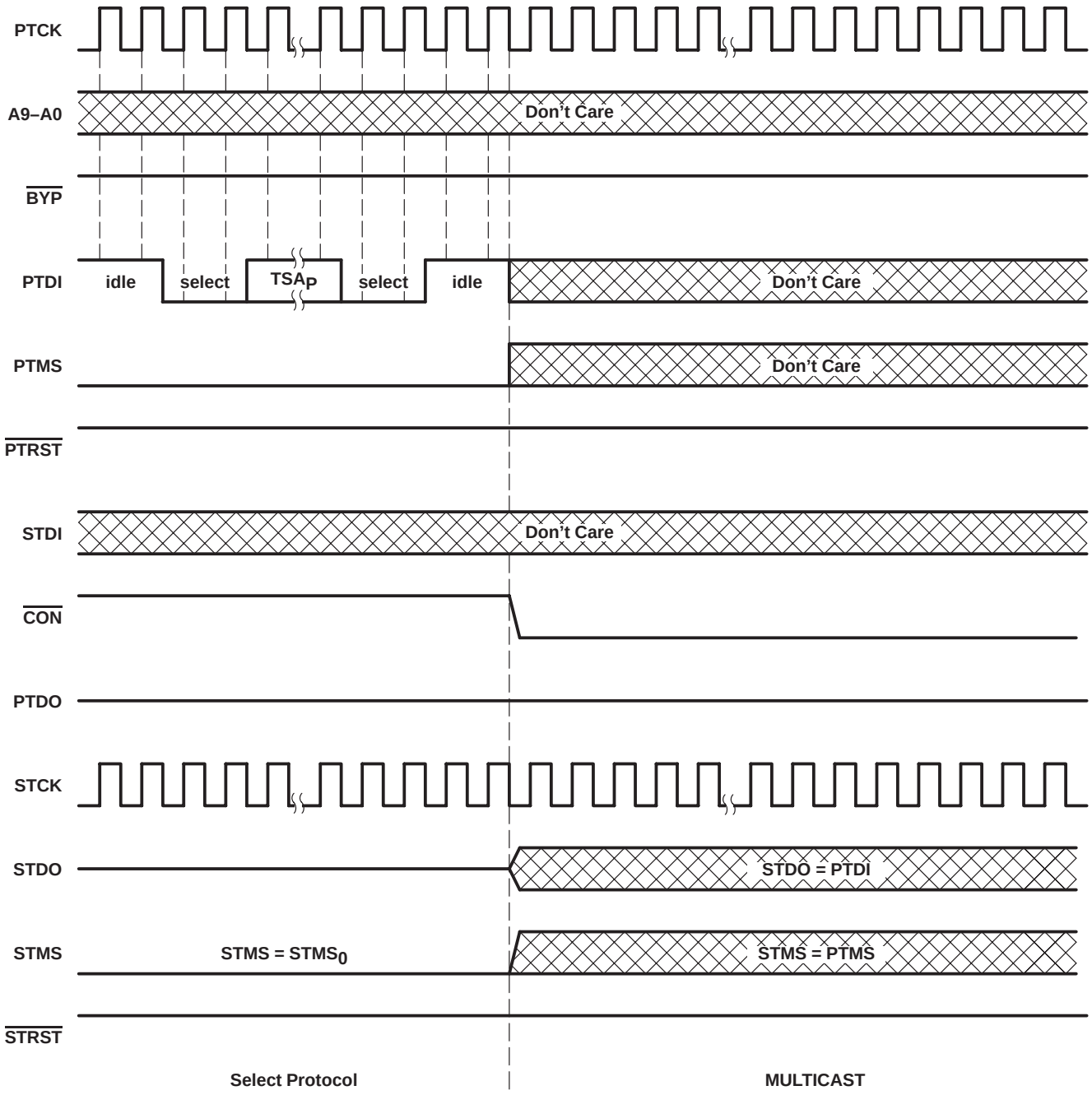
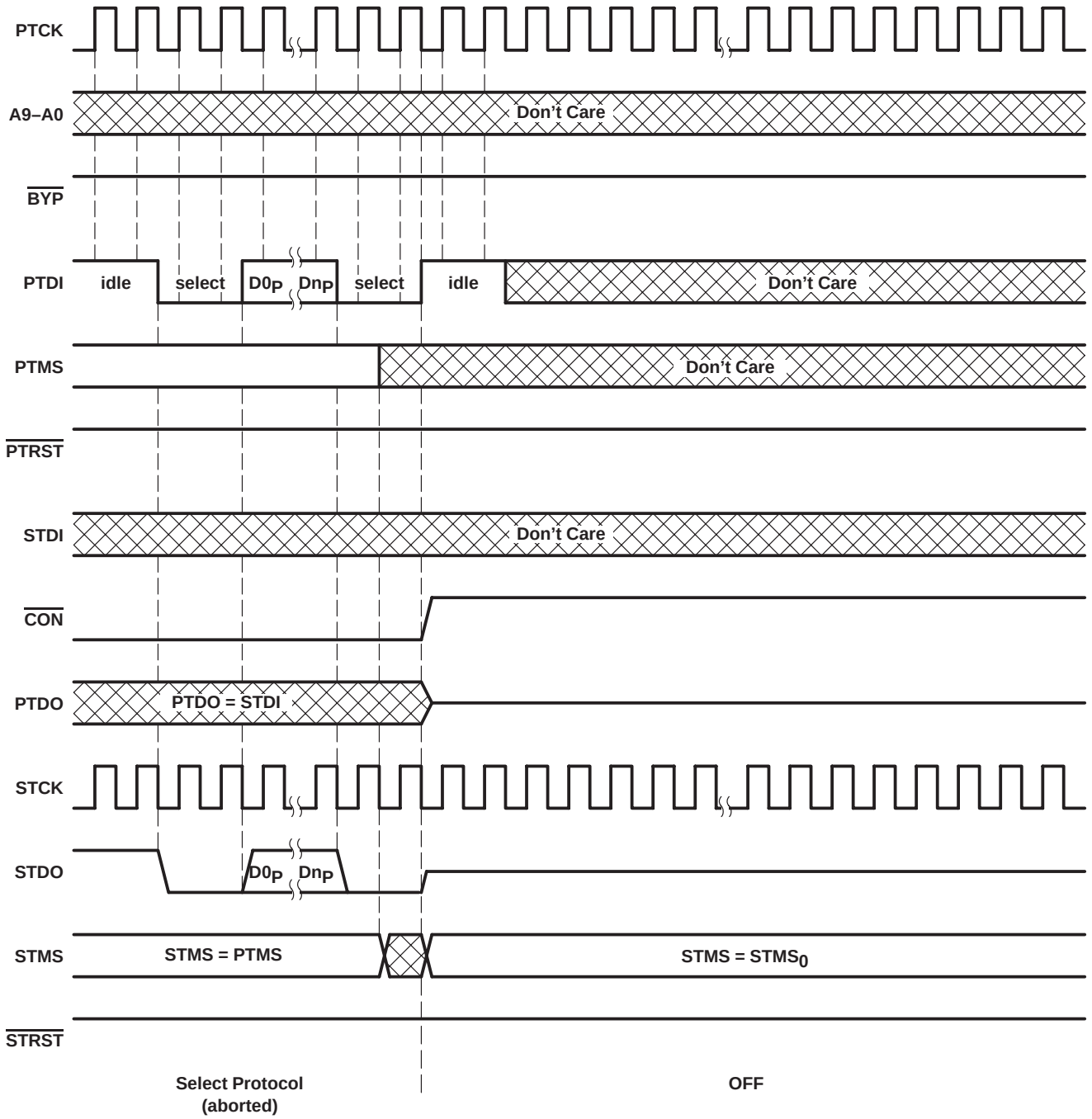
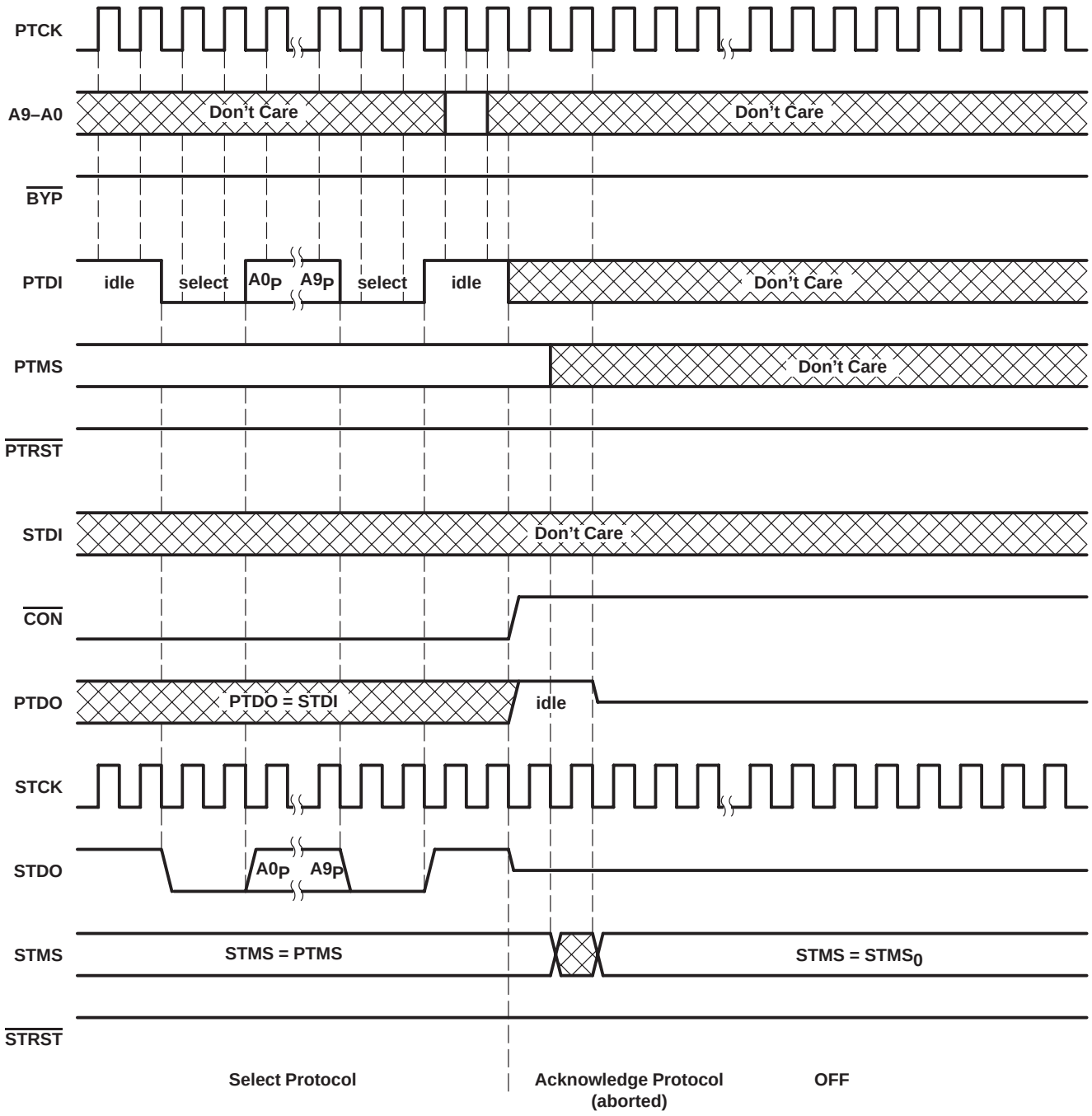


Figure 15. Shadow-Protocol Timing,
Protocol Result = TEST SYNCHRONIZATION, Prior Connect Status = OFF



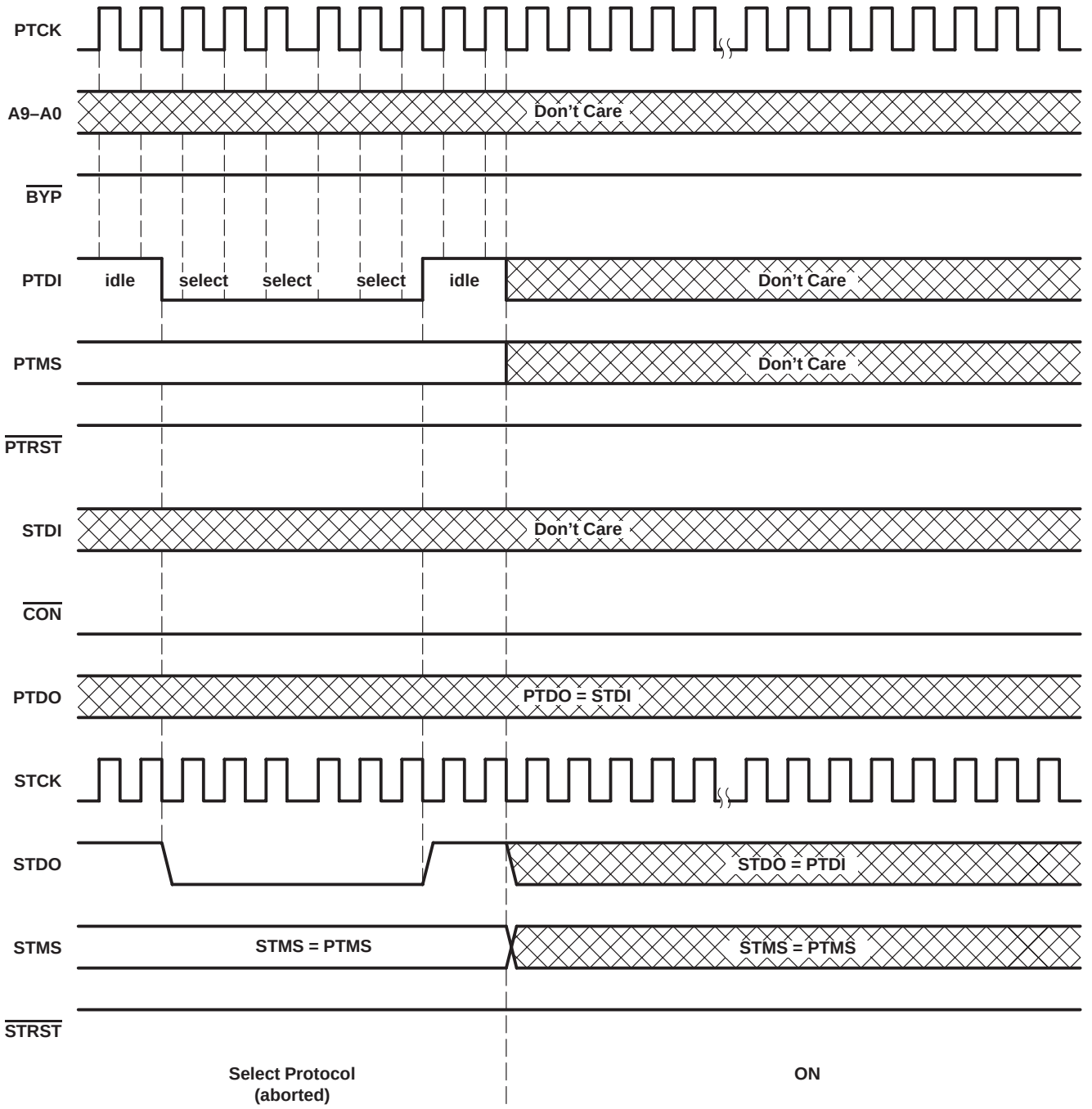
NOTE A: The position of PTMS shown in this figure is only one of many that would produce protocol result HARD ERROR.

Figure 16. Shadow-Protocol Timing,
Protocol Result = HARD ERROR (PTMS change during select protocol), Prior Connect Status = ON



NOTE A: The position of PTMS shown in this figure is only one of many that would produce protocol result HARD ERROR.

**Figure 17. Shadow-Protocol Timing,
Protocol Result = HARD ERROR (PTMS change during acknowledge protocol),
Prior Connect Status = ON**



NOTE A: The sequence of PTDI bits shown in this figure is only one of many that would produce protocol result SOFT ERROR.

**Figure 18. Shadow-Protocol Timing,
Protocol Result = SOFT ERROR, Prior Connect Status = ON**

protocol-bypass timing

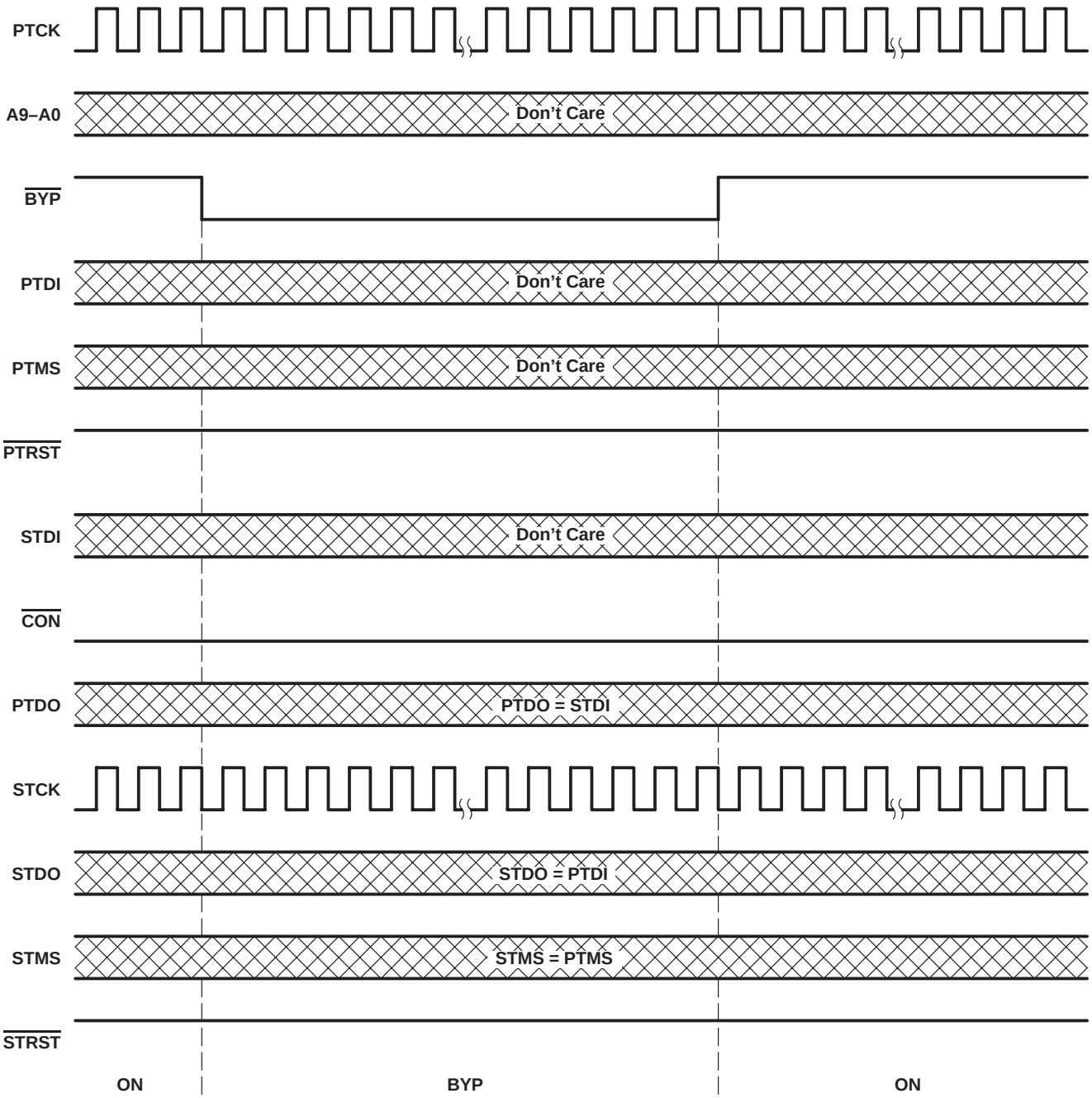


Figure 19. Protocol-Bypass Timing, Prior Connect Status = ON

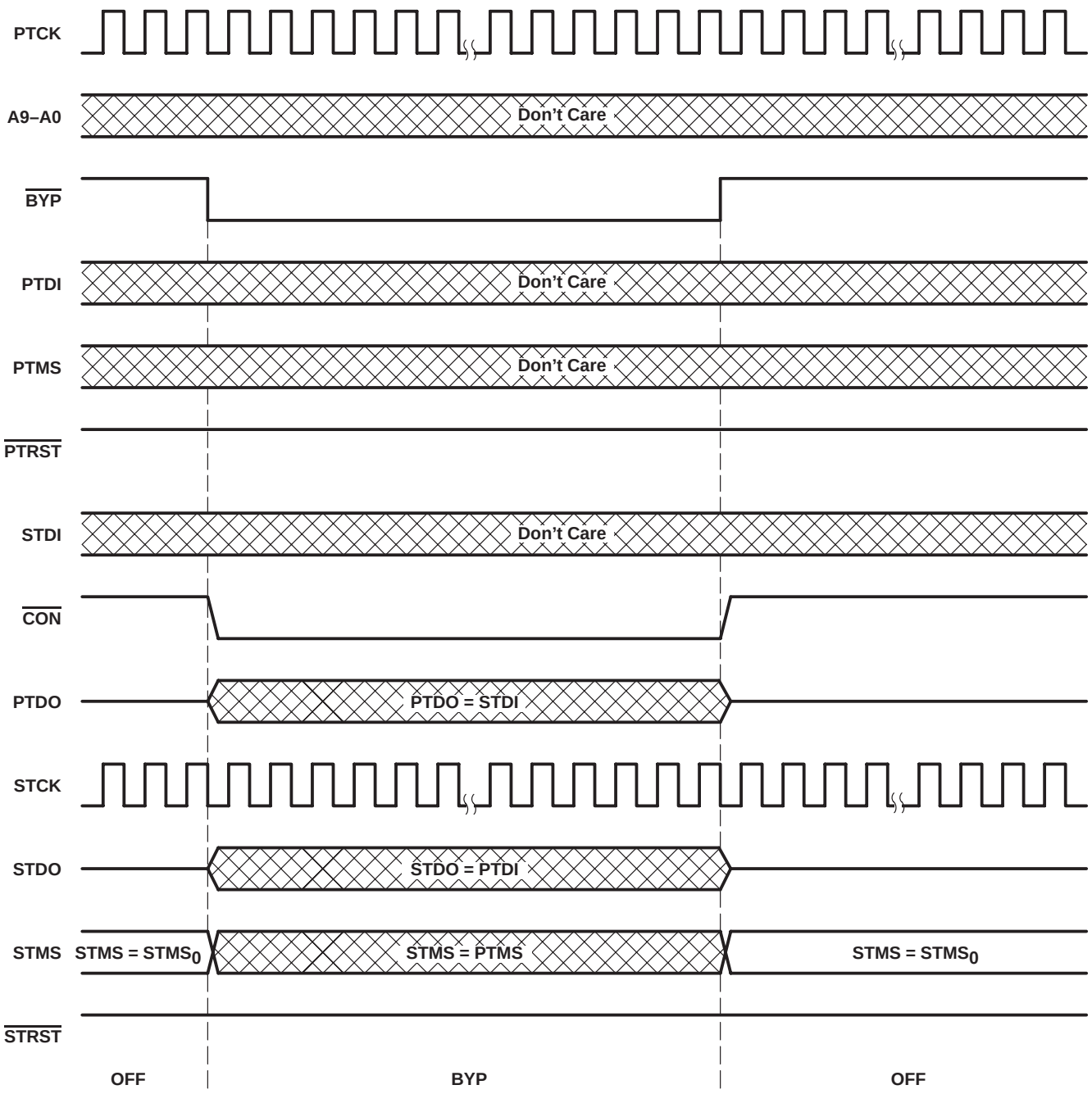


Figure 20. Protocol-Bypass Timing, Prior Connect Status = OFF

asynchronous reset timing

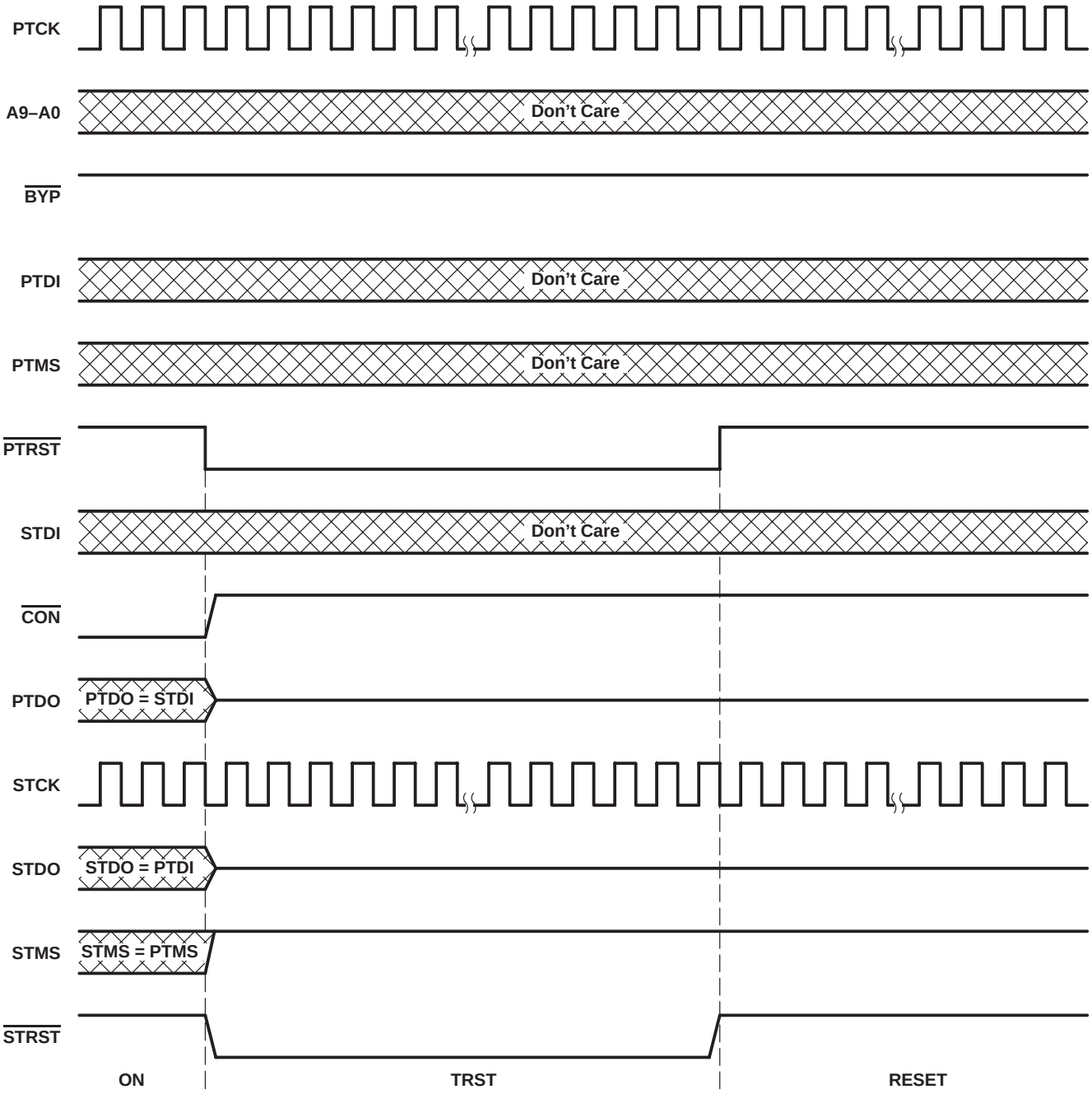


Figure 21. Asynchronous Reset Timing, Prior Connect Status = ON

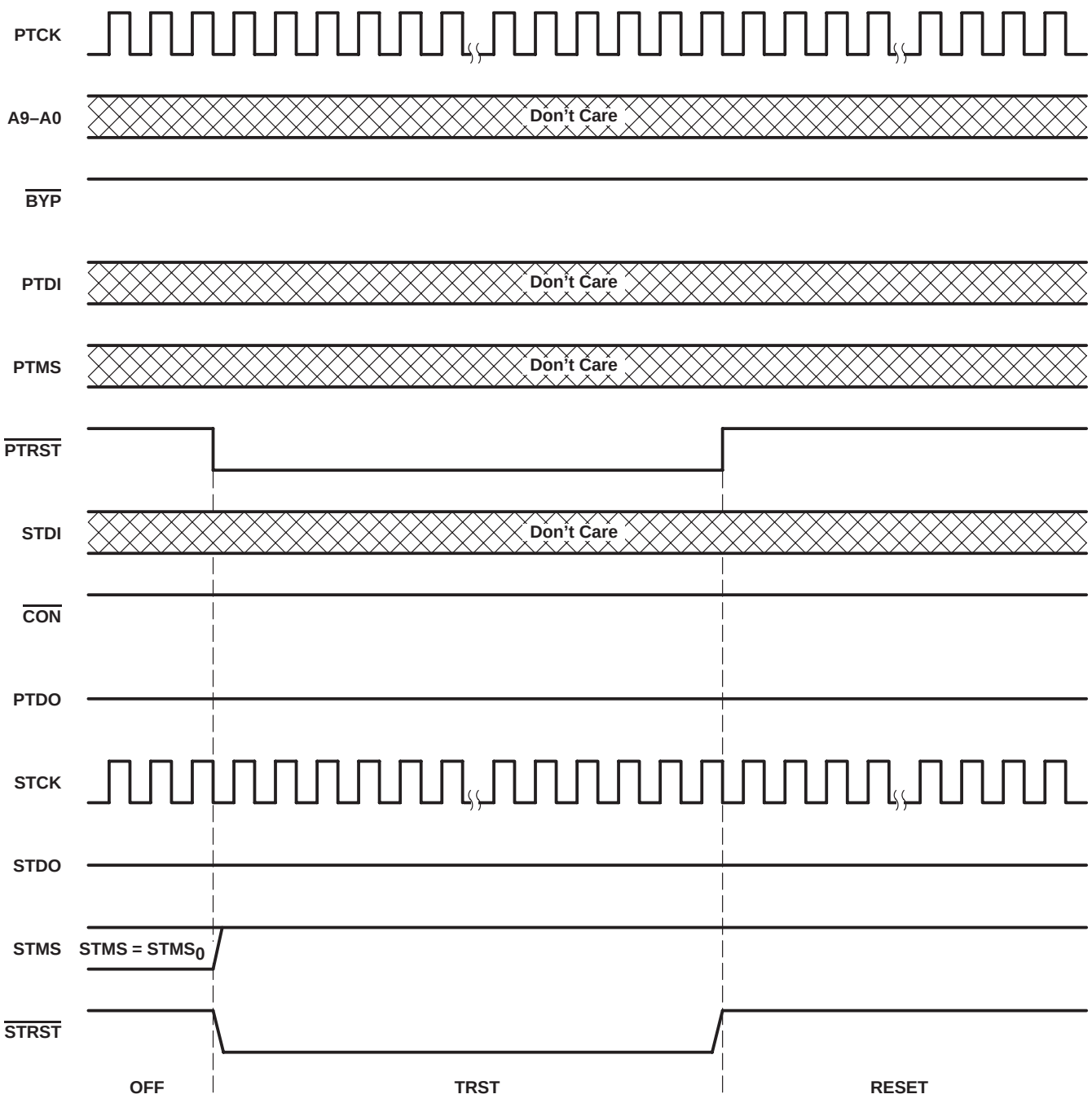


Figure 22. Asynchronous Reset Timing, Prior Connect Status = OFF

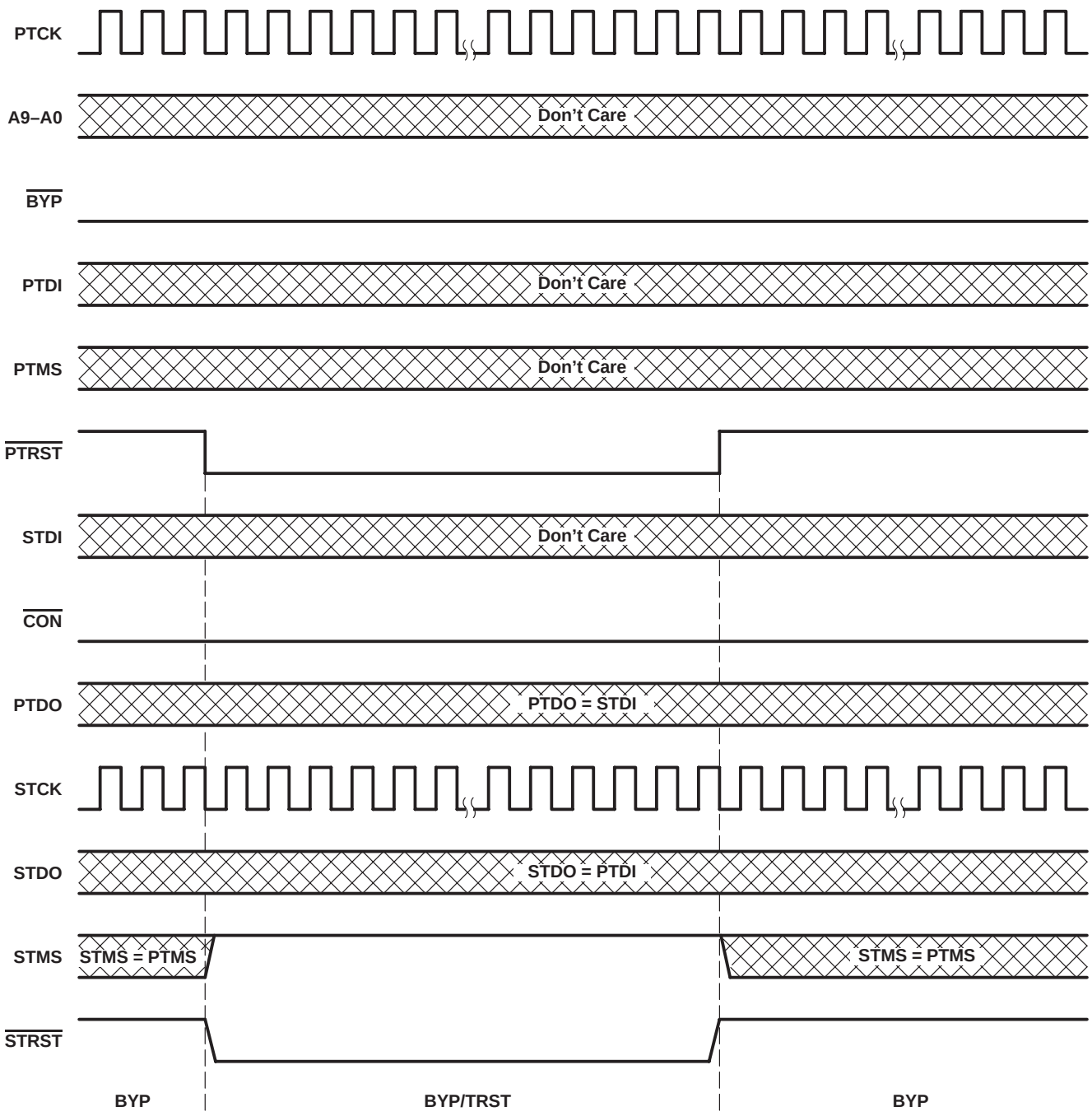


Figure 23. Asynchronous Reset Timing, $\overline{BYP}$ = L

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT8996 . . . . . 96 mA
SN74ABT8996 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 81°C/W
PW package . . . . . 120°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		SN54ABT8996		SN74ABT8996		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT8996		SN74ABT8996		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA		2			2				
		I_{OH} = –32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 0 to 5.5 V, V_I = V_{CC} or GND		PTCK			±1				±1	µA
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	PTDI, PTMS, $\overline{\text{PTRST}}$			10		10		10	µA
			A9–A0, $\overline{\text{BYP}}$, STDI			10		10		10	
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	PTDI, PTMS, $\overline{\text{PTRST}}$	–13		–50	–13	–50	–13	–50	µA
			A9–A0, $\overline{\text{BYP}}$, STDI	–38		–150	–38	–150	–38	–150	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V	PTDO, STDO			10		10		10	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V	PTDO, STDO			–10		–10		–10	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–110	–200	–50	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	OFF, STCK = H, STMS = H			0.8	1.5		1.5		1.5	mA
		ON, PTDO = L, STCK = L, STDO = L, STMS = L			13	18		18		18	
		ON, PTDO = H, STCK = H, STDO = H, STMS = H			3.2	5		5		5	
		TRST, STCK = L			6	8		8		8	
ΔI_{CC}§	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V				5						pF
C_o	V_O = 2.5 V or 0.5 V				8						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)

			SN54ABT8996		SN74ABT8996		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	PTCK	0	40	0	40	MHz
t_w	Pulse duration	$\overline{BYP}$ low†	4.9		4.9		ns
		PTCK high	12		12		
		PTCK low	6.5		6.5		
		$\overline{PTRST}$ low	2.6		2.6		
t_{su}	Setup time	A9–A0 before PTCK↓‡	6.6		6.6		ns
		PTDI before PTCK↑	4.9		4.9		
		PTMS before $\overline{BYP}$↑†	0.8		0.6		
		PTMS before PTCK↑	9		9		
t_h	Hold time	A9–A0 after PTCK↓‡	0.3		0.3		ns
		PTDI after PTCK↑	0.7		0.7		
		PTMS after $\overline{BYP}$↑†	2.4		2.4		
		PTMS after PTCK↑	1.3		1.3		

† In normal application of the ASP, such timing requirements with respect to $\overline{BYP}$ are met implicitly and, therefore, need not be considered.
‡ These requirements apply only in the case where the address inputs are changed during a shadow protocol. For normal application of the ASP, it is recommended that the address inputs remain static throughout any shadow protocols. In such cases, the timing of address inputs relative to PTCK need not be considered.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT8996					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}	PTCK		40			40		MHz
t_{PLH}	$\overline{BYP}\uparrow$	$\overline{CON}$	1	3	4.2	1	5.3	ns
t_{PHL}	$\overline{BYP}\downarrow$		1	3.8	5.2	1	6.3	
t_{PLH}	$\overline{BYP}\downarrow$	STMS	2.5	7.8	10	2.5	12.9	ns
t_{PHL}			2.5	5.2	7	2.5	8.9	
t_{PLH}	PTCK	STCK	1	2.2	3.1	1	3.7	ns
t_{PHL}			1	2.8	3.9	1	4.6	
t_{PLH}	PTCK↓	$\overline{CON}$	3.5	6.9	8.9	3.5	11.2	ns
t_{PHL}			3.5	7	9.3	3.5	11.6	
t_{PLH}	PTCK↓ (shadow-protocol acknowledge)	PTDO	3	7.6	9.9	3	12.6	ns
t_{PHL}			3	6.2	9.4	3	10.9	
t_{PLH}†	PTCK↓ (connect)	STMS	5.5	12.1	15.4	5.5	19.9	ns
t_{PHL}†			5.5	9.7	12.5	5.5	15.8	
t_{PLH}	PTDI	STDO	1	3.1	4.4	1	5.4	ns
t_{PHL}			1	3.3	4.5	1	5.6	
t_{PLH}	PTMS	STMS	1	3.2	4.4	1	5.5	ns
t_{PHL}			1	3.4	4.7	1	5.7	
t_{PLH}	$\overline{PTRST}$	$\overline{STRST}$	1	3.2	4.8	1	5.8	ns
t_{PHL}			1	3.3	4.7	1	5.7	
t_{PLH}	$\overline{PTRST}\downarrow$	$\overline{CON}$	3.5	7.4	9.5	3.5	12.1	ns
		STMS	2.5	5.6	7.7	2.5	9.6	
t_{PLH}	STDI	PTDO	1	2.8	4	1	4.9	ns
t_{PHL}			1	3.3	4.6	1	5.7	

† The transitions at STMS are possible only when a shadow-protocol select is issued while STMS is held (in the OFF status) at a level that differs from that at PTMS. Such operation is not recommended since state synchronization of the primary TAP to secondary TAP cannot be ensured.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued) (see Figure 24)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT8996					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PZH}†	$\overline{BYP}$↓	PTDO	1.5	4	5.5	1.5	6.9	ns
t_{PZL}			1.5	4.5	6.1	1.5	7.5	
t_{PZH}‡	$\overline{BYP}$↓	STDO	1.5	3.7	5.2	1.5	6.2	ns
t_{PZL}			1.5	4.2	5.8	1.5	6.9	
t_{PZH}†	PTCK↓	PTDO	4	7.2	9.5	4	12.1	ns
t_{PZH}‡	PTCK↓	STDO	4	7.6	10	4	12.5	ns
t_{PZL}			4	8.1	10.7	4	12.8	
t_{PHZ}†	$\overline{BYP}$↑	PTDO	1.5	3.6	4.8	1.5	5.5	ns
t_{PLZ}			1.3	3.6	4.9	1.3	5.8	
t_{PHZ}‡	$\overline{BYP}$↑	STDO	1.5	3.6	4.8	1.5	5.5	ns
t_{PLZ}			1.5	3	4.2	1.5	4.8	
t_{PHZ}†	PTCK↓	PTDO	3	6.2	8.2	3	11	ns
t_{PLZ}			1	6.9	9.5	1	13.1	
t_{PHZ}‡	PTCK↓	STDO	3.5	7.3	9.2	3.5	12	ns
t_{PLZ}§			1	7.1	8.7	1	10.4	
t_{PHZ}†	$\overline{PTRST}$↓	PTDO	3.5	6.6	9.2	3.5	11	ns
t_{PLZ}			1	7.4	10.2	1	13.4	
t_{PHZ}‡	$\overline{PTRST}$↓	STDO	4.5	9.4	12	4.5	13.6	ns
t_{PLZ}			3	7.3	9	3	10.5	

† In most applications, the node to which PTDO is connected has a pullup resistor. In such cases, this parameter is not significant.
‡ In most applications, the node to which STDO is connected has a pullup resistor. In such cases, this parameter is not significant.
§ This parameter applies only in case of protocol hard error.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT8996					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}	PTCK		40			40		MHz
t_{PLH}	$\overline{BYP}\uparrow$	$\overline{CON}$	1	3	4.2	1	4.8	ns
t_{PHL}	$\overline{BYP}\downarrow$		1	3.8	5.2	1	6	
t_{PLH}	$\overline{BYP}\downarrow$	STMS	2.5	7.8	10	2.5	12.2	ns
t_{PHL}			2.5	5.2	7	2.5	8.4	
t_{PLH}	PTCK	STCK	1	2.2	3.1	1	3.4	ns
t_{PHL}			1	2.8	3.9	1	4.5	
t_{PLH}	PTCK↓	$\overline{CON}$	3.5	6.9	8.9	3.5	10.6	ns
t_{PHL}			3.5	7	9.3	3.5	10.8	
t_{PLH}	PTCK↓ (shadow-protocol acknowledge)	PTDO	3	7.6	9.9	3	11.8	ns
t_{PHL}			3	6.2	9.4	3	10.2	
t_{PLH}†	PTCK↓ (connect)	STMS	5.5	12.1	15.4	5.5	18.6	ns
t_{PHL}†			5.5	9.7	12.5	5.5	14.9	
t_{PLH}	PTDI	STDO	1	3.1	4.4	1	5	ns
t_{PHL}			1	3.3	4.5	1	5.3	
t_{PLH}	PTMS	STMS	1	3.2	4.4	1	5.1	ns
t_{PHL}			1	3.4	4.7	1	5.5	
t_{PLH}	$\overline{PTRST}$	$\overline{STRST}$	1	3.2	4.8	1	5.7	ns
t_{PHL}			1	3.3	4.7	1	5.7	
t_{PLH}	$\overline{PTRST}\downarrow$	$\overline{CON}$	3.5	7.4	9.5	3.5	11.4	ns
		STMS	2.5	5.6	7.7	2.5	9.2	
t_{PLH}	STDI	PTDO	1	2.8	4	1	4.5	ns
t_{PHL}			1	3.3	4.6	1	5.4	

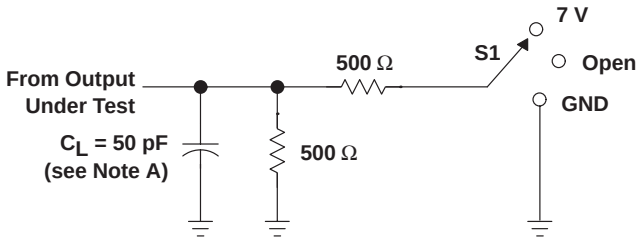
† The transitions at STMS are possible only when a shadow-protocol select is issued while STMS is held (in the OFF status) at a level that differs from that at PTMS. Such operation is not recommended since state synchronization of the primary TAP to secondary TAP cannot be ensured.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued) (see Figure 24)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT8996					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PZH}†	$\overline{BYP}$↓	PTDO	1.5	4	5.5	1.5	6.6	ns
t_{PZL}			1.5	4.5	6.1	1.5	7.2	
t_{PZH}‡	$\overline{BYP}$↓	STDO	1.5	3.7	5.2	1.5	6	ns
t_{PZL}			1.5	4.2	5.8	1.5	6.7	
t_{PZH}†	PTCK↓	PTDO	4	7.2	9.5	4	11.3	ns
t_{PZH}‡	PTCK↓	STDO	4	7.6	10	4	11.7	ns
t_{PZL}			4	8.1	10.7	4	12.2	
t_{PHZ}†	$\overline{BYP}$↑	PTDO	1.5	3.6	4.8	1.5	5.3	ns
t_{PLZ}			1.5	3.6	4.9	1.5	5.3	
t_{PHZ}‡	$\overline{BYP}$↑	STDO	1.5	3.6	4.8	1.5	5.4	ns
t_{PLZ}			1.5	3	4.2	1.5	4.4	
t_{PHZ}†	PTCK↓	PTDO	3	6.2	8	3	10.3	ns
t_{PLZ}			3	6.9	9.5	3	11.2	
t_{PHZ}‡	PTCK↓	STDO	3.5	7.3	9	3.5	10.9	ns
t_{PLZ}§			3.5	7.1	8.7	3.5	10.4	
t_{PHZ}†	$\overline{PTRST}$↓	PTDO	3.5	6.6	8.5	3.5	10.4	ns
t_{PLZ}			3.5	7.4	10.2	3.5	11.7	
t_{PHZ}‡	$\overline{PTRST}$↓	STDO	4.5	9.4	11.5	4.5	13.2	ns
t_{PLZ}			4.5	7.3	9	4.5	10.5	

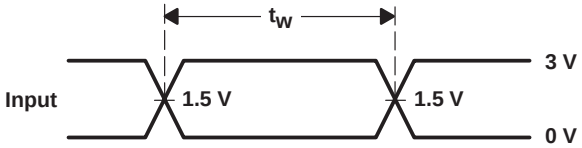
† In most applications, the node to which PTDO is connected has a pullup resistor. In such cases, this parameter is not significant.
‡ In most applications, the node to which STDO is connected has a pullup resistor. In such cases, this parameter is not significant.
§ This parameter applies only in case of protocol hard error.

PARAMETER MEASUREMENT INFORMATION

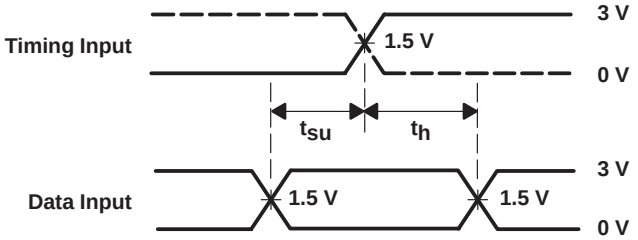


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

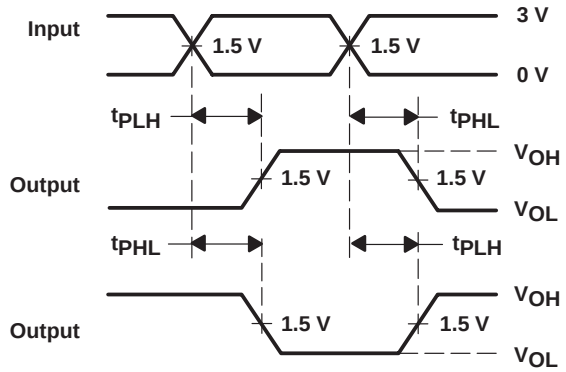
LOAD CIRCUIT



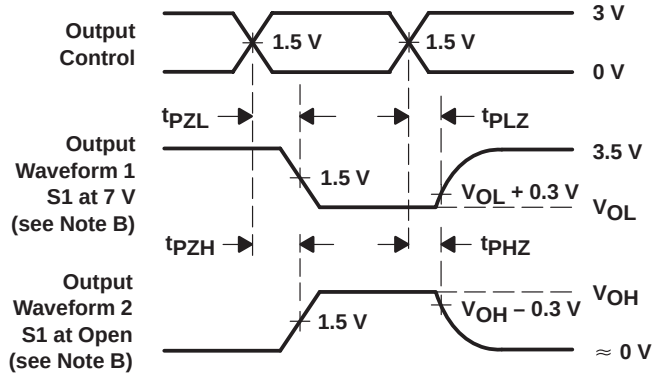
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 24. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-9681201Q3A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Call TI	-55 to 125	5962-9681201Q3A SNJ54ABT 8996FK	Samples
5962-9681201QKA	ACTIVE	CFP	W	24	1	TBD	Call TI	Call TI	-55 to 125	5962-9681201QKA SNJ54ABT8996W	Samples
5962-9681201QLA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Call TI	-55 to 125	5962-9681201QLA SNJ54ABT8996JT	Samples
CABT8996DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT8996	Samples
SN54ABT8996W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI			
SN74ABT8996DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT8996	Samples
SN74ABT8996DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT8996	Samples
SN74ABT8996PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AG996	Samples
SN74ABT8996PWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
SN74ABT8996PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AG996	Samples
SNJ54ABT8996FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9681201Q3A SNJ54ABT 8996FK	Samples
SNJ54ABT8996JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9681201QLA SNJ54ABT8996JT	Samples
SNJ54ABT8996W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9681201QKA SNJ54ABT8996W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ABT8996, SN74ABT8996 :

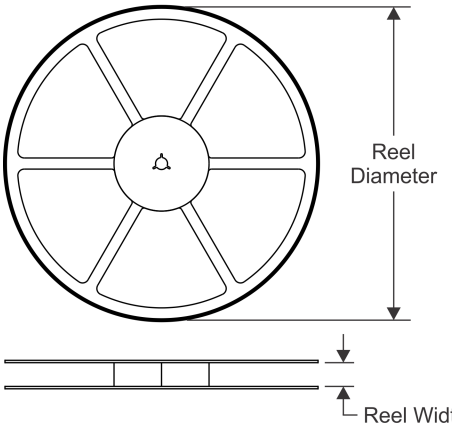
- Catalog: SN74ABT8996
- Military: SN54ABT8996

NOTE: Qualified Version Definitions:

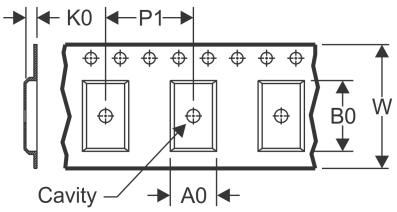
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

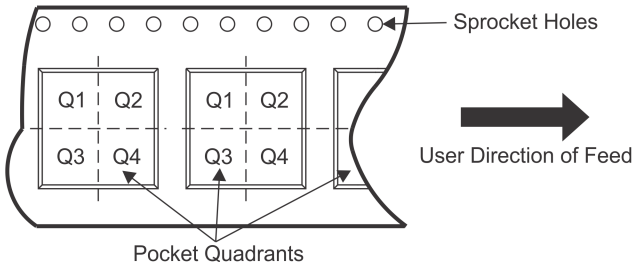


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

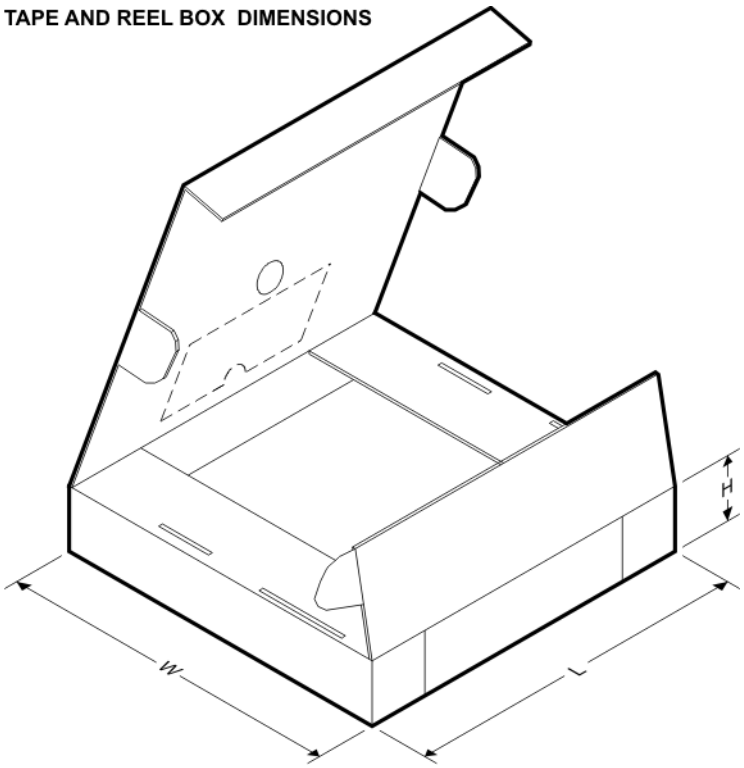
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT8996DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABT8996PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



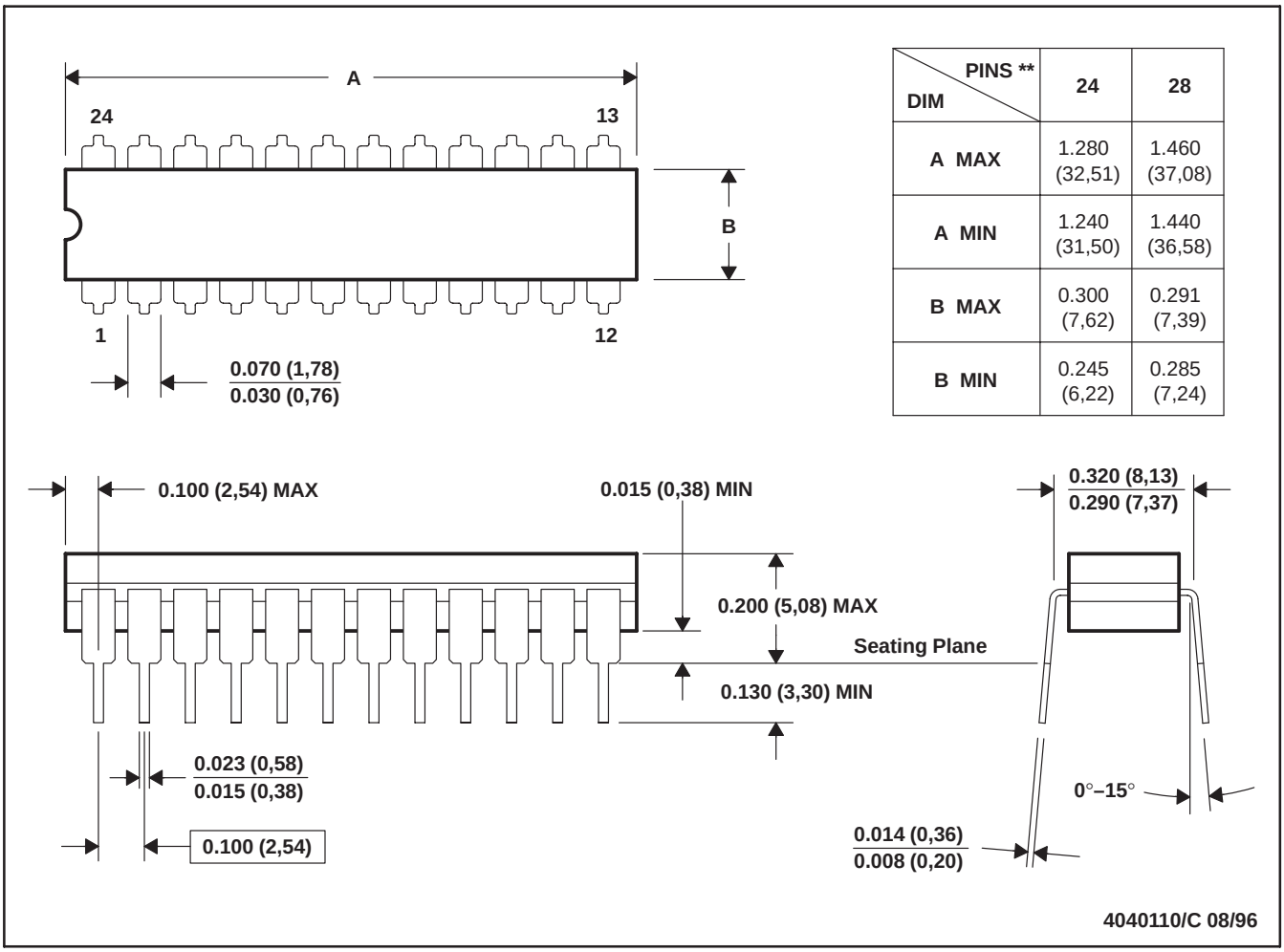
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT8996DWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74ABT8996PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

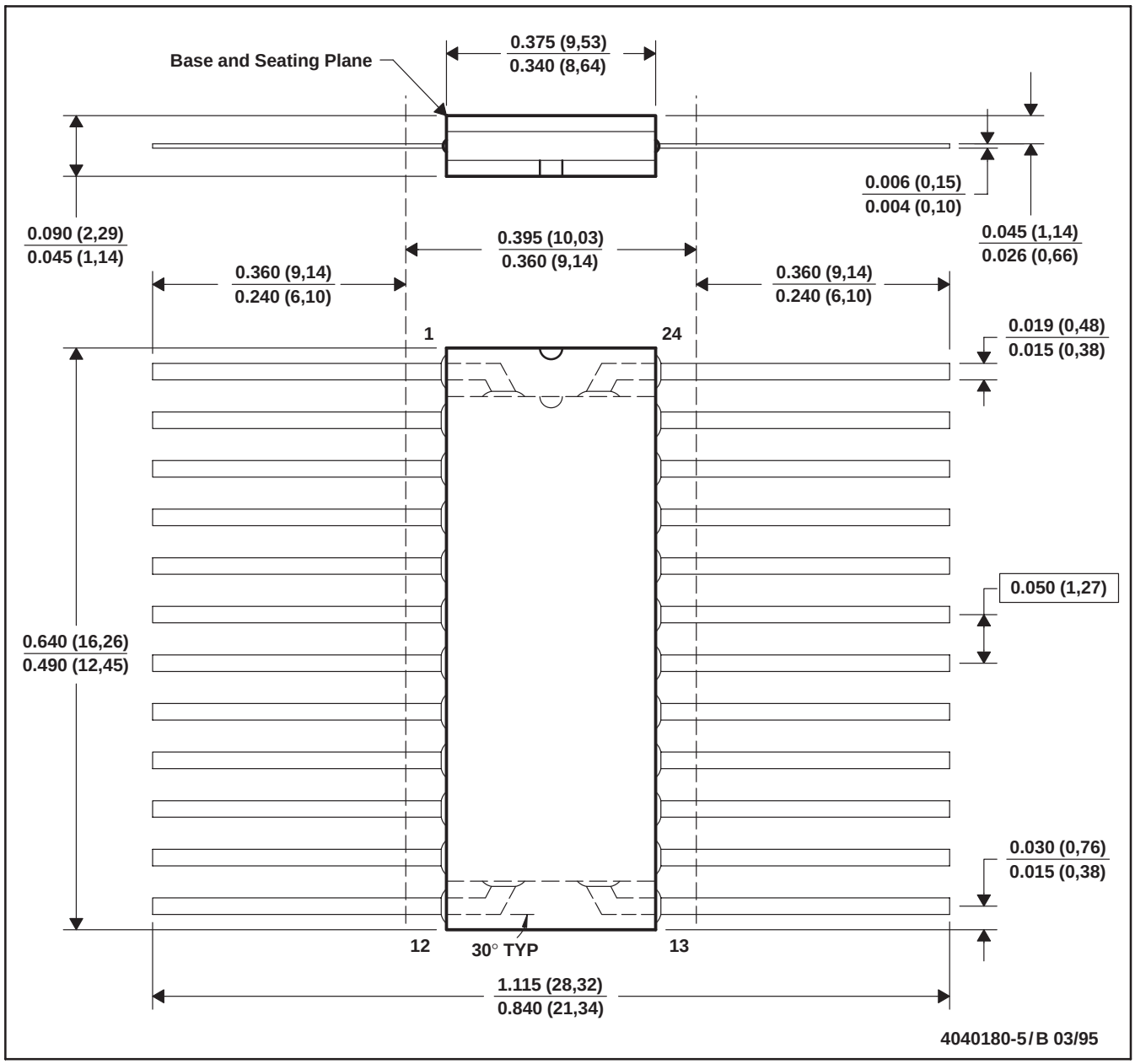
24 LEADS SHOWN



DIM \ PINS **	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

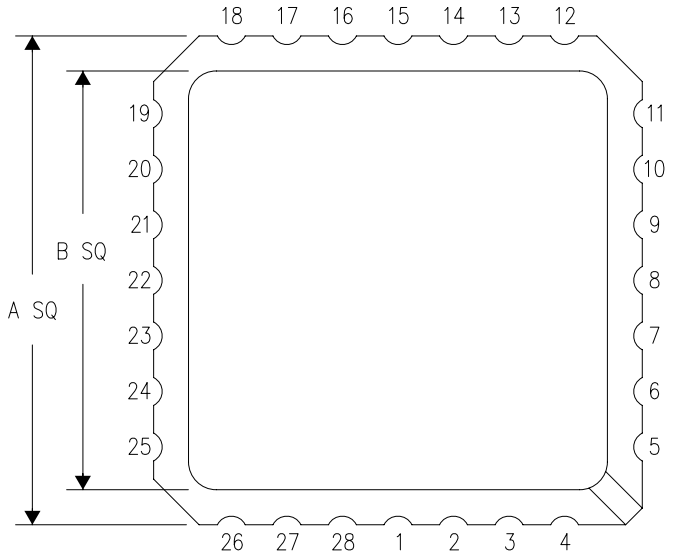
W (R-GDFP-F24) **CERAMIC DUAL FLATPACK**



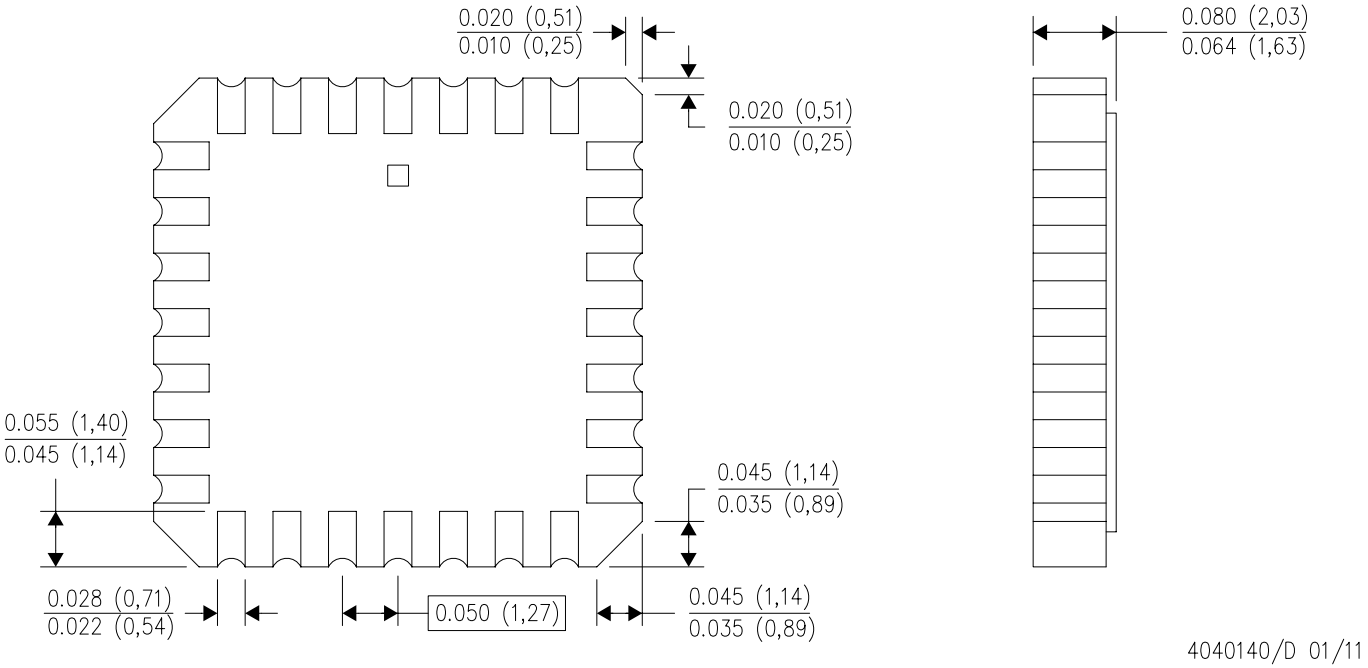
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
E. Index point is provided on cap for terminal identification only.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



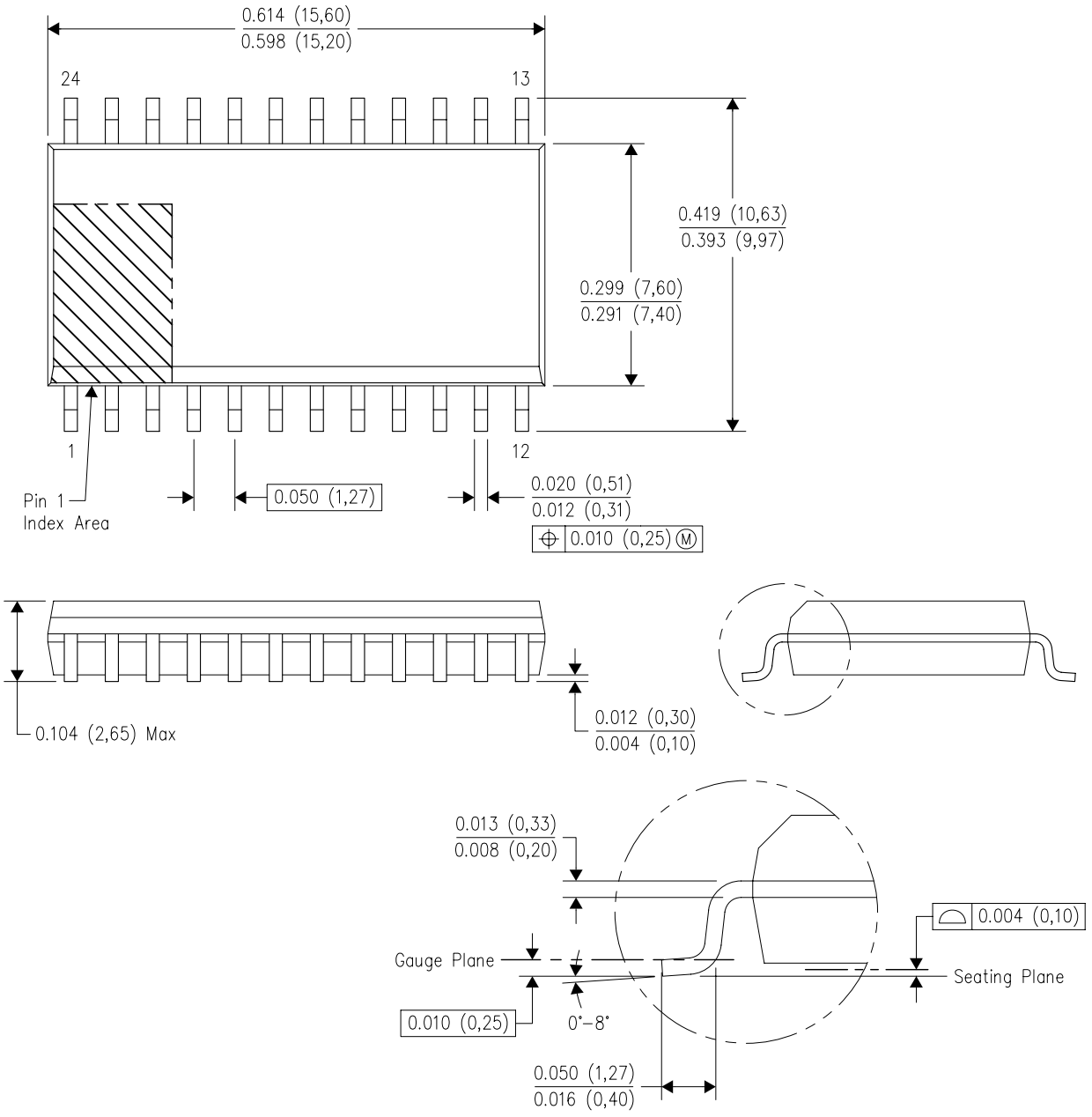
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

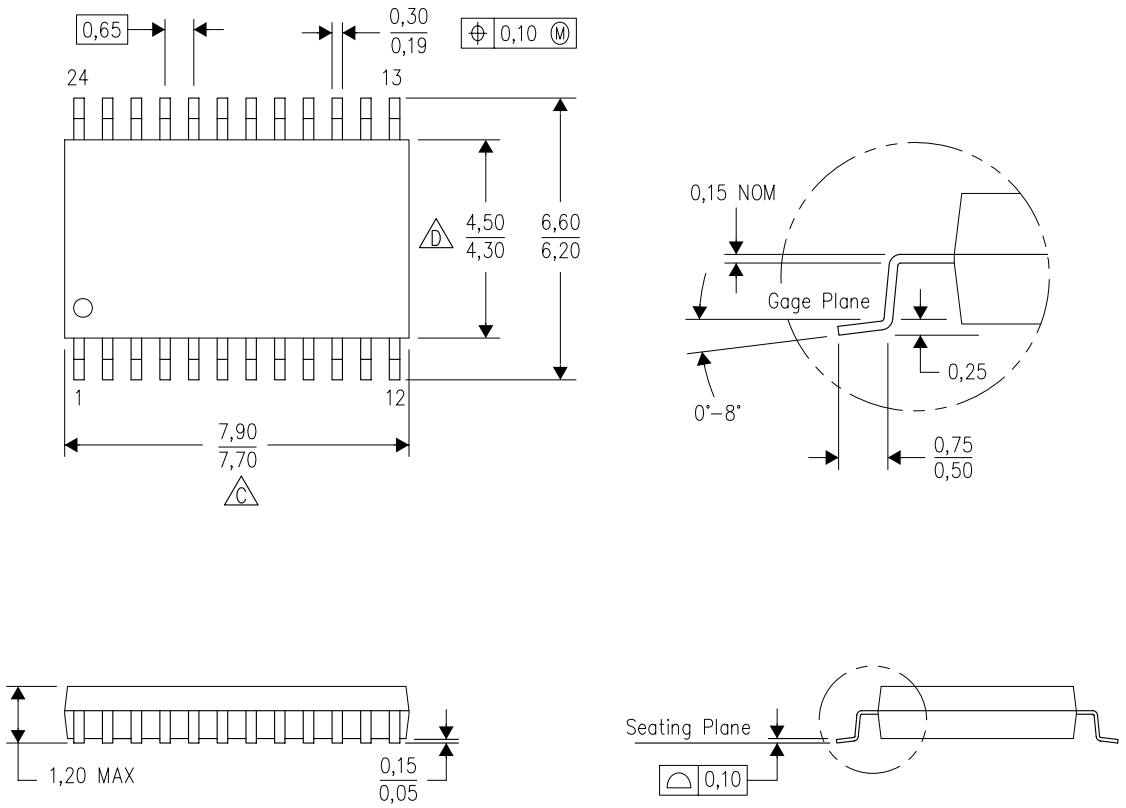
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

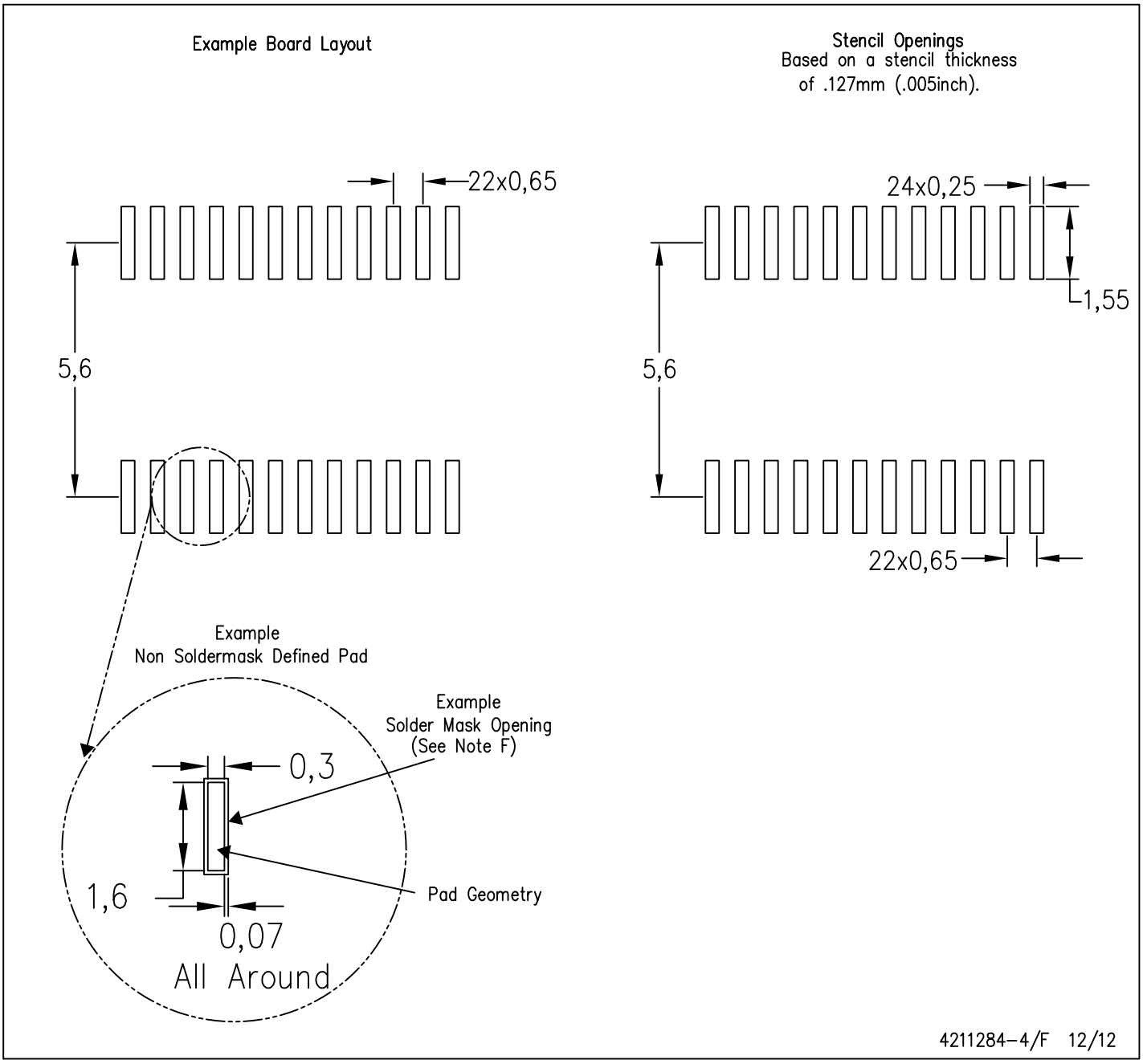
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331