TEXAS INSTRUMENTS

SN65HVD1470, SN65HVD1471, SN65HVD1473
SN65HVD1474, SN65HVD1476, SN65HVD1477

SLLSEJ8D – JUNE 2014 – REVISED OCTOBER 2014

# SN65HVD147x 3.3-V Full-Duplex RS-485 Transceivers With ±16-kV IEC ESD

## 1 Features

- 1/8 Unit-Load Options Available
  - Up to 256 Nodes on the Bus
- Bus I/O Protection
  - > ±30 kV HBM protection
  - > ±16 kV IEC61000-4-2 Contact Discharge
  - > ±4 kV IEC61000-4-4 Fast Transient Burst
- Extended Industrial Temperature Range: –40°C to 125°C
- Large Receiver Hysteresis (70 mV) for Noise Rejection
- Low Power Consumption
  - < 1.1 mA Quiescent Current During Operation
  - Low Standby Supply Current: 10 nA Typical, < 5 µA (maximum)
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications
- 5-V Tolerant Logic Inputs Compatible With 3.3-V or 5-V Controllers
- Signaling Rate Options Optimized for: 400 kbps (1470, 1471), 20 Mbps (1473, 1474), 50 Mbps (1476, 1477)

## 2 Applications

- Industrial Automation
- Encoders and Decoders
- Building Automation
- Security and Surveillance Networks
- Telecommunications

## 3 Description

The SN65HVD147x family of full-duplex transceivers feature the highest ESD protection in the RS-485 portfolio, supporting ±16-kV IEC61000-4-2 contact discharge and > ±30-kV HBM ESD protection. These RS-485 transceivers have robust 3.3-V drivers and receivers and are offered in a standard SOIC package as well as in a small-footprint MSOP package. The large receiver hysteresis of the SN65HVD147x devices provides immunity to conducted differential noise and the wide operating temperature enables reliability in harsh operating environments.

These devices each combine a differential driver and a differential receiver, which operate from a single 3.3-V power supply. Each driver and receiver has separate input and output pins for full-duplex bus communication designs. These devices all feature a wide common-mode voltage range which makes the devices suitable for multi-point applications over long cable runs.

The SN65HVD1471, SN65HVD1474, and SN65HVD1477 devices are fully enabled with no external enabling pins.

The SN65HVD1470, SN65HVD1473, and SN65HVD1476 devices have active-high driver enables and active-low receiver enables. A low, less than 5-µA standby current can be achieved by disabling both the driver and receiver.

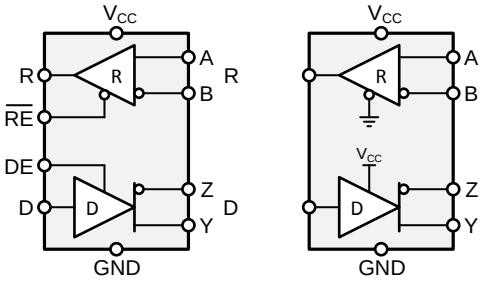
These devices are characterized from –40°C to 125°C.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN65HVD1471<br>SN65HVD1474<br>SN65HVD1477 | MSOP (8) | 3.00 mm × 3.00 mm |
| | SOIC (8) | 4.90 mm × 3.91 mm |
| SN65HVD1470<br>SN65HVD1473<br>SN65HVD1476 | MSOP (10) | 3.00 mm × 3.00 mm |
| | SOIC (14) | 8.65 mm × 3.91 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Block Diagram**




SN65HVD1470, SN65HVD1473, and SN65HVD1476

SN65HVD1471, SN65HVD1474, and SN65HVD1477

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (August 2014) to Revision D | Page |
|---|---|
| • Updated the MSOP–10 logic diagram | 4 |

| Changes from Revision B (July 2014) to Revision C | Page |
|---|---|
| • Updated the *Device Comparison Table* | 3 |

| Changes from Revision A (June 2014) to Revision B | Page |
|---|---|
| • Updated SN65HVD1470 and SN65HVD1471 specifications to production values | 3 |

| Changes from Original (May 2014) to Revision A | Page |
|---|---|
| • Changed device status from *Product Preview* to *Production Data* (mixed status) | 1 |

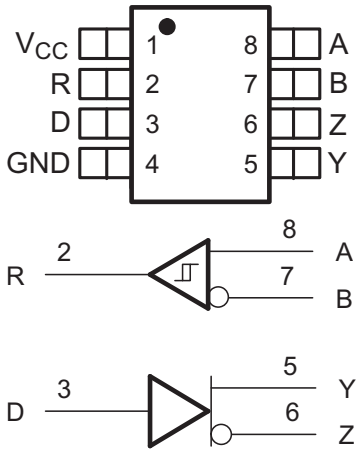
## 5 Device Comparison Table

| PART NUMBER(1) | SIGNALING RATE | DUPLEX | ENABLES | PACKAGE | NODES |
|---|---|---|---|---|---|
| SN65HVD1470 | up to 400 kbps | Full | DE, $\overline{RE}$ | SOIC-14<br>MSOP-10 | 256 |
| SN65HVD1471 | up to 400 kbps | Full | None | SOIC-8<br>MSOP-8 | 256 |
| SN65HVD1473 | up to 20 Mbps | Full | DE, $\overline{RE}$ | SOIC-14<br>MSOP-10 | 256 |
| SN65HVD1474 | up to 20 Mbps | Full | None | SOIC-8<br>MSOP-8 | 256 |
| SN65HVD1476 | up to 50 Mbps | Full | DE, $\overline{RE}$ | SOIC-14<br>MSOP-10 | 96 |
| SN65HVD1477 | up to 50 Mbps | Full | None | SOIC-8<br>MSOP-8 | 96 |

(1) For device status, see the *Mechanical, Packaging, and Orderable Information* section.

## 6 Pin Configuration and Functions

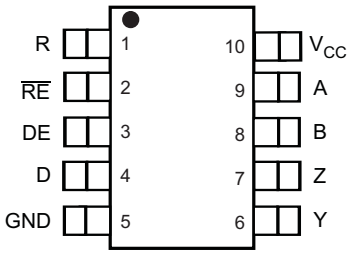
**SN65HVD1471, SN65HVD1474, SN65HVD1477**
**8-Pin SOIC, D Package, and 8-Pin MSOP, DGK Package**
**(Top View)**

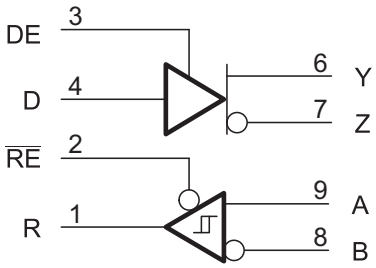



**Pin Functions — SOIC-8 and MSOP-8**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $V_{CC}$ | 1 | Supply | 3-V to 3.6-V supply |
| R | 2 | Digital output | Receive data output |
| D | 3 | Digital input | Driver data input |
| GND | 4 | Reference potential | Local device ground |
| Y | 5 | Bus output | Digital bus output, Y (Complementary to Z) |
| Z | 6 | Bus output | Digital bus output, Z (Complementary to Y) |
| B | 7 | Bus input | Digital bus input, B (Complementary to A) |
| A | 8 | Bus input | Digital bus input, A (Complementary to B) |

**SN65HVD1470, SN65HVD1473, SN65HVD1476**
**10-Pin MSOP, DGS Package**
**(Top View)**

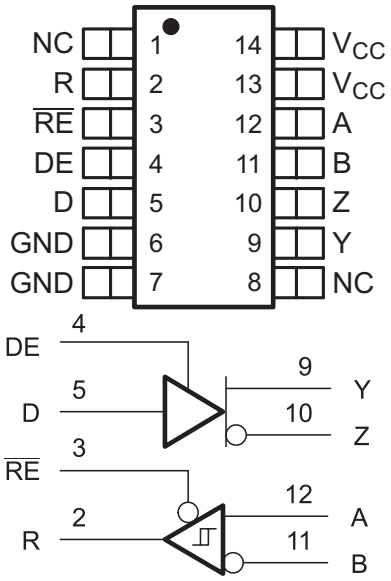



## Pin Functions — MSOP–10

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| R | 1 | Digital output | Receive data output |
| $\overline{RE}$ | 2 | Digital input | Receive enable *Low* |
| DE | 3 | Digital input | Driver enable *High* |
| D | 4 | Digital input | Driver data input |
| GND | 5 | Reference potential | Local device ground |
| Y | 6 | Bus output | Digital bus output, Y (Complementary to Z) |
| Z | 7 | Bus output | Digital bus output, Z (Complementary to Y) |
| B | 8 | Bus input | Digital bus input, B (Complementary to A) |
| A | 9 | Bus input | Digital bus input, A (Complementary to B) |
| $V_{CC}$ | 10 | Supply | 3-V to 3.6-V supply |

**SN65HVD1470, SN65HVD1473, SN65HVD1476**
**14-Pin SOIC, D Package**
**(Top View)**




NC = no internal connection

## Pin Functions — SOIC-14

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| NC | 1 | No connect | Not connected |
| | 8 | | |
| R | 2 | Digital output | Receive data output |
| $\overline{RE}$ | 3 | Digital input | Receive enable *Low* |
| DE | 4 | Digital input | Driver enable *High* |
| D | 5 | Digital input | Driver data input |
| GND | 6(1) | Reference potential | Local device ground |
| | 7(1) | | |
| Y | 9 | Bus output | Digital bus output, Y (Complementary to Z) |
| Z | 10 | Bus output | Digital bus output, Z (Complementary to Y) |
| B | 11 | Bus input | Digital bus input, B (Complementary to A) |
| A | 12 | Bus input | Digital bus input, A (Complementary to B) |
| $V_{CC}$ | 13(2) | Supply | 3-V to 3.6-V supply |
| | 14(2) | | |

(1) Pin 6 and pin 7 are connected internally.
(2) Pin 13 and pin 14 are connected internally.

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | –0.5 | 5.5 | V |
| Voltage | Range at any bus pin (A, B, Y, or Z) | –13 | 16.5 | V |
| Input voltage | Range at any logic pin (D, DE, or $\overline{RE}$) | –0.3 | 5.7 | V |
| | Voltage input range, transient pulse, any bus pin (A, B, Y, or Z) through 100 Ω | –100 | 100 | V |
| Output current | Receiver output | –24 | 24 | mA |
| Junction temperature, $T_J$ | | | 170 | °C |
| Continuous total power dissipation | | See the *Thermal Information* table | | |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 ESD (Contact Discharge), bus pins and GND | –16 | 16 | kV |
| | | IEC 61000-4-2 ESD (Air-Gap Discharge), bus pins and GND(1)(2) | –16 | 16 | kV |
| | | IEC 61000-4-4 EFT (Fast transient or burst), bus pins and GND | –4 | 4 | kV |
| | | IEC 60749-26 ESD (Human Body Model), bus pins and GND(2) | –30 | 30 | kV |
| | | Human body model (HBM), bus pins and GND(3) | –40 | 40 | kV |
| | | Human body model (HBM), per JEDEC specification JESD22-A114, all pins | –8 | 8 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins | –1.5 | 1.5 | kV |
| | | Machine model (MM), all pins | –300 | 300 | kV |

(1) By inference from contact-discharge results, see the *Application and Implementation* section
(2) Limited by tester capability.
(3) Modeled performance only; based on measured IEC ESD (Contact) capability.

## 7.3 Recommended Operating Conditions

| | IEC 61000-4-2 ESD (Contact Discharge), bus pins and GND | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | 3.3 | 3.6 | V |
| $V_I$ | Input voltage at any bus pin (separately or common mode) (1) | | –7 | | 12 | V |
| $V_{IH}$ | High-level input voltage (Driver, driver enable, and receiver enable inputs) | | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage (Driver, driver enable, and receiver enable inputs) | | 0 | | 0.8 | V |
| $V_{ID}$ | Differential input voltage | | –12 | | 12 | V |
| $I_O$ | Output current, Driver | | –60 | | 60 | mA |
| $I_O$ | Output current, Receiver | | –8 | | 8 | mA |
| $R_L$ | Differential load resistance | | 54 | 60 | | Ω |
| $C_L$ | Differential load capacitance | | | 50 | | pF |
| $1/t_{UI}$ | Signaling rate | HVD1470, HVD1471 | | | 400 | kbps |
| | | HVD1473, HVD1474 | | | 20 | Mbps |
| | | HVD1476, HVD1477 | | | 50 | |
| $T_A$ (2) | Operating free-air temperature (See the *Application and Implementation* for thermal information) | | –40 | | 125 | °C |
| $T_J$ | Junction Temperature | | –40 | | 150 | °C |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating because of internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

## 7.4 Thermal Information — D Packages

| THERMAL METRIC | | D (8 PINS) | D (14 PINS) | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 110.7 | 83.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54.7 | 42.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 51.3 | 37.8 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 9.2 | 9.3 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 50.7 | 37.5 | |
| $T_{J(TSD)}$ | Thermal shut-down junction temperature | 170 | | °C |

## 7.5 Thermal Information — DGS and DGK Packages

| THERMAL METRIC | | DGS (10 PINS) | DGK (8 PINS) | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 165.5 | 168.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 37.7 | 62.2 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 86.4 | 89.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.4 | 7.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 84.8 | 87.9 | |
| $T_{J(TSD)}$ | Thermal shut-down junction temperature | 170 | | °C |

## 7.6 Power Dissipation

| PARAMETER | | TEST CONDITIONS | | VALUE | UNIT |
|---|---|---|---|---|---|
| PD — Power Dissipation<br>driver and receiver enabled,<br>$V_{CC}$ = 3.6 V, $T_J$ = 150°C<br>50% duty cycle square-wave signal at signaling rate:<br>• HVD1470 and HVD1471 at 400 kbps<br>• HVD1473 and HVD1474 at 20 Mbps<br>• HVD1476 and HVD1477 at 50 Mbps | Unterminated | $R_L$ = 300 Ω, $C_L$ = 50 pF (driver) | HVD1470, HVD1471 | 150 | mW |
| | | | HVD1473, HVD1474 | 180 | |
| | | | HVD1476, HVD1477 | 220 | |
| | RS-422 load | $R_L$ = 100 Ω, $C_L$ = 50 pF (driver) | HVD1470, HVD1471 | 190 | mW |
| | | | HVD1473, HVD1474 | 220 | |
| | | | HVD1476, HVD1477 | 250 | |
| | RS-485 load | $R_L$ = 54 Ω, $C_L$ = 50 pF (driver) | HVD1470, HVD1471 | 230 | mW |
| | | | HVD1473, HVD1474 | 255 | |
| | | | HVD1476, HVD1477 | 285 | |

## 7.7 Electrical Characteristics

over recommended operating range (unless otherwise specified)

| PARAMETER | | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $\|V_{OD}\|$ | Driver differential output voltage magnitude | | $R_L$ = 60 Ω, 375 Ω on each output to –7 V to 12 V, See Figure 15 | | | 1.5 | 2 | | V |
| | | | $R_L$ = 54 Ω (RS-485), See Figure 16 | | | 1.5 | 2 | | V |
| | | | $R_L$ = 100 Ω (RS-422) $T_J$ ≥ 0°C, $V_{CC}$ ≥ 3.2 V, See Figure 16 | | | 2 | | | V |
| $\Delta\|V_{OD}\|$ | Change in magnitude of driver differential output voltage | | $R_L$ = 54 Ω, $C_L$ = 50 pF, See Figure 16 | | | –50 | 0 | 50 | mV |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | | Center of two 27-Ω load resistors, See Figure 16 | | | 1 | $V_{CC}$ / 2 | 3 | V |
| $\Delta V_{OC}$ | Change in differential driver output common-mode voltage | | | | | –50 | 0 | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak driver common-mode output voltage | | | | | | 500 | | mV |
| $C_{OD}$ | Differential output capacitance | | | | | | 15 | | pF |
| $V_{IT+}$ | Positive-going receiver differential input voltage threshold | | | | | See (1) | -70 | –20 | mV |
| $V_{IT–}$ | Negative-going receiver differential input voltage threshold | | | | | –200 | -140 | See (1) | mV |
| $V_{hys}$ | Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$) | | | | | 40 | 70 | | mV |
| $V_{OH}$ | Receiver high-level output voltage | | $I_{OH}$ = –8 mA | | | 2.4 | $V_{CC}$–0.3 | | V |
| $V_{OL}$ | Receiver low-level output voltage | | $I_{OL}$ = 8 mA | | | | 0.2 | 0.4 | V |
| $I_I$ | Driver input, driver enable, and receiver enable input current | | | | | –3 | | 3 | µA |
| $I_{OZ}$ | Receiver output high-impedance current | HVD1470, HVD1473, HVD1476 | $V_O$ = 0 V or $V_{CC}$, $\overline{RE}$ = $V_{CC}$ | | | –1 | | 1 | µA |
| $I_{OS}$ | Driver short-circuit output current | | | | | –150 | | 150 | mA |
| $I_I$ | Bus input current (disabled driver) | | $V_{CC}$ = 0 to ROC (max), DE = GND | HVD1470, HVD1473 | $V_I$ = 12 V | | 75 | 125 | µA |
| | | | | | $V_I$ = –7 V | –100 | –40 | | |
| | | | | HVD1476 | $V_I$ = 12 V | | 240 | 333 | |
| | | | | | $V_I$ = –7 V | –267 | –180 | | |

(1) Under any specific conditions, $V_{IT+}$ is assured to be at least $V_{hys}$ higher than $V_{IT–}$.

## Electrical Characteristics (continued)

over recommended operating range (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current (quiescent) | Driver and Receiver enabled | $\overline{DE}$ = $V_{CC}$, $\overline{RE}$ = GND, No load | | 750 | 1100 | µA |
| | | Driver enabled, receiver disabled | DE = $V_{CC}$, $\overline{RE}$ = $V_{CC}$, No load | | 350 | 650 | µA |
| | | Driver disabled, receiver enabled | $\overline{DE}$ = GND, $\overline{RE}$ = GND, No load | | 650 | 800 | µA |
| | | Driver and receiver disabled | $\overline{DE}$ = GND, D = open, $\overline{RE}$ = $V_{CC}$, No load | | 0.1 | 5 | µA |
| | Supply current (dynamic) | See the *Typical Characteristics* section | | | | | |
| $T_{sd}$ | Thermal Shut-down junction temperature | | | | | 170 | °C |

## 7.8 Switching Characteristics — 400 kbps

400-kbps devices (SN65HVD1470, SN65HVD1471) bit time ≥ 2 µs (over recommended operating conditions)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **DRIVER** | | | | | | | | |
| $t_r$, $t_f$ | Driver differential output rise/fall time | | $R_L$ = 54 Ω, $C_L$ = 50 pF | See Figure 17 | 100 | 400 | 750 | ns |
| $t_{PHL}$, $t_{PLH}$ | Driver propagation delay | | | | | 350 | 550 | ns |
| $t_{SK(P)}$ | Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$ | | | | | | 40 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Driver disable time | HVD1470 | | See Figure 18 and Figure 19 | | 50 | 200 | ns |
| $t_{PZH}$, $t_{PZL}$ | Driver enable time | | Receiver enabled | | | 300 | 750 | ns |
| | | | Receiver disabled | | | 3 | 8 | µs |
| **RECEIVER** | | | | | | | | |
| $t_r$, $t_f$ | Receiver output rise/fall time | | $C_L$ = 15 pF | See Figure 20 | | 13 | 25 | ns |
| $t_{PHL}$, $t_{PLH}$ | Receiver propagation delay time | | | | | 70 | 110 | ns |
| $t_{SK(P)}$ | Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$ | | | | | | 7 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Receiver disable time | HVD1470 | | | | 45 | 60 | ns |
| $t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$ | Receiver enable time | | Driver enabled | See Figure 21 | | 20 | 115 | ns |
| | | | Driver disabled | See Figure 22 | | 3 | 8 | µs |

## 7.9 Switching Characteristics — 20 Mbps

20-Mbps devices (SN65HVD1473, SN65HVD1474) bit time ≥ 50 ns (over recommended operating conditions)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **DRIVER** | | | | | | | | |
| $t_r$, $t_f$ | Driver differential output rise/fall time | | $R_L$ = 54 Ω, $C_L$ = 50 pF | See Figure 17 | 4 | 7 | 14 | ns |
| $t_{PHL}$, $t_{PLH}$ | Driver propagation delay | | | | 4 | 10 | 20 | ns |
| $t_{SK(P)}$ | Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$ | | | | | 0 | 4 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Driver disable time | HVD1473 | | See Figure 18 and Figure 19 | | 12 | 25 | ns |
| $t_{PZH}$, $t_{PZL}$ | Driver enable time | | Receiver enabled | | | 10 | 20 | ns |
| | | | Receiver disabled | | | 3 | 8 | µs |
| **RECEIVER** | | | | | | | | |
| $t_r$, $t_f$ | Receiver output rise/fall time | | $C_L$ = 15 pF | See Figure 20 | | 5 | 10 | ns |
| $t_{PHL}$, $t_{PLH}$ | Receiver propagation delay time | | | | | 60 | 90 | ns |
| $t_{SK(P)}$ | Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$ | | | | | 0 | 5 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Receiver disable time | HVD1473 | | | | 17 | 25 | ns |
| $t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$ | Receiver enable time | | Driver enabled | See Figure 21 | | 12 | 90 | ns |
| | | | Driver disabled | See Figure 22 | | 3 | 8 | µs |

## 7.10 Switching Characteristics — 50 Mbps

50-Mbps devices (SN65HVD1476, SN65HVD1477) bit time ≥ 20 ns (over recommended operating conditions)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **DRIVER** | | | | | | | | |
| $t_r$, $t_f$ | Driver differential output rise/fall time | | $R_L$ = 54 Ω, $C_L$ = 50 pF | See Figure 17 | 2 | 3 | 6 | ns |
| $t_{PHL}$, $t_{PLH}$ | Driver propagation delay | | | | 3 | 10 | 16 | ns |
| $t_{SK(P)}$ | Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$ | | | | | 0 | 3.5 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Driver disable time | HVD1476 | | See Figure 18 and Figure 19 | | 10 | 20 | ns |
| $t_{PZH}$, $t_{PZL}$ | Driver enable time | | Receiver enabled | | | 10 | 20 | ns |
| | | | Receiver disabled | | | 3 | 8 | µs |
| **RECEIVER** | | | | | | | | |
| $t_r$, $t_f$ | Receiver output rise/fall time | | $C_L$ = 15 pF | See Figure 20 | 1 | 3 | 6 | ns |
| $t_{PHL}$, $t_{PLH}$ | Receiver propagation delay time | | | | | 25 | 40 | ns |
| $t_{SK(P)}$ | Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$ | | | | | 0 | 2 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Receiver disable time | HVD1476 | | | | 8 | 15 | ns |
| $t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$ | Receiver enable time | | Driver enabled | See Figure 21 | | 8 | 90 | ns |
| | | | Driver disabled | See Figure 22 | | 3 | 8 | µs |

## 7.11 Typical Characteristics

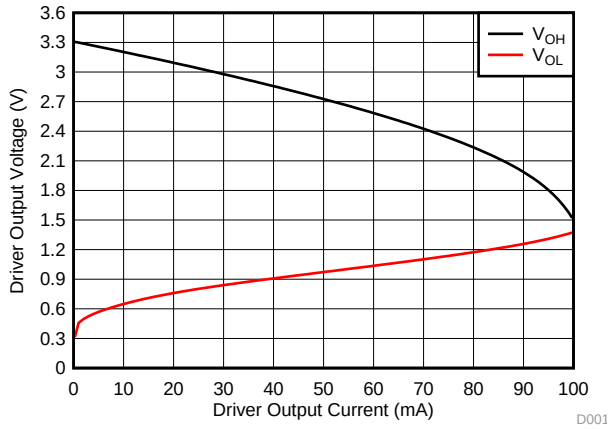



**Figure 1. Driver Output Voltage vs Driver Output Current**

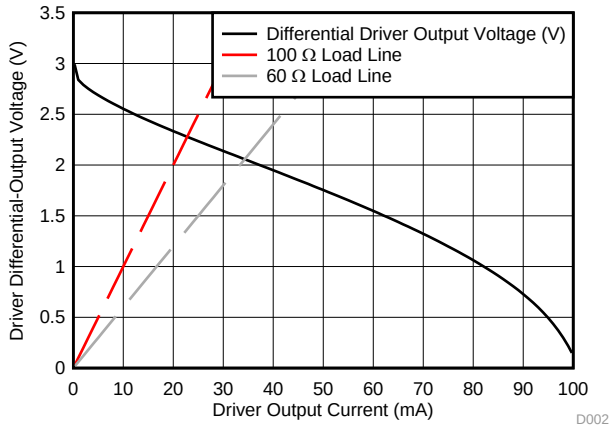



**Figure 2. Driver Differential-Output Voltage vs Driver Output Current**

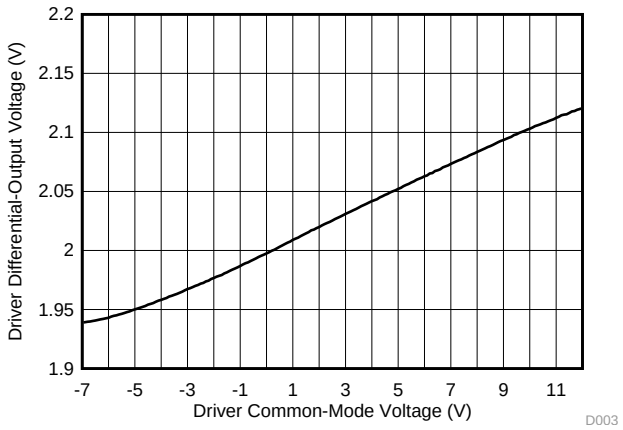



**Figure 3. Driver Differential-Output Voltage vs Driver Common-Mode Voltage**

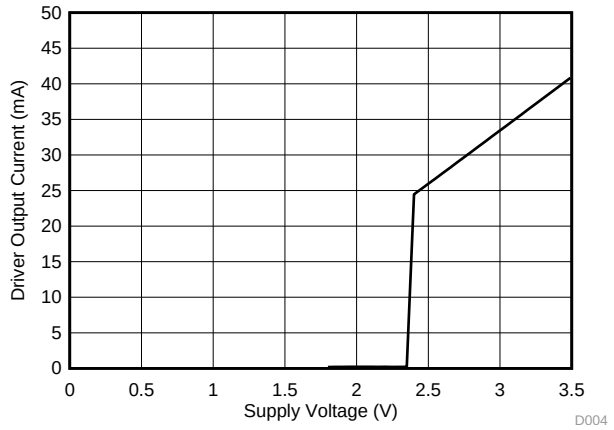



**Figure 4. Driver Output Current vs Supply Voltage**

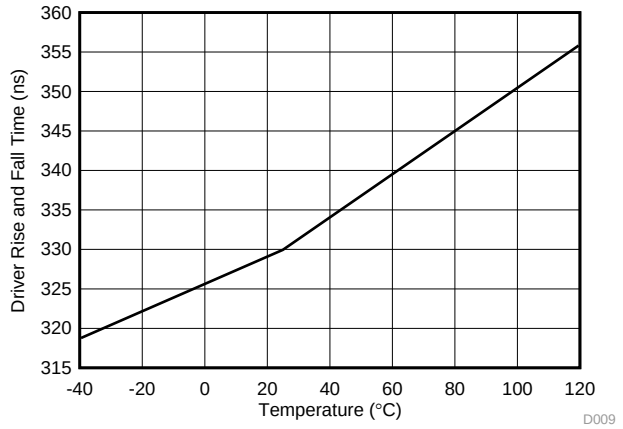



**Figure 5. SN65HVD1470, SN65HVD1471 Driver Rise and Fall Time vs Temperature**

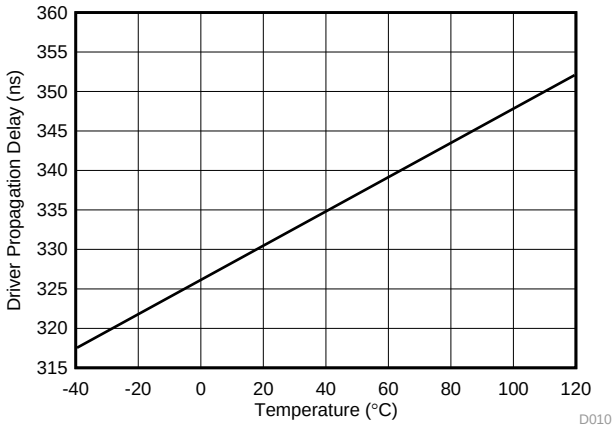



**Figure 6. SN65HVD1470, SN65HVD1471 Driver Propagation Delay vs Temperature**

## Typical Characteristics (continued)

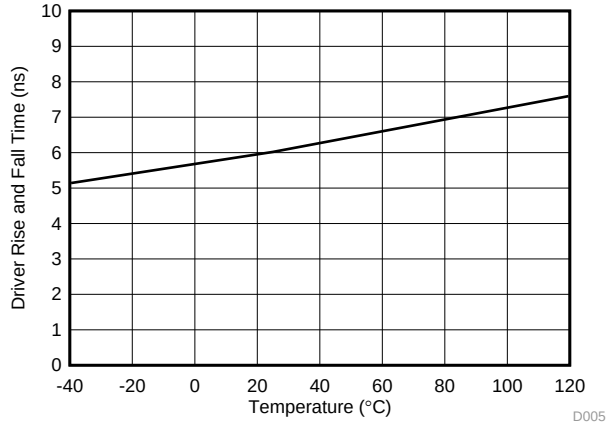



**Figure 7. SN65HVD1473, SN65HVD1474 Driver Rise and Fall Time vs Temperature**

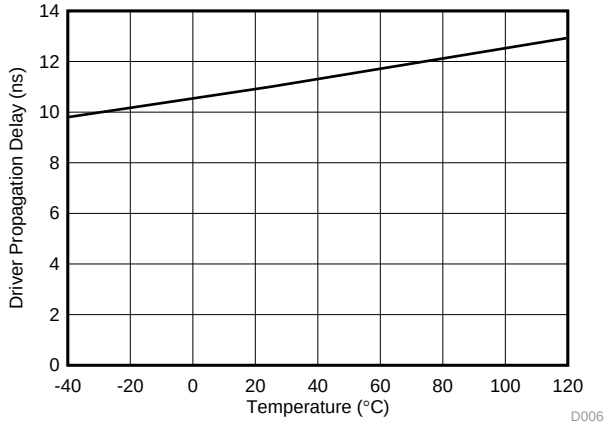



**Figure 8. SN65HVD1473, SN65HVD1474 Driver Propagation Delay vs Temperature**

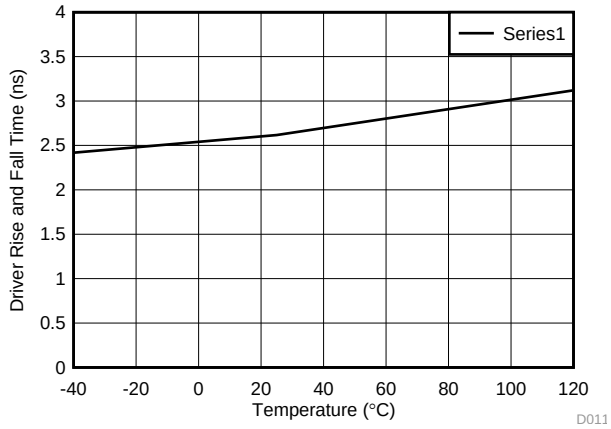



**Figure 9. SN65HVD1476, SN65HVD1477 Driver Rise and Fall Time vs Temperature**

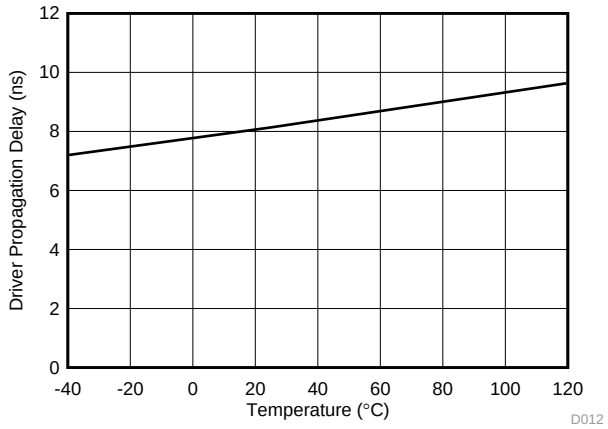



**Figure 10. SN65HVD1476, SN65HVD1477 Driver Propagation Delay vs Temperature**

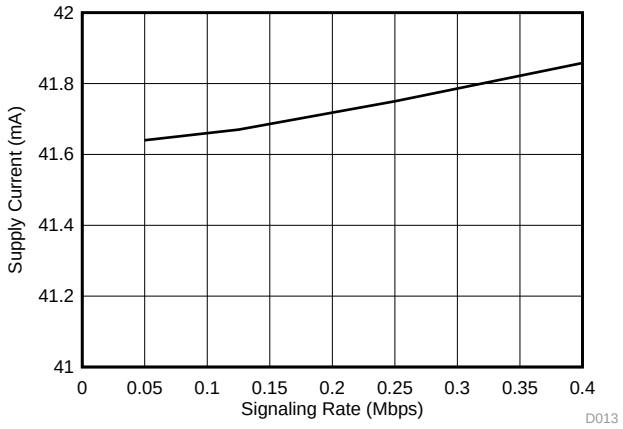



**Figure 11. SN65HVD1470, SN65HVD1471 Supply Current vs Signal Rate**

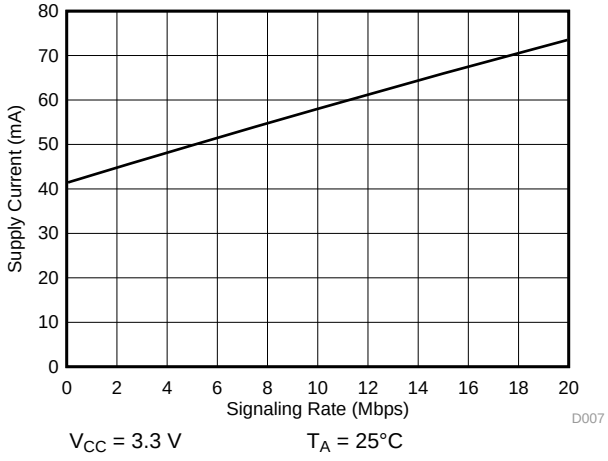



**Figure 12. SN65HVD1473, SN65HVD1474 Supply Current vs Signal Rate**

## Typical Characteristics (continued)

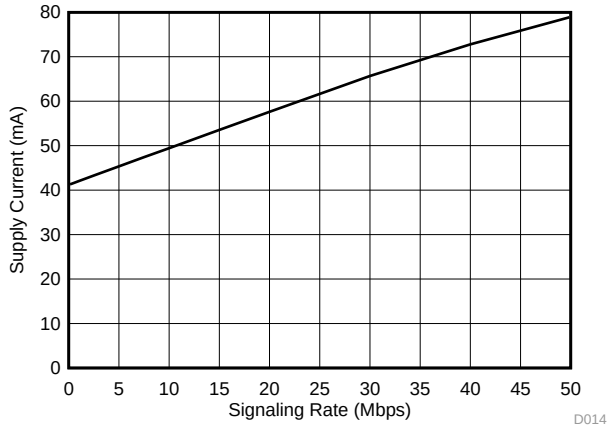



**Figure 13. SN65HVD1476, SN65HVD1477 Supply Current vs Signal Rate**

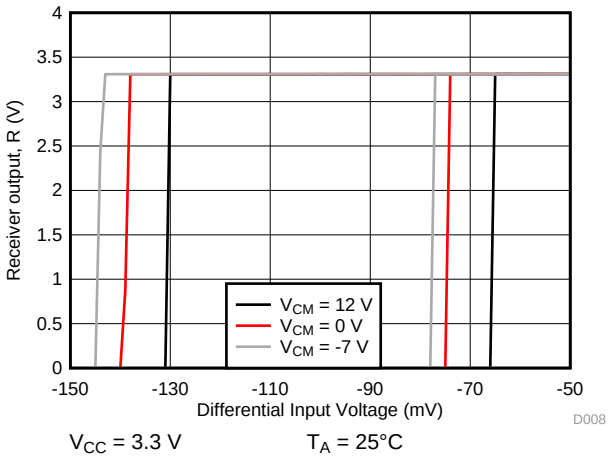



**Figure 14. Receiver Output vs Input**

## 8 Parameter Measurement Information

The input generator rate is 100 kbps with 50% duty cycle, than 6-ns rise and fall times, and 50-Ω output impedance.

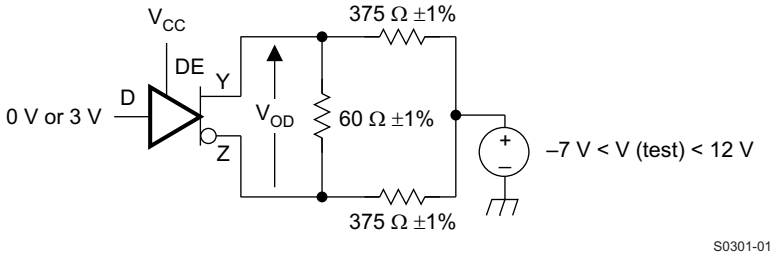



**Figure 15. Measurement of Driver Differential Output Voltage With Common-Mode Load**

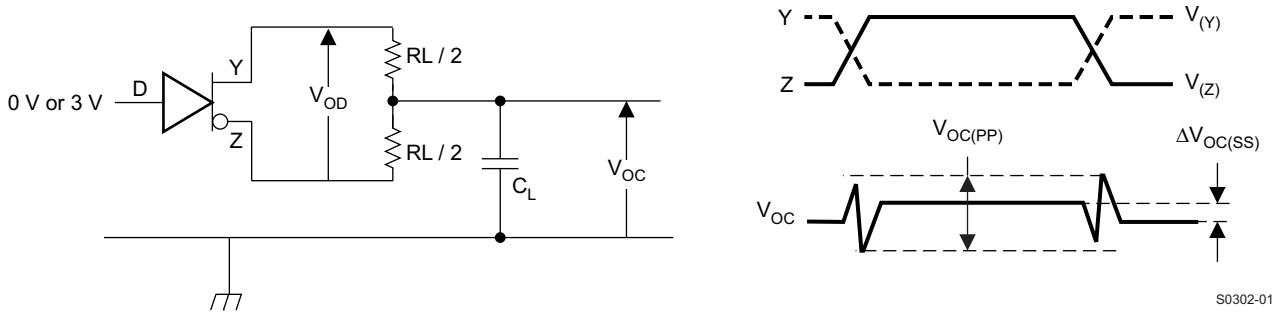



**Figure 16. Measurement of Driver Differential and Common-Mode Output With RS-485 Load**

## Parameter Measurement Information (continued)

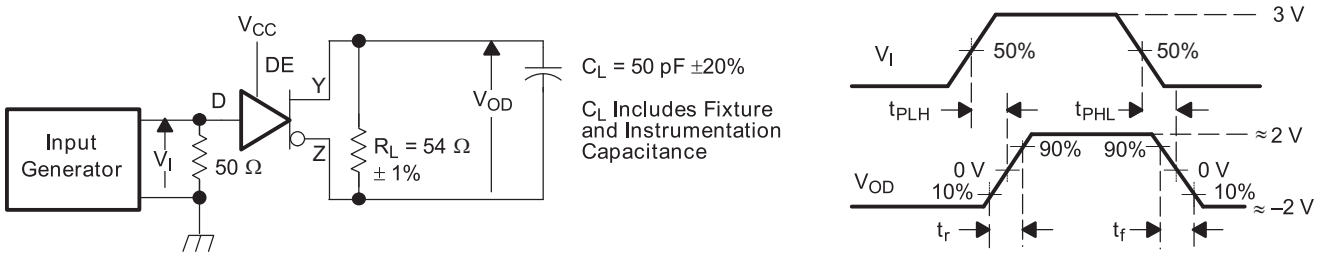
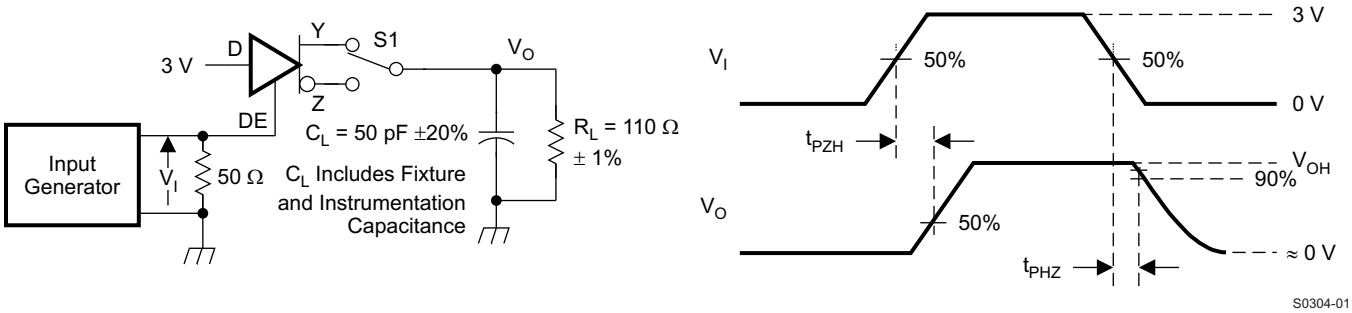
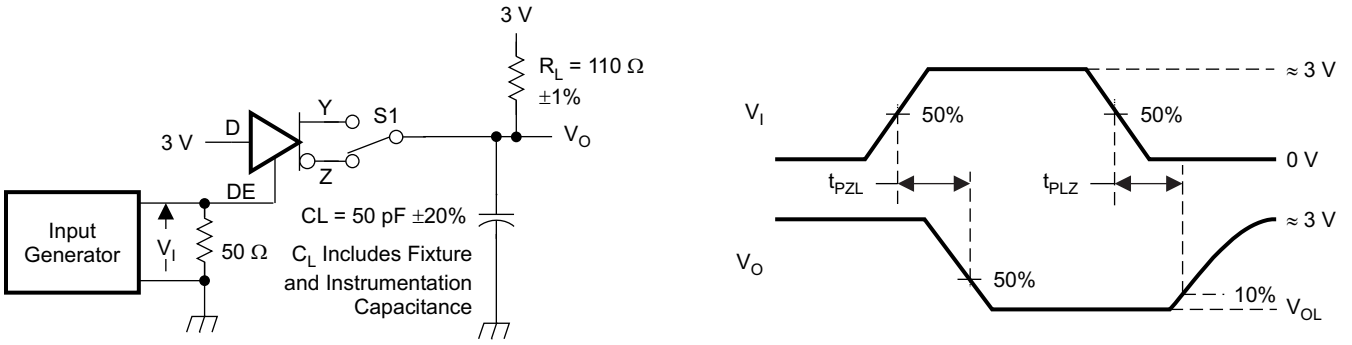



**Figure 17. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays**




D at 3 V to test non-inverting output, D at 0 V to test inverting output.

**Figure 18. Measurement of Driver Enable and Disable Times with Active-High Output and Pulldown Load**




D at 0 V to test non-inverting output, D at 3 V to test inverting output.

**Figure 19. Measurement of Driver Enable and Disable Times with Active-Low Output and Pullup Load**

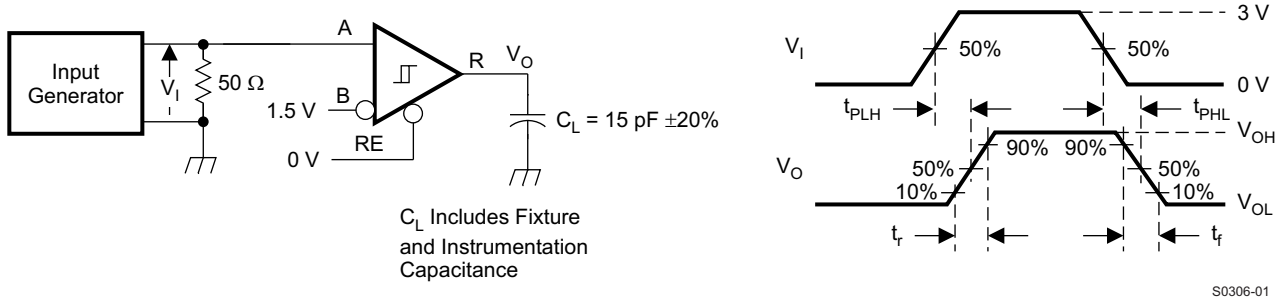



**Figure 20. Measurement of Receiver Output Rise and Fall Times and Propagation Delays**

## Parameter Measurement Information (continued)

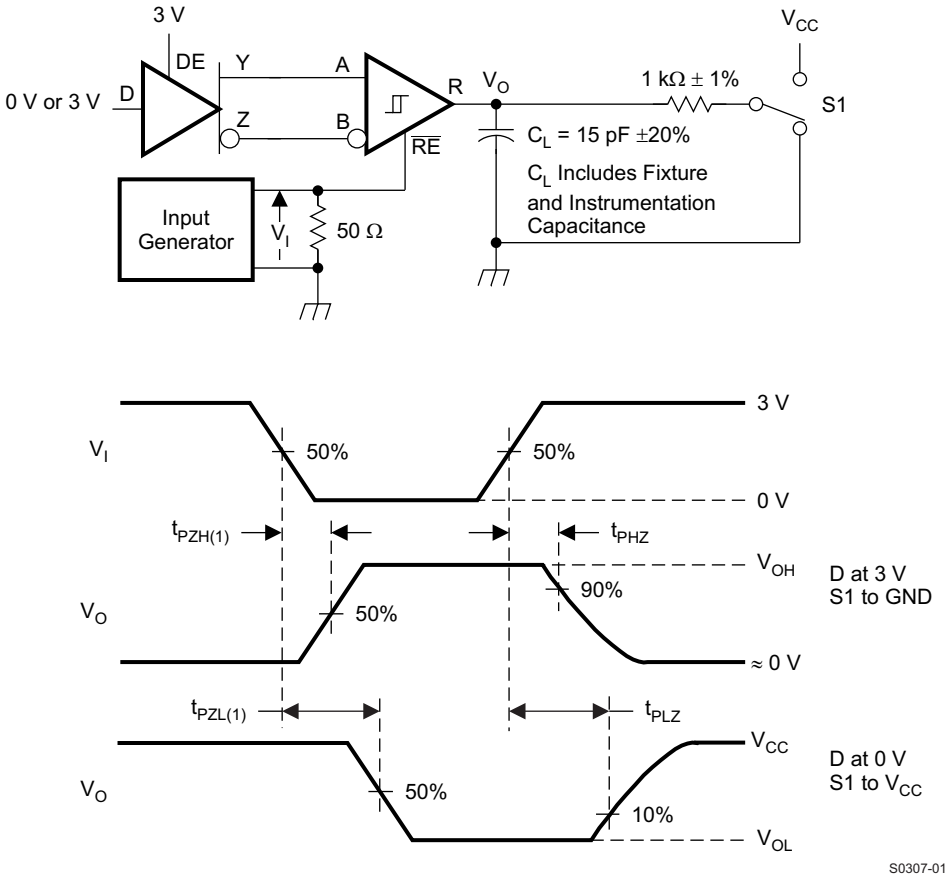



**Figure 21. Measurement of Receiver Enable and Disable Times With Driver Enabled**

## Parameter Measurement Information (continued)

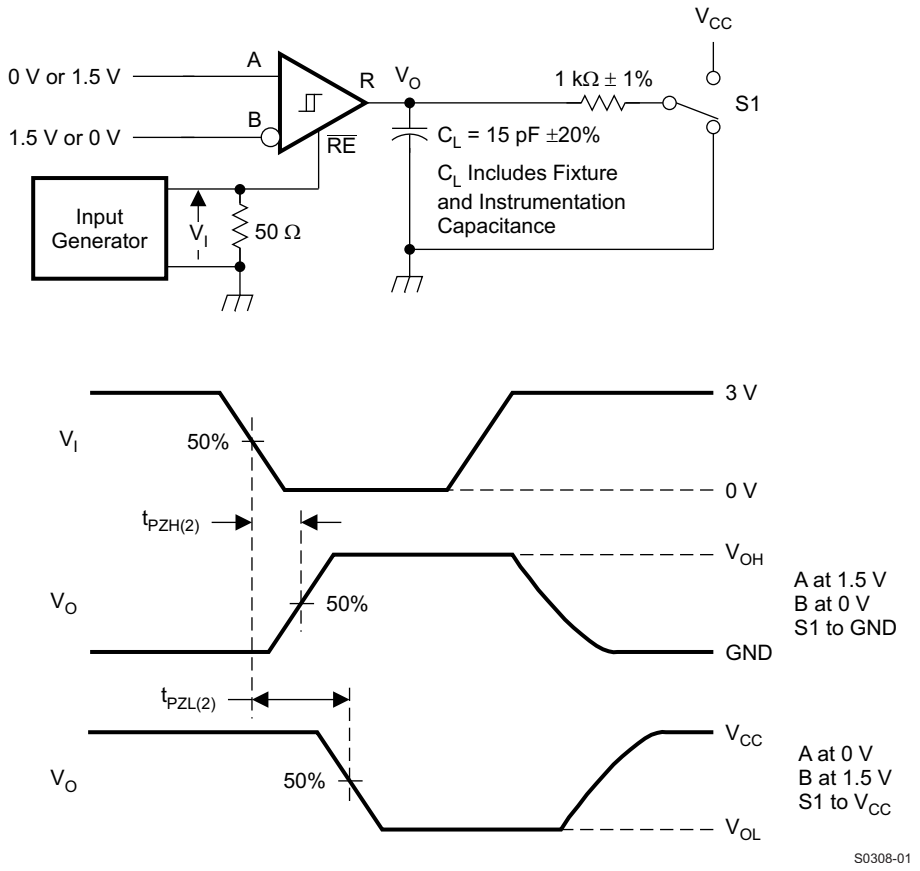



**Figure 22. Measurement of Receiver Enable Times With Driver Disabled**

# 9 Detailed Description

## 9.1 Overview

The SN65HVD1470, SN65HVD1471, SN65HVD1473, SN65HVD1474, SN65HVD1476, and SN65HVD1477 devices are low-power, full-duplex RS-485 transceivers available in three speed grades suitable for data transmission up to 400 kbps, 20 Mbps, and 50 Mbps.

The SN65HVD1471, SN65HVD1474, and SN65HVD1477 are fully enabled with no external enabling pins. The SN65HVD1470, SN65HVD1473, and SN65HVD1476 have active-high driver enables and active-low receiver enables. A standby current of less than 5 µA can be achieved by disabling both driver and receiver.

## 9.2 Functional Block Diagram

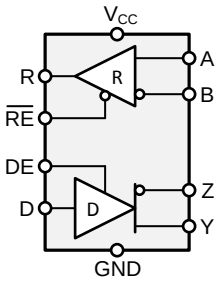



**Figure 23. Block Diagram**
**SN65HVD1470, SN65HVD1473, and SN65HVD1476**

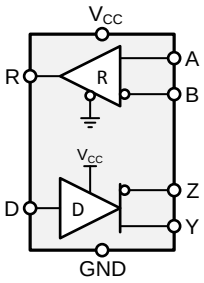



**Figure 24. Block Diagram**
**SN65HVD1471, SN65HVD1474, and SN65HVD1477**

## 9.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC61000-4-2 of up to ±16 kV, and against electrical fast transients (EFT) according to IEC61000-4-4 of up to ±4 kV.

The SN65HVD147x full-duplex family provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of $V_{IT+}$ = –20 mV and an input hysteresis of $V_{hys}$ = 40 mV, the receiver output remains logic high under a bus-idle or bus-short condition even in the presence of 120 $mV_{PP}$ differential noise without the need for external failsafe biasing resistors.

Device operation is specified over a wide temperature range from –40°C to 125°C.

## 9.4 Device Functional Modes

For the SN65HVD1470, SN65HVD1473, and SN65HVD1476, when the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and $V_{OD}$ is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to $V_{CC}$, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

**Table 1. Driver Function Table SN65HVD1470, SN65HVD1473, SN65HVD1476**

| INPUT | ENABLE | OUTPUTS | | FUNCTION |
|---|---|---|---|---|
| D | DE | Y | Z | |
| H | H | H | L | Actively drives the bus high |
| L | H | L | H | Actively drives the bus low |
| X | L | Z | Z | Driver disabled |
| X | OPEN | Z | Z | Driver disabled by default |
| OPEN | H | H | L | Actively drives the bus high by default |

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, $V_{IT+}$, the receiver output, R, turns high. When $V_{ID}$ is negative and less than the negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If $V_{ID}$ is between $V_{IT+}$ and $V_{IT–}$ the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of VID are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

**Table 2. Receiver Function Table SN65HVD1470, SN65HVD1473, SN65HVD1476**

| DIFFERENTIAL INPUT | ENABLE | OUTPUT | FUNCTION |
|---|---|---|---|
| $V_{ID} = V_{(A)} – V_{(B)}$ | $\overline{RE}$ | R | |
| $V_{IT+} < V_{ID}$ | L | H | Receives valid bus High |
| $V_{IT–} < V_{ID} < V_{IT+}$ | L | ? | Indeterminate bus state |
| $V_{ID} < V_{IT–}$ | L | L | Receives valid bus Low |
| X | H | Z | Receiver disabled |
| X | OPEN | Z | Receiver disabled by default |
| Open-circuit bus | L | H | Fail-safe high output |
| Short-circuit bus | L | H | Fail-safe high output |
| Idle (terminated) bus | L | H | Fail-safe high output |

For the SN65HVD1471, HVD1474, and HVD1477, the driver and receiver are fully enabled, thus the differential outputs Y and Z follow the logic states at data input D at all times. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and $V_{OD}$ is negative. The D pin has an internal pullup resistor to $V_{CC}$, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

**Table 3. Driver Function Table SN65HVD1471, SN65HVD1474, SN65HVD1477**

| INPUT | OUTPUTS | | FUNCTION |
|---|---|---|---|
| D | Y | Z | |
| H | H | L | Actively drives the bus High |
| L | L | H | Actively drives the bus Low |
| OPEN | H | L | Actively drives the bus High by default |

When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, $V_{IT+}$, the receiver output, R, turns high. When $V_{ID}$ is negative and less than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If $V_{ID}$ is between $V_{IT+}$ and $V_{IT–}$ the output is indeterminate. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

**Table 4. Receiver Function Table SN65HVD1471, SN65HVD1474, SN65HVD1477**

| DIFFERENTIAL INPUT | OUTPUT | FUNCTION |
|---|---|---|
| $V_{ID} = V_{(A)} – V_{(B)}$ | R | |
| $V_{IT+} < V_{ID}$ | H | Receives valid bus High |
| $V_{IT–} < V_{ID} < V_{IT+}$ | ? | Indeterminate bus state |
| $V_{ID} < V_{IT–}$ | L | Receives valid bus Low |
| Open-circuit bus | H | Fail-safe high output |
| Short-circuit bus | H | Fail-safe high output |
| Idle (terminated) bus | H | Fail-safe high output |

### 9.4.1 Equivalent Circuits

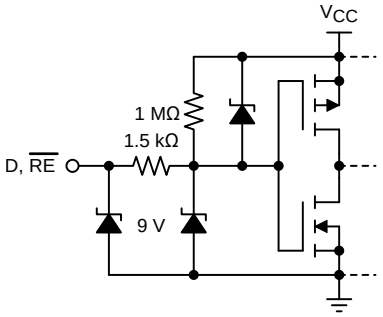



**Figure 25. D and $\overline{RE}$ Inputs**

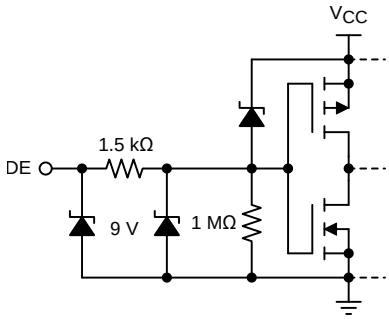



**Figure 26. DE Input**

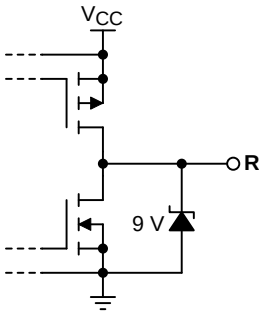



**Figure 27. R Output**

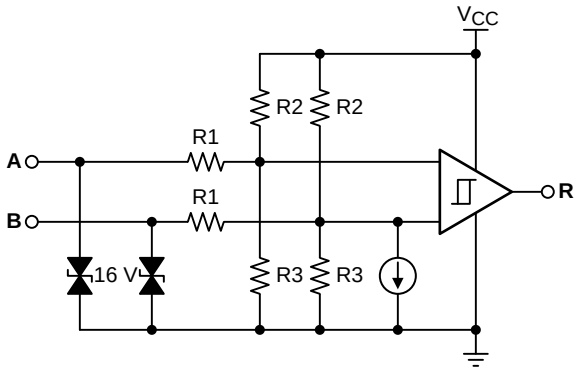



**Figure 28. Receiver Inputs**

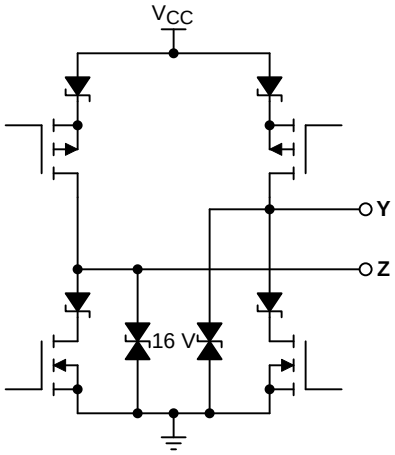



**Figure 29. Driver Outputs**

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The SN65HVD147x family consists of full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

To eliminate line reflections, each cable end is terminated with a termination resistor, $R_{(T)}$, whose value matches the characteristic impedance, $Z_0$, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

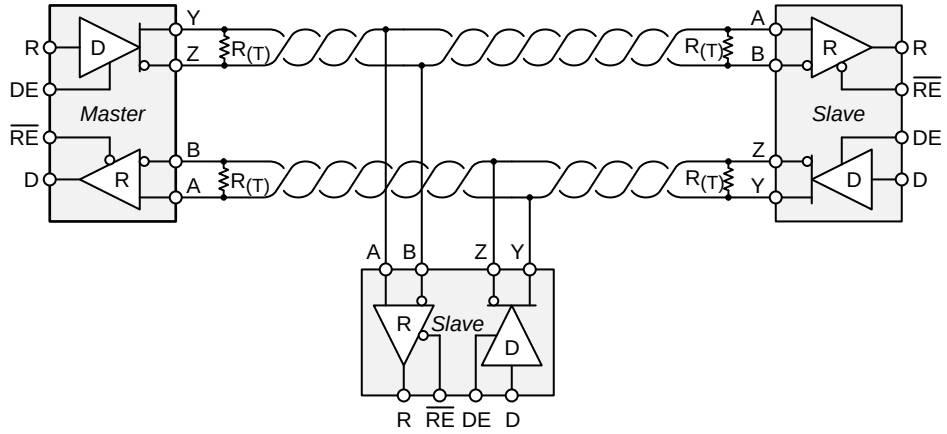



**Figure 30. Typical RS-485 Network With SN65HVD147x Full-Duplex Transceivers**

## 10.2 Typical Application

A full-duplex RS-485 network consists of multiple transceivers connecting in parallel to two bus cables. On one signal pair, a master driver transmits data to multiple slave receivers. The master driver and slave receivers may remain fully enabled at all times. On the other signal pair, multiple slave drivers transmit data to the master receiver. To avoid bus contention, the slave drivers must be intermittently enabled and disabled such that only one driver is enabled at any time, as in half-duplex communication. The master receiver may remain fully enabled at all times.

Because the driver may not be disabled, only one driver should be connected to the bus when using the SN65HVD1471, SN65HVD1474, or SN65HVD1477 device.


**Figure 31. Full-Duplex Transceiver Configurations**

## Typical Application (continued)

### 10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying parameter requirements, such as distance, data rate, and number of nodes.

#### *10.2.1.1 Data Rate and Bus Length*

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 ft and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

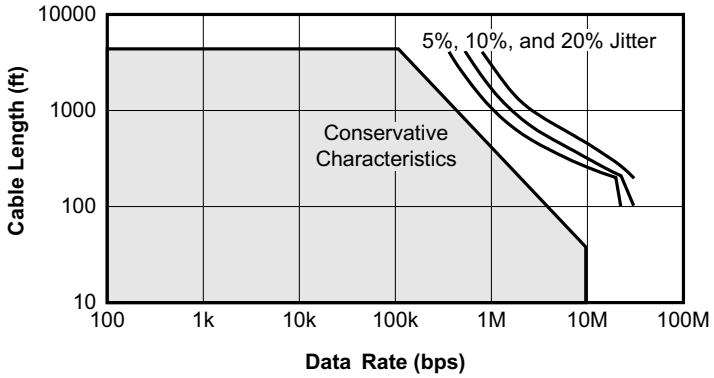



**Figure 32. Cable Length vs Data Rate Characteristic**

#### *10.2.1.2 Stub Length*

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- $t_r$ is the 10/90 rise time of the driver
- $v$ is the signal velocity of the cable or trace as a factor of $c$
- $c$ is the speed of light ($3 \times 10^8$ m/s)

Per Equation 1, Table 5 lists the maximum cable-stub lengths for the minimum-driver output rise-times of the SN65HVD147x full-duplex family of transceivers for a signal velocity of 78%.

**Table 5. Maximum Stub Length**

| DEVICE | MINIMUM DRIVER OUTPUT RISE TIME (ns) | MAXIMUM STUB LENGTH | |
|---|---|---|---|
| | | (m) | (ft) |
| SN65HVD1470 | 100 | 2.34 | 7.7 |
| SN65HVD1471 | 100 | 2.34 | 7.7 |
| SN65HVD1473 | 4 | 0.1 | 0.3 |
| SN65HVD1474 | 4 | 0.1 | 0.3 |
| SN65HVD1476 | 2 | 0.05 | 0.15 |
| SN65HVD1477 | 2 | 0.05 | 0.15 |

### 10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD147x family consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

### 10.2.1.4 Receiver Failsafe

The differential receivers of the SN65HVD147x family are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input $V_{ID}$ is more positive than 200 mV, and must output a Low when $V_{ID}$ is more negative than –200 mV. The receiver parameters which determine the failsafe performance are $V_{IT+}$, $V_{IT–}$, and $V_{hys}$ (the separation between $V_{IT+}$ and $V_{IT–}$). As shown in the Electrical Characteristics table, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the $V_{IT+}$ threshold, and the receiver output will be High. Only when the differential input is more than $V_{hys}$ below $V_{IT+}$ will the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, $V_{hys}$, as well as the value of $V_{IT+}$.

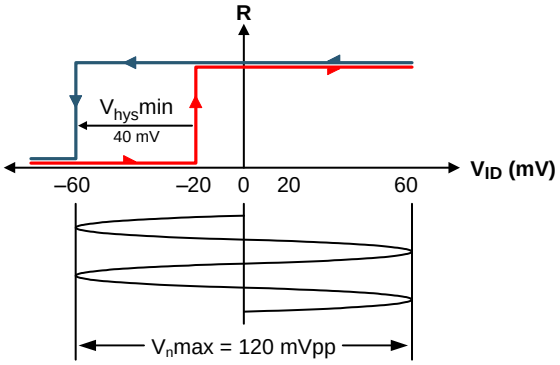



**Figure 33. SN65HVD147x Noise Immunity Under Bus Fault Conditions**

### 10.2.1.5 Transient Protection

The bus pins of the SN65HVD147x full-duplex transceiver family include on-chip ESD protection against ±30-kV HBM and ±16-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from contact discharge test results.

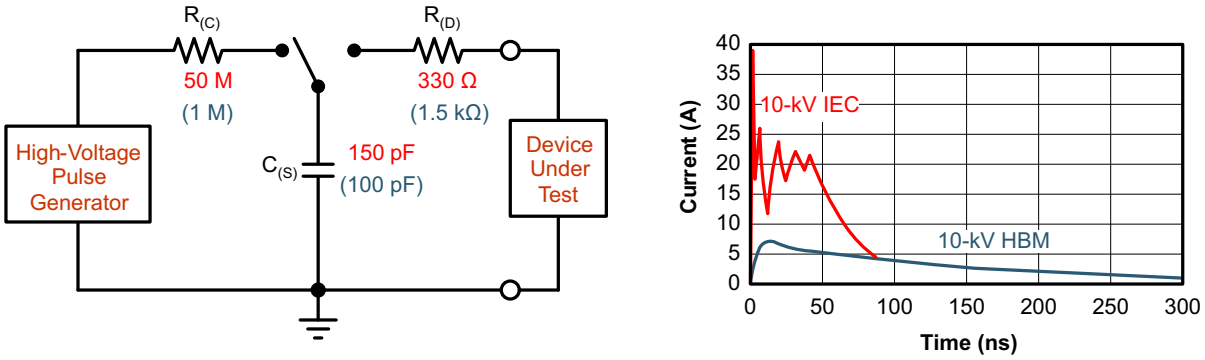



**Figure 34. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)**

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 35 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automations.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

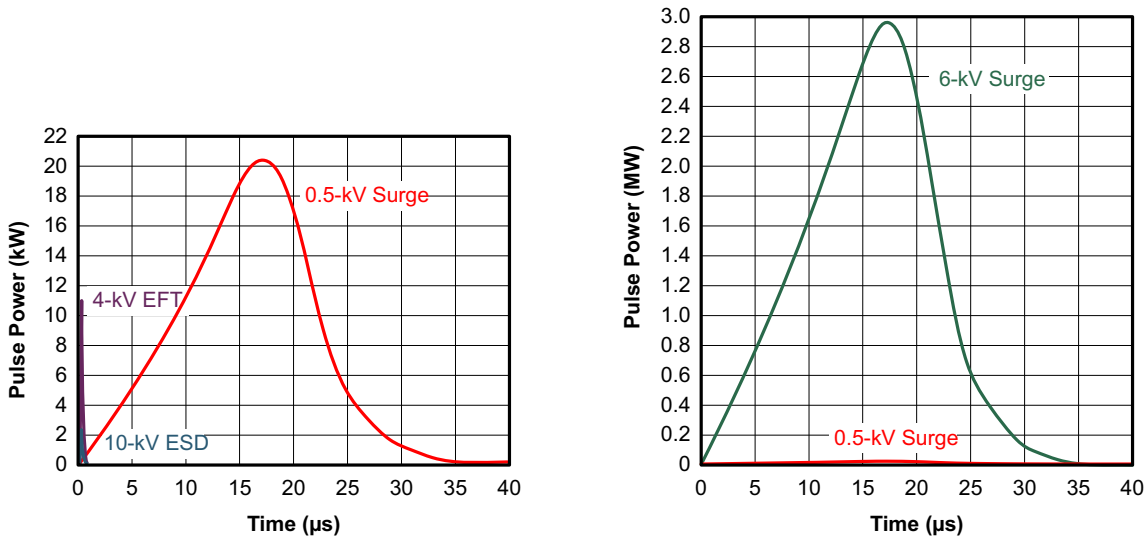



**Figure 35. Power Comparison of ESD, EFT, and Surge Transients**

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 36 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

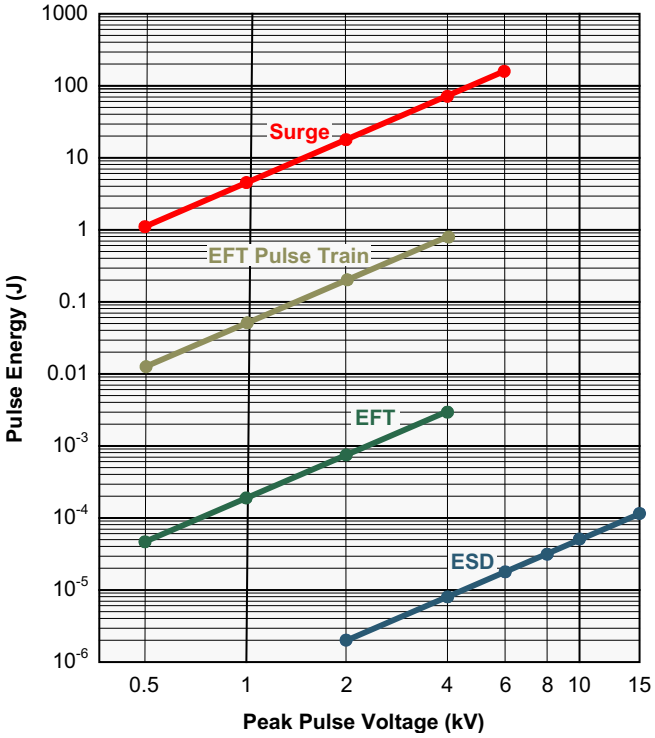



**Figure 36. Comparison of Transient Energies**

### 10.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is therefore necessary. Figure 37 shows a protection circuit against 16-kV ESD, 4-kV EFT, and 1-kV surge transients.

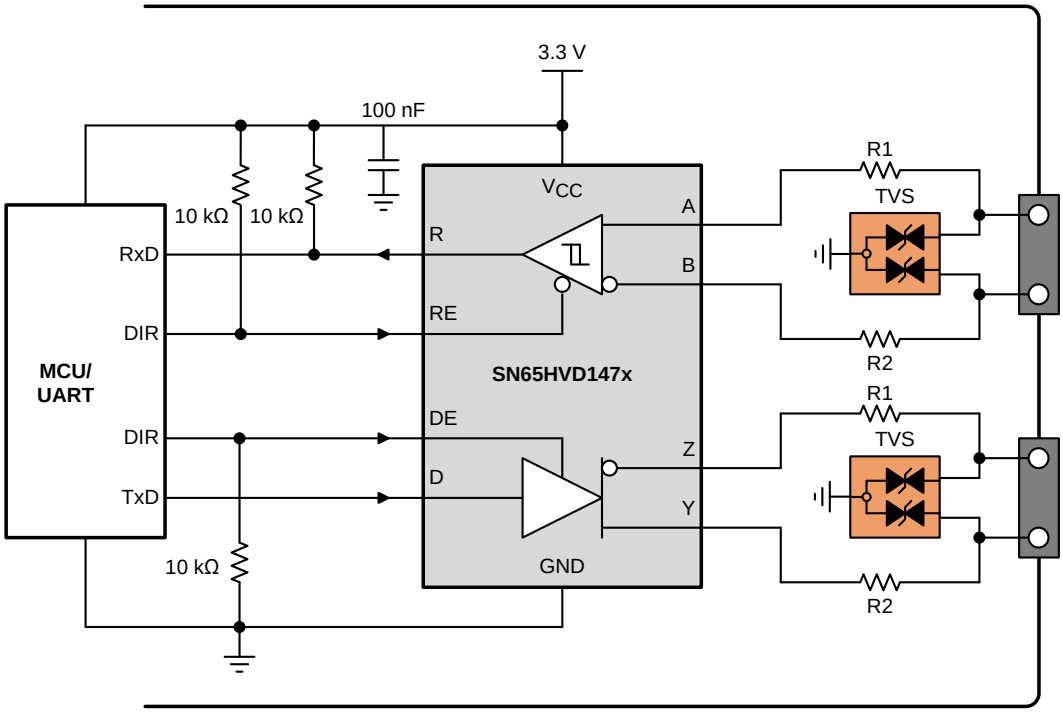
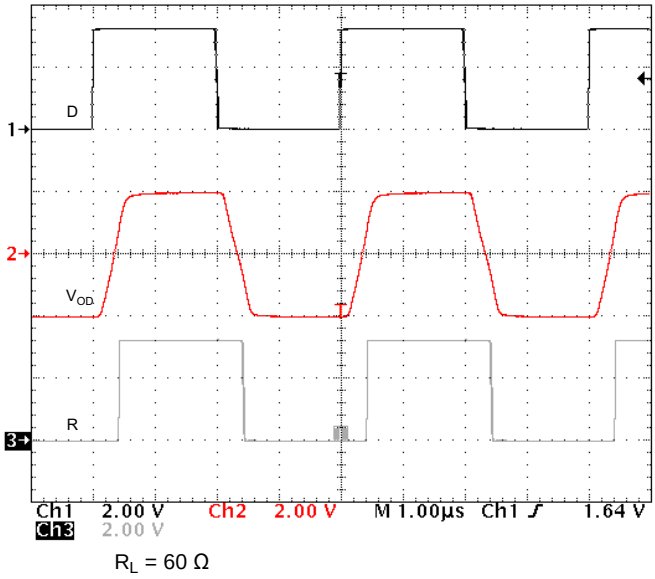



**Figure 37. Transient Protection Against ESD, EFT, and Surge transients**

**Table 6. Bill of Materials**

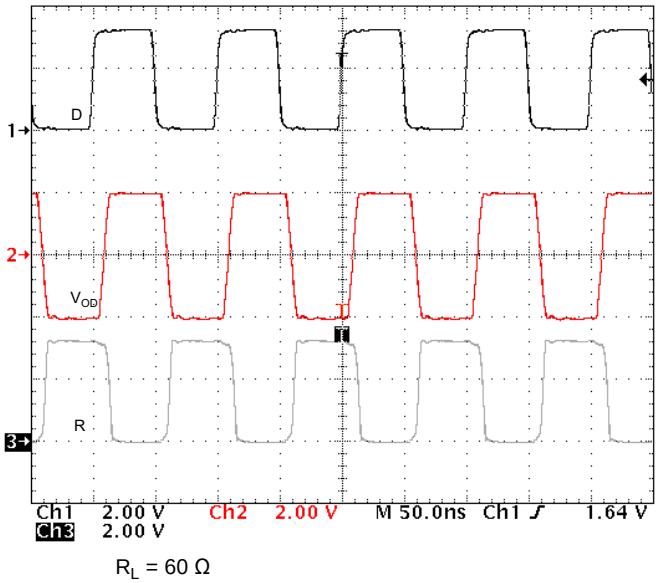
| DEVICE | FUNCTION | ORDER NUMBER | MANUFACTURER |
|---|---|---|---|
| XCVR | 3.3-V, full-duplex RS-485 transceiver | SN65HVD147xD | TI |
| R1 | 10-Ω, pulse-proof thick-film resistor | CRCW0603010RJNEAHP | Vishay |
| R2 | | | |
| TVS | Bidirectional 400-W transient suppressor | CDSOT23-SM712 | Bourns |

### 10.2.3 Application Curves



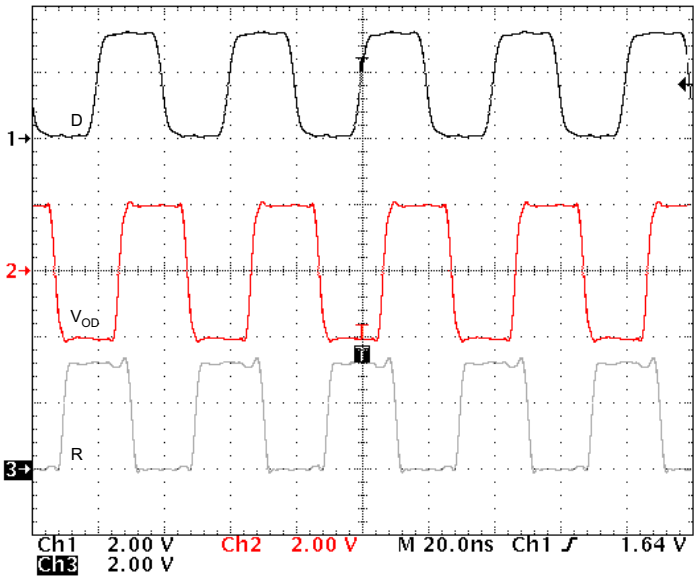

$R_L$ = 60 Ω

**Figure 38. SN65HVD1470 and SN65HVD1471, 500 kbps**




$R_L$ = 60 Ω

**Figure 39. SN65HVD1473 and SN65HVD1474, 20 Mbps**




$R_L$ = 60 Ω

**Figure 40. SN65HVD1476 and SN65HVD1477, 50 Mbps**

# 11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76333 is a linear voltage regulator suitable for the 3.3-V supply.

# 12 Layout

## 12.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design.

For successful PCB design, begin with the design of the protection circuit (see Figure 41).

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use $V_{CC}$ and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the $V_{CC}$-pins of transceiver, UART, controller ICs on the board (see Figure 41).
5. Use at least two vias for $V_{CC}$ and ground connections of bypass capacitors and protection devices to minimize effective via-inductance (see Figure 41).
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in theses lines during transient events (see Figure 41).
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up (see Figure 41).
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

## 12.2 Layout Example

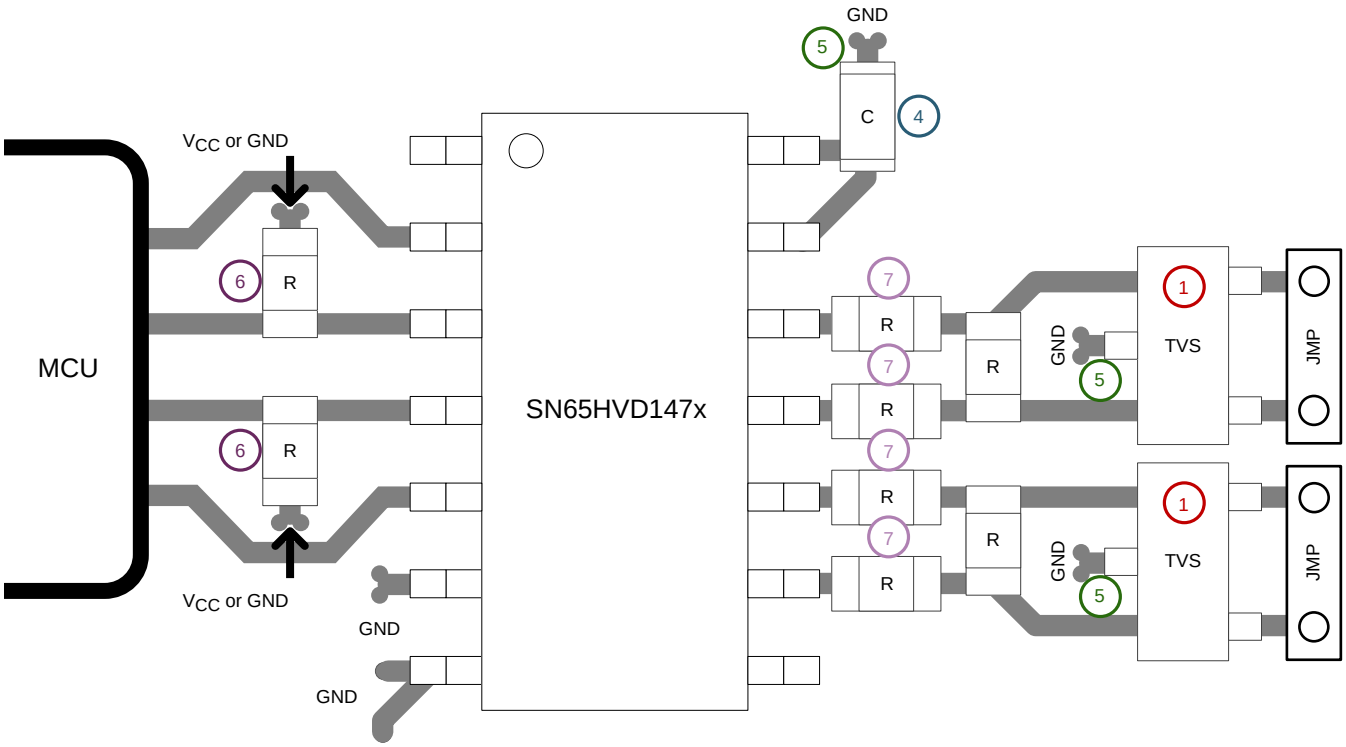



**Figure 41. SN65HVD147x Layout Example**

# 13 Device and Documentation Support

## 13.1 Device Support

### 13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

## 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 7. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN65HVD1470 | Click here | Click here | Click here | Click here | Click here |
| SN65HVD1471 | Click here | Click here | Click here | Click here | Click here |
| SN65HVD1473 | Click here | Click here | Click here | Click here | Click here |
| SN65HVD1474 | Click here | Click here | Click here | Click here | Click here |
| SN65HVD1476 | Click here | Click here | Click here | Click here | Click here |
| SN65HVD1477 | Click here | Click here | Click here | Click here | Click here |

## 13.3 Trademarks

All trademarks are the property of their respective owners.

## 13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD1470D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1470 | Samples |
| SN65HVD1470DGS | ACTIVE | VSSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1470 | Samples |
| SN65HVD1470DGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1470 | Samples |
| SN65HVD1470DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1470 | Samples |
| SN65HVD1471D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1471 | Samples |
| SN65HVD1471DGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1471 | Samples |
| SN65HVD1471DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1471 | Samples |
| SN65HVD1471DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1471 | Samples |
| SN65HVD1473D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1473 | Samples |
| SN65HVD1473DGS | ACTIVE | VSSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1473 | Samples |
| SN65HVD1473DGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1473 | Samples |
| SN65HVD1473DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1473 | Samples |
| SN65HVD1474D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1474 | Samples |
| SN65HVD1474DGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1474 | Samples |
| SN65HVD1474DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1474 | Samples |
| SN65HVD1474DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1474 | Samples |
| SN65HVD1476D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD1476DGS | ACTIVE | VSSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1476 | Samples |
| SN65HVD1476DGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1476 | Samples |
| SN65HVD1476DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 | Samples |
| SN65HVD1477D | ACTIVE | SOIC | D | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1477 | Samples |
| SN65HVD1477DGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1477 | Samples |
| SN65HVD1477DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1477 | Samples |
| SN65HVD1477DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1477 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

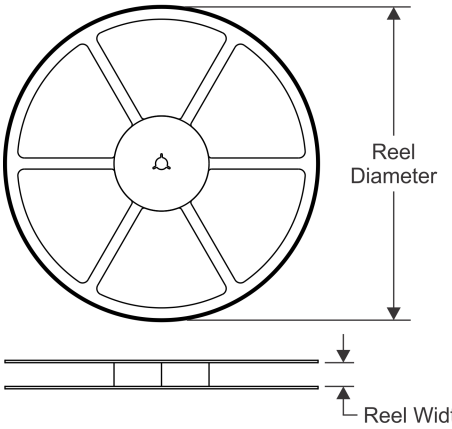
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

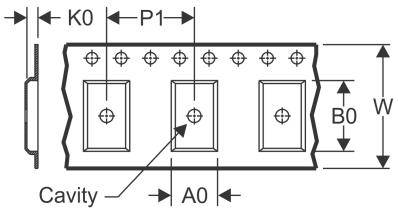
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

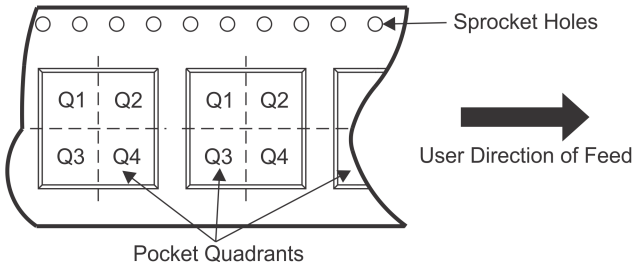



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

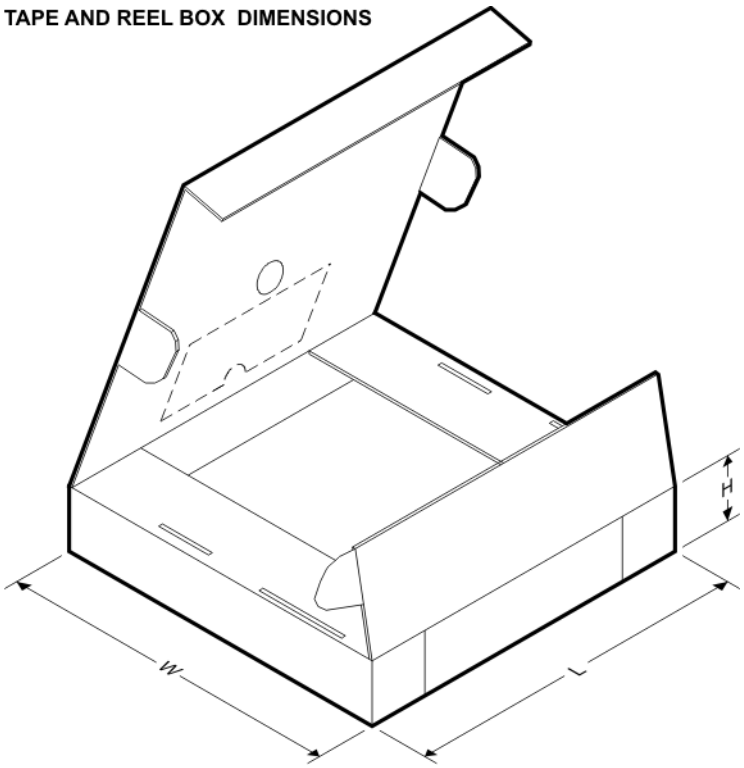
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD1470DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1470DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65HVD1471DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1473DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1474DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1474DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD1476DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1476DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65HVD1477DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

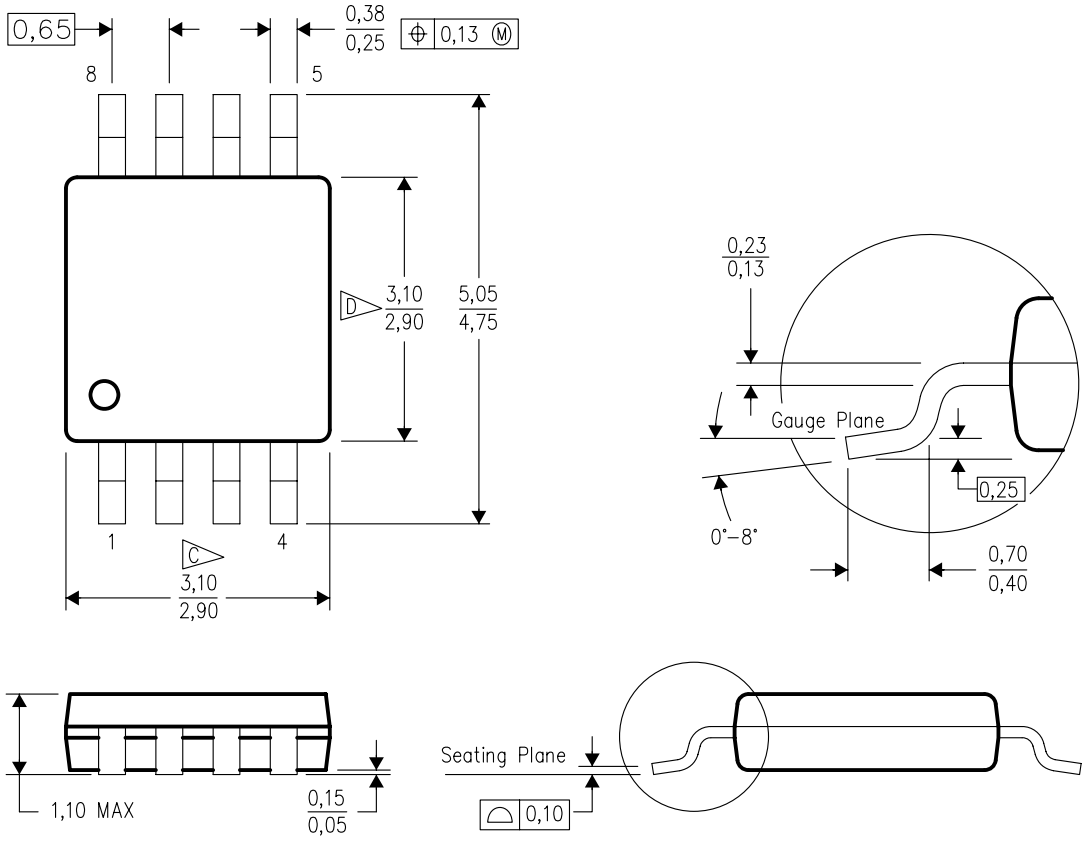
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65HVD1470DGSR | VSSOP | DGS | 10 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD1470DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN65HVD1471DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD1473DGSR | VSSOP | DGS | 10 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD1474DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD1474DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN65HVD1476DGSR | VSSOP | DGS | 10 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD1476DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN65HVD1477DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |

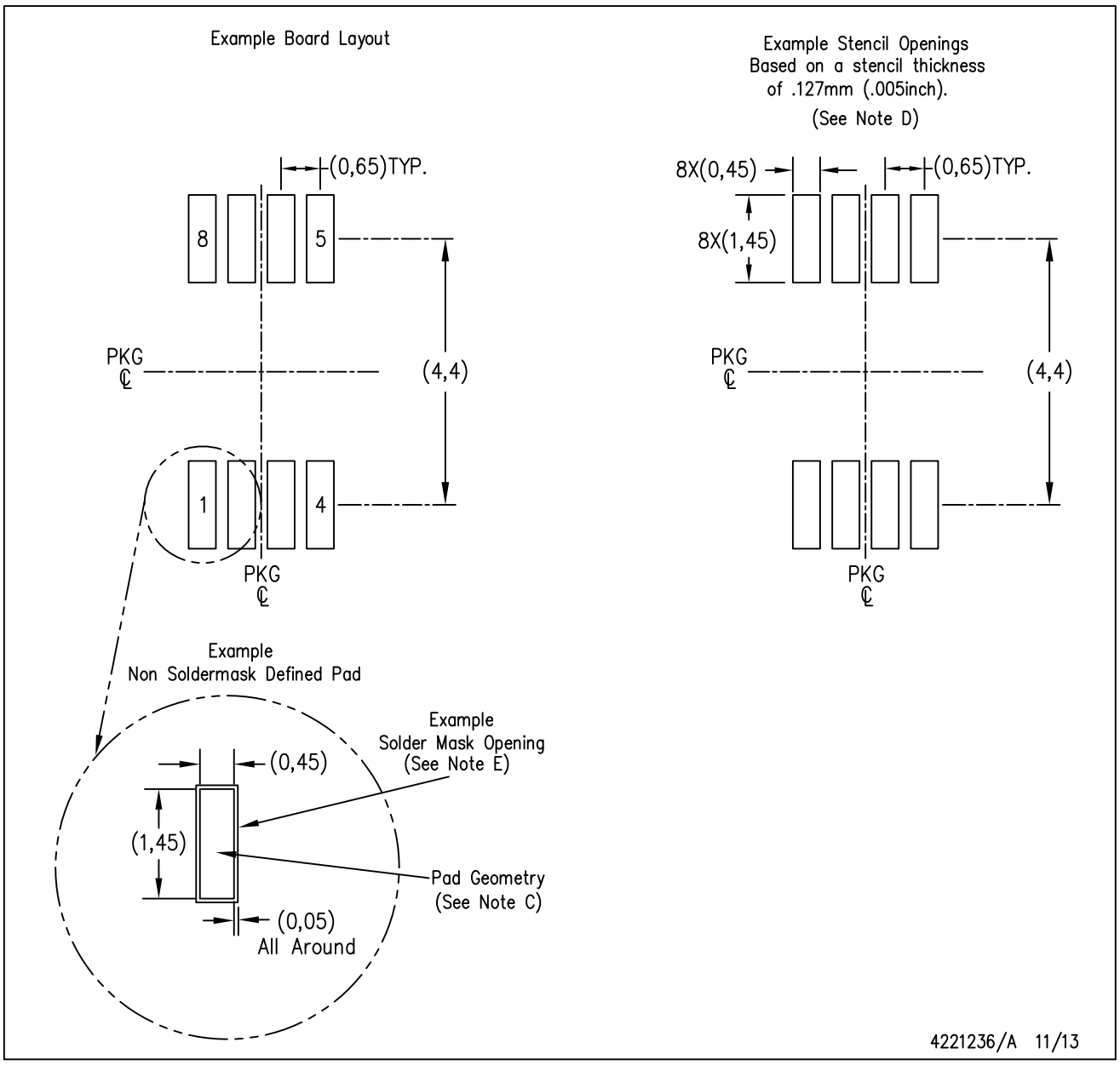
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

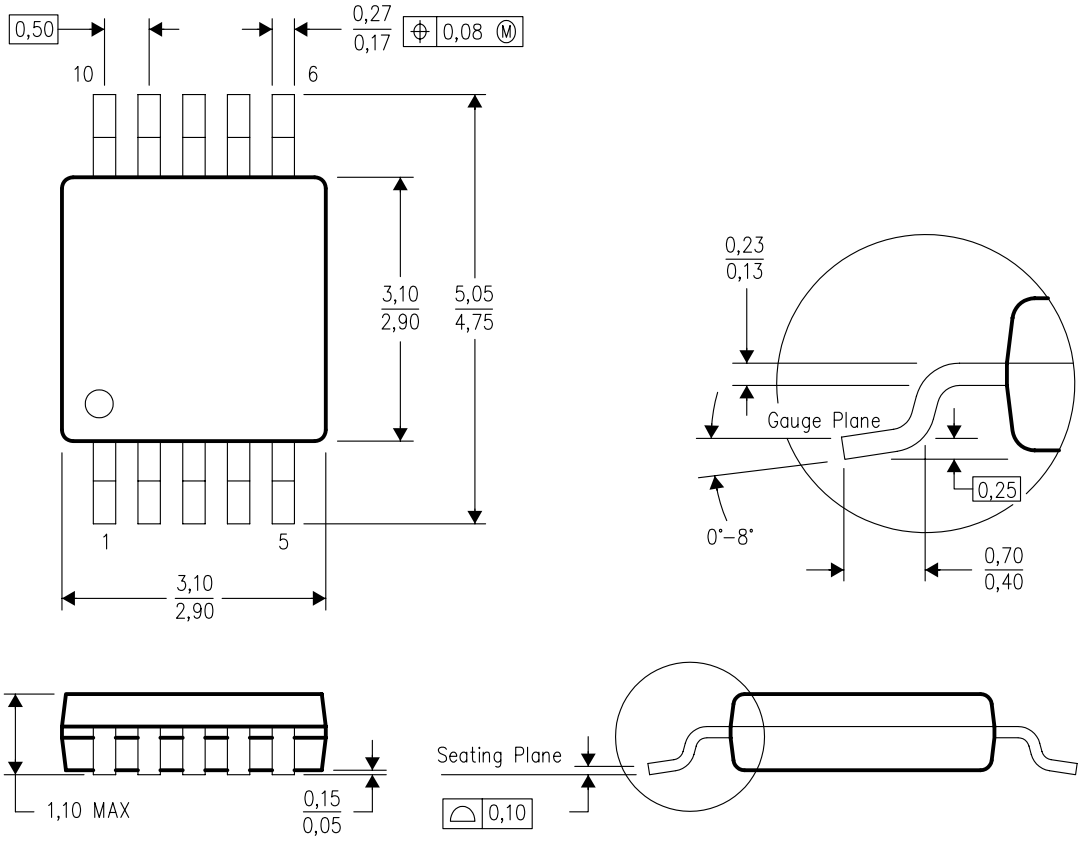
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

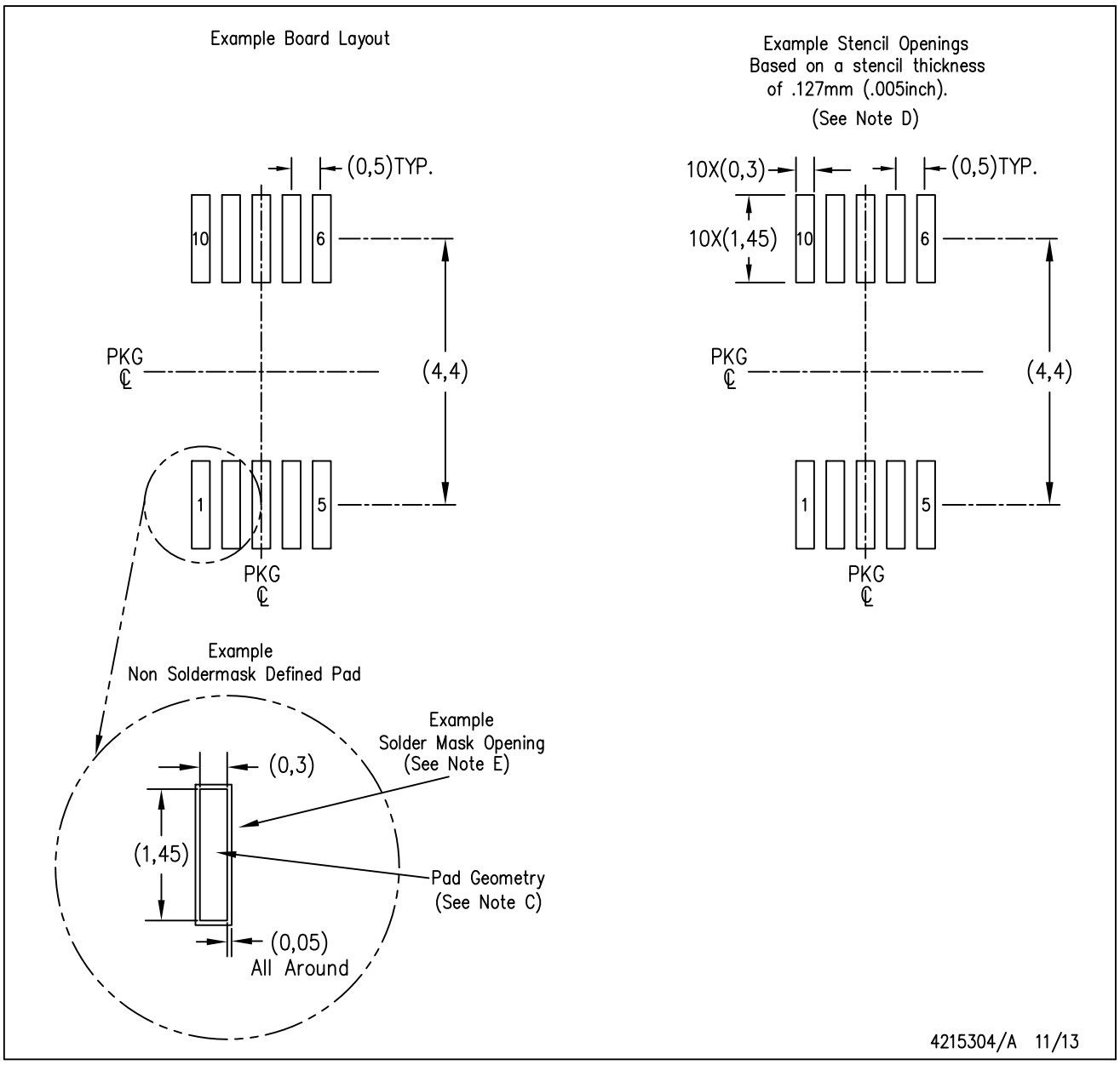
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE




4073272/C 02/04

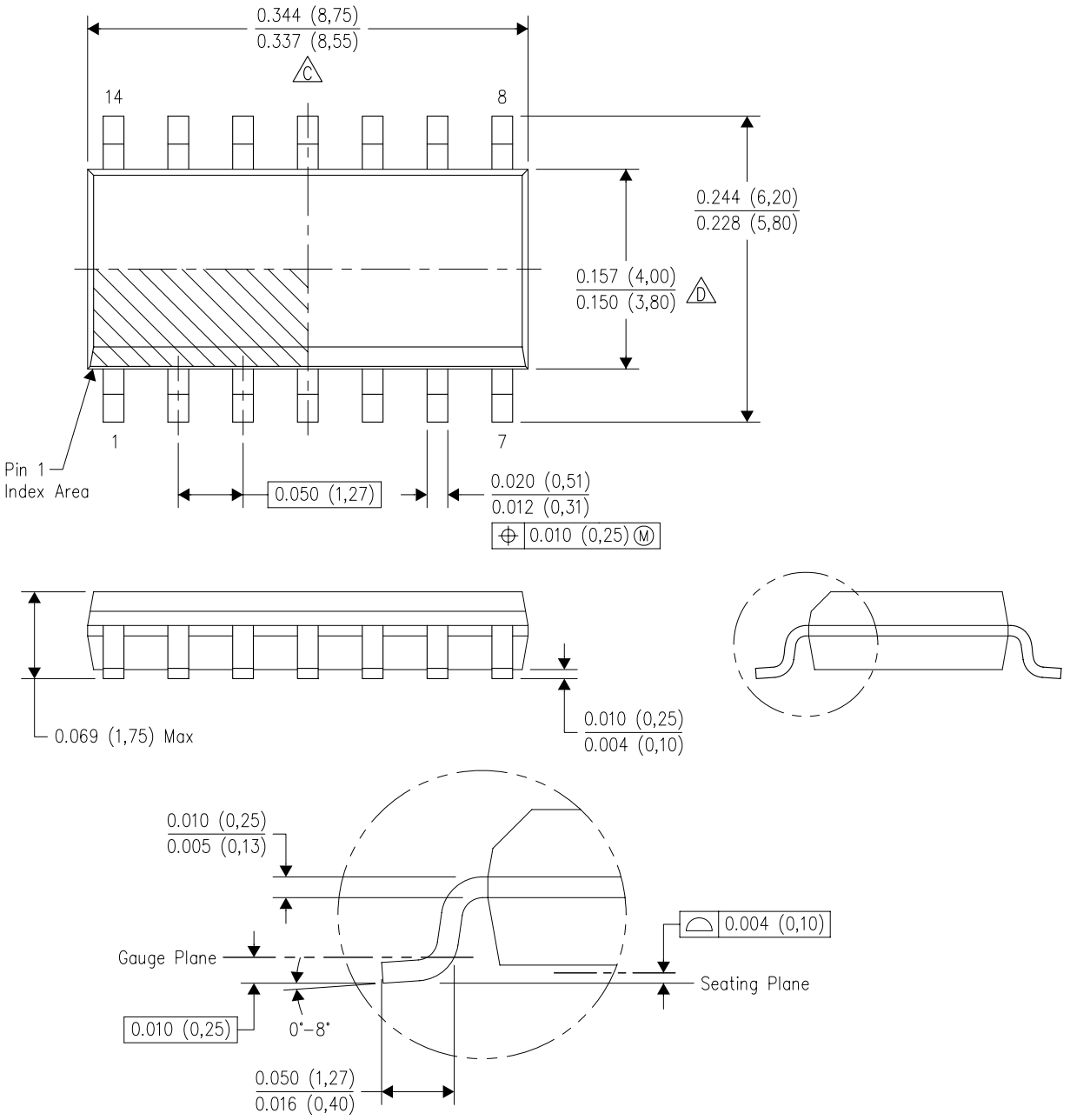
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

# DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

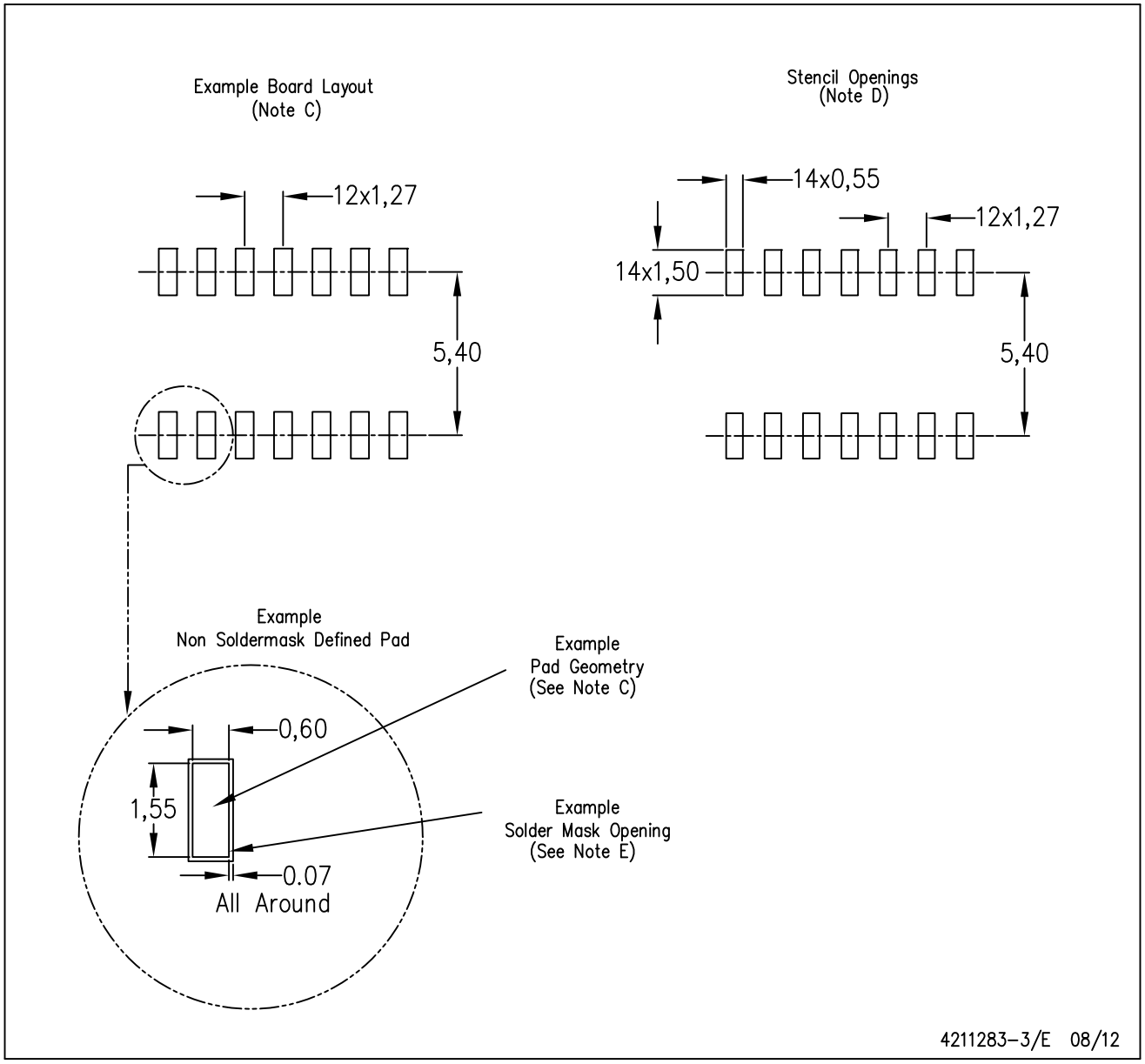
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

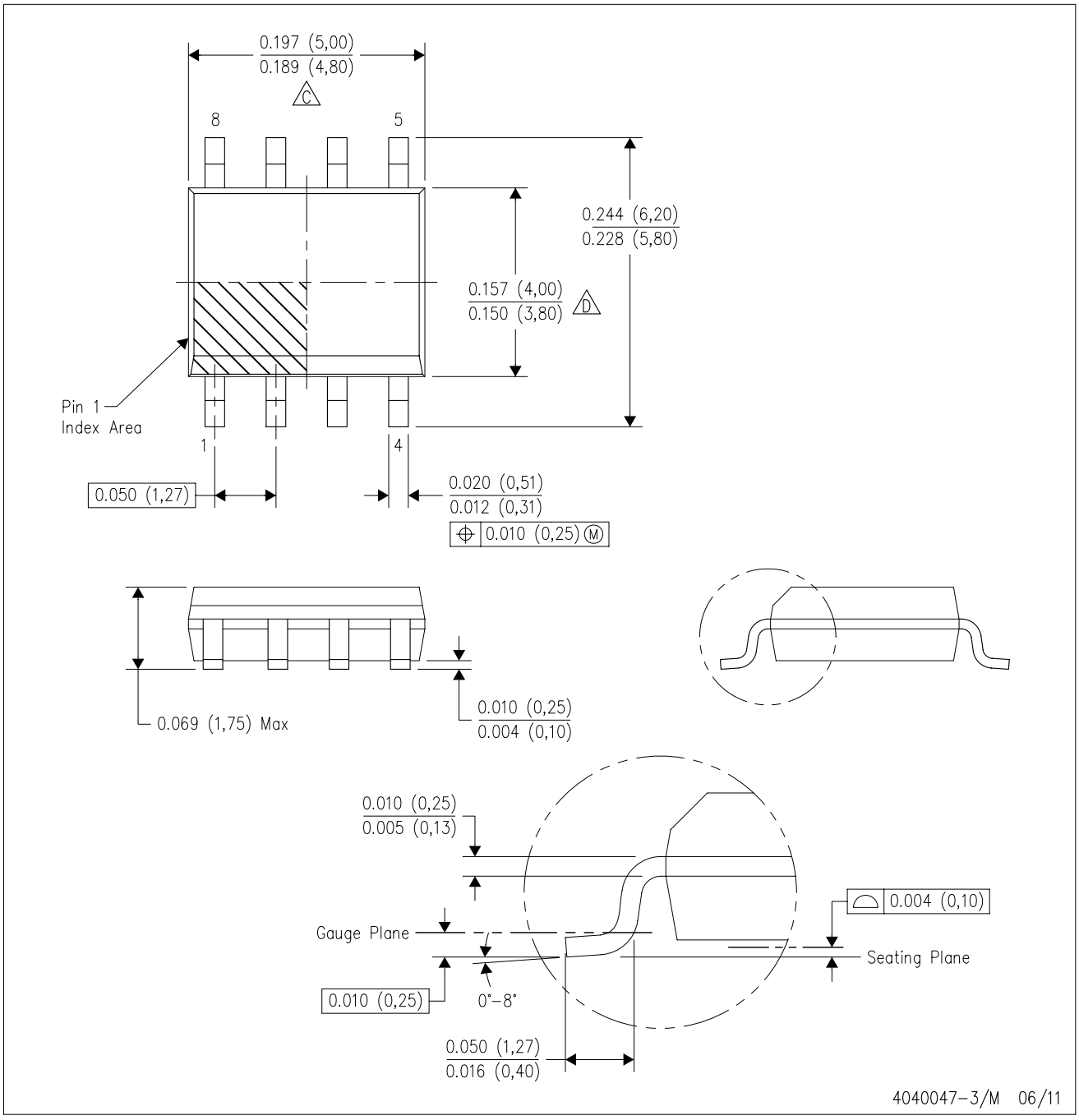
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



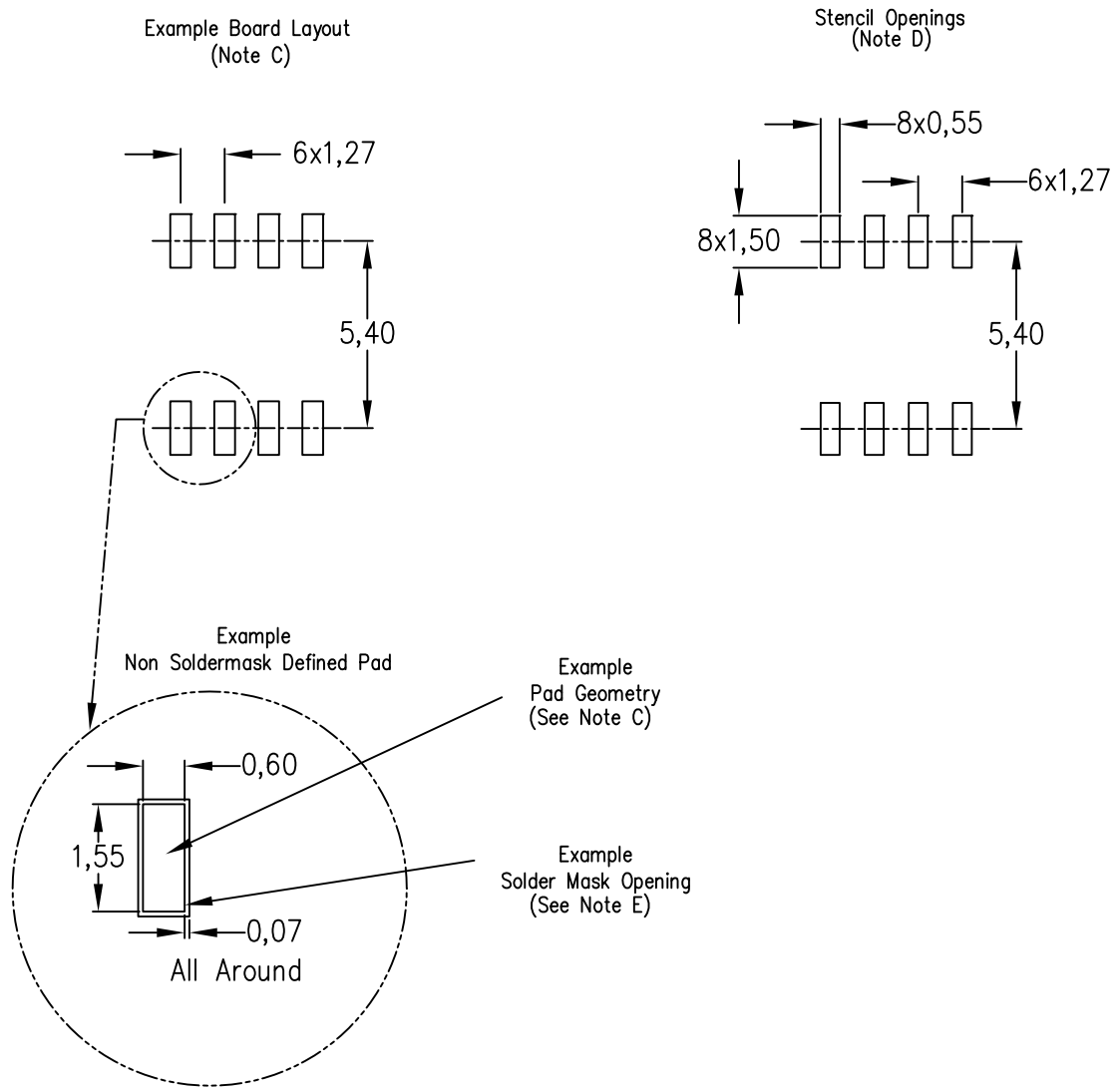

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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