Released Data Sheet

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iNAND *Extreme*™

e.MMC 5.0 with HS400 Interface

SanDisk®
951 SanDisk Drive, Milpitas, CA 95035

REVISION HISTORY

Doc. No	Revision	Date	Description
80-36-03680	0.1	15-Jul-13	Preliminary
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80-36-03680	0.5	14-Nov-13	- Remove boot area partition and RPMB area partition resize - Update register values and added e.MMC5.0 fields - Updated performance numbers
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80-36-03680	1.0	28-Jan-14	-Update device power numbers - Update device performance -Update register values: PNM, PWR_CL_DDR_200_360, CACHE_SIZE,PRODUCTION_STATE_AWARENESS_TIMEOUT - Smart Report updates - Added Reliability section
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1. INTRODUCTION

1.1. General Description

iNAND *Extreme* is an Embedded Flash Drive (EFD) designed for mobile handsets and consumer electronic devices. iNAND *Extreme* is a hybrid device combining an embedded thin flash controller and standard MLC NAND flash memory, with an industry standard e.MMC 5.0[1] interface.

Empowered with the new e.MMC 5.0 features such as HS400 interface, Product State Awareness, FFU, as well as legacy e.MMC 4.51 features such as Power Off Notifications, Packed commands, Cache, Boot / RPMB partitions, HPI, and HW Reset, the iNAND *Extreme* e.MMC is the optimal device for reliable code and data storage.

Designed specifically for mobile multimedia applications, iNAND *Extreme* is the most mature on board MMC device since 2005, providing mass storage of up to 64GB in JEDEC compatible form factors, with low power consumption and high performance - an ideal solution for multimedia handsets of 3G and 4G.

In addition to the high reliability and high system performance offered by the current iNAND family of products, iNAND *Extreme* offers plug-and-play integration and support for multiple NAND technology transitions, as well as features such as an advanced power management scheme.

iNAND *Extreme* uses advanced Multi-Level Cell (MLC) NAND flash technology, enhanced by SanDisk's embedded flash management software running as firmware on the flash controller.

The iNAND *Extreme* architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. In addition, SanDisk firmware employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and maximizing flash life expectancy.

SanDisk iNAND *Extreme* provides up to 64GB of memory for use in mass storage applications. In addition to the mass-storage-specific flash memory chip, iNAND *Extreme* includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

iNAND *Extreme* enables multimedia driven applications on mobile devices, such as music, imaging, video, TV, GPS, gaming, email, office and other applications.

The breakthrough in performance and design makes iNAND *Extreme* the ideal solution for high-end mobile handsets, tablets, and Automotive Infotainment vendors who require easy integration, fast time-to-market and high-capacity.

[1] Compatible to JESD84-B50

1.2. Plug-and-Play Integration

iNAND's optimized architecture eliminates the need for complicated software integration and testing processes thereby enabling plug-and-play integration into the host system. The replacement of one iNAND device with another of a newer generation requires virtually no changes to the host. This makes iNAND the perfect solution for mobile platforms and reference designs, as it allows for the utilization of more advanced NAND Flash technology with minimal integration or qualification efforts.

SanDisk's iNAND *Extreme* is well-suited to meet the needs of small, low power, electronic devices. With JEDEC form factors measuring 11.5x13mm (153 balls) for all capacities, iNAND *Extreme* is fit for a wide variety of portable devices such as high-end multimedia mobile handsets, tablets, and Automotive infotainment.

To support this wide range of applications, iNAND *Extreme* is offered with an MMC Interface. The MMC interface allows for easy integration into any design, regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device.

Figure 1 shows a block diagram of the SanDisk iNAND *Extreme* with MMC Interface.

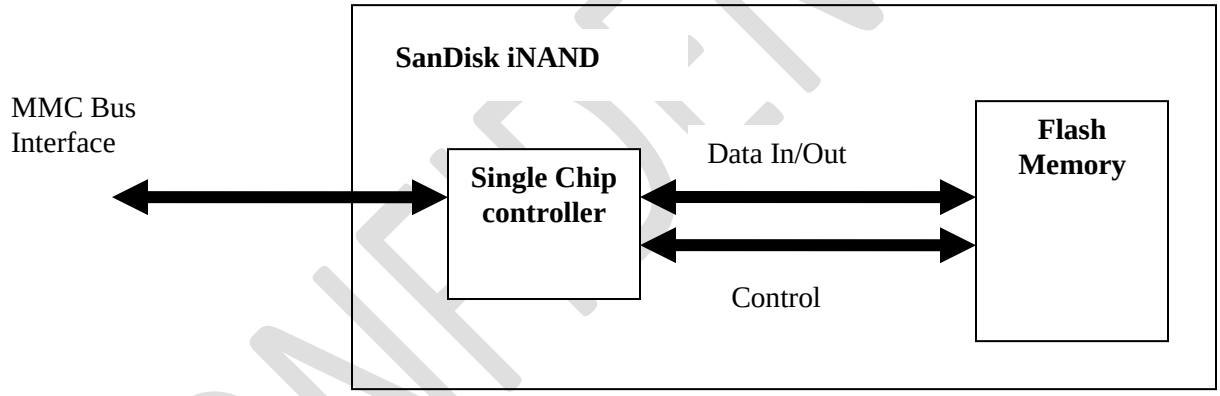

Figure 1 - SanDisk iNAND Extreme with MMC Interface Block Diagram

1.3. Feature Overview

SanDisk iNAND *Extreme*, with MMC interface, features include the following:

- Memory controller and NAND flash
- Mechanical design complies with JEDED Specification
- Offered in three TFBGA packages of e.MMC 5.0[2]
  - 11.5mm x 13mm x 1.0mm (16GB, 32GB, 64GB)
- Operating temperature range: –25C° to +85C°

[2] Refer to JEDEC Standards No. JESD84-B50

- Dual power system
- Core voltage (VCC) 2.7-3.6 V
- I/O (VCCQ) voltage, either: 1.7-1.95V or 2.7-3.6V
  - Note: Device operation under 3.3V VCCQ is limited to Max 1 hour
- Up to 64GB of data storage.
- Supports three data bus widths: 1bit (default), 4bit, 8bit.
- Complies with e.MMC Specification Ver. 5.0 HS400
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed), 0-200 MHz SDR (HS200), 0-200 MHz DDR (HS400)
- Up to 400 MB/sec bus transfer rate, using 8 parallel data lines at 200 MHz, HS400 Mode
- Correction of memory field errors
- Designed for portable and stationary applications that require high performance and reliable data storage

1.4. Defect and Error Management

The SanDisk iNAND *Extreme* contains a sophisticated defect and error management system. If necessary, iNAND will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume any user data space. In the extremely rare case that a read error does occur, iNAND has innovative algorithms to recover the data. These defect and error management systems, coupled with the solid state construction, give SanDisk iNAND *Extreme* unparalleled reliability.

1.5. MMC bus and Power Lines

SanDisk iNAND *Extreme* with MMC interface supports the MMC protocol. For more details regarding these buses refer to JEDEC standards No. JESD84-B50.

The iNAND bus has the following communication and power lines:

- CMD: Command is a bidirectional signal. The host and iNAND operate in two modes, open drain and push-pull.
- DAT0-7: Data lines are bidirectional signals. Host and iNAND operate in push-pull mode.
- CLK: Clock input.
- RST_n: Hardware Reset Input.
- VCCQ: VCCQ is the power supply line for host interface.
- VCC: VCC is the power supply line for internal flash memory.

- VDDi: VDDi is iNAND's internal power node, not the power supply. Connect 0.1uF capacitor from VDDi to ground.
- VSS, VSSQ: Ground lines.
- RCLK: Data strobe.
- VSF: Vendor specific functions used for debugging purposes.

1.5.1. Bus operating conditions

Table 1 - Bus operating conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA

Table 2 – Power supply voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ (Low)	1.7	1.95	V
	VCCQ (High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.3	0.3	V

Note1: HS400 mode only supports the 1.7 – 1.95 V VCCQ option

Note2: Device operation under 3.3V VCCQ is limited to Max 1 hour

2. e.MMC 5.0 Selected Features Overview

2.1. HS400 Interface

Support HS400 signaling to achieve a bus speed of 400 MB/s via a 200MHz dual data rate clock frequency. HS400 mode supports 4 or 8 bit bus width and the 1.7 – 1.95 VCCQ option. Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data. For additional information please refer to JESD84-B50 standard.

2.2. Production State Awareness (Auto Mode)

The e.MMC device could utilize the information of whether it is in production environment and operate differently than it operates in the field.

For example, content which was loaded into the storage device prior to soldering might get corrupted, at higher probability, during device soldering. The e.MMC device could use “special” internal operations for loading content prior to device soldering which would reduce production failures and use “regular” operations post-soldering.

For additional information please refer to JESD84-B50 standard and the SanDisk application note on this subject.

2.3. Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism the host downloads a new version of the firmware to the e.MMC device and, following a successful download, instructs the e.MMC device to install the new downloaded firmware into the device. The whole FFU process can happen while allowing the Host to perform other operations in parallel and without affecting the user / OS data. During the FFU process, the host can replace firmware files or single / all file systems.

The secure FFU (sFFU) usage model for firmware upgrades is as follows:

1. sFFU files are generated and signed at the SanDisk lab.
2. The sFFU files are handed to SanDisk’s customer.
3. SanDisk’s customer can push the firmware updates to their end-users in a transparent way.

   Note 1: The sFFU process and sFFU files are protected against leakage to unauthorized entities.

   Note 2: During the sFFU process the Host may retrieve the exact status of the process using the smart report feature.

For additional information please refer to JESD84-B50 standard and the SanDisk application note on this subject.

2.4. Cache

The eMMC cache is dedicated volatile memory at the size of 512KB. Caching enables to improve iNAND performance for both sequential and random access. For additional information please refer to JESD84-B50 standard.

2.5. Discard

iNAND supports discard command as defined in e.MMC 5.0 spec[3]. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of iNAND and reduce amount of housekeeping operation.

2.6. Power off Notifications

iNAND supports power off notifications as defined in e.MMC 5.0 spec[4]. The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on. Note that the device may be set into sleep mode while power off notification is enabled.

Power off notification long allows the device to shutdown properly and save important data for fast boot time on the next power cycle.

2.7. Packed Commands

To enable optimal system performance, iNAND supports packed commands as defined in e.MMC 5.0 spec[5]. It allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overheads.

2.8. Boot Partition

iNAND supports e.MMC 5.0 boot operation mode: Factory configuration supplies two boot partitions each 4MB in size for 16GB-64GB

2.9. RPMB Partition

iNAND supports e.MMC 5.0 RPMB operation mode: Factory configuration supplies one RPMB partition 4MB in size for 16GB-64GB

2.10. Automatic Sleep Mode

A unique feature of iNAND is automatic entrance and exit from sleep mode. Upon completion of an operation, iNAND enters sleep mode to conserve power if no further commands are received. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most

[3] For additional information refer to JEDEC Standard No. JESD84-B50

[4] For additional information refer to JEDEC Standard No. JESD84-B50

[5] For additional information refer to JEDEC Standard No. JESD84-B50

systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep and respond immediately.

2.11.Sleep (CMD5)

An iNAND *Extreme* device may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The VCC power supply may be switched off in Sleep state to enable even further system power consumption saving.

For additional information please refer to JESD84-B50.

2.12.Enhanced Reliable Write

iNAND *Extreme* supports enhanced reliable write as defined in e.MMC 5.0 spec[6].

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

2.13.Sanitize

The Sanitize operation is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue the sanitize operation, with busy asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

After the sanitize operation is complete no data should exist in the unmapped host address space.

2.14.Secure Erase

For backward compatibility reasons, in addition to the standard erase command the iNAND *Extreme* supports the optional Secure Erase command[7].

This command allows the host to erase the provided range of LBAs and ensure no older copies of this data exist in the flash.

[6] For additional information refer to JEDEC Standards No. JESD84-B50

[7] For additional information refer to JEDEC Standards No. JESD84-B50

2.15.Secure Trim

For backward compatibility reasons, iNAND *Extreme* support Secure Trim command. The Secure Trim[8] command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups.

The secure trim command is performed in two steps:

1) Mark the LBA range as candidate for erase.
2) Erase the marked address range and ensure no old copies are left.

2.16.Partition Management

iNAND *Extreme* offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block area scan be classified as follows

- Factory configuration supplies two boot partitions (refer to section 2.8) implemented as enhanced storage media and one RPMB partitioning of 4MB in size (refer to section 2.9).
- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size can be programmed once in device life-cycle (one-time programmable).

2.17.Device Health

Device Health is similar to SMART features of modern hard disks, it provides only vital NAND flash program/erase cycles information in percentage of useful flash life span.

The host can query Device Health information utilizing standard MMC command, to get the extended CSD structure:

DEVICE_LIFE_TIME_EST_TYP_A[268], The host may use it to query SLC device health information

DEVICE_LIFE_TIME_EST_TYP_B[269], The host may use it to query MLC device health information

The device health feature will provide a % of the wear of the device in 10% fragments.

2.18.EOL Status

EOL status is implemented according to the eMMC 5.0 spec. One additional state (state 4) was added to INAND *Extreme* which indicates that the device is in EOL mode.

[8] For additional information refer to JEDEC Standards No. JESD84-B50

2.19.Enhanced Write Protection

To allow the host to protect data against erase or write iNAND *Extreme* supports two levels of write protect command

- The entire iNAND *Extreme* (including the Boot Area Partitions, General Purpose Area Partition, and User Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD.
- Specific segments of iNAND *Extreme* may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register.

For additional information please refer to the JESD84-B50 standard.

2.20.High Priority Interrupt (HPI)

The operating system usually uses demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

The high priority interrupt (HPI) as defined in JESD84-B50 enables low read latency operation by suspending a lower priority operation before it is actually completed.

For additional information on the HPI function, refer to JESD84-B50.

2.21.H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted. For more information, refer to JESD84-B50 standard.

3. TECHNICAL NOTES

3.1. Smart Report

Smart Report helps the user to obtain important information on certain features procedures.

In order to extract Smart Report information the following procedure shall be followed:

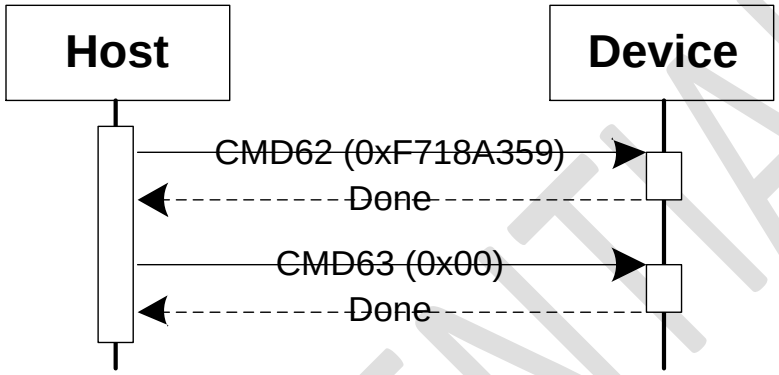

Figure 2 - SanDisk iNAND Extreme Smart Report Extraction flow

The table below shows the structure of the iNAND *Extreme* smart report which includes mainly Production Awareness (offsets 0-49) and Field Firmware Upgrade (FFU, offsets 51) information.

Table 3 – Smart Report Parameters

Field offset	Field name	Description
0	currState	The current state of preloading: 1) NONE: Preloading not started yet. 2) PRELOADING: Preloading in-progress. 3) HANDLING: Preloading finished, now performing relocations. 4) FINISHED: Finished relocations of all preloaded data.
1	maxMlcPercent	The maximum percentage of MLC partition allowed for preloading data
2	bImplicitDefault	Whether implicit mode is turned on or not (DEFAULT = On). Implicit mode allows customers / host systems that do not support eMMC 5.0 to use the production awareness feature by turning on preloading by default without a command from the host. *Note*: Auto preloading modes are based on eMMC 5.0.
3	preloadingMode	Mode of last preloading done (Implicit / Auto).

Field offset	Field name	Description
4	maxMlcSectors	Maximum MLC sectors allowed for preloading. This field is calculated based on the maxMlcPercent field.
8	maxMlcInImplicit	Maximum MLC sectors allowed for preloading in Implicit mode. In implicit mode more data can be written, this parameter describes the additional percentage beyond the maxMlcPercent parameter that can be preloaded (DEFAULT = 3%).
12	configuredSectors	Only relevant during the PRELOADING state and notifies on how much data the host is going to preload.
16	sectorsDone	Only relevant during the PRELOADING state and notifies on how much data the host has already preloaded to this point. This parameters includes both MLC and enhanced partition information.
20	mlcSectorsDone	Only relevant during the PRELOADING state and notifies on how much data into the MLC partition the host has already preloaded to this point. MLC size cannot be larger than defined by maxMlcSectors.
24	mlcPercentDone	Only relevant during the PRELOADING state and notifies on how much percentage of data is preloaded out of the MLC partition.
28	unhandledSectors	When PRELOADING is done the data is relocated to the regular MLC area gradually. This field is populated in the HANDLING state and notified on how much data was not relocated to MLC.
32-49	Spare for Production Awareness	
50	sFFU Failure Reason	sFFU session status: 0: Success 1 - 255: Failure Reasons
51-511	Reserved	

4. PRODUCT SPECIFICATIONS

4.1. Typical Power Requirements

Table 4 – iNAND Extreme Sleep Power Consumption (Ta=25°C@3.3/1.8V)

	Max Value	Units
Sleep (CMD5 – VCCQ, VCC off)	360	uA

Table 5 - iNAND Extreme Active Power Consumption, Absolute Peak VCC / VCCQ (Ta=25°C@3.3V/1.8V)

			16GB	32GB	64GB	Units
HS400	**Active**	Absolute Peak VCC	380	500	500	mA
		Absolute Peak VCCQ	480	500	500	mA
HS200	**Active**	Absolute Peak VCC	360	500	500	mA
		Absolute Peak VCCQ	400	400	400	mA

Table 6 - iNAND Extreme Active Power Consumption, RMS VCC / VCCQ (Ta=25°C@3.3V/1.8V)

			16GB	32GB	64GB	Units
HS400	**Read**	RMS [100ms window] VCC	180	220	220	mA
		RMS [100ms window] VCCQ	350	350	350	mA
	Write	RMS [100ms window] VCC	120	200	200	mA
		RMS [100ms window] VCCQ	175	210	210	mA
HS200	**Read**	RMS [100ms window] VCC	115	140	140	mA
		RMS [100ms window] VCCQ	270	270	270	mA
	Write	RMS [100ms window] VCC	120	200	200	mA
		RMS [100ms window] VCCQ	175	210	210	mA

Note 1: In sleep state, triggered by CMD5, Flash VCC power supply is switched off

Note 2: Assumption is max Read/Write sustained sequential performance.

Note 3: Current specs include a statistical margin (4 standard deviations over measured mean) to show worst possible current that could be observed over the lifetime of the product.

4.2. Operating Conditions

4.2.1. Operating and Storage Temperature Specifications

Table 7 - Operating and Storage Temperatures

Temperature	Minimum and Maximum Operating*	-25° C to 85° C
	Minimum and Maximum Non-Operating: After soldered onto PCBA	-40° C to 85° C

* Per eMMC5.0 specification (JESD84-B50): To achieve optimized power/performance, maximum Tcase temperature should not exceed 85°C.

4.2.2. Moisture Sensitivity

The moisture sensitivity level for iNAND *Extreme* is MSL = 3.

4.3. Reliability

SanDisk iNAND Extreme product meets or exceeds NAND type of products Endurance and Data Retention requirements as per evaluated representative usage models for designed market and relevant sections of JESD47I standard.

Table 8 - Critical Reliability Characteristics

Reliability Characteristics	Description	Value
Uncorrectable Bit Error Rate (UBER)	Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. In such rare events data can be lost.	1 sector in 10^{15} bits read
Write Endurance Specification (TBW)	Write endurance is commonly classified in Total Terabytes Written (TBW) to a device. This is the total amount of data that can be written to the device over its useful life time and depends on workload. Representative workload description: • 84% Sequential write , 16% Random Write • Chunk Size IOs Distribution: 30% : 4KB, 27% : 16KB, 42% : Mix of 8KB, 32KB-256KB, 1% : 512KB • Cache On, Packed Off • Host data is 4K aligned	Total Terabytes Written [TBW] Per representative Android workload: 16GB: 16 [TB] 32GB: 32 [TB] 64GB: 64 [TB]
Data Retention Specification (Years)	Data Retention for fresh and cycled up to 10% of maximum Write Endurance specification devices	10 years of Data Retention @ 55°C
	Data Retention for cycled up to maximum Write Endurance specification devices	1 year of Data Retention @ 55°C

4.4. System Performance

All performance values for iNAND *Extreme* in Table were measured under the following conditions:

- Voltage range:

  Core voltage (VCC): 2.7-3.6 V

  Host voltage (VCCQ), either: 1.7-1.95 V or 2.7-3.6V

Note: Device operation under 3.3V VCCQ is limited to Max 1 hour

- Operating temperature -25° C to 85° C

Table 9 – Sustained Sequential Performance

SKU	Write (MB/s)		Read (MB/s)
	Cache ON	Cache OFF	
SDIN9DW4-16G	45	40	300
SDIN9DW4-32G SDIN9DW4-64G	80	75	300

Table 10 – Random Performance

SKU	Write (IOPS)		Read (IOPS)
	Cache ON	Cache OFF	
SDIN9DW4-16G SDIN9DW4-32G SDIN9DW4-64G	3000	1,500	6000

Note 1: Sustained Sequential Read/Write performance is measured under HS400 mode with a bus width of 8 bit at 200 MHz DDR mode, chunk size of 512KB, and data transfer of 1GB.

Note 2: Random performance is measured with a chunk size of 4KB and address range of 1GB.

Note 3: All performance is measured using SanDisk proprietary test environment, without file system overhead and host turn-around time (HTAT).

Table 11 – System Timing Performance

Operation	Values		Unit	Remark
	Worst Case	Typical		
CMD1 to Ready after Power-up	1000	<300	ms	
CMD1 to Ready after PoN LONG And Power up	100	60	ms	
Enter / Exit Automatic Sleep Mode (Cache Off)	1	0.6	ms	
Enter / Exit Automatic Sleep Mode (Cache On)	25	<10	ms	
Enter CMD5 Sleep state	5	2.5	ms	
Exit CMD5 sleep (VCC OFF)	10	5	ms	
HPI	50	<10	ms	
Secure Erase/Trim	2.5	1	min	For 512KB
Erase/Trim	900	<10	ms	
Sanitize	8	1	min	16GB device
Block Read Access Time	100	0.5	ms	
Block Write Access Time	250	1	ms	

5. PHYSICAL SPECIFICATIONS

The SanDisk iNAND Extreme is a 153-pin, thin fine-pitched ball grid array (BGA). See Figure 3, Figure 4, and Tables 12/13 for physical specifications and dimensions.

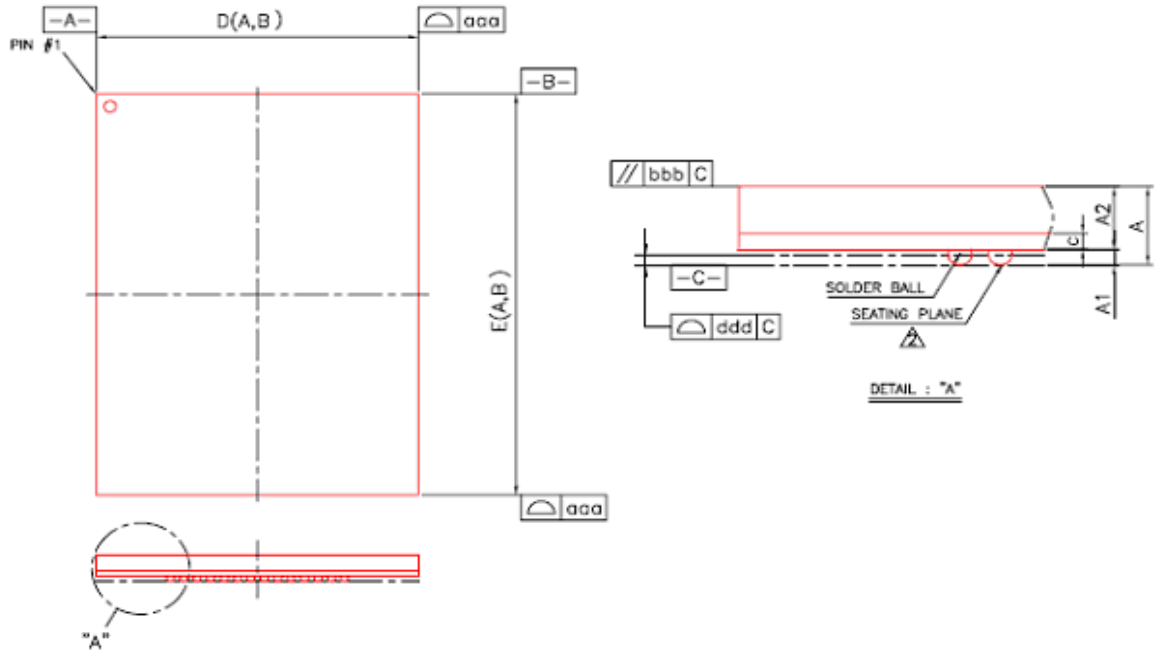

Figure 3 - INAND Extreme Specification Top and Side View (Detail A)

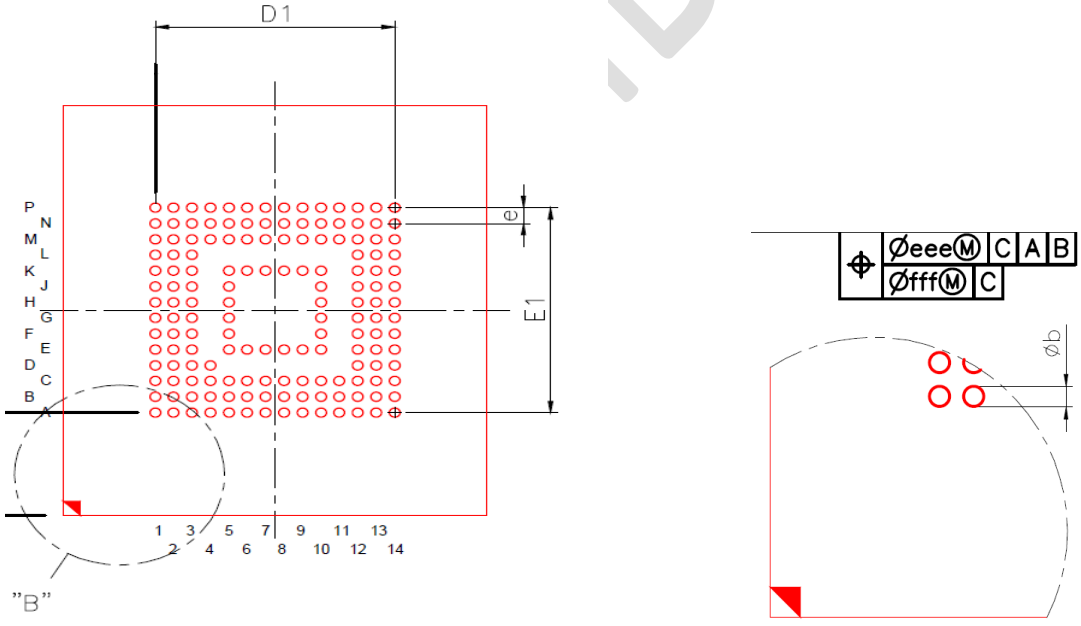

Figure 4- Package Outline Drawing – bottom view

Table 12 – iNAND Extreme Package Specification 16-32GB

	Dimension in millimeters			Dimension in inches		
Symbol	**Minimum**	**Nominal**	**Maximum**	**Minimum**	**Nominal**	**Maximum**
A	---	---	1.00	---	---	0.039
A1	0.17	0.22	0.27	0.007	0.009	0.011
A2	0.61	0.66	0.73	0.024	0.026	0.029
C	0.07	0.10	0.13	0.003	0.004	0.005
D(A,B)	11.43	11.50	11.57	0.450	0.453	0.456
E(A,B)	12.93	13.00	13.07	0.509	0.513	0.514
D1	---	6.50	---	---	0.256	---
E1	---	6.50	---	---	0.256	---
e	---	0.50	---	---	0.020	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.05			0.002		
MD/ME	14/14			14/14		

Table 13 – iNAND Extreme Package Specification 64GB

	Dimension in millimeters			Dimension in inches		
Symbol	**Minimum**	**Nominal**	**Maximum**	**Minimum**	**Nominal**	**Maximum**
A	---	---	1.0	---	---	0.039
A1	0.17	0.22	0.27	0.007	0.009	0.011
A2	0.62	0.67	0.76	0.024	0.026	0.03
C	0.07	0.10	0.13	0.003	0.004	0.005
D(A,B)	11.43	11.50	11.57	0.450	0.453	0.456
E(A,B)	12.93	13.00	13.07	0.509	0.511	0.514
D1	---	6.50	---	---	0.256	---
E1	---	6.50	---	---	0.256	---
e	---	0.50	---	---	0.020	---
b	0.25	0.3	0.35	0.010	0.012	0.014
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.05			0.002		
MD/ME	14/14			14/14		

6. INTERFACE DESCRIPTION

6.1. MMC I/F Ball Array

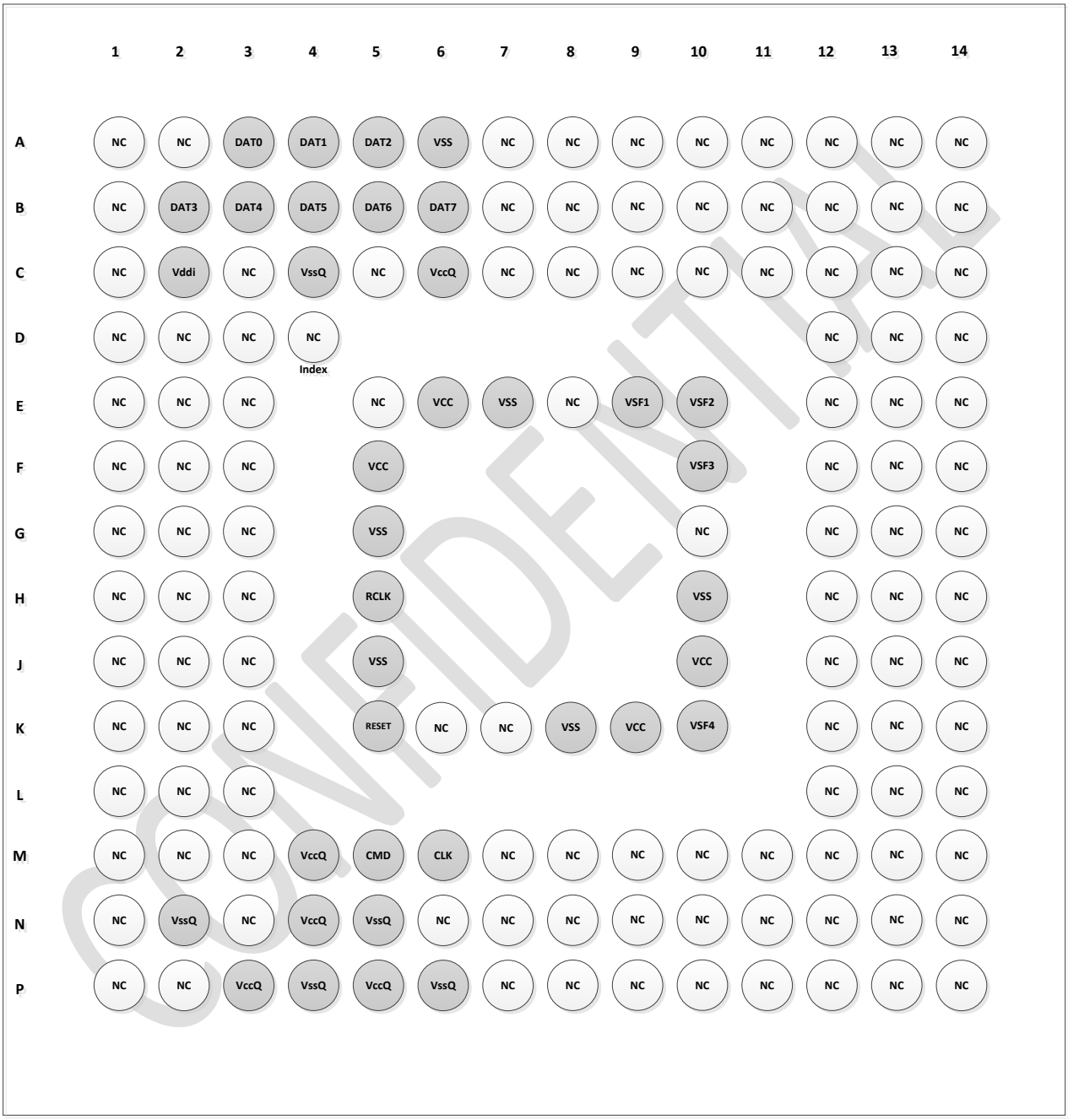

Figure 5 - 153 balls - Ball Array (Top View)

6.2. Pins and Signal Description

Table 14 contains the SanDisk iNAND *Extreme*, with MMC interface (153 balls), functional pin assignment.

Table 14 – Functional Pin Assignment, 153 balls

Ball No.	Ball Signal	Type	Description
A3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RST_n		Hardware Reset
H5	RCLK	Output	Data Strobe
E6	VCC	Supply	Flash I/O and memory power supply
F5	VCC		
J10	VCC		
K9	VCC		
C6	VCCQ	Supply	Memory controller core and MMC I/F I/O power supply
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
E7	VSS	Supply	Flash I/O and memory ground connection
G5	VSS		
H10	VSS		
K8	VSS		
A6	VSS		
J5	VSS		
C4	VSSQ	Supply	Memory controller core and MMC I/F ground connection
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
C2	VDDi		Internal power node. Connect 0.1uF capacitor from VDDi to ground
E9	VSF1	VSF	Vendor Specific Function balls for test/debug. VSF balls should be floating and be brought out to test pads.
E10	VSF2		
F10	VSF3		
K10	VSF4		

Note: All other pins are not connected [NC] and can be connected to GND or left floating

6.3. iNAND *Extreme* Registers

6.3.1. OCR Register

Parameter	OCR slice	Description	Value	Width
Access Mode	[30:29]	Access mode	2h	2
	[23:15]	VDD: 2.7 - 3.6 range	1FFh	9
	[14:8]	VDD: 2.0 - 2.6 range	00h	7
	[7]	VDD: 1.7 - 1.95 range	1h	1

Note: Bit 30 is set because the device is High Capacity; bit 31 will be set only when the device is ready.

6.3.2. CID Register

Parameter	CID slice	Description	Value	Width
MMC MID	[127:120]	Manufacturer ID	45h	8
CBX	[113:112]	Card BGA	1h	2
OID	[111:104]	OEM/Application ID	01h	8
PNM	[103:56]	Product name	16GB: (“SDW16G" = 534457313647h) 32GB: ("SDW32G" = 534457333247h) 64GB: (“SDW64G” = 534457363447h)	48
PRV	[55:48]	Product revision	01h	8
PSN	[47:16]	Product serial number	Random by Production	32
MDT	[15:8]	Manufacturing date	month, year	8
CRC	[7:1]	CRC7 checksum	00h	7

Note: Please refer to the definition of the MDT field as defined in eMMC Spec version 5.0.

6.3.3. DSR Register

Parameter	DSR slice	Description	Value	Width
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

Note: DSR is not implemented; in case of read, a value of 0x0404 will be returned.

6.3.4. CSD Register

Parameter	CSD Slice	Description	Value	Width
CSD_STRUCTURE	[127:126]	CSD structure	3h	3
SPEC_VERS	[125:122]	System specification version	4h	4
TAAC	[119:112]	Data read access-time 1	0Fh	8
NSAC	[111:104]	Data read access-time 2 in CLK cycles (NSAC*100)	00h	8

TRAN_SPEED	[103:96]	Max. bus clock frequency	32h	8
CCC	[95:84]	Card command classes	0F5h	12
READ_BL_LEN	[83:80]	Max. read data block length	9h	4
READ_BL_PARTIAL	[79:79]	Partial blocks for read allowed	0b	1
WRITE_BLK_MISALIGN	[78:78]	Write block misalignment	0b	1
READ_BLK_MISALIGN	[77:77]	Read block misalignment	0b	1
DSR_IMP	[76:76]	DSR implemented	0b	1
*C_SIZE	[73:62]	Device size	FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. read current @ VDD min	7h	3
VDD_R_CURR_MAX	[58:56]	Max. read current @ VDD max	7h	3
VDD_W_CURR_MIN	[55:53]	Max. write current @ VDD min	7h	3
VDD_W_CURR_MAX	[52:50]	Max. write current @ VDD max	7h	3
C_SIZE_MULT	[49:47]	Device size multiplier	7h	3
ERASE_GRP_SIZE	[46:42]	Erase group size	1Fh	5
ERASE_GRP_MULT	[41:37]	Erase group size multiplier	1Fh	5
WP_GRP_SIZE	[36:32]	Write protect group size	0Fh	5
WP_GRP_ENABLE	[31:31]	Write protect group enable	1h	1
DEFAULT_ECC	[30:29]	Manufacturer default	0h	2
R2W_FACTOR	[28:26]	Write speed factor	2h	3
WRITE_BL_LEN	[25:22]	Max. write data block length	9h	4
WRITE_BL_PARTIAL	[21:21]	Partial blocks for write allowed	0h	1
CONTENT_PROT_APP	[16:16]	Content protection application	0h	1
FILE_FORMAT_GRP	[15:15]	File format group	0h	1
COPY	[14:14]	Copy flag (OTP)	1h	1
PERM_WRITE_PROTECT	[13:13]	Permanent write protection	0h	1
TMP_WRITE_PROTECT	[12:12]	Temporary write protection	0h	1
FILE_FORMAT	[11:10]	File format	0h	2
ECC	[9:8]	ECC code	0h	2
CRC	[7:1]	Calculated CRC	00h	7

6.3.5. EXT_CSD Register

Parameter	ECSD slice [bytes]	Description	Value
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background operations support	1h
MAX_PACKED_READS	[501]	Max packed read commands	3Fh
MAX_PACKED_WRITES	[500]	Max packed write commands	3Fh
DATA_TAG_SUPPORT	[499]	Data Tag Support	1h

Parameter	ECSD slice [bytes]	Description	Value
TAG_UNIT_SIZE	[498]	Tag Unit Size	3h
TAG_RES_SIZE	[497]	Tag Resources Size	3h
CONTEXT_CAPABILITIES	[496]	Context management capabilities	5h
LARGE_UNIT_SIZE_M1	[495]	Large Unit size	0h
EXT_SUPPORT	[494]	Extended partitions attribute support	3h
SUPPORTED_MODES	[493]	FFU supported modes	3h
FFU_FEATURES	[492]	FFU features	0h
OPERATION_CODES_TIMEOUT	[491]	Operation codes timeout	10h
FFU_ARG	[490:487]	FFU Argument	0h
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	Number of FW sectors correctly programmed	0h
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	Vendor proprietary health report	0h
DEVICE_LIFE_TIME_EST_TYP_B	[269]	Device life time estimation type B (MLC)	1h
DEVICE_LIFE_TIME_EST_TYP_A	[268]	Device life time estimation type A (SLC)	1h
PRE_EOL_INFO	[267]	Pre EOL information	1h
OPTIMAL_READ_SIZE	[266]	Optimal read size	8h
OPTIMAL_WRITE_SIZE	[265]	Optimal write size	8h
OPTIMAL_TRIM_UNIT_SIZE	[264]	Optimal trim unit size	8h
DEVICE_VERSION	[263:262]	Device version	0h
FIRMWARE_VERSION	[261:254]	Firmware version	FW Version
PWR_CL_DDR_200_360	[253]	Power class for 200MHz, DDR at VCC= 3.6V	DDh
CACHE_SIZE	[252:249]	Cache size	1000h
GENERIC_CMD6_TIME	[248]	Generic CMD6 timeout	19h
POWER_OFF_LONG_TIME	[247]	Power off notification(long) timeout	Ah
BKOPS_STATUS	[246]	Background operations status	Default = 0h
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of correctly programmed sectors	Default = 0h
INI_TIMEOUT_AP	[241]	1st Initialization time after partitioning	50h
PWR_CL_DDR_52_360	[239]	Power class for 52MHz, DDR at VCC = 3.6V	00h
PWR_CL_DDR_52_195	[238]	Power class for 52MHz, DDR at VCC = 1.95V	DDh
PWR_CL_200_195	[237]	Power class for 200MHz at VCCQ =1.95V, VCC = 3.6V	DDh
PWR_CL_200_130	[236]	Power class for 200MHz, at VCCQ =1.3V, VCC = 3.6V	0h
MIN_PERF_DDR_W_8_52	[235]	Minimum Write Performance for 8bit at 52MHz in DDR mode	0h
MIN_PERF_DDR_R_8_52	[234]	Minimum Read Performance for 8bit at	0h

Parameter	ECSD slice [bytes]	Description	Value
		52MHz in DDR mode	
TRIM _MULT	[232]	TRIM Multiplier	3h
SEC_FEATURE_SUPPORT	[231]	Secure Feature support	55h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	A6h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	A6h
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULT	[226]	Boot partition size	20h
ACCESS_SIZE	[225]	Access size	8h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase unit size	1h (see WP group size table below)
ERASE_TIMEOUT_MULT	[223]	High capacity erase time out	3h
REL_WR_SEC_C	[222]	Reliable write sector count	10h
HC_WP_GRP_SIZE	[221]	High capacity write protect group size	10h (see WP group size table below)
S_C_VCC	[220]	Sleep current [VCC]	8h
S_C_VCCQ	[219]	Sleep current [VCCQ]	7h
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218]	Production state awareness timeout	Ch
S_A_TIMEOUT	[217]	Sleep/Awake time out	12h
SLEEP_NOTIFICATION_TIME	[216]	Sleep notification time out	Dh
SEC_COUNT	[215:212]	Sector count	See exported capacity table below
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	Ah
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	Ah
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	Ah
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	Ah
PWR_CL_26_360	[203]	Power Class for 26MHz @ 3.6V	0x0
PWR_CL_52_360	[202]	Power Class for 52MHz @ 3.6V	0x0
PWR_CL_26_195	[201]	Power Class for 26MHz @ 1.95V	DDh
PWR_CL_52_195	[200]	Power Class for 52MHz @ 1.95V	DDh
PARTITION_SWITCH_TIME	[199]	Partition switching timing	3h

Parameter	ECSD slice [bytes]	Description	Value
OUT_OF_INTERRUPT_TIME	[198]	Out-of-interrupt busy timing	5h
DRIVER_STRENGTH	[197]	I/O Driver Strength	1h
DEVICE_TYPE	[196]	Device Type	57h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	7h
CMD_SET	[191]	Command Set	Default = 0h Updated in runtime
CMD_SET_REV	[189]	Command Set Revision	0h
POWER_CLASS	[187]	Power Class	Dh
HS_TIMING	[185]	High Speed Interface Timing	Default = 0h Updated in runtime by the host
DATA_STRB_MODE_SUPPORT	[184]	Data strobe mode support	1h
BUS_WIDTH	[183]	Bus Width Mode	Default = 0h Updated in runtime by the host
ERASE_MEM_CONT	[181]	Content of explicit erased memory range	0h
PARTITION_CONFIG	[179]	Partition Configuration	Default = 0h Updated in runtime by the host
BOOT_CONFIG_PROT	[178]	Boot config protection	Default = 0h Updated in runtime by the host
BOOT_BUS_CONDITIONS	[177]	Boot bus width1	Default = 0h Updated in runtime by the host
ERASE_GROUP_DEF	[175]	High-density erase group definition	Default = 0h Updated in runtime by the host
BOOT_WP_STATUS	[174]	Boot write protection status registers	Default = 0h Updated in runtime
BOOT_WP	[173]	Boot area write protect register	0h
USER_WP	[171]	User area write protect register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	20h
WR_REL_SET	[167]	Write reliability setting register	1Fh
WR_REL_PARAM	[166]	Write reliability parameter register	5h
SANITIZE_START	[165]	Start Sanitize operation	Default = 0h

Parameter	ECSD slice [bytes]	Description	Value
			Updated in runtime by the host
BKOPS_START	[164]	Manually start background operations	Default = 0h Updated in runtime by the host
BKOPS_EN	[163]	Enable background operations handshake	0h
RST_n_FUNCTION	[162]	H/W reset function	Default = 0h Updated by the host
HPI_MGMT	[161]	HPI management	Default = 0h Updated by the host
PARTITIONING SUPPORT	[160]	Partitioning support	7h Note: EUDA is not supported
MAX_ENH_SIZE_MULT	[159:157]	Max Enhanced Area Size	16GB = 0x37C 32GB = 0x6E8 64GB = 0xDD2
PARTITIONS_ATTRIBUTE	[156]	Partitions Attribute	Default = 0h Updated by the host
PARTITION_SETTING_ COMPLETED	[155]	Partitioning Setting	Default = 0h Updated by the host
GP_SIZE_MULT	[154:143]	General Purpose Partition Size (GP4)	0h
GP_SIZE_MULT	[151:149]	General Purpose Partition Size (GP3)	0h
GP_SIZE_MULT	[148:146]	General Purpose Partition Size (GP2)	0h
GP_SIZE_MULT	[145:143]	General Purpose Partition Size (GP1)	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management mode	0h
PRODUCTION_STATE_AWARENESS	[133]	Production state awareness	0h
TCASE_SUPPORT	[132]	Package Case Temperature is controlled	0h
PERIODIC_WAKEUP	[131]	Periodic Wake-up	0h
PROGRAM_CID_CSD_DDR_SUPPORT	[130]	Program CID/CSD in DDR mode support	1h
VENDOR_SPECIFIC_FIELD	[127:64]	Vendor Specific Fields	Reserved
NATIVE_SECTOR_SIZE	[63]	Native sector size	0h
USE_NATIVE_SECTOR	[62]	Sector size emulation	0h
DATA_SECTOR_SIZE	[61]	Sector size	0h
INI_TIMEOUT_EMU	[60]	1st initialization after disabling sector size emulation	Ah
CLASS_6_CTRL	[59]	Class 6 commands control	0h

Parameter	ECSD slice [bytes]	Description	Value
DYNCAP_NEEDED	[58]	Number of addressed group to be Released	0h
EXCEPTION_EVENTS_CTRL	[57:56]	Exception events control	0h
EXCEPTION_EVENTS_STATUS	[55:54]	Exception events status	0h
EXT_PARTITIONS_ATTRIBUTE	[53:52]	Extended Partitions Attribute	0h
CONTEXT_CONF	[51:37]	Context configuration	Default = 0h
PACKED_COMMAND_STATUS	[36]	Packed command status	Default = 0h Updated in runtime
PACKED_FAILURE_INDEX	[35]	Packed command failure index	Default = 0h Updated in runtime
POWER_OFF_NOTIFICATION	[34]	Power Off Notification	Default = 0h Updated in runtime by the host
CACHE_CTRL	[33]	Control to turn the Cache ON/OFF	0h
FLUSH_CACHE	[32]	Flushing of the cache	0h
MODE_CONFIG	[30]	Mode config	0h
MODE_OPERATION_CODES	[29]	Mode operation codes	0h
FFU_STATUS	[26]	FFU status	0h
PRE_LOADING_DATA_SIZE	[25:22]	Pre loading data size	0h
MAX_PRE_LOADING_DATA_SIZE	[21:18]	Max pre loading data size	See Max Preloading size table below
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17]	Product state awareness enablement	2h
SECURE_REMOVAL_TYPE	[16]	Secure Removal Type	9h

6.3.6. User Density

The following table shows the capacity available for user data for the different device sizes:

Table 15: Capacity for user data

Capacity	LBA [Hex]	LBA [Dec]	Capacity [Bytes]
SDIN9DW4-16G	0x1D5A000	30,777,344	15,758,000,128
SDIN9DW4-32G	0x3A3E000	61,071,360	31,268,536,320
SDIN9DW4-64G	0x747C000	122,142,720	62,537,072,640

Table 8: Write protect group size

SKU	HC_ERASE_GROUP _SIZE	HC_WP_GRP_SIZE	Erase Unit Size [MB]	Write Protect Group Size [MB]
SDIN9DW4-16G	1h	10h	0.5MB	8MB
SDIN9DW4-32G	1h	10h	0.5MB	8MB
SDIN9DW4-64G	1h	10h	0.5MB	8MB

Table 17: Max Preloading Data Size

SKU	Type A: MAX_PRE_LOADING_DATA_SIZE LBA[Hex]	Type B: MAX_PRE_LOADING_DATA_SIZE LBA[Hex]
SDIN9DW4-16G	0x75C7F5	0xD3B4B9
SDIN9DW4-32G	0xE957F1	0x1A3B7E5
SDIN9DW4-64G	0x1D24FFB	0x3470FF7

Note:

Type A: FW that supports preloaded size up to 25% of the exported capacity

Type B: FW that supports preloaded size up to 45% of the exported capacity

7. POWER DELIVERY AND CAPACITOR SPECIFICATIONS

7.1. SanDisk iNAND *Extreme* Power Domains

SanDisk iNAND *Extreme* has three power domains assigned to VCCQ, VCC and VDDi, as shown in Table 18 below.

Table 18 - Power Domains

Pin	Power Domain	Comments
VCCQ	Host Interface	Supported voltage ranges:
		Low Voltage Region: 1.8V (nominal)
VCC	Memory	Supported voltage range:
		High Voltage Region: 3.3V (nominal)
VDDi	Internal	VDDi is the internal regulator connection to an external decoupling capacitor.

7.2. Capacitor Connection Guidelines

It is recommended to place the following capacitors on VCC & VCCQ domains:

- Cin1 = 4.7uF
- Cin2 = 0.1uF

For VDDi (1.1V), it is recommended to place:

- 0.1uF <= Cin(VDDi) <= 2.2uF
- For HS200 can use 0.1 uF <= Cin(VDDi) <= 2.2uF

Capacitors Type:

- SMT-Ceramic
- X5R/X7R
- 6.3V/10V
- Min height – 0.55mm
- Foot Print: 0402 or above

When using a low value ceramic input filter capacitor, it should be located as close to the supply ball as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply

Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

Make all of the power (high current) traces as short, direct, and thick as possible. The capacitors should be as close to each other as possible, as it reduces EMI radiated by the power traces due to the high switching currents through them. In addition it shall also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringings, and resistive losses which produce voltage errors.

The grounds of the IC capacitors should be connected close together directly to a ground plane. It is also recommended to have a ground plane on both sides of the PCB, as it reduces noise by reducing ground loop errors as well.

The loop inductance per capacitor shall not exceed 3nH (both on VCC/VCCQ & VSS/VSSQ loops).

Cin2 shall be placed closer (from both distance & inductance POV) to the iNAND power & ground balls.

Multiple via connections are recommended per each capacitor pad.

On test platforms, where the iNAND socket is in use, the loop inductance per capacitor shall not exceed 5nH (both on VCC/VCCQ & VSS/VSSQ loop).

No passives should be placed below the iNAND device (between iNAND & PCB).

VSF balls (VSF1/4) should have exposed and floated test pads on the PCB, with near exposed GND for better measurement.

Signal Traces:

- Data, CMD, CLK & RCLK bus trace length mismatch should be minimal (up to +/-1mm).
- Traces should be 50ohm controlled impedance.

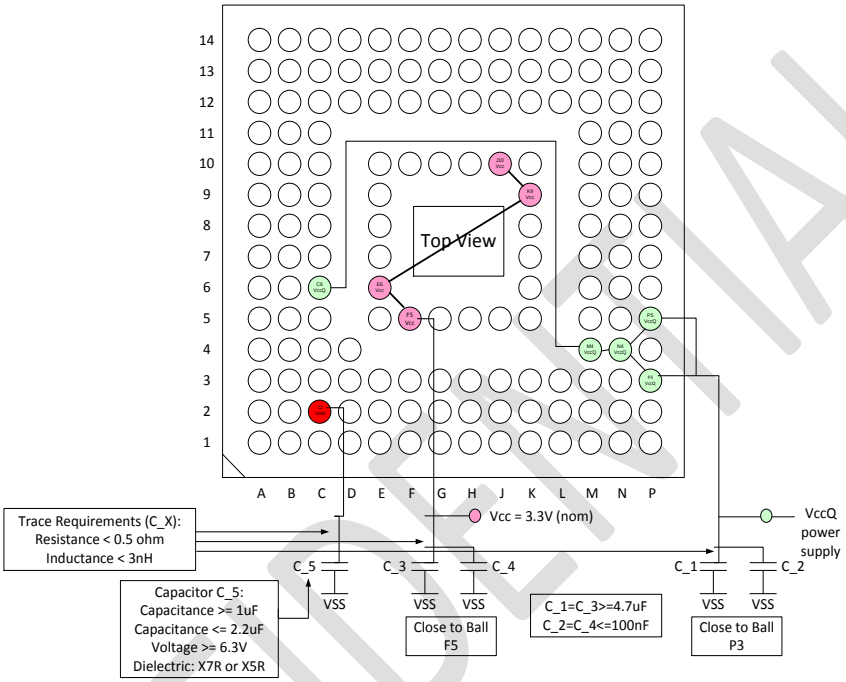

Figure 6 - Recommended Power Domain Connections

Note: Signal routing in the diagram is for illustration purposes only and the final routing depends final PCB layout.

For clarity, the diagram does not include VSS connection. All balls marked VSS shall be connected to a ground (GND) plane.

7.3. Host-Device Synchronization Flow (Enhanced STROBE)

According to e.MMC5.0, DATA supports the HS400 interface, while CMD and Response are compliant with single data rate (SDR) HS200. That means that DATA Out signals are synced with STROBE while CMD/Response is synced with CLK.

Limitations of eMMC 5.0 specification:

- Host and device need to use a mechanism for Tuning Command even when HS400 is used (for the CMD line).
- Needs to precede HS400 with HS200 to allow Tuning (since tuning must be done based on CLK, not STROBE).
- Tuning process may take tens of milliseconds.
- In addition transition from HS200 to HS400 is not possible, this adds time and complication.
- In case CMD Line sync loss occurs there is no mechanism to regain sync. It means:
    - Tuning Command cannot be used -> Response cannot be validated.
    - Switch CMD cannot be used -> Response cannot be validated.
    - Only reset can be done -> Reset is a huge overhead.

The above limitations impose an overhead on the device and host while ignoring the advantage of using the STROBE mechanism.

The Enhanced STROBE feature as implemented for iNAND *Extreme* allows utilizing STROBE to synchronize also the CMD response:

- CMD clocking stays SDR (similar to legacy DDR52).
- Host commands are clocked out with the rising edge of the host clock (as done in legacy eMMC devices).
- iNAND *Extreme* will provide STROBE signaling synced with the CMD response in addition to DATA Out.
- Host may use the STROBE signaling for DAT and CMD-Response capturing eliminating the need for a tuning mechanism.

This feature requires support by the host to enable faster and more reliable operation.

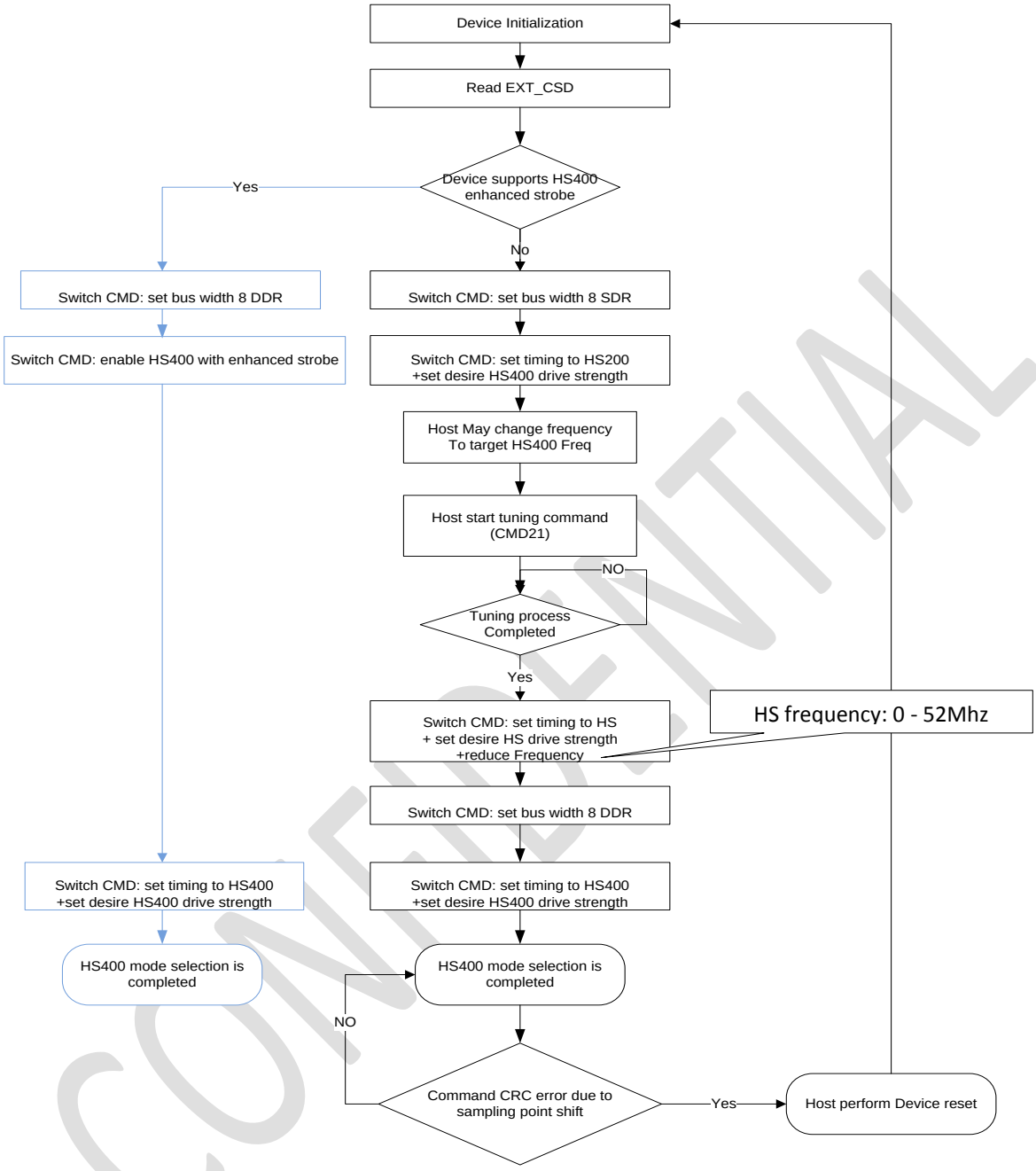

Figure 7 – Enhanced Strobe mode operation

8. MARKING

First row: Simplified SanDisk Logo

Second row: Sales item P/N

Third row: Country of origin i.e. 'TAIWAN' or 'CHINA'

* No ES marking for product in mass production.

Fourth row: Y- Last digit of year

WW- Work week

D- A day within the week.

MTLLLXXX – Internal use

2D barcode: Store the 12 Digital unique ID information as reflected in the fourth row.

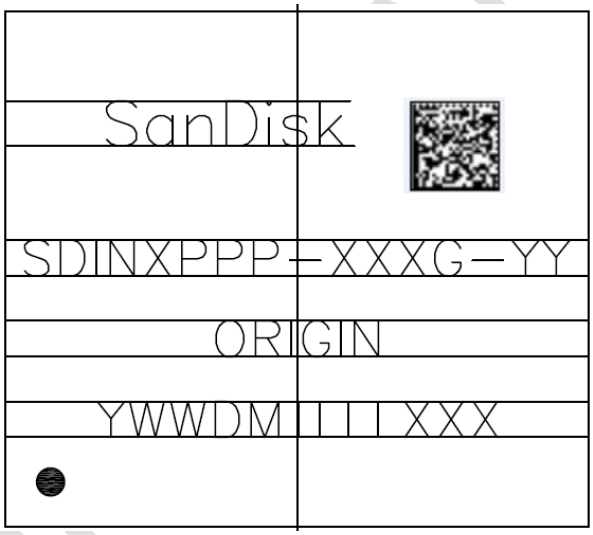

Figure 8 - Product marking

9. ORDERING INFORMATION

Table 19 – Ordering Information

Capacity	Technology	Part Number	Samples Part Number	Package
16GB	X2	SDIN9DW4-16G	SDIN9DW4-16G -Q	11.5mm x 13mm x 1.0mm
32GB	X2	SDIN9DW4-32G	SDIN9DW4-32G-Q	11.5mm x 13mm x 1.0mm
64GB	X2	SDIN9DW4-64G	SDIN9DW4-64G-Q	11.5mm x 13mm x 1.0mm

Note: Optional Customer Code, when applicable, will be added at the end of the part number (e.g. SDIN9DW4-16G-XXX or SDIN9DW4-16G-XXXQ).

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