

# 74LVC377

Octal D-type flip-flop with data enable; positive-edge trigger

Rev. 6 — 20 November 2012

Product data sheet

## 1. General description

The 74LVC377 has eight edge-triggered D-type flip-flops with individual inputs (D) and outputs (Q). A common clock input (CP) loads all flip-flops simultaneously when data enable input ( $\bar{E}$ ) is LOW. The state of each D input, one set-up time before the LOW to HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. Input  $\bar{E}$  must be stable only one set-up time prior to the LOW to HIGH transition for predictable operation.

## 2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50  $\Omega$  transmission lines at 125 °C
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC377D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC377DB	–40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVC377PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1



### 4. Functional diagram

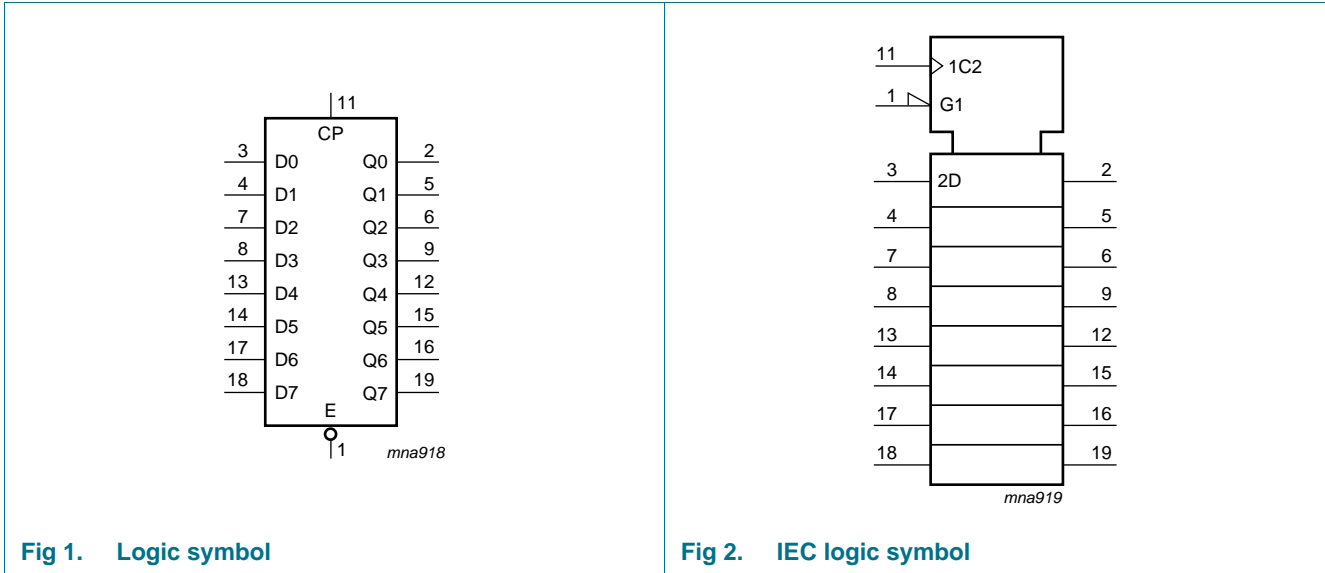


Fig 1. Logic symbol

Fig 2. IEC logic symbol

### 5. Pinning information

#### 5.1 Pinning

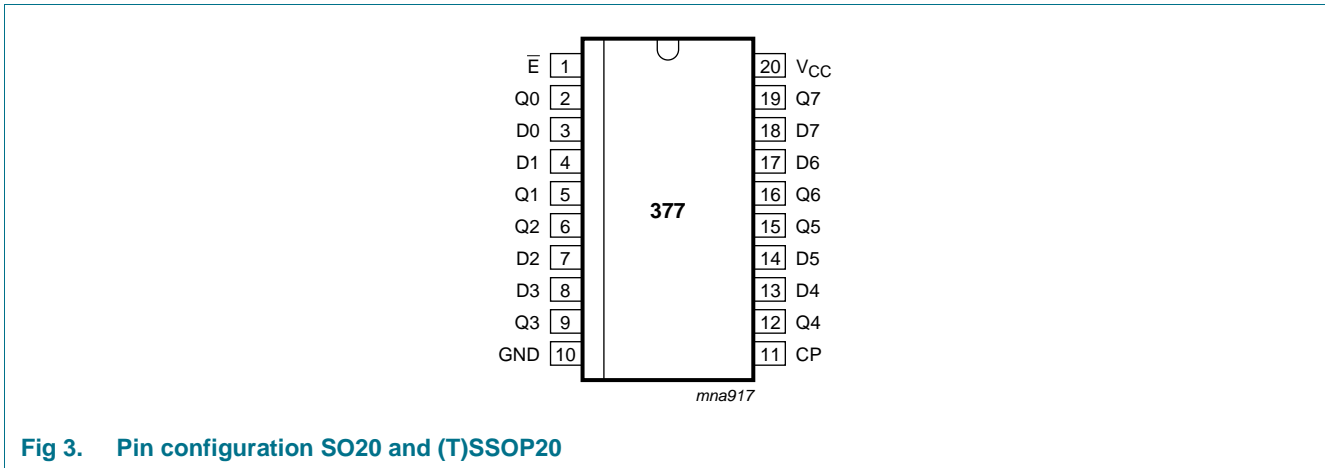


Fig 3. Pin configuration SO20 and (T)SSOP20

#### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\bar{E}$	1	data enable input (active LOW)
CP	11	clock input (LOW to HIGH; edge-triggered)
D[0:7]	3, 4, 7, 8, 13, 14, 17, 18	data input

Table 2. Pin description *?continued*

Symbol	Pin	Description
Q[0:7]	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
GND	10	ground (0 V)
V <sub>CC</sub>	20	power supply

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Control		Input	Output
	CP	$\overline{E}$	Dn	Qn
Load 1	↑	l	h	H
Load 0	↑	l	l	L
Hold	↑	h	X	NC
Do nothing	X	H	X	NC

- [1] H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW to HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW to HIGH CP transition  
↑ = LOW to HIGH CP transition  
NC = no change  
X = don't care

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
V <sub>I</sub>	input voltage		<sup>[1]</sup> -0.5	+5.5	V
V <sub>O</sub>	output voltage		<sup>[2]</sup> -0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	<sup>[3]</sup> -	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.  
[2] The output voltage ratings may be exceeded if the output current ratings are observed.  
[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
For (T)SSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	0.65 × V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	-	±20	μA

**Table 6. Static characteristics** *?ontinued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	CP to Qn; see <a href="#">Figure 4</a>	-	15	-	-	-	ns
		V <sub>CC</sub> = 1.2 V	-	15	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.5	7.4	14.5	2.5	15.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.8	4.4	8.5	1.8	9.1	ns
		V <sub>CC</sub> = 2.7 V	1.5	4.3	7.9	1.5	10.0	ns
t <sub>w</sub>	pulse width	clock HIGH or LOW; see <a href="#">Figure 4</a>	1.5	4.0	7.6	1.5	9.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	4.0	7.6	1.5	9.5	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	6.0	-	-	6.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	5.0	-	-	5.0	-	ns
		V <sub>CC</sub> = 2.7 V	5.0	1.6	-	5.0	-	ns
t <sub>su</sub>	set-up time	$\bar{E}$ to CP; see <a href="#">Figure 5</a>	3.0	0.2	-	3.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.0	0.2	-	3.0	-	ns
		V <sub>CC</sub> = 2.7 V	4.0	0.6	-	4.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	4.5	-	-	4.5	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	5.5	-	-	5.5	-	ns
		Dn to CP; see <a href="#">Figure 5</a>	2.0	0.7	-	2.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	0.7	-	2.0	-	ns
		V <sub>CC</sub> = 2.7 V	3.0	1.0	-	3.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	4.5	-	-	4.5	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	5.5	-	-	5.5	-	ns

**Table 7. Dynamic characteristics** *continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>h</sub>	hold time	$\bar{E}$ to CP; see <a href="#">Figure 5</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	-	-	1.5	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	-	-	0.5	-	ns
		V <sub>CC</sub> = 2.7 V	0.0	-1.0	-	0.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	0	-	1.0	-	ns
		Dn to CP; see <a href="#">Figure 5</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	-	-	1.5	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	-	-	0.5	-	ns
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 4</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	80	-	-	64	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	100	-	-	80	-	MHz
		V <sub>CC</sub> = 2.7 V	150	-	-	120	-	MHz
t <sub>sk(o)</sub>	output skew time	V <sub>CC</sub> = 3.0 V to 3.6 V <a href="#">[3]</a>	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation capacitance	per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub> <a href="#">[4]</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	12.1	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	15.8	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	19.0	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

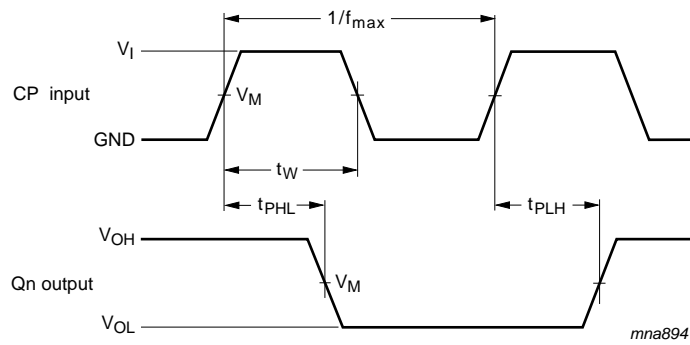
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

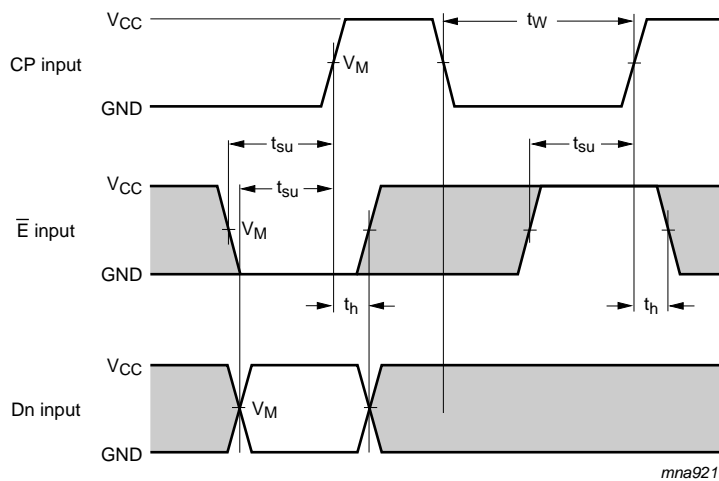
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

11. Waveforms



Measurement points are given in [Table 8](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 4. Propagation delay clock (CP) to output (Qn), pulse width clock (CP), and maximum frequency**

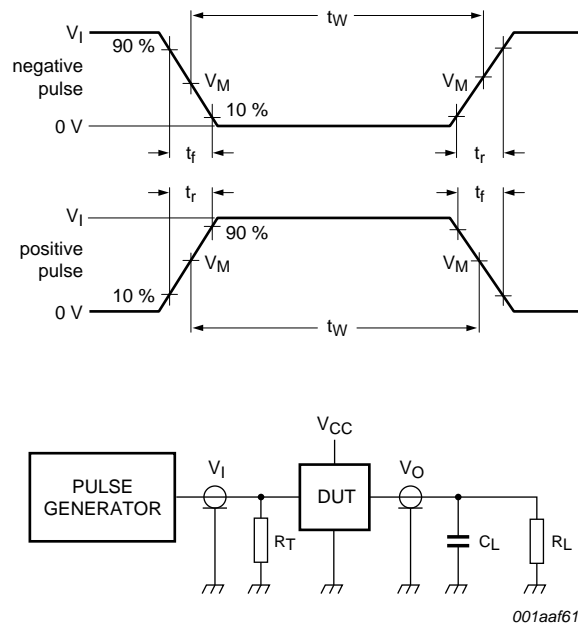


Measurement points are given in [Table 8](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 5. Data set-up and hold times of data input (Dn) and enable input ( $\bar{E}$ ) and pulse width of enable input ( $\bar{E}$ )**

**Table 8. Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
1.65 V to 1.95V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

**Fig 6. Test circuit for switching times**

**Table 9. Test data**

Supply voltage	Input		Load	
	$V_I$	$t_r, t_f$	$C_L$	$R_L$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$



12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

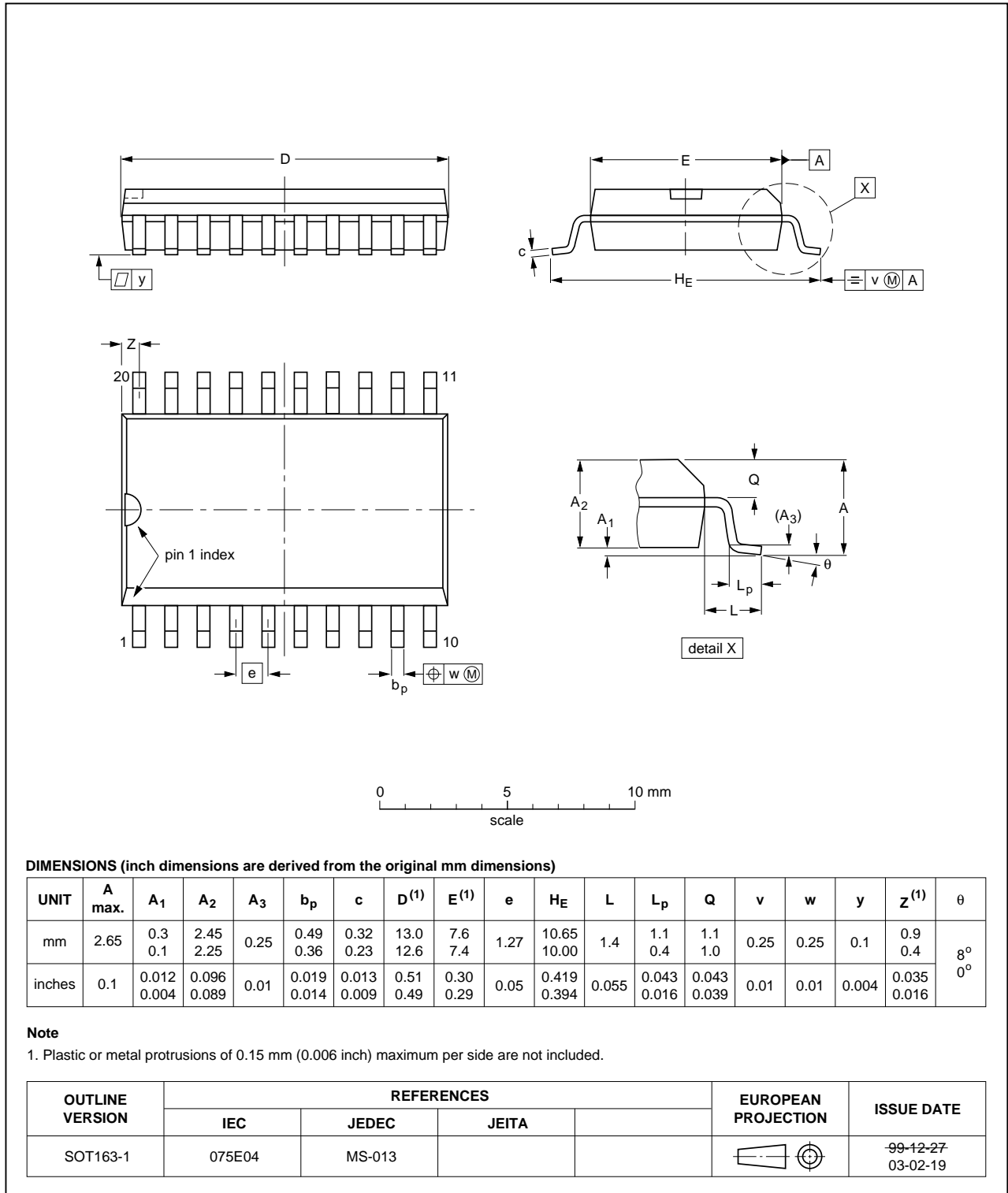


Fig 7. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

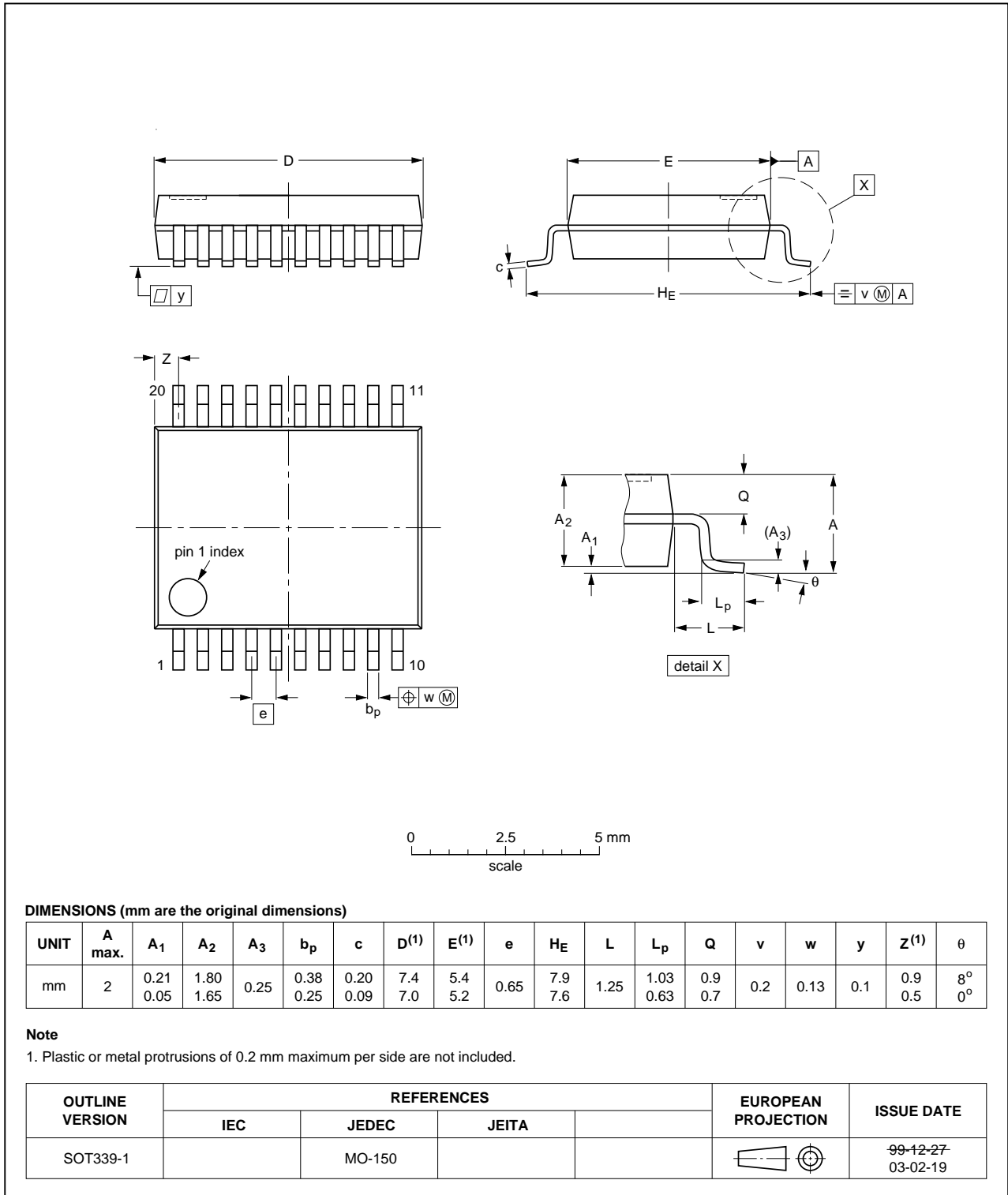


Fig 8. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 9. Package outline SOT360-1 (TSSOP20)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC377 v.6	20121120	Product data sheet	-	74LVC377 v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, <a href="#">Table 8</a>, and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC377 v.5	20050221	Product specification	-	74LVC377 v.4
74LVC377 v.4	20040528	Product specification	-	74LVC377 v.3
74LVC377 v.3	20021023	Product specification	-	74LVC377 v.2
74LVC377 v.2	19980729	Product specification	-	74LVC377 v.1
74LVC377 v.1	19990606	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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