# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# 74HC/HCT4046A
## Phase-locked-loop with VCO

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC06

1997 Nov 25

Philips
Semiconductors

PHILIPS

## FEATURES

- Low power consumption
- Centre frequency of up to 17 MHz (typ.) at $V_{CC}$ = 4.5 V
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- $I_{CC}$ category: MSI.

## GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the “4046” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the “4046A” forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between $R_1$ and GND) or two external resistors R1 and R2 (between $R_1$ and GND, and $R_2$ and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 ($DEM_{OUT}$). In contrast to conventional techniques where the $DEM_{OUT}$ voltage is one threshold voltage lower than the VCO input voltage, here the $DEM_{OUT}$ voltage equals that of the VCO input. If $DEM_{OUT}$ is used, a load resistor ($R_S$) should be connected from $DEM_{OUT}$ to GND; if unused, $DEM_{OUT}$ should be left open. The VCO output ($VCO_{OUT}$) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The sections of the comparator are identical, so that there is no difference in the $SIG_{IN}$ (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and HCT versions.

### Phase comparators

The signal input ($SIG_{IN}$) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

*Phase comparator 1 (PC1)*

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies ($f_i$) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is: $V_{DEMOUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

where $V_{DEMOUT}$ is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

The phase comparator gain is: $K_p = \frac{V_{CC}}{\pi}(V/r)$.

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 ($V_{DEMOUT}$), is the resultant of the phase differences of signals ($SIG_{IN}$) and the comparator input ($COMP_{IN}$) as shown in Fig.6. The average of $V_{DEMOUT}$ is equal to $\frac{1}{2}V_{CC}$ when there is no signal or noise at $SIG_{IN}$ and with this input the VCO oscillates at the centre frequency ($f_o$). Typical waveforms for the PC1 loop locked at $f_o$ are shown in Fig.7.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range.
This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

*Phase comparator 2 (PC2)*

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of $SIG_{IN}$ and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig.5) where $SIG_{IN}$ causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed,

is: $V_{DEMOUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

where $V_{DEMOUT}$ is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The phase comparator gain is: $K_p = \frac{V_{CC}}{4\pi}(V/r)$.

$V_{DEMOUT}$ is the resultant of the initial phase differences of $SIG_{IN}$ and $COMP_{IN}$ as shown in Fig.8. Typical waveforms for the PC2 loop locked at $f_o$ are shown in Fig.9.

When the frequencies of $SIG_{IN}$ and $COMP_{IN}$ are equal but the phase of $SIG_{IN}$ leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held “ON” for a time corresponding to the phase difference ($\phi_{DEMOUT}$). When the phase of $SIG_{IN}$ lags that of $COMP_{IN}$, the n-type driver is held “ON”.

When the frequency of $SIG_{IN}$ is higher than that of $COMP_{IN}$, the p-type output driver is held “ON” for most of the input signal cycle time, and for the remainder of the cycle both n and p- type drivers are ”OFF” (3-state). If the $SIG_{IN}$ frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held “ON” for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output ($PCP_{OUT}$) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between $SIG_{IN}$ and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are “OFF” for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at $SIG_{IN}$ the VCO adjusts, via PC2, to its lowest frequency.

*Phase comparator 3 (PC3)*

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of $SIG_{IN}$ and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed,

is: $V_{DEMOUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

where $V_{DEMOUT}$ is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC3OUT}$ (via low-pass filter).

The phase comparator gain is: $K_p = \frac{V_{CC}}{2\pi}(V/r)$.

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 ($V_{DEMOUT}$), is the resultant of the phase differences of $SIG_{IN}$ and $COMP_{IN}$ as shown in Fig.10. Typical waveforms for the PC3 loop locked at $f_o$ are shown in Fig.11.

The phase-to-output response characteristic of PC3 (Fig.10) differs from that of PC2 in that the phase angle between $SIG_{IN}$ and $COMP_{IN}$ varies between 0° and 360° and is 180° at the centre frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at $SIG_{IN}$ the VCO adjusts, via PC3, to its lowest frequency.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $f_o$ | VCO centre frequency | C1 = 40 pF; R1 = 3 kΩ; $V_{CC}$ = 5 V | 19 | 19 | MHz |
| $C_I$ | input capacitance (pin 5) | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per package | notes 1 and 2 | 24 | 24 | pF |

**Notes**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz.

   $f_o$ = output frequency in MHz.

   $C_L$ = output load capacitance in pF.

   $V_{CC}$ = supply voltage in V.

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

## ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

## APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control.

## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

**PIN DESCRIPTION**

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | $PCP_{OUT}$ | phase comparator pulse output |
| 2 | $PC1_{OUT}$ | phase comparator 1 output |
| 3 | $COMP_{IN}$ | comparator input |
| 4 | $VCO_{OUT}$ | VCO output |
| 5 | INH | inhibit input |
| 6 | $C1_A$ | capacitor C1 connection A |
| 7 | $C1_B$ | capacitor C1 connection B |
| 8 | GND | ground (0 V) |
| 9 | $VCO_{IN}$ | VCO input |
| 10 | $DEM_{OUT}$ | demodulator output |
| 11 | $R_1$ | resistor R1 connection |
| 12 | $R_2$ | resistor R2 connection |
| 13 | $PC2_{OUT}$ | phase comparator 2 output |
| 14 | $SIG_{IN}$ | signal input |
| 15 | $PC3_{OUT}$ | phase comparator 3 output |
| 16 | $V_{CC}$ | positive supply voltage |

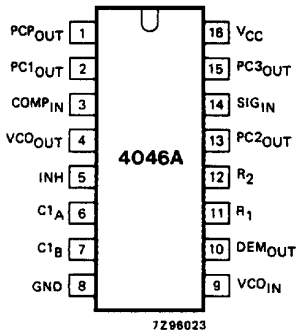



Fig.1 Pin configuration.

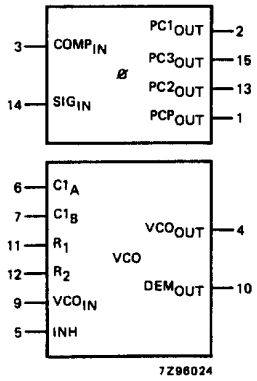



Fig.2 Logic symbol.

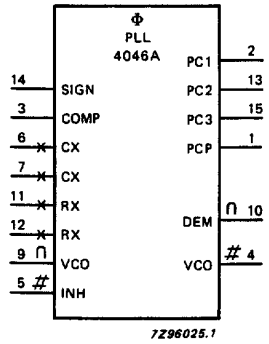



Fig.3 IEC logic symbol.

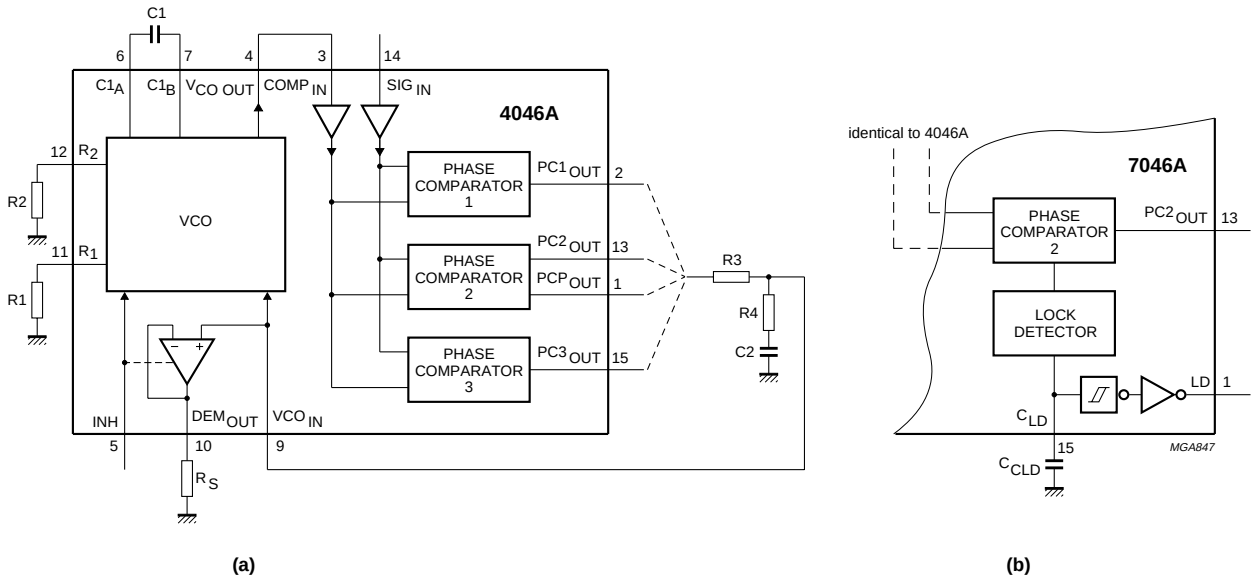



Fig.4 Functional diagram.

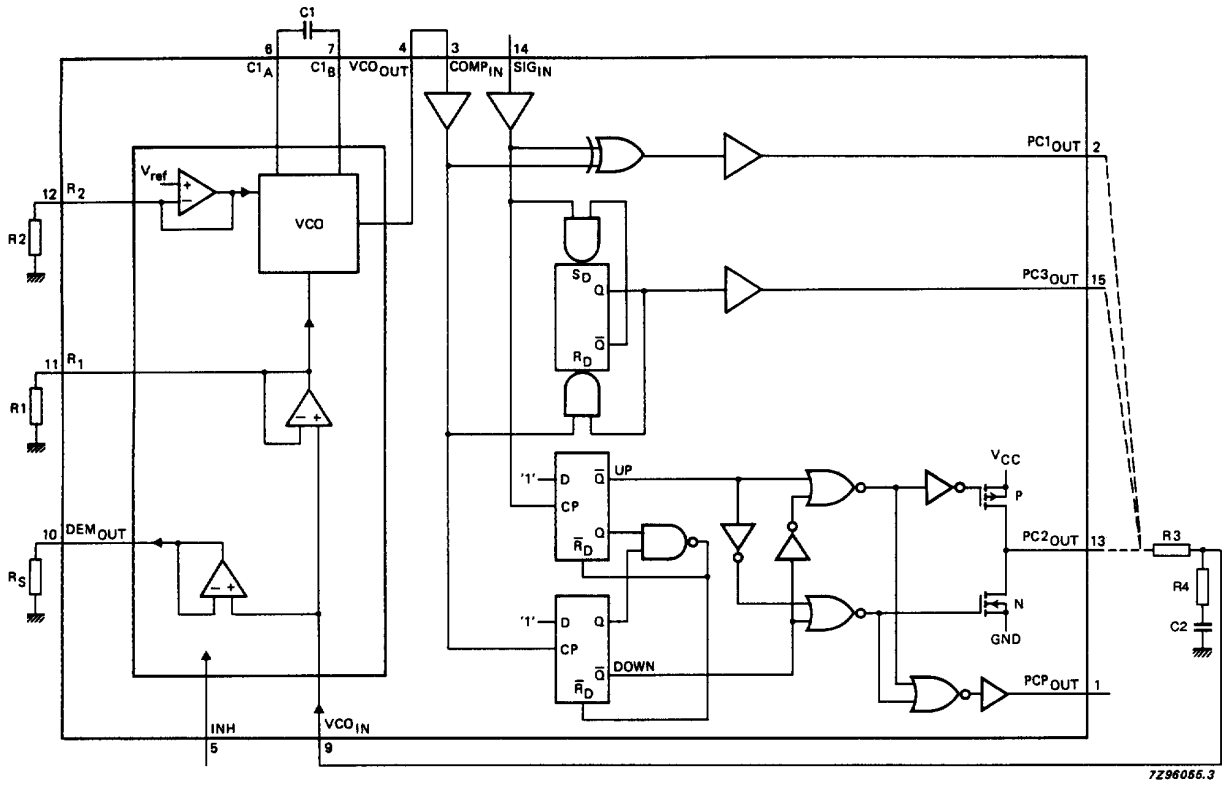
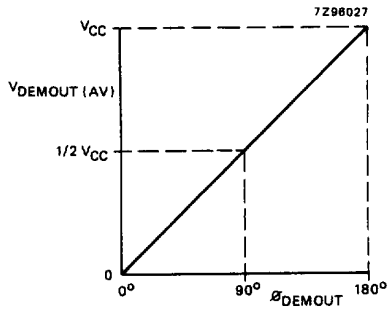



Fig.5 Logic diagram.




$V_{DEMOUT} = V_{PC2OUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

Fig.6 Phase comparator 1: average output voltage versus input phase difference.

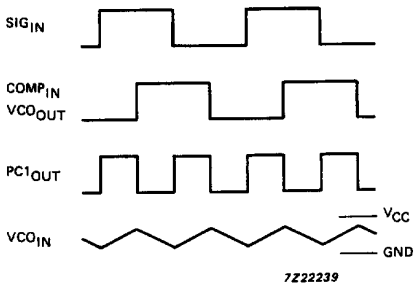
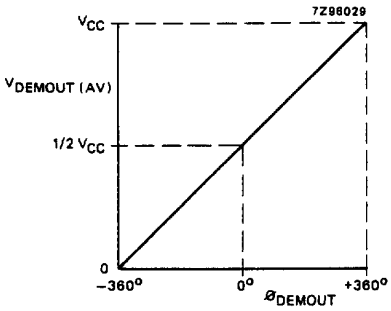



Fig.7 Typical waveforms for PLL using phase comparator 1, loop locked at $f_o$.




$V_{DEMOUT} = V_{PC2OUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi C_{OMPIN})$.

Fig.8 Phase comparator 2: average output voltage versus input phase difference.

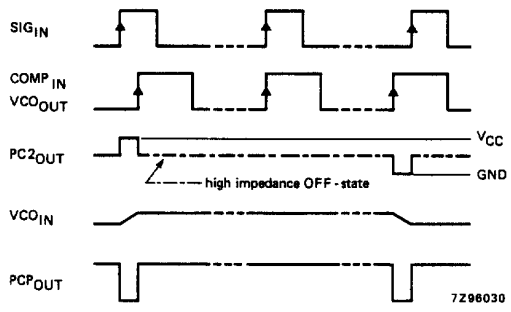
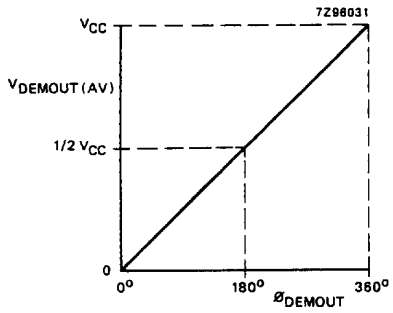



Fig.9 Typical waveforms for PLL using phase comparator 2, loop locked at $f_o$.




$V_{DEMOUT} = V_{PC3OUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

Fig.10 Phase comparator 3: average output voltage versus input phase difference:

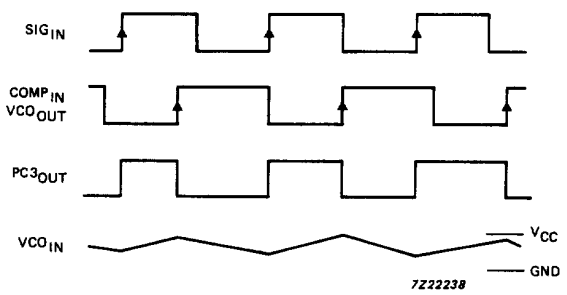



Fig.11 Typical waveforms for PLL using phase comparator 3, loop locked at $f_o$.

**RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT**

| SYMBOL | PARAMETER | 74HC | | | 74HCT | | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | min. | typ. | max. | | |
| $V_{CC}$ | DC supply voltage | 3.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V | |
| $V_{CC}$ | DC supply voltage if VCO section is not used | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V | |
| $V_I$ | DC input voltage range | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V | |
| $V_O$ | DC output voltage range | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V | |
| $T_{amb}$ | operating ambient temperature range | –40 | | +85 | –40 | | +85 | °C | see DC and AC CHARACTERISTICS |
| $T_{amb}$ | operating ambient temperature range | –40 | | +125 | –40 | | +125 | °C | |
| $t_r$, $t_f$ | input rise and fall times (pin 5) | | 6.0 | 1000 | | 6.0 | 500 | ns | $V_{CC}$ = 2.0 V |
| | | | 6.0 | 500 | | 6.0 | 500 | ns | $V_{CC}$ = 4.5 V |
| | | | 6.0 | 400 | | 6.0 | 500 | ns | $V_{CC}$ = 6.0 V |

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | –0.5 | +7 | V | |
| $\pm I_{IK}$ | DC input diode current | | 20 | mA | for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V |
| $\pm I_{OK}$ | DC output diode current | | 20 | mA | for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V |
| $\pm I_O$ | DC output source or sink current | | 25 | mA | for $-0.5$ V $< V_O < V_{CC} + 0.5$ V |
| $\pm I_{CC}$; $\pm I_{GND}$ | DC $V_{CC}$ or GND current | | 50 | mA | |
| $T_{stg}$ | storage temperature range | –65 | +150 | °C | |
| $P_{tot}$ | power dissipation per package | | | | for temperature range: – 40 to +125 °C 74HC/HCT |
| | plastic DIL | | 750 | mW | above + 70 °C: derate linearly with 12 mW/K |
| | plastic mini-pack (SO) | | 500 | mW | above + 70 °C: derate linearly with 8 mW/K |

## DC CHARACTERISTICS FOR 74HC

### Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $I_{CC}$ | quiescent supply current (VCO disabled) | | | 8.0 | | 80.0 | | 160.0 | μA | 6.0 | pins 3, 5, and 14 at $V_{CC}$; pin 9 at GND; $I_I$ at pins 3 and 14 to be excluded |

### Phase comparator section

Voltages are referenced to GND (ground = 0 V)

| SYM-BOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | $V_I$ | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| $V_{IH}$ | DC coupled HIGH level input voltage $SIG_{IN}$, $COMP_{IN}$ | 1.5<br>3.15<br>4.2 | 1.2<br>2.4<br>3.2 | | 1.5<br>3.15<br>4.2 | | 1.5<br>3.15<br>4.2 | | V | 2.0<br>4.5<br>6.0 | | |
| $V_{IL}$ | DC coupled LOW level input voltage $SIG_{IN}$, $COMP_{IN}$ | | 0.8<br>2.1<br>2.8 | 0.5<br>1.35<br>1.8 | | 0.5<br>1.35<br>1.8 | | 0.5<br>1.35<br>1.8 | V | 2.0<br>4.5<br>6.0 | | |
| $V_{OH}$ | HIGH level output voltage $PCP_{OUT}$, $PC_{nOUT}$ | 1.9<br>4.4<br>5.9 | 2.0<br>4.5<br>6.0 | | 1.9<br>4.4<br>5.9 | | 1.9<br>4.4<br>5.9 | | V | 2.0<br>4.5<br>6.0 | $V_{IH}$ or $V_{IL}$ | $-I_O$ = 20 μA<br>$-I_O$ = 20 μA<br>$-I_O$ = 20 μA |
| $V_{OH}$ | HIGH level output voltage $PCP_{OUT}$, $PC_{nOUT}$ | 3.98<br>5.48 | 4.32<br>5.81 | | 3.84<br>5.34 | | 3.7<br>5.2 | | V | 4.5<br>6.0 | $V_{IH}$ or $V_{IL}$ | $-I_O$ = 4.0 mA<br>$-I_O$ = 5.2 mA |
| $V_{OL}$ | LOW level output voltage $PCP_{OUT}$, $PC_{nOUT}$ | | 0<br>0<br>0 | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | V | 2.0<br>4.5<br>6.0 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 20 μA<br>$I_O$ = 20 μA<br>$I_O$ = 20 μA |
| $V_{OL}$ | LOW level output voltage $PCP_{OUT}$, $PC_{nOUT}$ | | 0.15<br>0.16 | 0.26<br>0.26 | | 0.33<br>0.33 | | 0.4<br>0.4 | V | 4.5<br>6.0 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 4.0 mA<br>$I_O$ = 5.2 mA |
| $\pm I_I$ | input leakage current $SIG_{IN}$, $COMP_{IN}$ | | | 3.0<br>7.0<br>18.0<br>30.0 | | 4.0<br>9.0<br>23.0<br>38.0 | | 5.0<br>11.0<br>27.0<br>45.0 | μA | 2.0<br>3.0<br>4.5<br>6.0 | $V_{CC}$ or GND | |
| $\pm I_{OZ}$ | 3-state OFF-state current $PC2_{OUT}$ | | | 0.5 | | 5.0 | | 10.0 | μA | 6.0 | $V_{IH}$ or $V_{IL}$ | $V_O = V_{CC}$ or GND |

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | $V_I$ | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| $R_I$ | input resistance $SIG_{IN}$, $COMP_{IN}$ | | 800<br>250<br>150 | | | | | | kΩ<br>kΩ<br>kΩ | 3.0<br>4.5<br>6.0 | $V_I$ at self-bias operating point; $\Delta V_I$ = 0.5 V; see Figs 12, 13 and 14 | |

**VCO section**

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | $V_I$ | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| $V_{IH}$ | HIGH level input voltage INH | 2.1<br>3.15<br>4.2 | 1.7<br>2.4<br>3.2 | | 2.1<br>3.15<br>4.2 | | 2.1<br>3.15<br>4.2 | | V | 3.0<br>4.5<br>6.0 | | |
| $V_{IL}$ | LOW level input voltage INH | | 1.3<br>2.1<br>2.8 | 0.9<br>1.35<br>1.8 | | 0.9<br>1.35<br>1.8 | | 0.9<br>1.35<br>1.8 | V | 3.0<br>4.5<br>6.0 | | |
| $V_{OH}$ | HIGH level output voltage $VCO_{OUT}$ | 2.9<br>4.4<br>5.9 | 3.0<br>4.5<br>6.0 | | 2.9<br>4.4<br>5.9 | | 2.9<br>4.4<br>5.9 | | V | 3.0<br>4.5<br>6.0 | $V_{IH}$ or $V_{IL}$ | $-I_O$ = 20 μA<br>$-I_O$ = 20 μA<br>$-I_O$ = 20 μA |
| $V_{OH}$ | HIGH level output voltage $VCO_{OUT}$ | 3.98<br>5.48 | 4.32<br>5.81 | | 3.84<br>5.34 | | 3.7<br>5.2 | | V | 4.5<br>6.0 | $V_{IH}$ or $V_{IL}$ | $-I_O$ = 4.0 mA<br>$-I_O$ = 5.2 mA |
| $V_{OL}$ | LOW level output voltage $VCO_{OUT}$ | | 0<br>0<br>0 | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | V | 3.0<br>4.5<br>6.0 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 20 μA<br>$I_O$ = 20 μA<br>$I_O$ = 20 μA |
| $V_{OL}$ | LOW level output voltage $VCO_{OUT}$ | | 0.15<br>0.16 | 0.26<br>0.26 | | 0.33<br>0.33 | | 0.4<br>0.4 | V | 4.5<br>6.0 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 4.0 mA<br>$I_O$ = 5.2 mA |
| $V_{OL}$ | LOW level output voltage $C1_A$, $C1_B$ | | | 0.40<br>0.40 | | 0.47<br>0.47 | | 0.54<br>0.54 | V | 4.5<br>6.0 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 4.0 mA<br>$I_O$ = 5.2 mA |
| $\pm I_I$ | input leakage current INH, $VCO_{IN}$ | | | 0.1 | | 1.0 | | 1.0 | μA | 6.0 | $V_{CC}$ or GND | |
| R1 | resistor range | 3.0<br>3.0<br>3.0 | | 300<br>300<br>300 | | | | | kΩ | 3.0<br>4.5<br>6.0 | | note 1 |

| SYM-BOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | $V_I$ | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| $R_2$ | resistor range | 3.0<br>3.0<br>3.0 | | 300<br>300<br>300 | | | | | kΩ | 3.0<br>4.5<br>6.0 | | note 1 |
| C1 | capacitor range | 40<br>40<br>40 | | no limit | | | | | pF | 3.0<br>4.5<br>6.0 | | |
| $V_{VCOIN}$ | operating voltage range at $VCO_{IN}$ | 1.1<br>1.1<br>1.1 | | 1.9<br>3.4<br>4.9 | | | | | V | 3.0<br>4.5<br>6.0 | | over the range specified for R1; for linearity see Figs 20 and 21 |

**Note**

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/ or R2 are/is > 10 kΩ.

**Demodulator section**

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ V | OTHER |
| | | +25 | | | −40 to+85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $R_S$ | resistor range | 50<br>50<br>50 | | 300<br>300<br>300 | | | | | kΩ | 3.0<br>4.5<br>6.0 | at $R_S$ > 300 kΩ the leakage current can influence $V_{DEMOUT}$ |
| $V_{OFF}$ | offset voltage $VCO_{IN}$ to $V_{DEMOUT}$ | | ±30<br>±20<br>±10 | | | | | | mV | 3.0<br>4.5<br>6.0 | $V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over $R_S$ range; see Fig.15 |
| $R_D$ | dynamic output resistance at $DEM_{OUT}$ | | 25<br>25<br>25 | | | | | | Ω | 3.0<br>4.5<br>6.0 | $V_{DEMOUT} = 1/2\ V_{CC}$ |

## AC CHARACTERISTICS FOR 74HC

### Phase comparator section

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay $SIG_{IN}$, $COMP_{IN}$ to $PC1_{OUT}$ | | 63 | 200 | | 250 | | 300 | ns | 2.0 | Fig.16 |
| | | | 23 | 40 | | 50 | | 60 | | 4.5 | |
| | | | 18 | 34 | | 43 | | 51 | | 6.0 | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay $SIG_{IN}$, $COMP_{IN}$ to $PCP_{OUT}$ | | 96 | 340 | | 425 | | 510 | ns | 2.0 | Fig.16 |
| | | | 35 | 68 | | 85 | | 102 | | 4.5 | |
| | | | 28 | 58 | | 72 | | 87 | | 6.0 | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay $SIG_{IN}$, $COMP_{IN}$ to $PC3_{OUT}$ | | 77 | 270 | | 340 | | 405 | ns | 2.0 | Fig.16 |
| | | | 28 | 54 | | 68 | | 81 | | 4.5 | |
| | | | 22 | 46 | | 58 | | 69 | | 6.0 | |
| $t_{PZH}$/ $t_{PZL}$ | 3-state output enable time $SIG_{IN}$, $COMP_{IN}$ to $PC2_{OUT}$ | | 83 | 280 | | 350 | | 420 | ns | 2.0 | Fig.17 |
| | | | 30 | 56 | | 70 | | 84 | | 4.5 | |
| | | | 24 | 48 | | 60 | | 71 | | 6.0 | |
| $t_{PHZ}$/ $t_{PLZ}$ | 3-state output disable time $SIG_{IN}$, $COMP_{IN}$ to $PC2_{OUT}$ | | 99 | 325 | | 405 | | 490 | ns | 2.0 | Fig.17 |
| | | | 36 | 65 | | 81 | | 98 | | 4.5 | |
| | | | 29 | 55 | | 69 | | 83 | | 6.0 | |
| $t_{THL}$/ $t_{TLH}$ | output transition time | | 19 | 75 | | 95 | | 110 | ns | 2.0 | Fig.16 |
| | | | 7 | 15 | | 19 | | 22 | | 4.5 | |
| | | | 6 | 13 | | 16 | | 19 | | 6.0 | |
| $V_{I(p-p)}$ | AC coupled input sensitivity (peak-to-peak value) at $SIG_{IN}$ or $COMP_{IN}$ | | 9 | | | | | | mV | 2.0 | $f_i$ = 1 MHz |
| | | | 11 | | | | | | | 3.0 | |
| | | | 15 | | | | | | | 4.5 | |
| | | | 33 | | | | | | | 6.0 | |

**VCO section**

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | typ. | max. | min. | max. | | | |
| $\Delta f/T$ | frequency stability with temperature change | | | | 0.20<br>0.15<br>0.14 | | | | %/K | 3.0<br>4.5<br>6.0 | $V_I = V_{VCOIN} = 1/2\ V_{CC}$; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig.18 |
| $f_o$ | VCO centre frequency (duty factor = 50%) | 7.0<br>11.0<br>13.0 | 10.0<br>17.0<br>21.0 | | | | | | MHz | 3.0<br>4.5<br>6.0 | $V_{VCOIN} = 1/2\ V_{CC}$; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig.19 |
| $\Delta f_{VCO}$ | VCO frequency linearity | | 1.0<br>0.4<br>0.3 | | | | | | % | 3.0<br>4.5<br>6.0 | R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21 |
| $\delta_{VCO}$ | duty factor at $VCO_{OUT}$ | | 50<br>50<br>50 | | | | | | % | 3.0<br>4.5<br>6.0 | |

**DC CHARACTERISTICS FOR 74HCT**

**Quiescent supply current**

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $I_{CC}$ | quiescent supply current (VCO disabled) | | | 8.0 | | 80.0 | | 160.0 | μA | 6.0 | pins 3, 5 and 14 at $V_{CC}$; pin 9 at GND; $I_I$ at pins 3 and 14 to be excluded |
| $\Delta I_{CC}$ | additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V | | 100 | 360 | | 450 | | 490 | μA | 4.5 to 5.5 | pins 3 and 14 at $V_{CC}$; pin 9 at GND; $I_I$ at pins 3 and 14 to be excluded |

**Note**

1. The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given above.
   To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| INH | 1.00 |

**DC CHARACTERISTICS FOR 74HCT**

**Phase comparator section**

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | $V_I$ | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | | |
| | | min | typ. | max | min | max | min. | max. | | | | |
| $V_{IH}$ | DC coupled HIGH level input voltage $SIG_{IN}$, $COMP_{IN}$ | 3.15 | 2.4 | | | | | | V | 4.5 | | |
| $V_{IL}$ | DC coupled LOW level input voltage $SIG_{IN}$, $COMP_{IN}$ | | 2.1 | 1.35 | | | | | V | 4.5 | | |
| $V_{OH}$ | HIGH level output voltage $PCP_{OUT}$, $PC_{nOUT}$ | 4.4 | 4.5 | | 4.4 | | 4.4 | | V | 4.5 | $V_{IH}$ or $V_{IL}$ | $-I_O$ = 20 μA |
| $V_{OH}$ | HIGH level output voltage $PCP_{OUT}$, $PC_{nOUT}$ | 3.98 | 4.32 | | 3.84 | | 3.7 | | V | 4.5 | $V_{IH}$ or $V_{IL}$ | $-I_O$ = 4.0 mA |
| $V_{OL}$ | LOW level output voltage $PCP_{OUT}$, $PC_{nOUT}$ | | 0 | 0.1 | | 0.1 | | 0.1 | V | 4.5 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 20 μA |
| $V_{OL}$ | LOW level output voltage $PCP_{OUT}$, $PC_{nOUT}$ | | 0.15 | 0.26 | | 0.33 | | 0.4 | V | 4.5 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 4.0 mA |
| $\pm I_I$ | input leakage current $SIG_{IN}$, $COMP_{IN}$ | | | 30 | | 38 | | 45 | μA | 5.5 | $V_{CC}$ or GND | |
| $\pm I_{OZ}$ | 3-state OFF-state current $PC2_{OUT}$ | | | 0.5 | | 5.0 | | 10.0 | μA | 5.5 | $V_{IH}$ or $V_{IL}$ | $V_O$ = $V_{CC}$ or GND |
| $R_I$ | input resistance $SIG_{IN}$, $COMP_{in}$ | | 250 | | | | | | kΩ | 4.5 | $V_I$ at self-bias operating point; $\Delta V_I$ = 0.5 V; see Figs 12, 13 and 14 | |

**DC CHARACTERISTICS FOR 74HCT**

**VCO section**

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | $V_I$ | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | | |
| | | min | typ. | max | min | max | min. | max. | | | | |
| $V_{IH}$ | HIGH level input voltage INH | 2.0 | 1.6 | | 2.0 | | 2.0 | | V | 4.5 to 5.5 | | |
| $V_{IL}$ | LOW level input voltage INH | | 1.2 | 0.8 | | 0.8 | | 0.8 | V | 4.5 to 5.5 | | |
| $V_{OH}$ | HIGH level output voltage $VCO_{OUT}$ | 4.4 | 4.5 | | 4.4 | | 4.4 | | V | 4.5 | $V_{IH}$ or $V_{IL}$ | $-I_O$ = 20 μA |
| $V_{OH}$ | HIGH level output voltage $VCO_{OUT}$ | 3.98 | 4.32 | | 3.84 | | 3.7 | | V | 4.5 | $V_{IH}$ or $V_{IL}$ | $-I_O$ = 4.0 mA |
| $V_{OL}$ | LOW level output voltage $VCO_{OUT}$ | | 0 | 0.1 | | 0.1 | | 0.1 | V | 4.5 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 20 μA |
| $V_{OL}$ | LOW level output voltage $VCO_{OUT}$ | | 0.15 | 0.26 | | 0.33 | | 0.4 | V | 4.5 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 4.0 mA |
| $V_{OL}$ | LOW level output voltage $C1_A$, $C1_B$ (test purposes only) | | | 0.40 | | 0.47 | | 0.54 | V | 4.5 | $V_{IH}$ or $V_{IL}$ | $I_O$ = 4.0 mA |
| $\pm I_I$ | input leakage current INH, $VCO_{IN}$ | | | 0.1 | | 1.0 | | 1.0 | μA | 5.5 | $V_{CC}$ or GND | |
| R1 | resistor range | 3.0 | | 300 | | | | | kΩ | 4.5 | | note 1 |
| $R_2$ | resistor range | 3.0 | | 300 | | | | | kΩ | 4.5 | | note 1 |
| C1 | capacitor range | 40 | | no limit | | | | | pF | 4.5 | | |
| $V_{VCOIN}$ | operating voltage range at $VCO_{IN}$ | 1.1 | | 3.4 | | | | | V | 4.5 | | over the range specified for R1; for linearity see Figs 20 and 21 |

**Note**

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

## DC CHARACTERISTICS FOR 74HCT

### Demodulator section

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $R_S$ | resistor range | 50 | | 300 | | | | | kΩ | 4.5 | at $R_S$ > 300 kΩ the leakage current can influence $V_{DEMOUT}$ |
| $V_{OFF}$ | offset voltage $VCO_{IN}$ to $V_{DEMOUT}$ | | ±20 | | | | | | mV | 4.5 | $V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over $R_S$ range; see Fig.15 |
| $R_D$ | dynamic output resistance at $DEM_{OUT}$ | | 25 | | | | | | Ω | 4.5 | $V_{DEMOUT} = 1/2\ V_{CC}$ |

## AC CHARACTERISTICS FOR 74HCT

### Phase comparator section

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay $SIG_{IN}$, $COMP_{IN}$ to $PC1_{OUT}$ | | 23 | 40 | | 50 | | 60 | ns | 4.5 | Fig.16 |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay $SIG_{IN}$, $COMP_{IN}$ to $PCP_{OUT}$ | | 35 | 68 | | 85 | | 102 | ns | 4.5 | Fig.16 |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay $SIG_{IN}$, $COMP_{IN}$ to $PC3_{OUT}$ | | 28 | 54 | | 68 | | 81 | ns | 4.5 | Fig.16 |
| $t_{PZH}$/ $t_{PZL}$ | 3-state output enable time $SIG_{IN}$, $COMP_{IN}$ to $PC2_{OUT}$ | | 30 | 56 | | 70 | | 84 | ns | 4.5 | Fig.17 |

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHZ}$/ $t_{PLZ}$ | 3-state output disable time $SIG_{IN}$, $COMP_{IN}$ to $PC2_{OUT}$ | | 36 | 65 | | 81 | | 98 | ns | 4.5 | Fig.17 |
| $t_{THL}$/ $t_{TLH}$ | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.16 |
| $V_{I\ (p\text{-}p)}$ | AC coupled input sensitivity (peak-to-peak value) at $SIG_{IN}$ or $COMP_{IN}$ | | 15 | | | | | | mV | 4.5 | $f_i$ = 1 MHz |

**VCO section**

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | OTHER |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max | min. | max | min. | max. | | | |
| $\Delta f/T$ | frequency stability with temperature change | | | | 0.15 | | | | %/K | 4.5 | $V_I = V_{VCOIN}$ within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig.18b |
| $f_o$ | VCO centre frequency (duty factor = 50%) | 11.0 | 17.0 | | | | | | MHz | 4.5 | $V_{VCOIN}$ = 1/2 $V_{CC}$; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig.19 |
| $\Delta f_{VCO}$ | VCO frequency linearity | | 0.4 | | | | | | % | 4.5 | R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21 |
| $\delta_{VCO}$ | duty factor at $VCO_{OUT}$ | | 50 | | | | | | % | 4.5 | |

**FIGURE REFERENCES FOR DC CHARACTERISTICS**

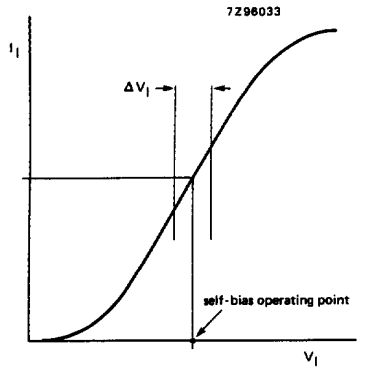



Fig.12 Typical input resistance curve at $SIG_{IN}$, $COMP_{IN}$.

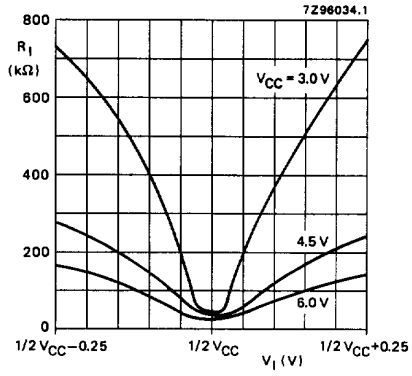



Fig.13 Input resistance at $SIG_{IN}$, $COMP_{IN}$ with $\Delta V_I$ = 0.5 V at self-bias point.

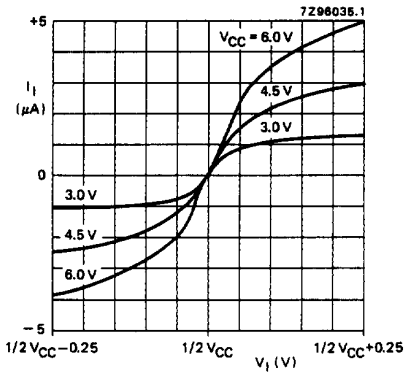
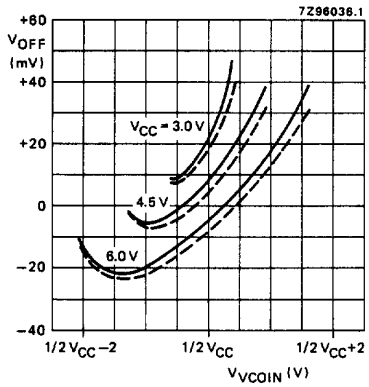


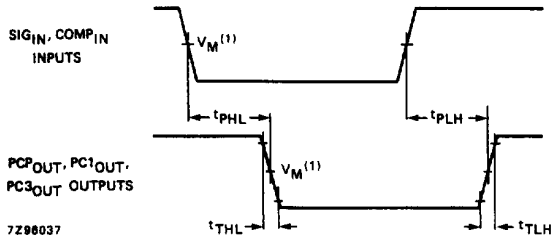

Fig.14 Input current at $SIG_{IN}$, $COMP_{IN}$ with $\Delta V_I$ = 0.5 V at self-bias point.




—— $R_S$ = 50 kΩ
- - - - $R_S$ = 300 kΩ

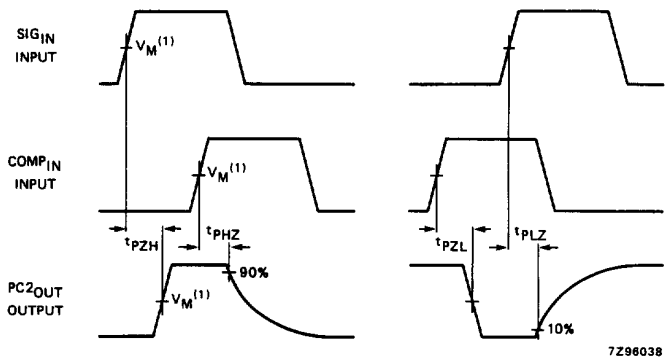
Fig.15 Offset voltage at demodulator output as a function of $VCO_{IN}$ and $R_S$.

**AC WAVEFORMS**



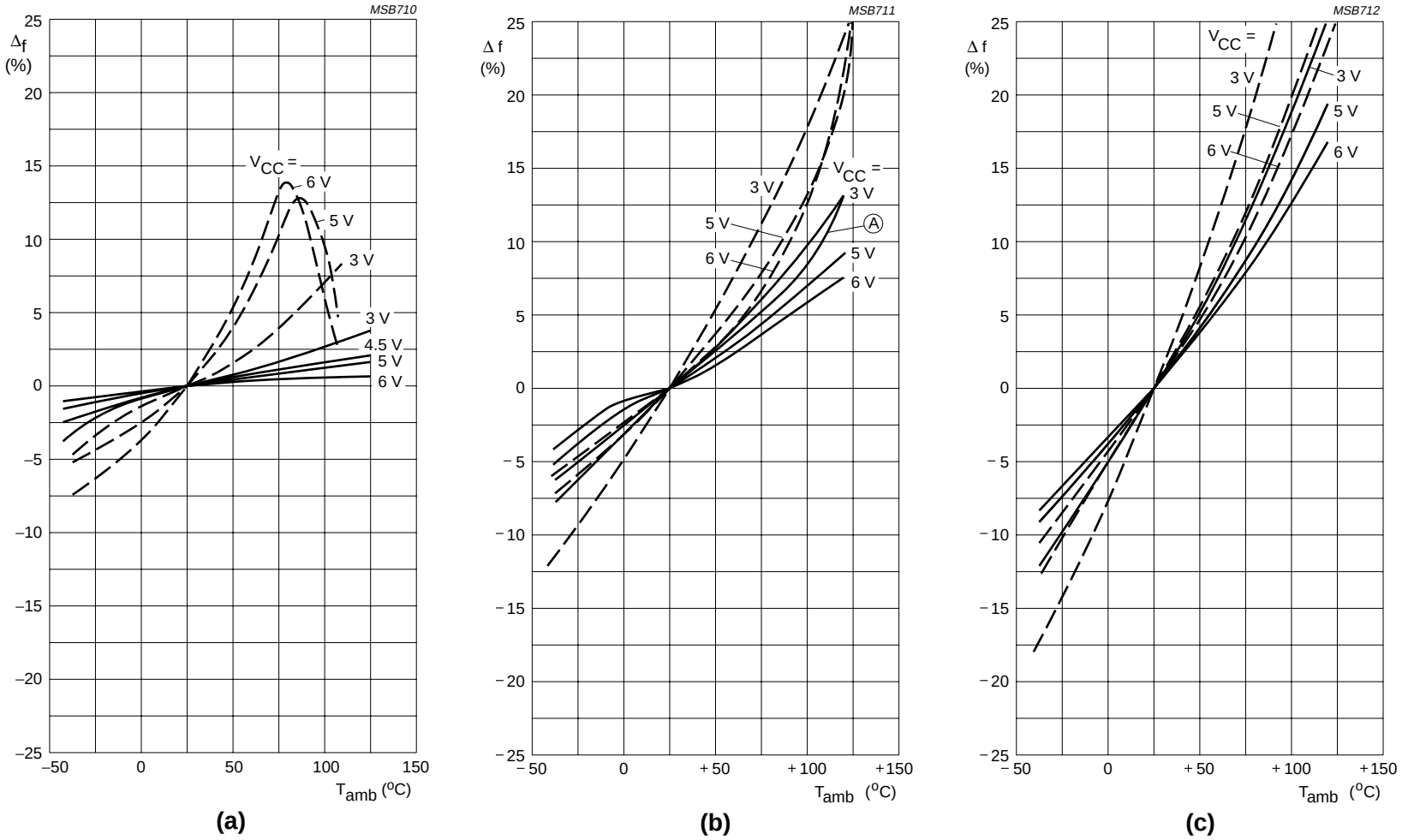

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$

Fig.16 Waveforms showing input ($SIG_{IN}$, $COMP_{IN}$) to output ($PCP_{OUT}$, $PC1_{OUT}$, $PC3_{OUT}$) propagation delays and the output transition times.



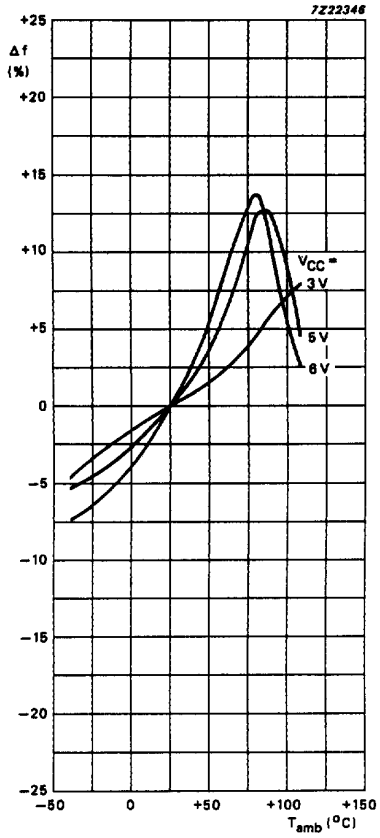

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$

Fig.17 Waveforms showing the 3-state enable and disable times for $PC2_{OUT}$.

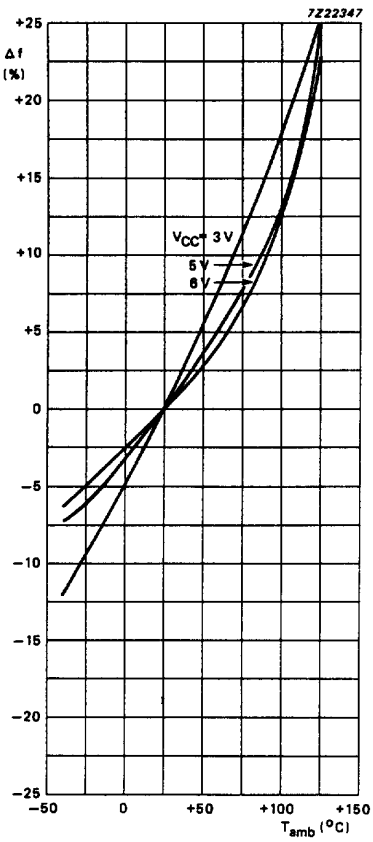



To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

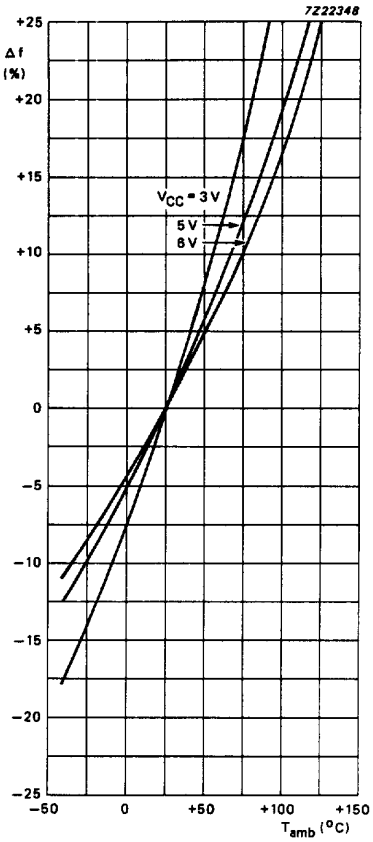
Fig.18 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.
—— without offset (R2 = ∞): (a) R1 = 3 kΩ; (b) R1 = 10 kΩ; (c) R1 = 300 kΩ.
– – – with offset (R1 = ∞): (a) R2 = 3 kΩ; (b) R2 = 10 kΩ; (c) R2 = 300 kΩ.
In (b), the frequency stability for R1 = R2 = 10 kΩ at 5 V is also given (curve A). This curve is set by the total VCO bias current, and is not simply the addition of the two 10 kΩ stability curves. C1 = 100 pF; $V_{VCO\ IN}$ = 0.5 $V_{CC}$.




**(d) $R_2$ = 3 kΩ**
**$R_1$ = ∞**



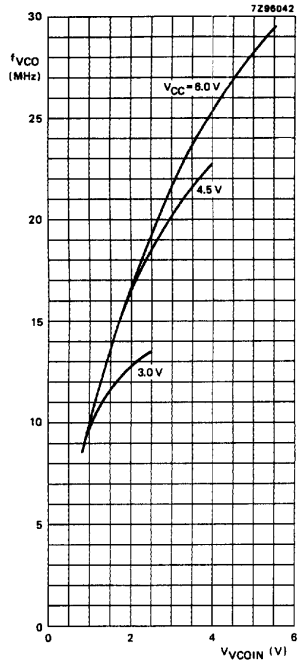

**(e) $R_2$ = 10 kΩ**
**$R_1$ = ∞**



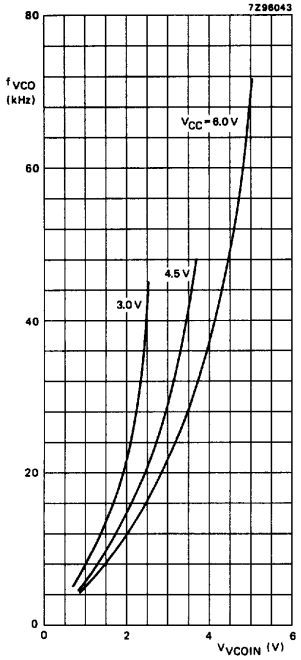

**(f) $R_2$ = 300 kΩ**
**$R_1$ = ∞**

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

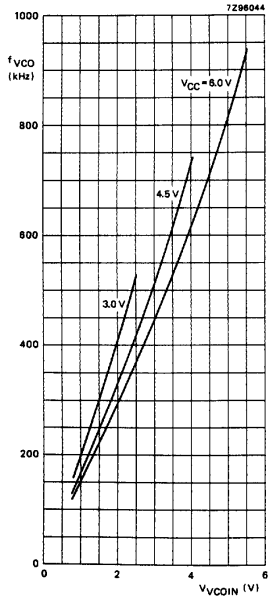
Fig.18 Continued.



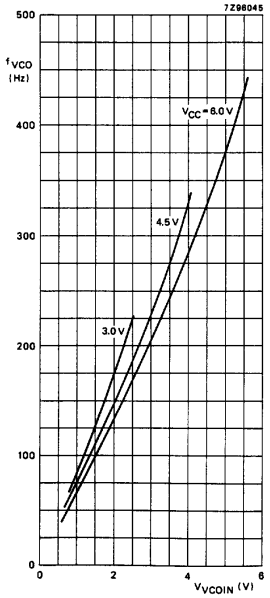

**(a) $R_1$ = 3 kΩ; $C_1$ = 40 pF**




**(b) $R_1$ = 3 kΩ; $C_1$ = 100 nF**




**(c) $R_1$ = 300 kΩ; $C_1$ = 40 pF**




**(d) $R_1$ = 300 kΩ; $C_1$ = 100 nF**

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

Fig.19 Graphs showing VCO frequency ($f_{VCO}$) as a function of the VCO input voltage ($V_{VCOIN}$).

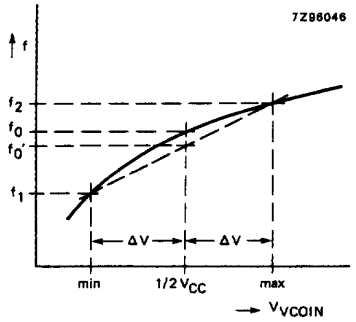



Fig.20 Definition of VCO frequency linearity: $\Delta V = 0.5$ V over the $V_{CC}$ range: for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2}$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

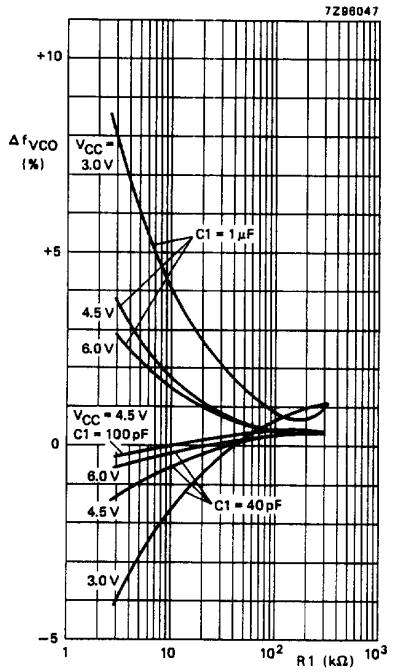
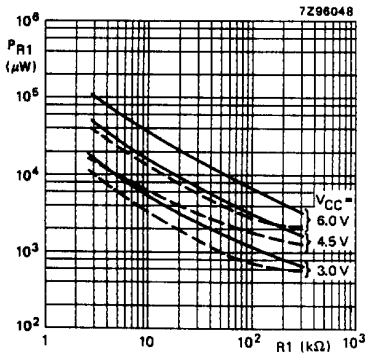
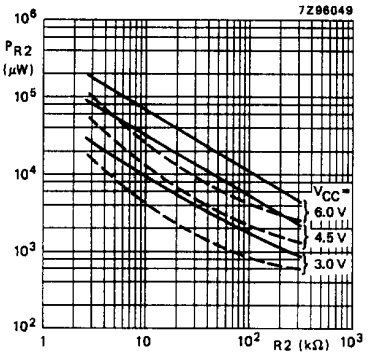



Fig.21 Frequency linearity as a function of R1, C1 and $V_{CC}$: R2 = ∞ and $\Delta V = 0.5$ V.




—— C1 = 40 pF
- - - -C1 = 1 μF

Fig.22 Power dissipation versus the value of R1: $C_L = 50$ pF; R2 = ∞; $V_{VCOIN} = 1/2\ V_{CC}$; $T_{amb} = 25$ °C.




—— C1 = 40 pF
- - - - C1 = 1 μF

Fig.23 Power dissipation versus the value of R2: $C_L = 50$ pF; R1 = ∞; $V_{VCOIN}$ = GND = 0 V; $T_{amb} = 25$ °C.

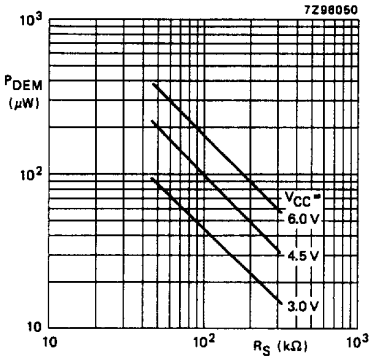



Fig.24 Typical dc power dissipation of demodulator sections as a function of $R_S$: R1 = R2 = ∞; $T_{amb} = 25$ °C; $V_{VCOIN} = 1/2\ V_{CC}$.

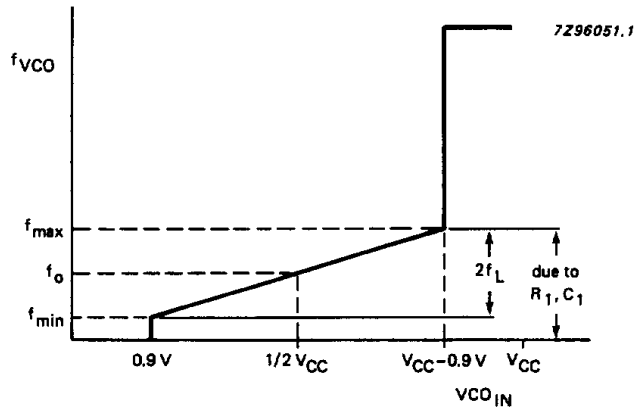
## APPLICATION INFORMATION

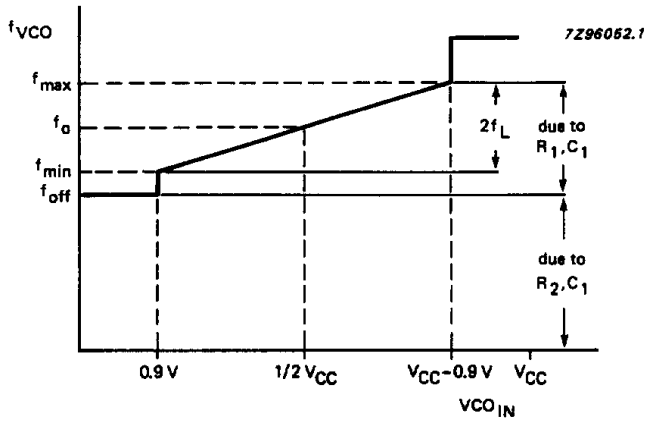
This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-lock-loop system.

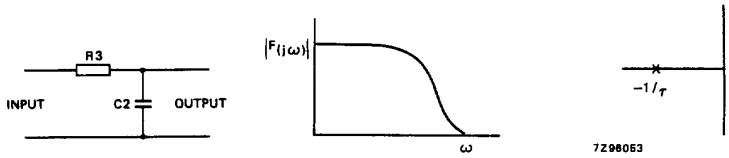
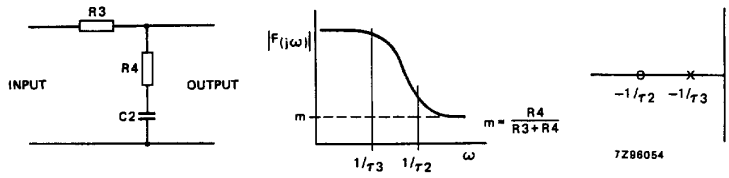
References should be made to Figs 29, 30 and 31 as indicated in the table.

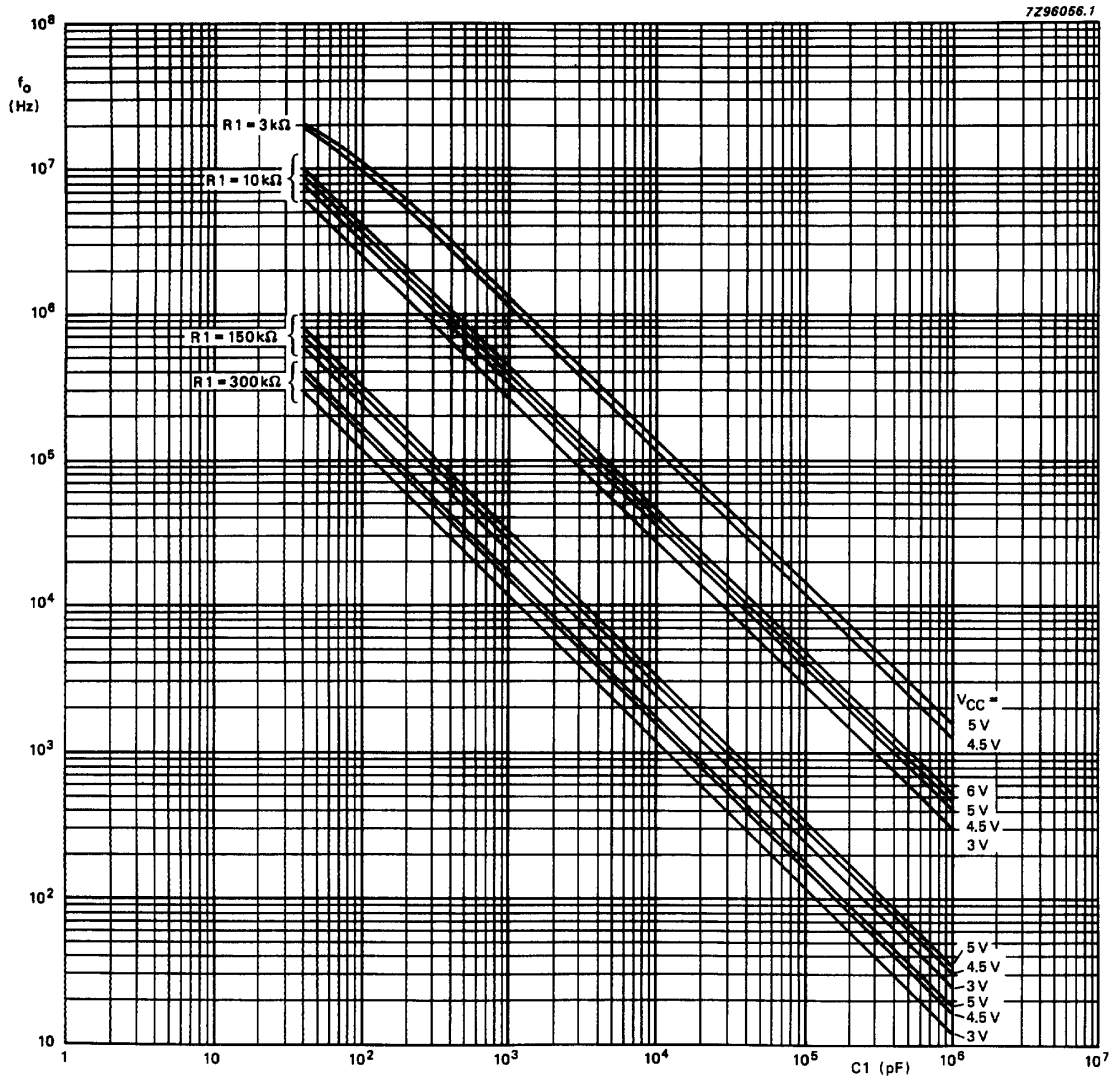
Values of the selected components should be within the following ranges:

R1 between 3 kΩ and 300 kΩ;
R2 between 3 kΩ and 300 kΩ;
R1 + R2 parallel value > 2.7 kΩ;
C1 greater than 40 pF.

| SUBJECT | PHASE COMPARATOR | DESIGN CONSIDERATIONS |
|---|---|---|
| VCO frequency **without extra offset** | PC1, PC2 or PC3 | **VCO frequency characteristic**<br>With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.25. (Due to R1, C1 time constant a small offset remains when R2 = ∞.). |
| | |  <br>Fig.25 Frequency characteristic of VCO operating without offset: $f_0$ = centre frequency; $2f_L$ = frequency lock range. |
| | PC1 | **Selection of R1 and C1**<br>Given $f_o$, determine the values of R1 and C1 using Fig.29. |
| | PC2 or PC3 | Given $f_{max}$ and $f_o$, determine the values of R1 and C1 using Fig.29, use Fig.31 to obtain $2f_L$ and then use this to calculate $f_{min}$. |

| SUBJECT | PHASE COMPARATOR | DESIGN CONSIDERATIONS |
|---|---|---|
| VCO frequency **with extra offset** | PC1, PC2 or PC3 | **VCO frequency characteristic**<br>With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.26.<br>  <br><br>Fig.26 Frequency characteristic of VCO operating with offset: $f_o$ = centre frequency; $2f_L$ = frequency lock range. |
| | PC1, PC2 or PC3 | **Selection of R1, R2 and C1**<br>Given $f_o$ and $f_L$, determine the value of product R1C1 by using Fig.31.<br>Calculate $f_{off}$ from the equation $f_{off} = f_o — 1.6f_L$.<br>Obtain the values of C1 and R2 by using Fig.30.<br>Calculate the value of R1 from the value of C1 and the product R1C1. |
| PLL conditions with no signal at the $SIG_{IN}$ input | PC1 | VCO adjusts to $f_o$ with $\phi_{DEMOUT}$ = 90° and $V_{VCOIN}$ = 1/2 $V_{CC}$ (see Fig.6). |
| | PC2 | VCO adjusts to $f_o$ with $\phi_{DEMOUT}$ = –360° and $V_{VCOIN}$ = min. (see Fig.8). |
| | PC3 | VCO adjusts to $f_o$ with $\phi_{DEMOUT}$ = –360° and $V_{VCOIN}$ = min. (see Fig.10). |

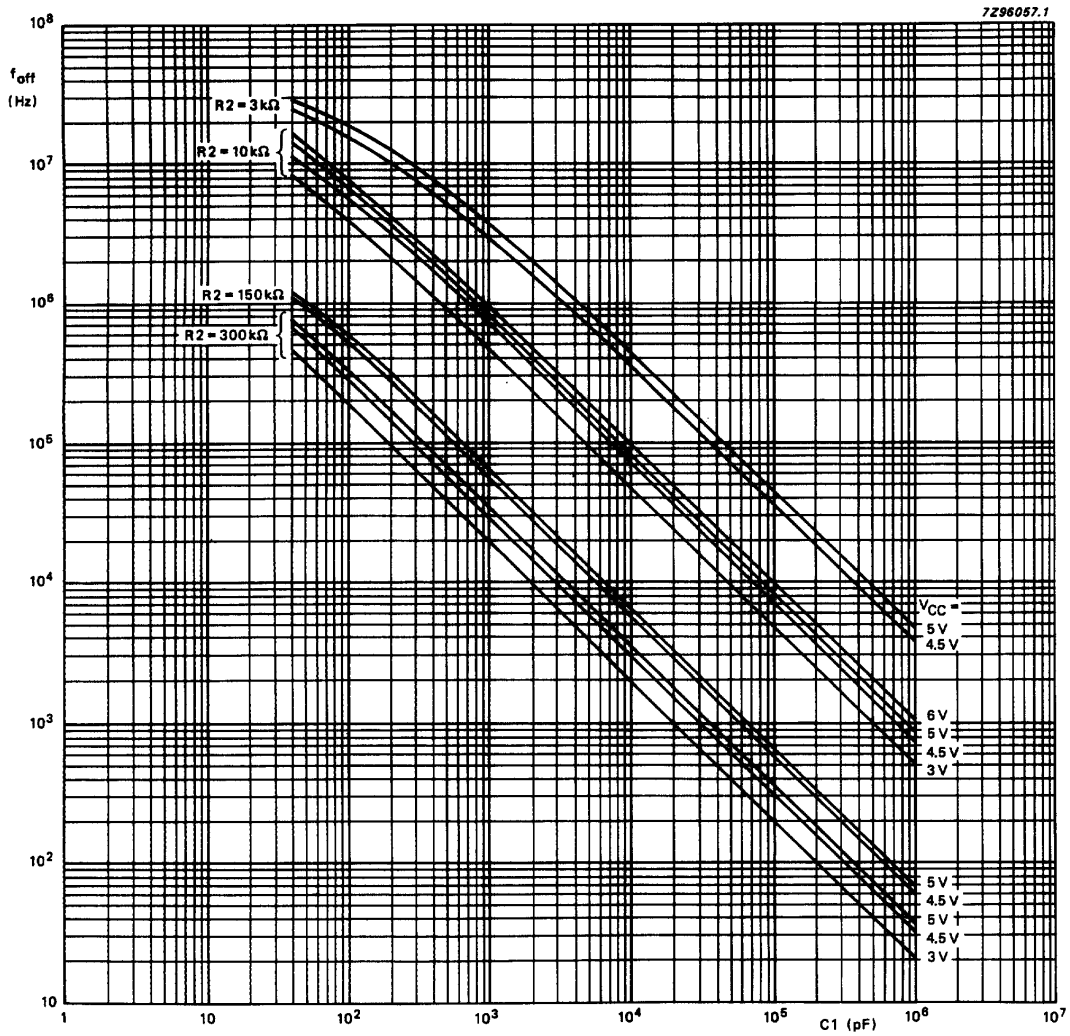
| SUBJECT | PHASE COMPARATOR | DESIGN CONSIDERATIONS |
|---|---|---|
| PLL frequency capture range | PC1, PC2 or PC3 | **Loop filter component selection**<br>  <br><br>(a) $\tau$ = R3 x C2 (b) amplitude characteristic (c) pole-zero diagram<br>A small capture range ($2f_c$) is obtained if $2f_c \approx \frac{1}{\pi}\sqrt{2\pi f_L/\tau}$<br>Fig. 27 Simple loop filter for PLL without offset; R3 ≥ 500 Ω.<br>  <br><br>(a) $\tau 1$ = R3 x C2; (b) amplitude characteristic (c) pole-zero diagram<br>$\tau 2$ = R4 x C2;<br>$\tau 3$ = (R3 + R4) x C2<br>Fig.28 Simple loop filter for PLL with offset; R3 + R4 ≥ 500 Ω. |
| PLL locks on harmonics at centre frequency | PC1 or PC3 | yes |
| | PC2 | no |
| noise rejection at signal input | PC1 | high |
| | PC2 or PC3 | low |
| AC ripple content when PLL is locked | PC1 | $f_r = 2f_i$, large ripple content at $\phi_{DEMOUT}$ = 90° |
| | PC2 | $f_r = f_i$, small ripple content at $\phi_{DEMOUT}$ = 0° |
| | PC3 | $f_r = f_i$, large ripple content at $\phi_{DEMOUT}$ = 180° |




To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.

Interpolation for various values of R1 can be easily calculated because a constant R1C1 product will produce almost the same VCO output frequency.

Fig.29 Typical value of VCO centre frequency ($f_o$) as a function of C1: R2 = ∞; $V_{VCOIN}$ = 1/2 $V_{CC}$; INH = GND; $T_{amb}$ = 25 °C.




To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
Interpolation for various values of R2 can be easily calculated because a constant R2C1 product will produce almost the same VCO output frequency.

Fig.30 Typical value of frequency offset as a function of C1: R1 = ∞; $V_{VCOIN}$ = 1/2 $V_{CC}$; INH = GND; $T_{amb}$ = 25 °C.

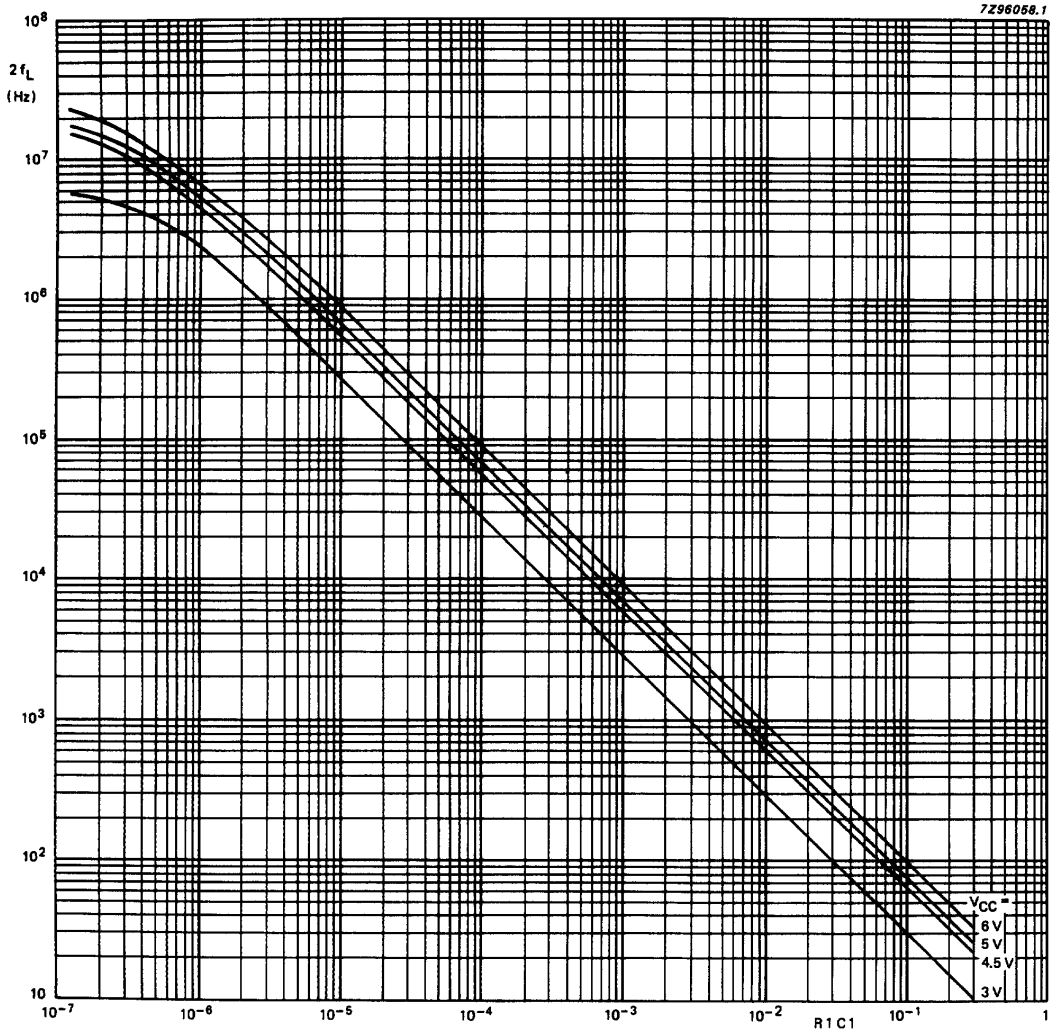



Fig.31 Typical frequency lock range ($2f_L$) versus the product R1C1: $V_{VCOIN}$ range = 0.9 to ($V_{CC}$ – 0.9) V; R2 = ∞; VCO gain:

$$K_V = \frac{2f_L}{V_{VCOIN}\ \text{range}} 2\pi\,(r/s/V)\,.$$

**PLL design example**

The frequency synthesizer, used in the design example shown in Fig.32, has the following parameters:

Output frequency: 2 MHz to 3 MHz
frequency steps : 100 kHz
settling time : 1 ms
overshoot : < 20%

The open-loop gain is
H (s) x G (s) = $K_p \times K_f \times K_o \times K_n$.

**Where:**

$K_p$ = phase comparator gain
$K_f$ = low-pass filter transfer gain
$K_o$ = $K_v$/s VCO gain
$K_n$ = 1/n divider ratio

The programmable counter ratio $K_n$ can be found as follows:

$$N_{min.} = \frac{f_{out}}{f_{step}} = \frac{2\ \text{MHz}}{100\ \text{kHz}} = 20$$

$$N_{max.} = \frac{f_{out}}{f_{step}} = \frac{3\ \text{MHz}}{100\ \text{kHz}} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 kΩ (adjustable). The values can be determined using the information in the section "DESIGN CONSIDERATIONS". With $f_o$ = 2.5 MHz and $f_L$ = 500 kHz this gives the following values ($V_{CC}$ = 5.0 V):
R1 = 10 kΩ
R2 = 10 kΩ
C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} =$$

$$= \frac{1\ \text{MHz}}{3.2} \times 2\pi \approx 2 \times 10^6\ \text{r/s/V}$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4\ \text{V/r}.$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)\, s}.$$

**Where:**
$\tau_1$ = R3C2 and $\tau_2$ = R4C2.

The characteristics equation is:
1 + H (s) × G (s) = 0.

This results in:

$$s^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} s +$$

$$\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0.$$

The natural frequency $\omega_n$ is defined as follows:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}.$$

and the damping value ζ is defined as follows:

$$\zeta = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}$$

In Fig.33 the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine $\omega_n$. From Fig.33 it can be seen that the damping ratio ζ = 0.45 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t$ = 5. The required settling time is 1 ms.
This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3\ \text{r/s}.$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}.$$

The maximum overshoot occurs at $N_{max.}$:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011\ \text{s}.$$

When C2 = 470 nF, then

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \zeta - 1}{K_p \times K_v \times K_n \times C2} = 315\ \Omega$$

now R3 can be calculated:

$$R3 = \frac{\tau_1}{C2} - R4 = 2\ \text{k}\Omega.$$

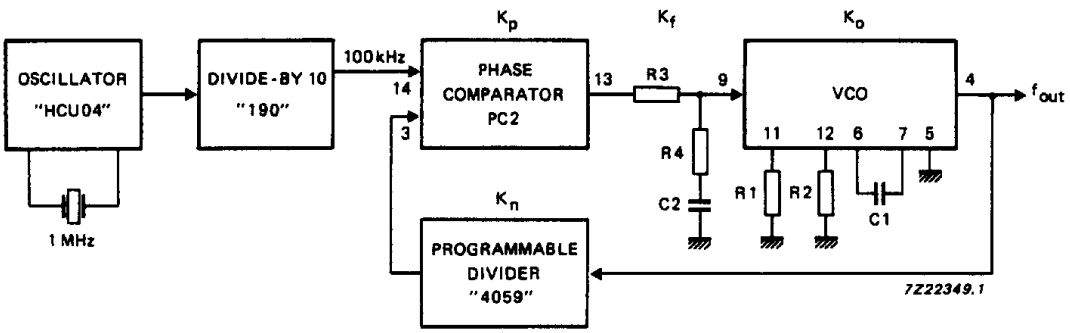



Fig.32 Frequency synthesizer.

**note**

For an extensive description and application example please refer to application note ordering number 9398 649 90011.
Also available a computer design program for PLL's ordering number 9398 961 10061.

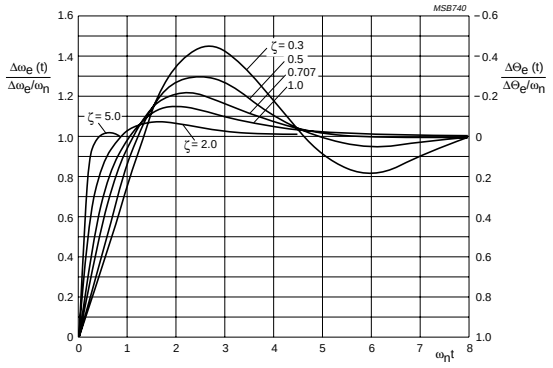



Fig.33 Type 2, second order frequency step response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.

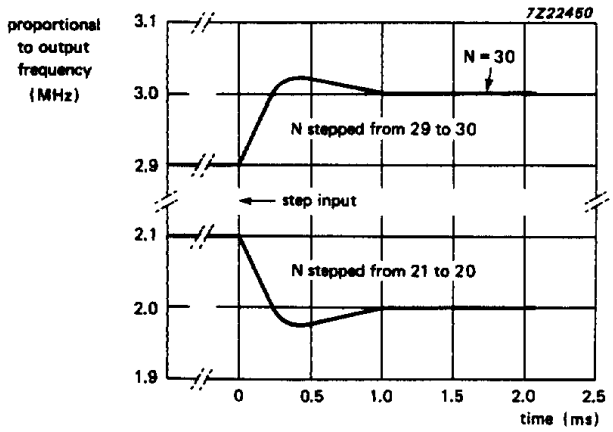



Fig.34 Frequency compared to the time response.

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### SO, SSOP and TSSOP

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

**Even with these conditions:**

- **Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**
- **Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

## LIFE SUPPORT APPLICATIONS

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Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

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Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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