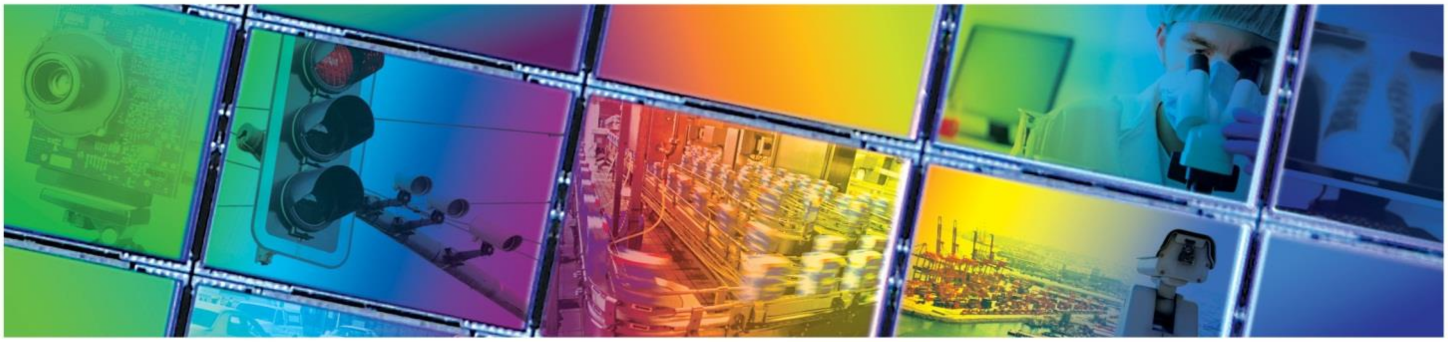
ON Semiconductor®

KAF-1603 IMAGE SENSOR

1536 (H) X 1024 (V) FULL FRAME CCD IMAGE SENSOR



JUNE 18, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0036

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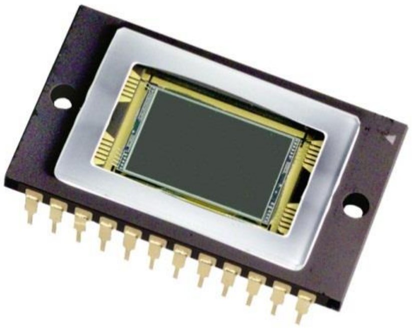
Summary Specification

KAF-1603 Image Sensor



DESCRIPTION

The KAF-1603 Image Sensor is a high performance monochrome area CCD (charge-coupled device) image sensor with 1536 H x 1024 V photoactive pixels designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Optional microlenses focus the majority of the light through the transparent gate, increasing the optical response further.

FEATURES

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for high sensitivity

APPLICATION

- Scientific Imaging

Parameter	Typical Value
Architecture	Full Frame CCD
Total Number of Pixels	1552 (H) x 1032 (V)
Number of Active Pixels	1536 (H) x 1024 (V) = approx. 1.6 M
Pixel Size	9.0 µm (H) x 9.0 µm (V)
Active Image Size	13.8 mm (H) x 9.2 mm (V)
Die Size	15.5 mm (H) x 10 mm (V)
Aspect Ratio	3:2
Saturation Signal	100,000 electrons
Output Sensitivity	10 µV/e^-
Quantum Efficiency (with microlens)	Peak: 77% 400 nm: 45%
Quantum Efficiency (no microlens)	Peak: 65% 400 nm: 30%
Read Noise	15 electrons
Dark Current (T = 25 °C)	<10 pA/cm^2
Dark Current Doubling Temperature	6.3 °C
Dynamic Range	74 dB
Charge Transfer Efficiency	>0.99999
Blooming Suppression	None
Maximum Data Rate	10 MHz
Package	CERDIP Package (sidebrazed)
Cover Glass	Clear or AR coated, 2sides

Parameters above are specified at 25 °C, unless otherwise noted.

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0217	KAF-1603-ABA-CD-B2	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 2	KAF-1603-ABA [Serial Number]
4H0219	KAF-1603-ABA-CD-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0222	KAF-1603-ABA-CP-B2	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 2	
4H0223	KAF-1603-ABA-CP-B3	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 3	
4H0224	KAF-1603-ABA-CP-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0337	KAF-1603-AAA-CP-B2	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 2	KAF-1603-AAA [Serial Number]
4H0339	KAF-1603-AAA-CP-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0078	KEK-4H0078-KAF-1602/1603-12-5	Evaluation Board (Complete Kit)	N/A

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

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Device Description

ARCHITECTURE

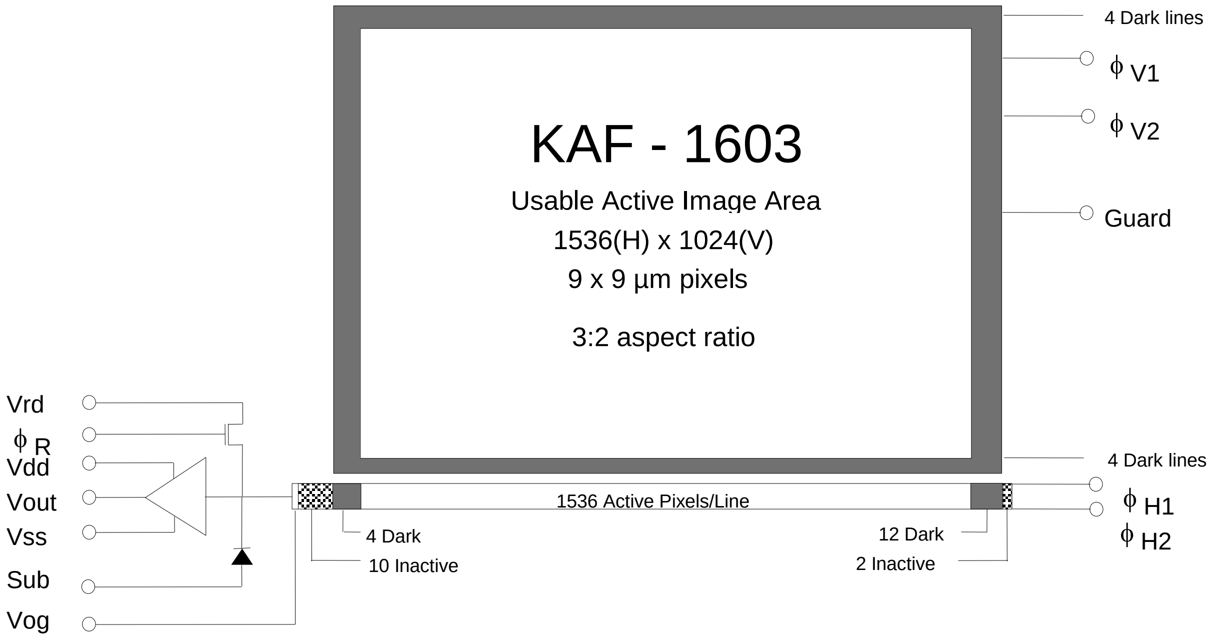


Figure 1: Block Diagram

The sensor consists of 1552 parallel (vertical) CCD shift registers each 1032 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The parallel (vertical) CCD registers transfer the image one line at a time into a single 1564 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

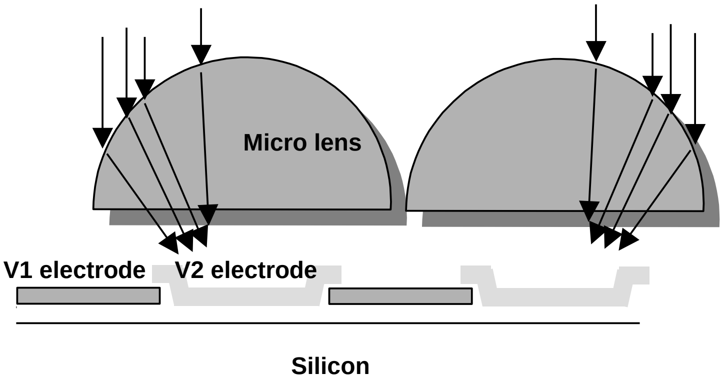


Figure 2: Microlens Cross-Section

Micro lenses are formed along each row. They are effectively half of a cylinder centered on the transparent gates, extending continuously in the row direction. They act to direct the photons away from the polysilicon gate and through the transparent gate. This increases the response, especially at the shorter wavelengths (< 600 nm).

Dark Reference Pixels

There are 4 light shielded pixels at the beginning of each line, and 12 at the end. There are 4 dark lines at the start of every frame and 4 dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Output Structure

Charge presented to the floating diffusion is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the floating diffusion. Once the signal has been sampled by the system electronics, the reset gate (φR) is clocked to remove the signal, and the floating diffusion is reset to the potential applied by Vrd (see Figure 3). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device such as shown in Figure 4.

Dummy Pixels

Within the horizontal shift register are 10 leading additional pixels that are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions. There are two more dummy pixels at the end of each line

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the φV1 and φV2 register clocks are held at a constant (low) level, and the sensor is illuminated. See Figure 8. The sensor must be illuminated only during the integration period. Light must not reach the sensor during the time the image is read out. This is usually accomplished with the use of a mechanical shutter or a pulsed light source.

CHARGE TRANSPORT

Referring to Figure 9, the integrated charge from each photogate is transported to the output using a two-step process. During this readout time, the sensor needs to be protected from all light through the use of a shutter or pulsed light source. Each line (row) of charge is first moved from the vertical CCD to the horizontal CCD register using the φV1 and φV2 register clocks. The horizontal CCD is presented a new line on the falling edge of φV2 while φH1 is held high. The horizontal CCD then transports each line, pixel by pixel, to the output structure by alternately clocking the φH1 and φH2 pins in a complementary fashion. On each falling edge of φH2 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

HORIZONTAL REGISTER

Output Structure

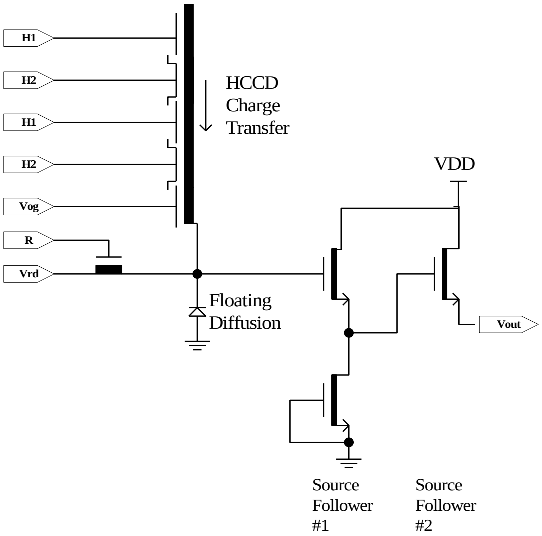


Figure 3: Output Schematic

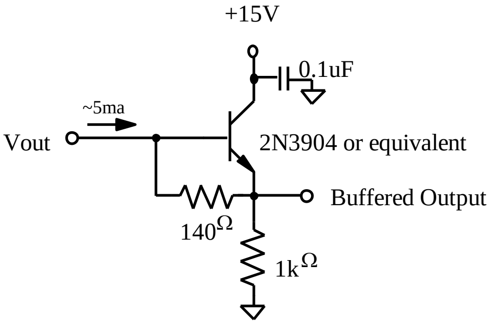


Figure 4: Output Structure Load Diagram

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

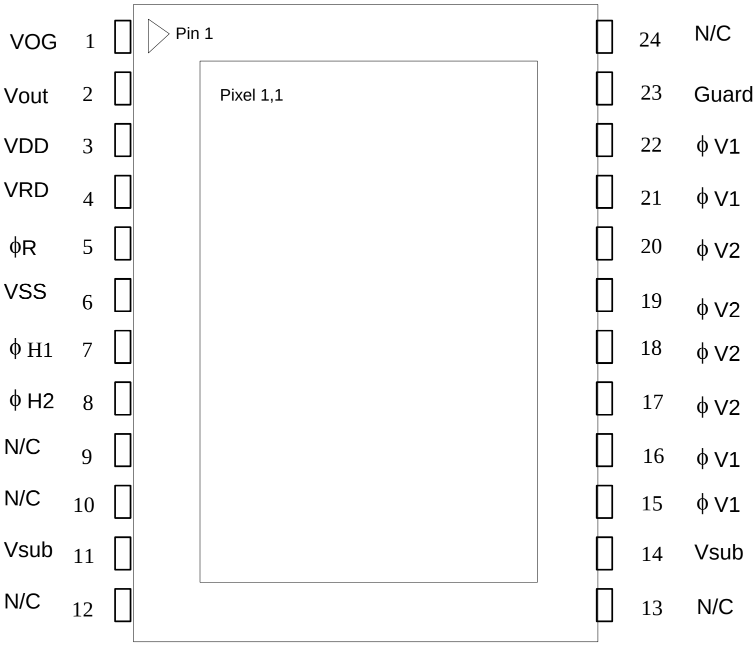


Figure 5: Pinout Diagram

Notes:

1. The KAF-1603 is mechanically the same and electrically identical to the KAF-0402 sensor. It is also mechanically the same as the KAF-0261 and KAF-3200 sensors. There are some electrical differences since the KAF-0261 has two outputs and two additional clock inputs. The KAF-3200 requires that pin 11 be a “No connect” and be electrically floating. Refer to their specifications for details.

Pin	Name	Description
1	Vog	Output Gate
2	Vout	Video Output
3	Vdd	Amplifier Supply
4	Vrd	Reset Drain
5	φR	Reset Clock
6	Vss	Amplifier Supply Return
7	φH1	Horizontal CCD Clock - Phase 1
8	φH2	Horizontal CCD Clock - Phase 2
9	N/C	No Connection (open pin)
10	N/C	No Connection (open pin)
11	Vsub	Substrate (Ground)
12	N/C	No Connection (open pin)

Pin	Name	Description
13	N/C	No Connection (open pin)
14	Vsub	Substrate (Ground)
15	φV1	Vertical CCD Clock - Phase 1
16	φV1	Vertical CCD Clock - Phase 1
17	φV2	Vertical CCD Clock - Phase 2
18	φV2	Vertical CCD Clock - Phase 2
19	φV2	Vertical CCD Clock - Phase 2
20	φV2	Vertical CCD Clock - Phase 2
21	φV1	Vertical CCD Clock - Phase 1
22	φV1	Vertical CCD Clock - Phase 1
23	Guard	Guard Ring
24	N/C	No Connection (open pin)

Imaging Performance

TYPICAL OPERATIONAL CONDITIONS

All values measured at 25 °C, and nominal operating conditions. These parameters exclude defective pixels.

SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Saturation Signal	Nsat				electrons/pixel	1	design[9]
Vertical CCD capacity		85000	100000				
Horizontal CCD capacity		170000	200000				
Output Node capacity		190000	220000	240000			
Quantum Efficiency (microlens)				77%	%QE		design[9]
Quantum Efficiency (no microlens)				65%			
Photoresponse Non-Linearity	PRNL		1.0	2.0	%	2	design[9]
Photoresponse Non-Uniformity	PRNU		0.8		%	3	die[8]
Dark Signal	Jdark		10	50	electrons/pixel/sec	4	die[8]
			2	10	pA/cm^2		
Dark Signal Doubling Temperature			6.3	7	°C		design[9]
Dark Signal Non-Uniformity	DSNU		10	50	electrons/pixel/sec	5	die[8]
Dynamic Range	DR	72	74		DB	6	design[9]
Charge Transfer Efficiency	CTE	0.99997	0.99999				die[8]
Output Amplifier DC Offset	Vodc	Vrd	Vrd + 0.5	Vrd + 1.0	V		die[8]
Output Amplifier Sensitivity	$Vout/Ne^-$	9	10		$\mu V/e^-$		design[9]
Output Amplifier Output Impedance	Zout	180	200	220	Ohms		design[9]
Noise Floor	ne^-		15	20	electrons	7	die[8]

Notes:

1. For pixel binning applications, electron capacity up to 330000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst-case deviation from straight line fit, between 2% and 90% of Vsat.
3. One Sigma deviation of a 128 x 128 sample when CCD illuminated uniformly at half of saturation.
4. Average of all pixels with no illumination at 25 °C
5. Average dark signal of any of 11 x 8 blocks within the sensor (each block is 128 x 128 pixels).
6. 20log (Nsat / ne^-) at nominal operating frequency and 25 °C.
7. Noise floor is specified at the nominal pixel frequency and excludes any dark or pattern noises. It is dominated by the output amplifier power spectrum with a bandwidth = 5 * pixel rate.
8. A parameter that is measured on every sensor during production testing.
9. A parameter that is quantified during the design verification activity.

Typical Performance Curves

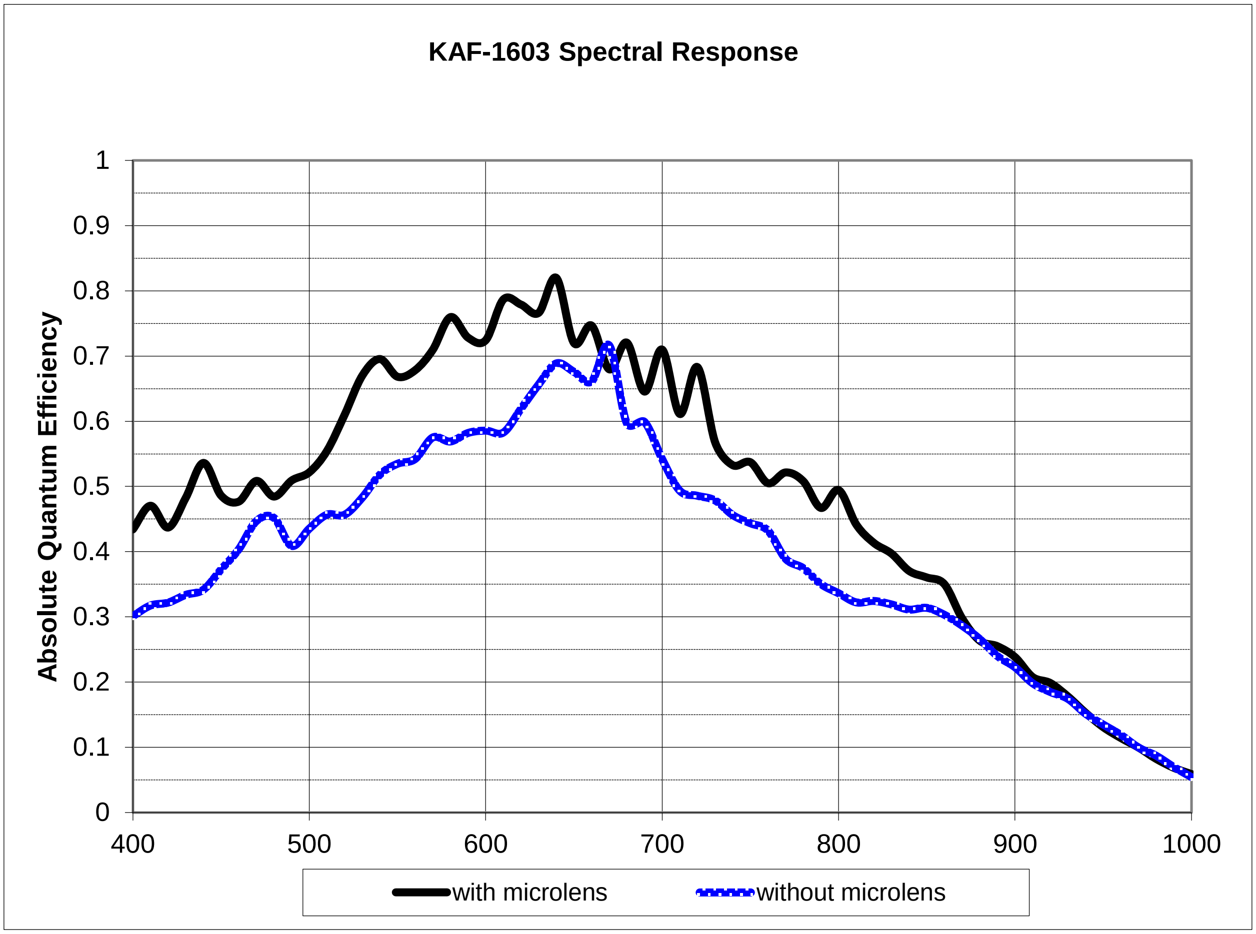


Figure 6: Typical Spectral Response

Defect Definitions

OPERATING CONDITIONS

All tests performed at T = 25 °C

SPECIFICATIONS

Classification	Point Defect		Cluster Defect		Column Defect	
	Total	Zone A	Total	Zone A	Total	Zone A
C2	≤10	≤5	≤4	≤2	0	0

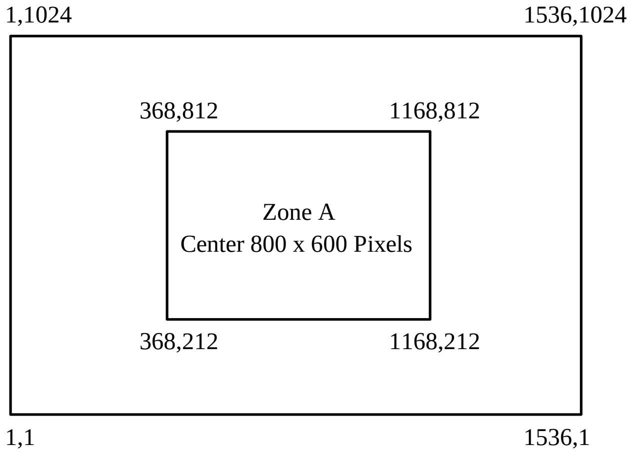


Figure 7: Active Pixel Region

Point Defects	Dark: A pixel that deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation. -- OR -- Bright: A pixel with a dark current greater than 5000 e^-/pixel/sec at 25 °C.
Cluster Defect	A grouping of not more than 5 adjacent point defects.
Column Defect	A grouping of more than 5 contiguous point defects along a single column. A column containing a pixel with dark current greater than 12,000 e^-/pixel/sec (bright column). A column that does not meet the minimum vertical CCD charge capacity (low charge capacity column). A column which loses more than 250 e^- under 2 ke^- illumination (trap defect).
Neighboring Pixels	The surrounding 128 x 128 pixels or ± 64 column/rows.
Defect Separation	Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

Operation

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1, 2
Gate Pin Voltages	Vgate1	-16	16	V	1, 3, 6
Output Bias Current	Iout		-10	mA	4
Output Load Capacitance	Cload		15	pF	4
Storage Temperature	T	-20	80	°C	
Humidity	RH	5	90	%	5

Notes:

1. Referenced to pin Vsub or between each pin in this group.
2. Includes pins: Vrd, Vdd, Vss, Vout.
3. Includes pins: φV1, φV2, φH1, φH2, Vog, Vlg, φR.
4. Avoid shorting output pins to ground or any low impedance source during operation.
5. T = 25 °C. Excessive humidity will degrade MTTF.
6. This sensor contains gate protection circuits to provide some protection against ESD events. The circuits will turn on when greater than 16 volts appears between any two gate pins. Permanent damage can result if excessive current is allowed to flow under these conditions.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	Vrd	10.5	11.0	11.5	V	0.01	
Output Amplifier Return	Vss	1.5	2.0	2.5	V	-0.5	
Output Amplifier Supply	Vdd	14.5	15	15.5	V	Iout	
Substrate	Vsub	0	0	0	V	0.01	
Output Gate	Vog	3.75	4	5	V	0.01	
Guard Ring	Vlg	8.0	9.0	12.0	V	0.01	
Video Output Current	Iout		-5	-10	mA	-	1

Note:

1. An output load sink must be applied to Vout to activate output amplifier - see Figure 4.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance
Vertical CCD Clock - Phase 1	φV1	Low	-10.5	-10.0	-9.5	V	6 nf (all φV1 pins)
Vertical CCD Clock - Phase 1	φV1	High	0	0.5	1.0	V	6 nf (all φV1 pins)
Vertical CCD Clock - Phase 2	φV2	Low	-10.5	-10.0	-9.5	V	6 nf (all φV2 pins)
Vertical CCD Clock - Phase 2	φV2	High		0.5	1.0	V	6 nf (all φV2 pins)
Horizontal CCD Clock - Phase 1	φH1	Low	-4.5	-4.0	-3.5	V	50 pF
Horizontal CCD Clock - Phase 1	φH1	Amplitude	9.5	10.0	10.5	V	50 pF
Horizontal CCD Clock - Phase 2	φH2	Low	-4.5	-4.0	-3.5	V	50 pF
Horizontal CCD Clock - Phase 2	φH2	Amplitude	9.5	10.0	10.5	V	50 pF
Reset Clock	φR	Low	-3.0	-2.0	-1.75	V	50 pF
Reset Clock	φR	Amplitude	5.0	6.0	7.0	V	50 pF

Notes:

1. All pins draw less than 10 μA DC current.
2. Capacitance values relative to VSUB.

Timing

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
φH1, φH2 Clock Frequency	f_H		4250	10	MHz	1, 2, 3
Pixel Period (I count)	t_e	100	1		ns	
φH1, φH2 Setup Time	$t_{\varphi HS}$	0.5	5		μs	
φV1, φV2 Clock Pulse Width	$t_{\varphi V}$	4	20		μs	2
Reset Clock Width	$t_{\varphi R}$	10	420		ns	4
Readout Time	$t_{readout}$	178			ms	5
Integration Time	t_{int}		407			6
Line Time	t_{line}	172.4			μs	7

Notes:

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. φR should be clocked continuously.
5. $t_{readout} = (1032^* t_{line})$.
6. Integration time is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = (3^* t_{\varphi V}) + t_{\varphi HS} + (1564^* t_e) + t_e$.

FRAME TIMING

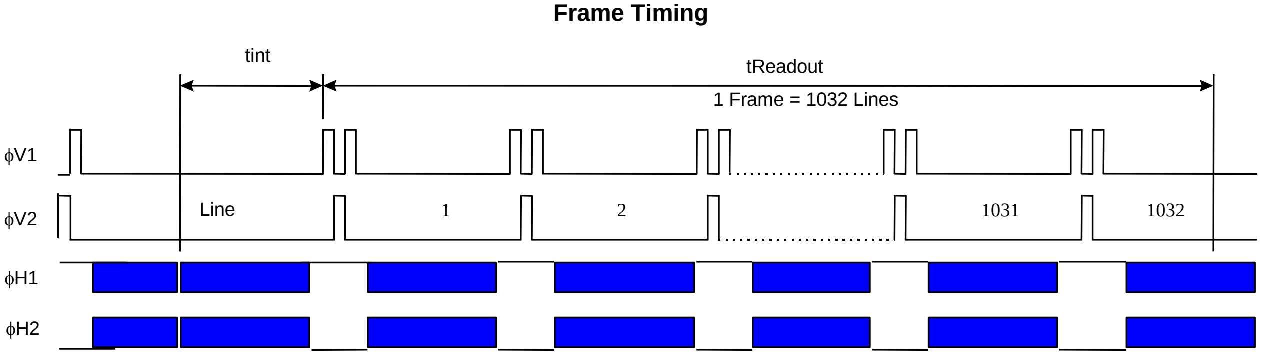
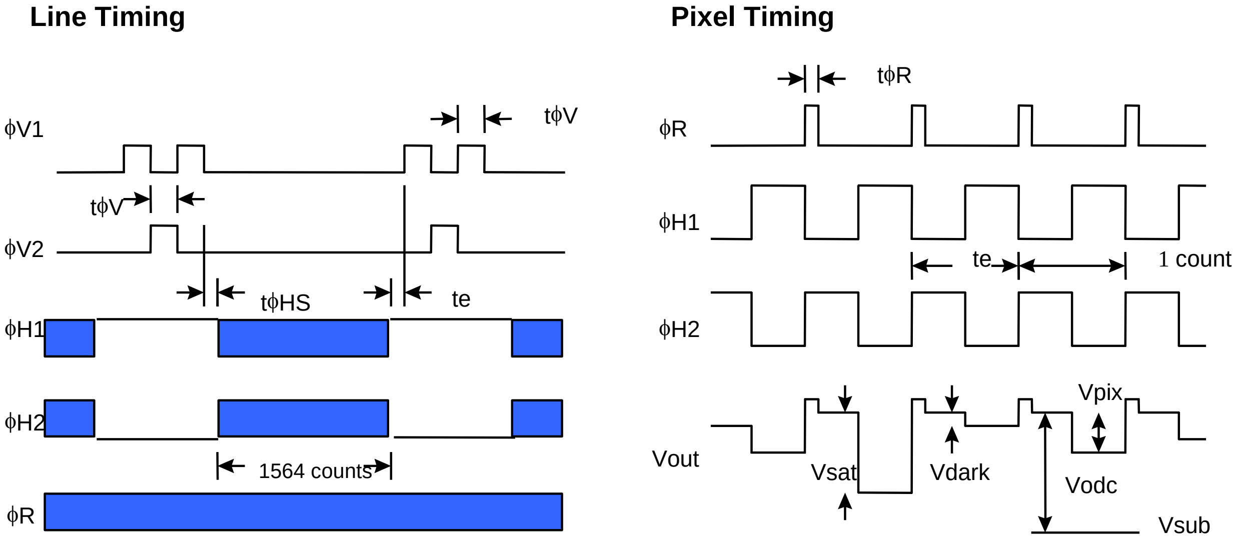


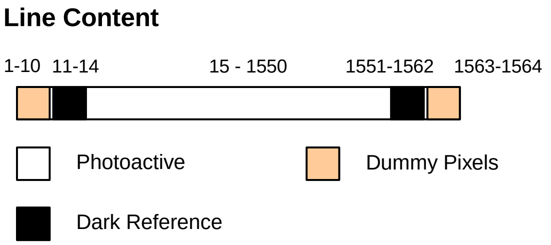
Figure 8: Frame Timing

LINE TIMING (EACH OUTPUT)


Line Timing

Pixel Timing

Figure 9: Line Timing


Line Content

Vsat	Saturated pixel video output
Vdark	Video output signal in no light situation, (Not zero due to Jdark and Hclock feedthrough)
Vpix	Pixel video output signal level, more electrons =less positive*
Vodc	Video level offset with respect to vsub
Vsub	Analog Ground

* See Image Aquisition section

Figure 10: Timing Diagrams

Storage and Handling

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	80	°C	1
Operating Temperature	T_{OP}	-60	60	°C	

Notes:

1. Storage toward the maximum temperature will accelerate color filter degradation.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices.*

ENVIRONMENTAL EXPOSURE

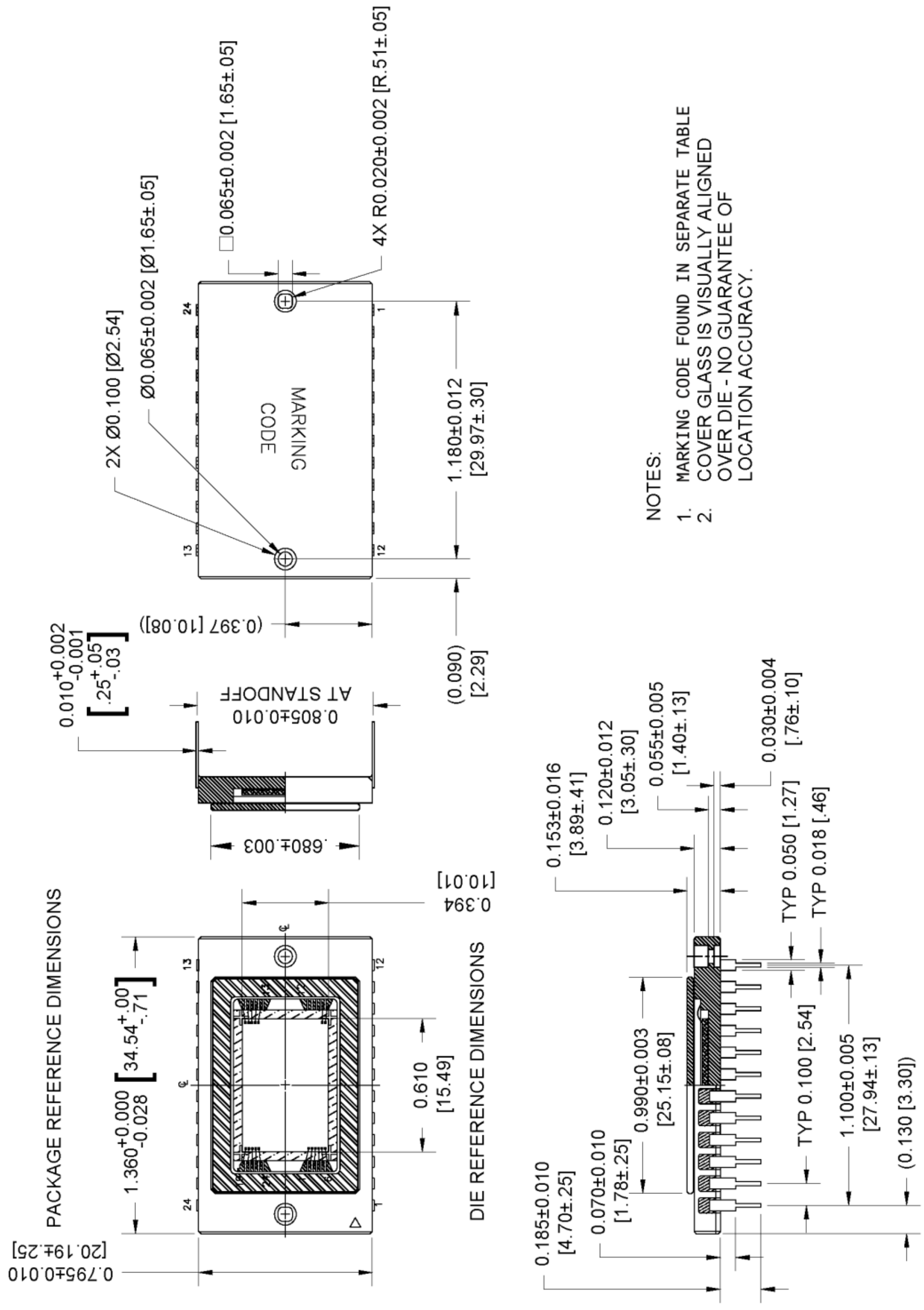
1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

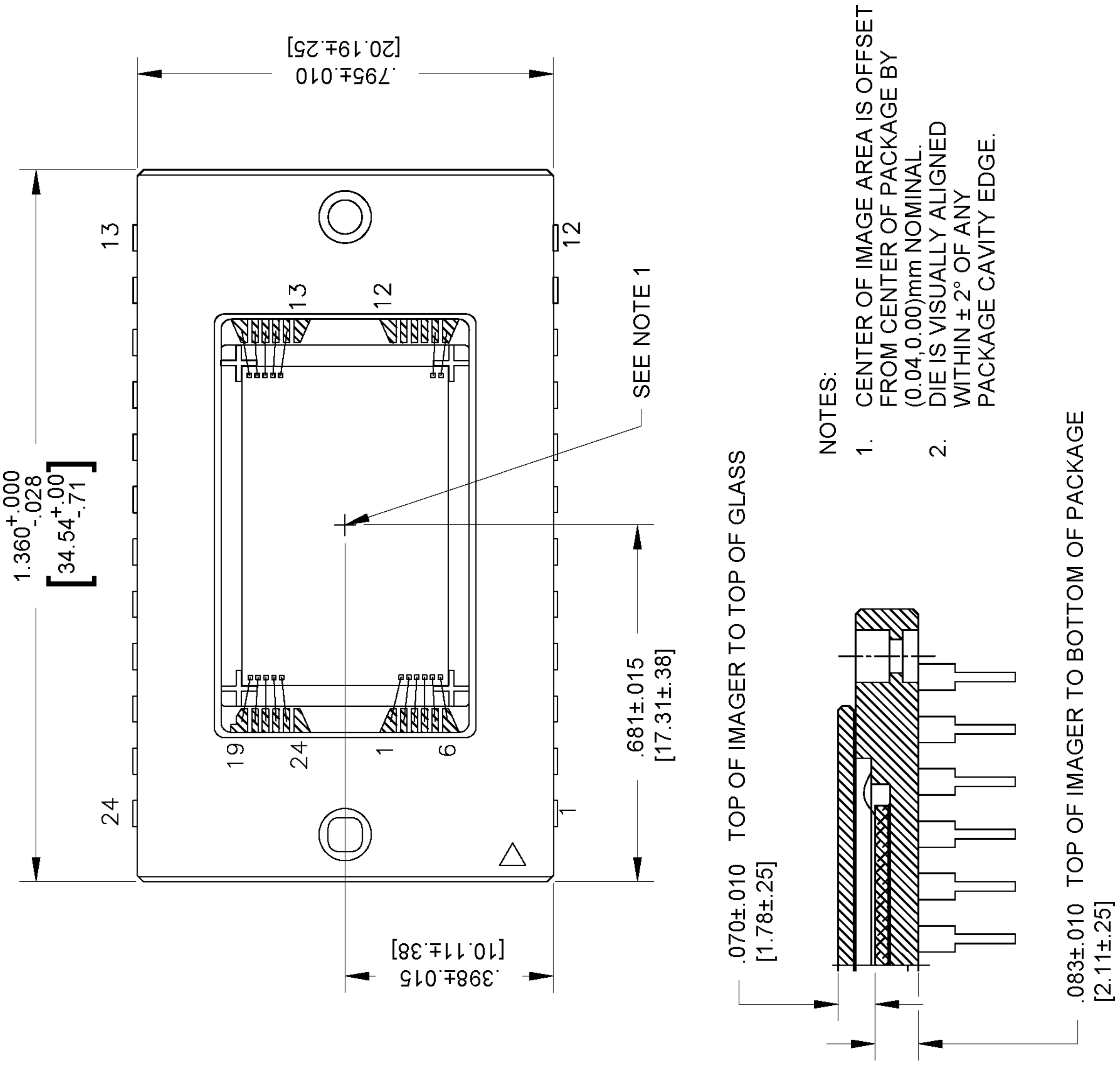
Mechanical Information

COMPLETED ASSEMBLY



NOTES:
1. MARKING CODE FOUND IN SEPARATE TABLE
2. COVER GLASS IS VISUALLY ALIGNED OVER DIE - NO GUARANTEE OF LOCATION ACCURACY.

Figure 11: Completed Assembly (1 of 2)



NOTES:

1. CENTER OF IMAGE AREA IS OFFSET FROM CENTER OF PACKAGE BY (0.04,0.00)mm NOMINAL.
2. DIE IS VISUALLY ALIGNED WITHIN ± 2° OF ANY PACKAGE CAVITY EDGE.

Figure 12: Completed Assembly (2 of 2)

Quality Assurance and Reliability

QUALITY AND RELIABILITY

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

REPLACEMENT

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

LIABILITY OF THE CUSTOMER

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-0666

Revision Number	Description of Changes
1.0	• Initial Release.
2.0	• Remove Grade 3 device option (p9). • Add cover glass configurations (p15). • Update ESD (p10) and Cleanliness (p14) sections.
3.0	• Updated format. Removed part numbers.
3.1	• Correct table headings (p.14).
3.2	• Remove Class 1 parts from the defect specification table
4.0	• Removed part numbers 4H0342 and 4H0344

PS-0036

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections
1.1	• Updated branding

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