

PHKD13N03LT

Dual N-channel TrenchMOS logic level FET

Rev. 5 — 27 December 2011

Product data sheet

1. Product profile

1.1 General description

Dual logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- DC-to-DC convertors
- Lithium-ion battery applications
- Notebook computers
- Portable equipment

1.4 Quick reference data

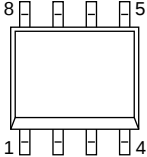
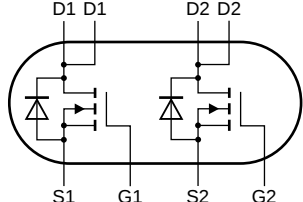
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 150\text{ }^{\circ}\text{C}$	-	-	30	V
I_D	drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; [1] see Figure 3	-	-	10.4	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ }^{\circ}\text{C}$; see Figure 2	-	-	3.57	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 8\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 9 ; see Figure 10	-	17	20	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $V_{DS} = 15\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 11	-	3.9	-	nC

[1] Single device conducting.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 SOT96-1 (SO8)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHKD13N03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

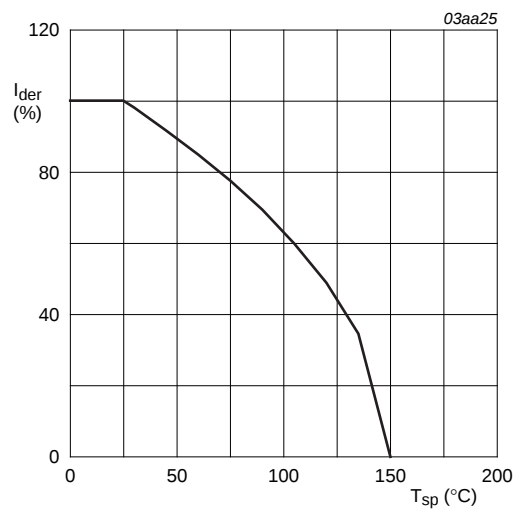
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	30	V	
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 150 °C; R _{GS} = 20 kΩ	-	30	V	
V _{GS}	gate-source voltage		-20	20	V	
I _D	drain current	T _{sp} = 100 °C; V _{GS} = 10 V; see Figure 1	[1]	-	6.6	A
		T _{sp} = 25 °C; V _{GS} = 10 V; see Figure 1 ; see Figure 3	[1]	-	10.4	A
I _{DM}	peak drain current	T _{sp} = 25 °C; pulsed; t _p ≤ 10 μs; see Figure 3	[1]	-	42	A
P _{tot}	total power dissipation	T _{sp} = 25 °C; see Figure 2	-	3.57	W	
T _{stg}	storage temperature		-55	150	°C	
T _j	junction temperature		-55	150	°C	

Source-drain diode

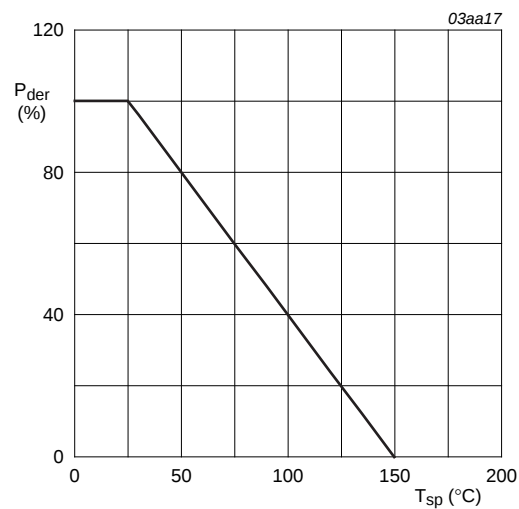
I_S	source current	$T_{sp} = 25\text{ °C}$	[1]	-	3.2	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	[1]	-	42	A

[1] Single device conducting.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature

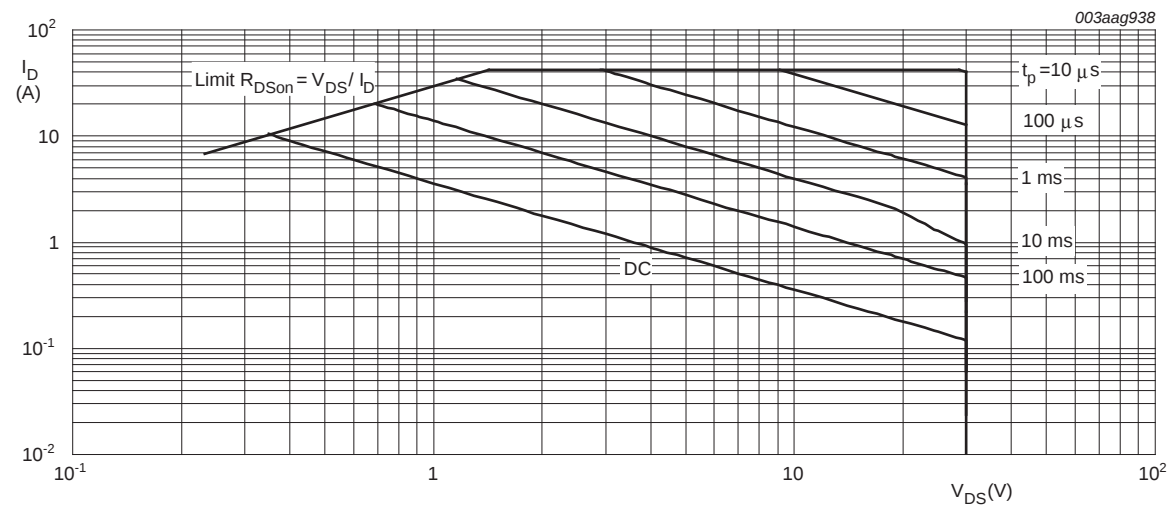


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	35	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	70	-	K/W

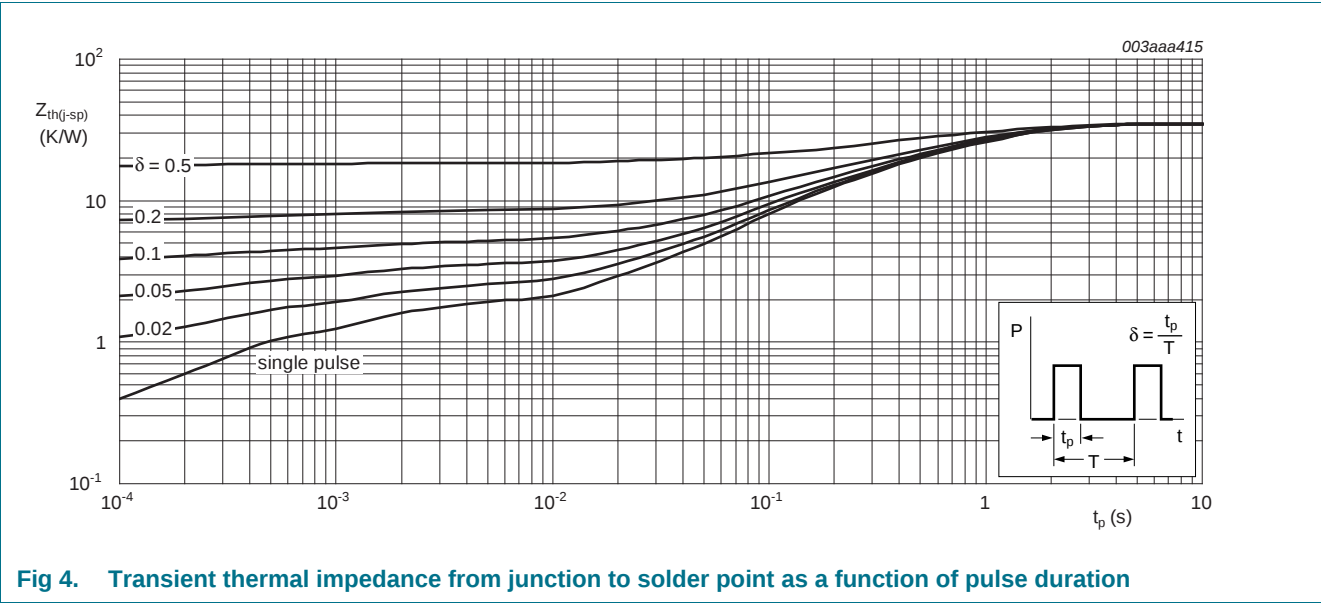


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	27	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 8	-	-	2.2	V
		I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 150 °C; see Figure 8	0.5	-	-	V
		I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 8	1	1.5	2	V
I _{DSS}	drain leakage current	V _{DS} = 24 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μA
		V _{DS} = 24 V; V _{GS} = 0 V; T _j = 100 °C	-	-	5	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 8 A; T _j = 150 °C; see Figure 9 ; see Figure 10	-	-	34	mΩ
		V _{GS} = 4.5 V; I _D = 7 A; T _j = 25 °C; see Figure 9	-	21	26	mΩ
		V _{GS} = 10 V; I _D = 8 A; T _j = 25 °C; see Figure 9 ; see Figure 10	-	17	20	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 15 V; V _{GS} = 5 V; T _j = 25 °C; see Figure 11	-	10.7	-	nC
Q _{GS}	gate-source charge		-	2.7	-	nC
Q _{GD}	gate-drain charge		-	3.9	-	nC
C _{iss}	input capacitance	V _{DS} = 15 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 12	-	752	-	pF
C _{oss}	output capacitance		-	200	-	pF
C _{rss}	reverse transfer capacitance		-	130	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; R _L = 10 Ω; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C; I _D = 1.5 A	-	6	-	ns
t _r	rise time		-	7	-	ns
t _{d(off)}	turn-off delay time		-	23	-	ns
t _f	fall time		-	11	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 7 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 13	-	0.86	1.1	V
t _{rr}	reverse recovery time	I _S = 7 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 30 V; T _j = 25 °C	-	25	-	ns
Q _r	recovered charge	V _{DS} = 30 V; T _j = 25 °C	-	5	-	nC

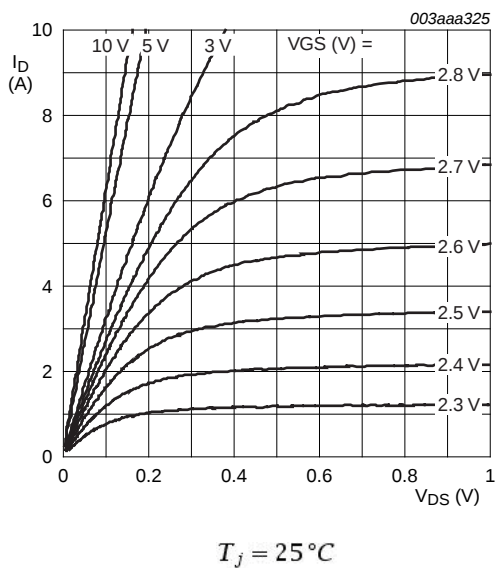


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

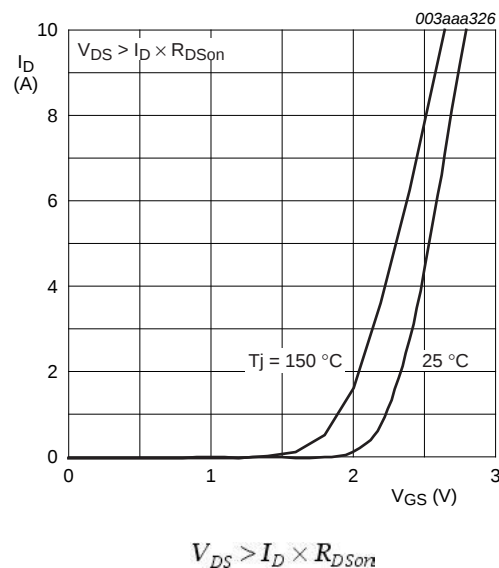


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

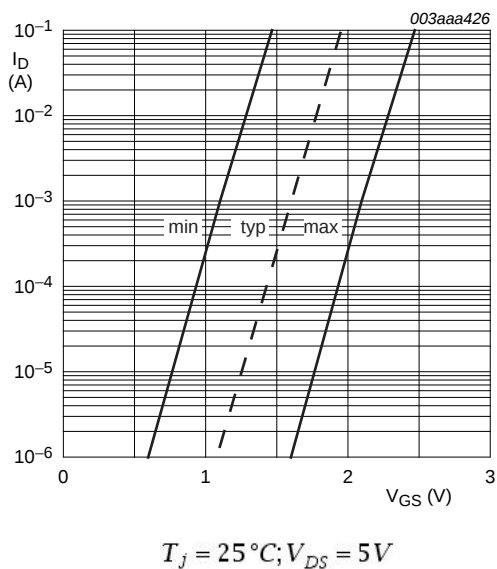


Fig 7. Sub-threshold drain current as a function of gate-source voltage

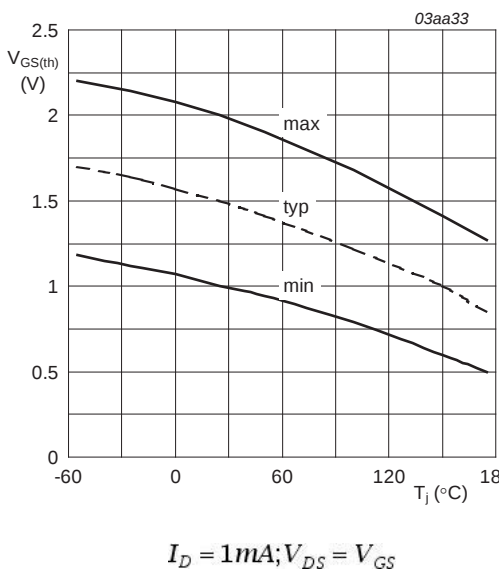
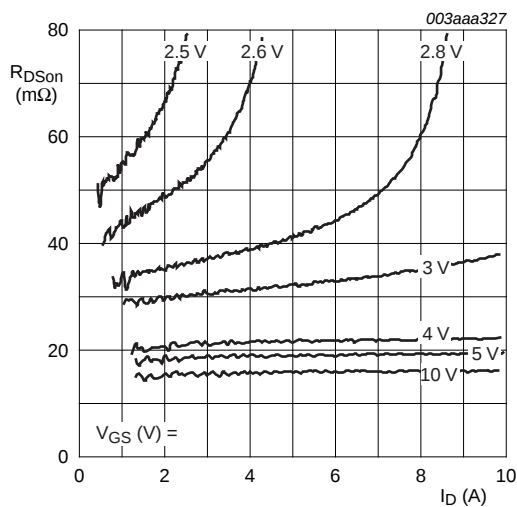
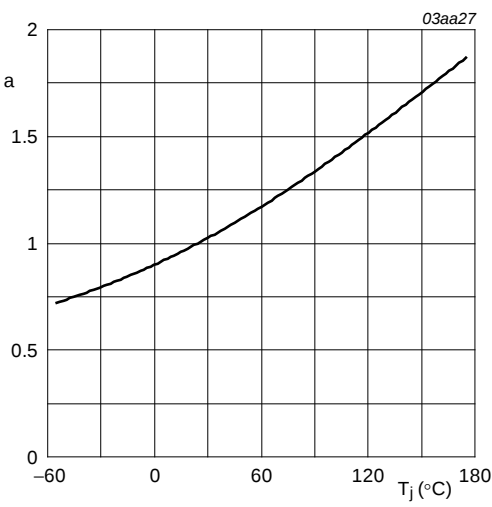


Fig 8. Gate-source threshold voltage as a function of junction temperature



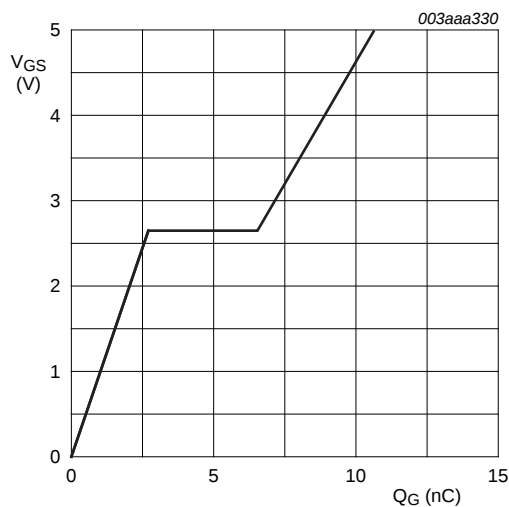
$T_j = 25^\circ C$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



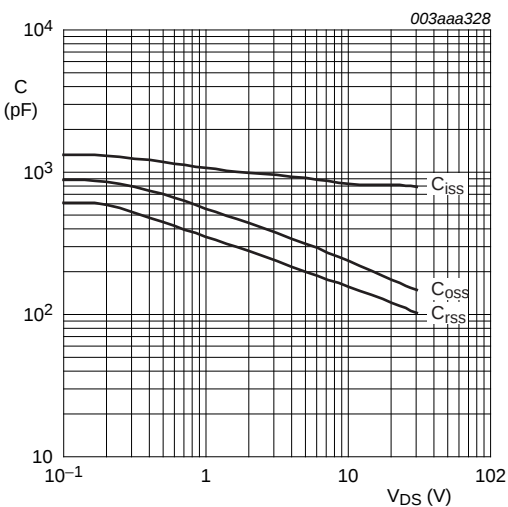
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = 8 A; V_{DD} = 15 V$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 V; f = 1 MHz$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

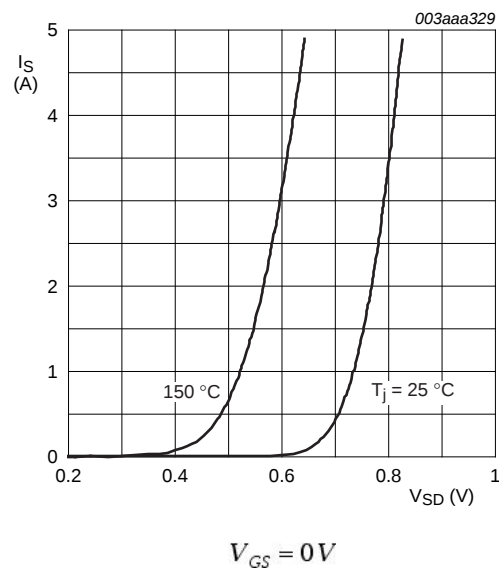


Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1

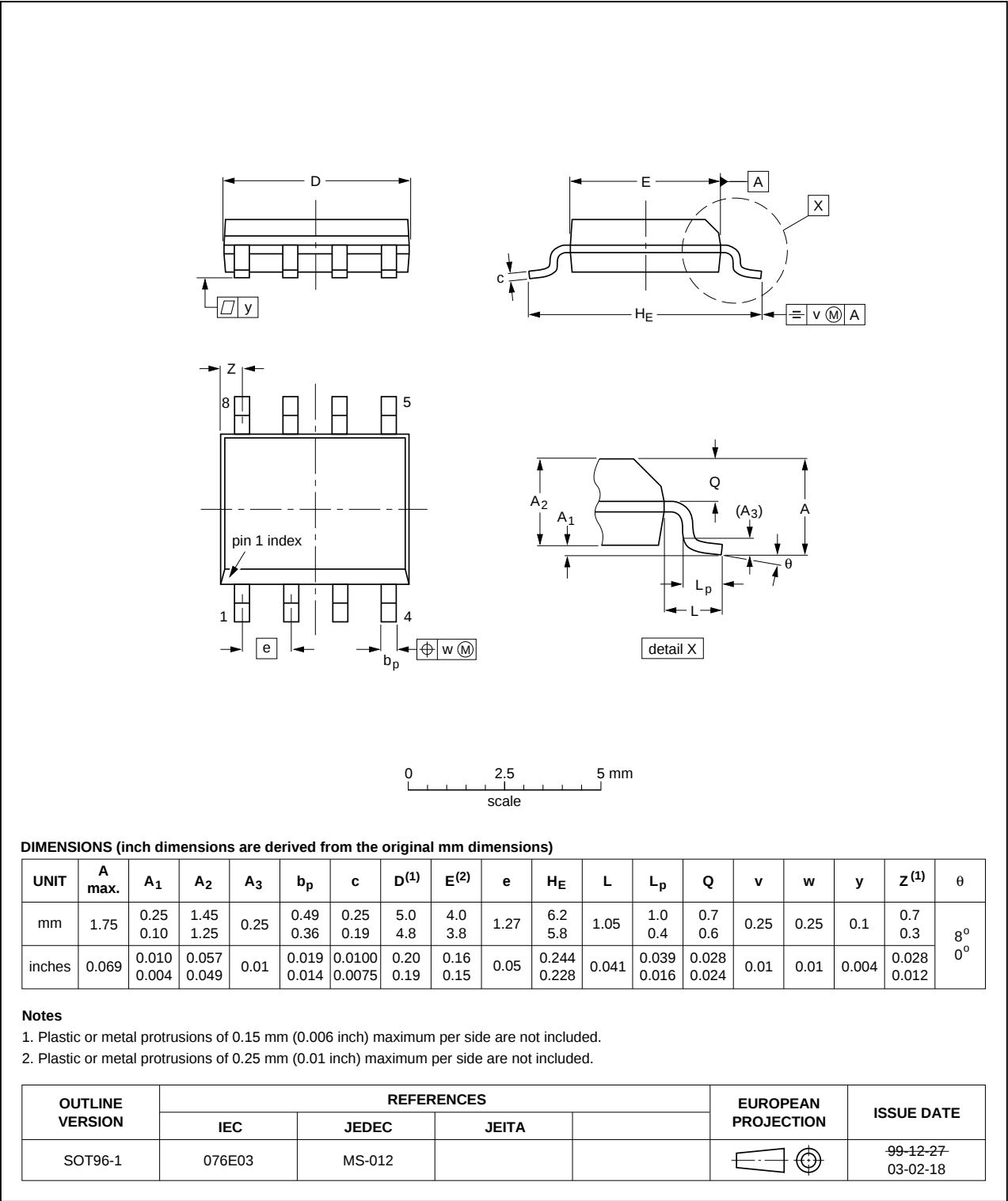


Fig 14. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHKD13N03LT v.5	20111227	Product data sheet	-	PHKD13N03LT v.4
Modifications:	• Various changes to content.			
PHKD13N03LT v.4	20111122	Product data sheet	-	PHKD13N03LT v.3

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	9
8	Revision history	10
9	Legal information	11
9.1	Data sheet status	11
9.2	Definitions	11
9.3	Disclaimers	11
9.4	Trademarks	12
10	Contact information	12

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