Xilinx CoolRunner-II CPLD quick start

From DP

Features

- 1.5volt - 3.3volt IO, 1.8volt core supply required
- Multiple IO banks can be operated at different voltage for level translation
- Compare Xilinx XC9500 and CoolRunner-II
- Unlike most FPGA, CPLDs are static and store their configuration permanently
- Several devices in easy-to-solder TQFP-44 packages
- Available at Digikey, among others

Resources

- CoolRunner-II homepage (http://www.xilinx.com/products/silicon-devices/cpld/coolrunner-ii/index.htm)
- CoolRunner-II CPLD development board hardware design
- XC2C64A CPLD dev-board introduction
- **CoolRunner-II CPLD quick start**
- CoolRunner-II family manual (http://www.xilinx.com/support/documentation/data_sheets/ds090.pdf)
- XC2C64A device datasheet (http://www.xilinx.com/support/documentation/data_sheets/ds311.pdf)
- XC2C32A device datasheet (http://www.xilinx.com/support/documentation/data_sheets/ds310.pdf) (smaller version of XC2C64A used on Bus Blaster v2)

Development and programming

Xilinx has a free FPGA and CPLD development package called ISE WebPack (http://www.xilinx.com/tools/webpack.htm) . This is the only development tool we're aware of.

JTAG cables

CoolRunner-II uses a JTAG programming interface.

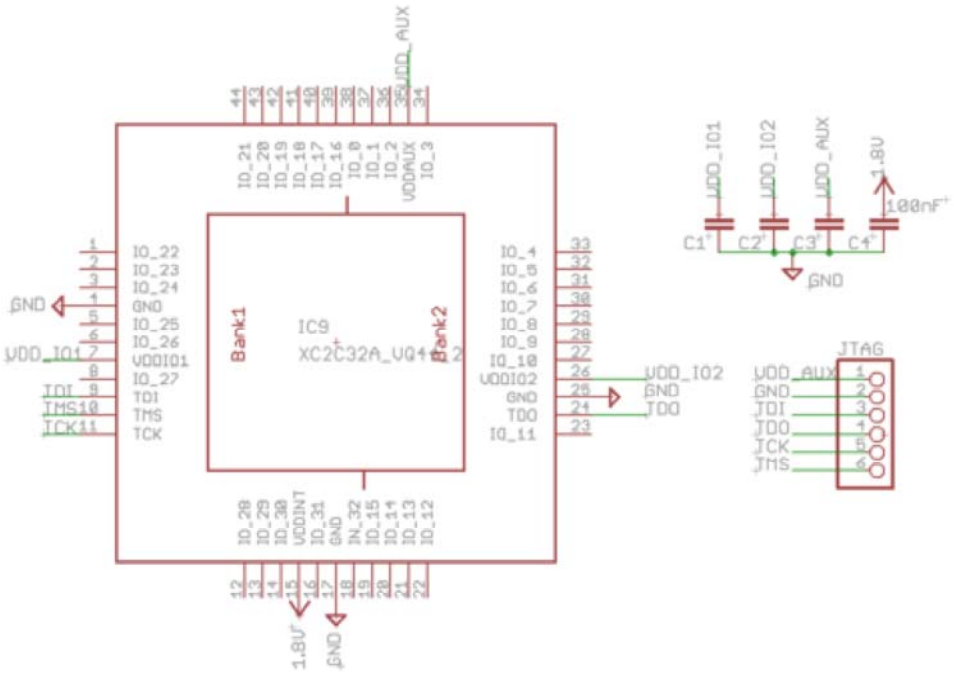
- Parallel cable and ISE
- FT2232 JTAG

Loaders

Load configurations into the CPLD or FPGA by 'playing' an (X)SVF encoded file with a JTAG cable.

- UrJTAG (http://urjtag.sourceforge.net/) - load SVF with a number of programmers, including common FT2232 programmers
- OpenOCD (http://www.openocd.org) - detects FPGA/CPLDs, but doesn't do much with them

Basic circuit



Power

Requires, at minimum, a 1.8volt supply.

- 1.8volts - core supply (VDDINT)
- 1.5volt-3.3volts - auxiliary supply for JTAG interface pins, use your preferred interface voltage (VDDAUX)
- 1.5volts-3.3volts - IO supply for the IO pins, use your preferred interface voltage (VDDIOx)

Reset

There is no default reset pin on the CoolRunner-II, but similar functionality can be programmed.

- GSR pins have an optimized path to the Set/Reset signal of all macrocells. These pins can be used to synchronously reset all the macrocells in the CPLS with minimum extra resource. This feature must be enabled in the CPLD design, or the pins will be normal IO.

JTAG programming connections

6x1 JTAG pinout

Pin	Signal	Direction

1	V+	
2	GND	
3	TCK	Input
4	TDO	Input
5	TDI	Output
6	TMS	Input

Common Xilinx JTAG pinout.

Clock source

A clock source is only required if your design needs it. If you plan to use a clock, connect it to a GCK pin for best results.

- GCK pins are optimized to distribute a clock signal to all macrocells with minimum skew and extra resources. If you plan to use a clock with the CPLD, connect it to one of these pins if possible. The GCK features must be applied in the CPLD design or the GCK pin will be an ordinary IO pin.

Peripherals

IO

- Pin current depends on the power supply and acceptable voltage levels, though roughly 8mA (ideal) to 20mA (acceptable) should be possible
- The chip is divided into banks that each accept an independent supply from 1.5volts to 3.3volts. Feed the supply to the IOx supply pin
- Pins have "bus hold" feature that gently pulls the pin to the current input value (up or down), uses less current than a pull-up resistor
- Bus hold **or** pull-up resistors (not both) can be applied globally to all pins. The bus hold or pull-up can then be disabled on individual pins

There are also some pins with special features, though they are not used unless specifically enabled in the CPLD synthesis:

- GCK (global clock) - optimized to distribute a clock signal to all macrocells with minimum skew and extra resources
- GSR (global set reset) - optimized path to the Set/Reset signal of all macrocells, allows synchronous reset of the flip-flop in all cells with minimum extra resources
- GTS (global tri-state) - optimized to put all CPLD pins in a high impedance state
- More (http://www.xilinx.com/support/answers/3122.htm) , even more (http://www.xilinx.com/itp/xilinx10/isehelp/ise_r_comp_gck_gts_gsr.htm)

Resources

- CPLD development tutorials
- CoolRunner-II primitives (http://www.xilinx.com/itp/xilinx5/data/docs/lib/lib0030_14.html)
- Xilinx CPLDs: XC9500 vs CoolRunner-II

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