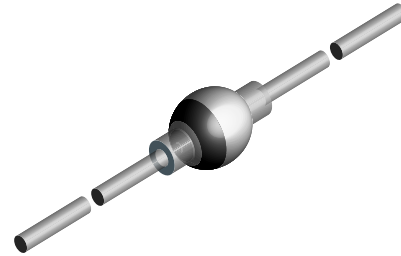


## Standard Sinterglass Diode

### Features

- Cavity-free glass passivated junction
- High temperature metallurgically bonded construction
- Hermetically sealed package
- Medium switching for improved efficiency



17133

### Mechanical Data

**Case:** Sintered glass case, G4

**Terminals:** Solder plated axial leads, solderable per MIL-STD-750, Method 2026

**Polarity:** Color band denotes cathode end

**Mounting Position:** Any

**Weight:** approx. 1040 mg

### Parts Table

| Part   | Type differentiation     | Package |
|--------|--------------------------|---------|
| 1N5550 | $V_{RRM} = 200\text{ V}$ | G-4     |
| 1N5551 | $V_{RRM} = 400\text{ V}$ | G-4     |
| 1N5552 | $V_{RRM} = 600\text{ V}$ | G-4     |

### Absolute Maximum Ratings

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

| Parameter   | Test condition   | Part   | Symbol          | Value         | Unit               |
|---|--|--------|-----------------|---------------|--------------------|
| Reverse voltage = Repetitive peak reverse voltage | see electrical characteristics   | 1N5550 | $V_R = V_{RRM}$ | 200           | V                  |
|   |  | 1N5551 | $V_R = V_{RRM}$ | 400           | V                  |
|   |  | 1N5552 | $V_R = V_{RRM}$ | 600           | V                  |
| Maximum average forward rectified current         | 0.375 " (9.5 mm) lead length at $T_{amb} = 55\text{ }^{\circ}\text{C}$ |        | $I_{F(AV)}$     | 3.0           | A                  |
| Peak forward surge current                        | 8.3 ms single half sine-wave superimposed on rated load (JEDEC Method) |        | $I_{FSM}$       | 100           | A                  |
| Operating and storage temperature range           |  |        | $T_J, T_{STG}$  | - 55 to + 175 | $^{\circ}\text{C}$ |

### Maximum Thermal Resistance

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

| Parameter                                | Test condition | Symbol          | Value | Unit |
|--|----------------|-----------------|-------|------|
| Typical thermal resistance <sup>1)</sup> |                | $R_{\theta JA}$ | 22    | K/W  |
|  |                | $R_{\theta JL}$ | 12    | K/W  |

<sup>1)</sup> Thermal resistance from junction to ambient and from junction to lead at 0.375" (9.5mm) lead length, with both leads mounted between heat sinks.

### Electrical Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

| Parameter                             | Test condition   | Part   | Symbol     | Min | Typ. | Max | Unit          |
|---------------------------------------|--|--------|------------|-----|------|-----|---------------|
| Minimum reverse breakdown voltage     | $I_R = 50\text{ }\mu\text{A}$                                    | 1N5550 | $V_{(BR)}$ | 240 |      |     | V             |
|                                       |  | 1N5551 | $V_{(BR)}$ | 460 |      |     | V             |
|                                       |  | 1N5552 | $V_{(BR)}$ | 660 |      |     | V             |
| Maximum instantaneous forward voltage | $I_F = 9.0\text{ A}$   |        | $V_F$      |     |      | 1.2 | V             |
| Maximum reverse current               | $V_R = V_{RRM}, T_{amb} = 25\text{ }^{\circ}\text{C}$            |        | $I_R$      |     |      | 1.0 | $\mu\text{A}$ |
|                                       | $V_R = V_{RRM}, T_{amb} = 100\text{ }^{\circ}\text{C}$           |        | $I_R$      |     |      | 25  | $\mu\text{A}$ |
| Maximum junction capacitance          | $V_R = 12\text{ V}, f = 1\text{ MHz}$                            | 1N5550 | $C_j$      |     |      | 150 | pF            |
|                                       |  | 1N5551 | $C_j$      |     |      | 120 | pF            |
|                                       |  | 1N5552 | $C_j$      |     |      | 100 | pF            |
| Maximum reverse recovery time         | $I_F = 0.5\text{ A}, I_R = 1.0\text{ A}, I_{rr} = 0.25\text{ A}$ |        | $t_{rr}$   |     |      | 2.0 | $\mu\text{s}$ |

### Typical Characteristics ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

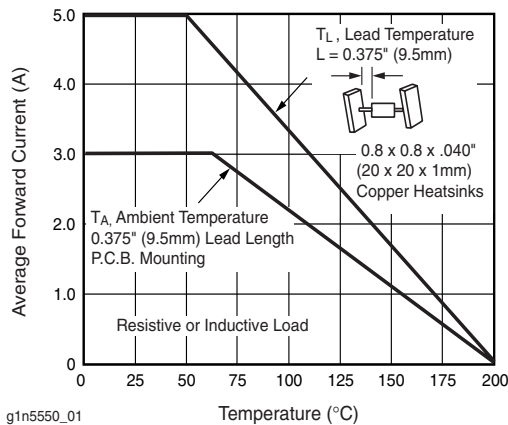


Figure 1. Forward Current Derating Curve

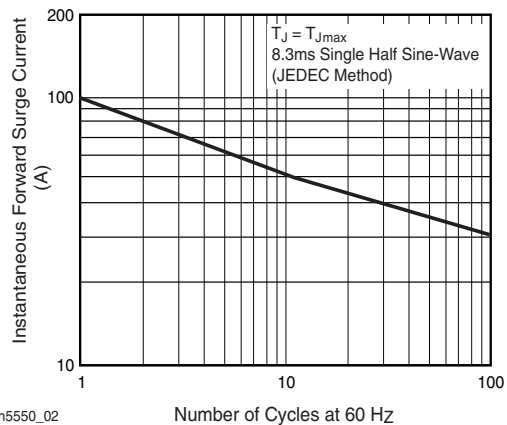


Figure 2. Maximum Non-Repetitive Peak Forward Surge Current

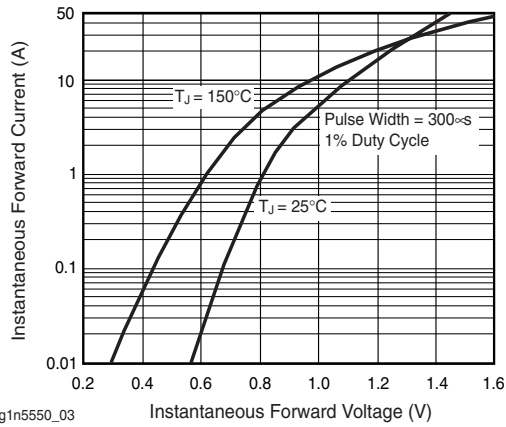


Figure 3. Typical Instantaneous Forward Characteristics

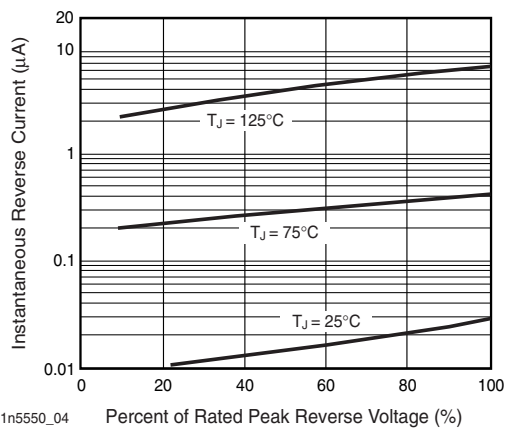


Figure 4. Typical Reverse Characteristics

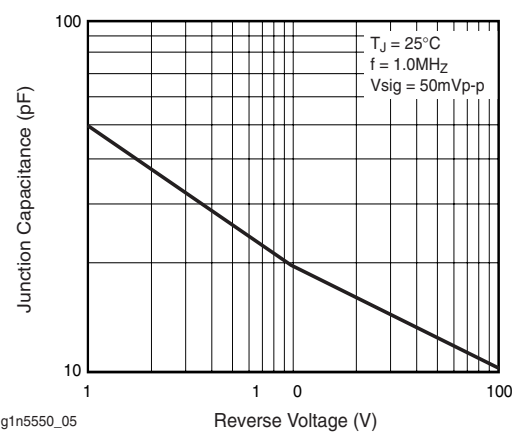


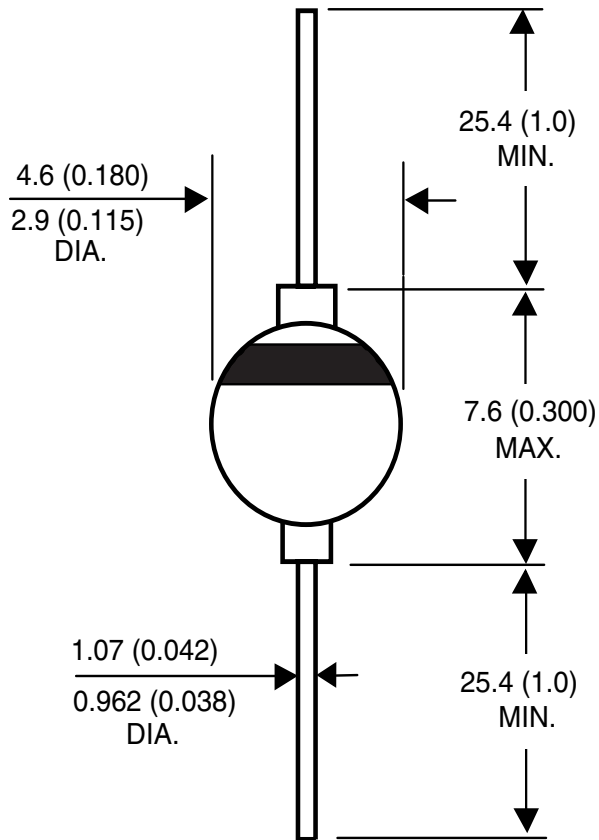
Figure 5. Typical Junction Capacitance

# 1N5550 to 1N5552

Vishay Semiconductors



## Package Dimensions in mm (Inches)



17032



## Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**Vishay Semiconductor GmbH** has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**Vishay Semiconductor GmbH** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

**We reserve the right to make changes to improve technical design  
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