

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications

## **74HC/HCT40105** 4-bit x 16-word FIFO register

Product specification  
Supersedes data of December 1990  
File under Integrated Circuits, IC06

1998 Jan 23

## 4-bit x 16-word FIFO register

## 74HC/HCT40105

## FEATURES

- Independent asynchronous inputs and outputs
- Expandable in either direction
- Reset capability
- Status indicators on inputs and outputs
- 3-state outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT40105 are high-speed Si-gate CMOS devices and are pin compatible with the "40105" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40105 are first-in/first-out (FIFO) "elastic" storage registers that can store sixteen 4-bit words. The "40105" is capable of handling input and output data at

different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripples through to the output end, the status of the first control flip-flop (data-in ready output - DIR) indicates if the FIFO is full, and the status of the last flip-flop (data-out ready output - DOR) indicates if the FIFO contains data. As the earliest data is removed from the bottom of the data stack (output end), all data entered later will automatically ripple toward the output.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay MR to DIR, DOR $\overline{S}O$ to Q <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	16	15	ns
			37	35	ns
t <sub>PHL</sub>	propagation delay SI to DIR $\overline{S}O$ to DOR		16	18	ns
			17	18	ns
f <sub>max</sub>	maximum clock frequency		33	31	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	134	145	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz.

f<sub>o</sub> = output frequency in MHz.

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5

# 4-bit x 16-word FIFO register

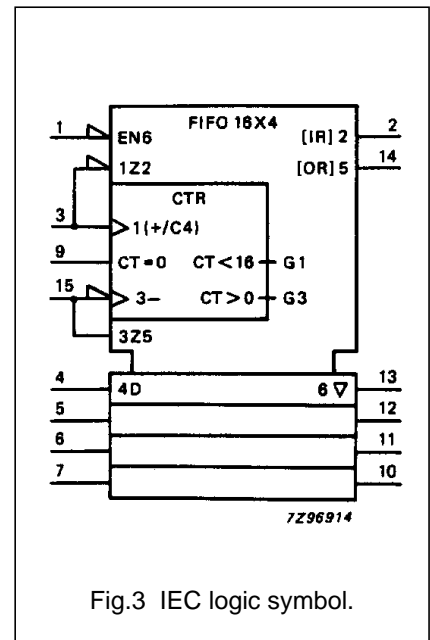
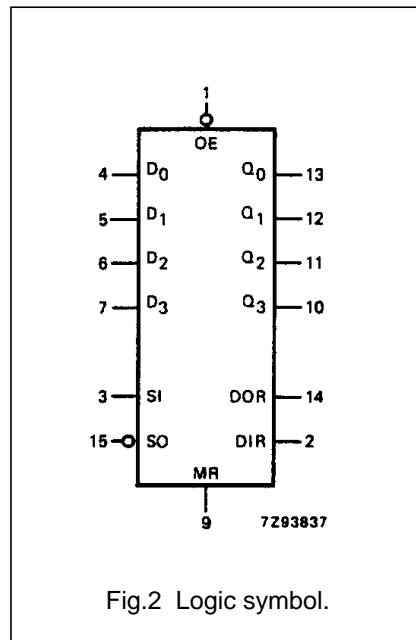
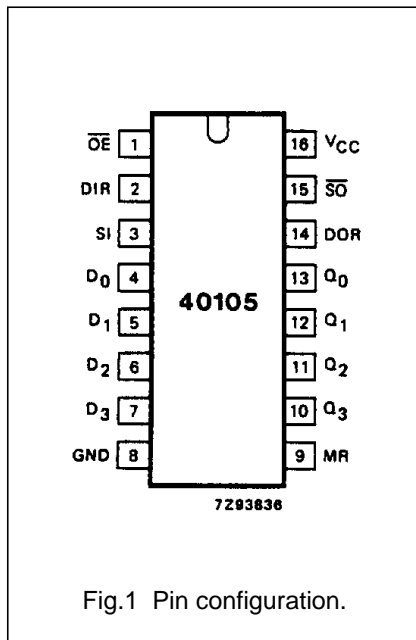
# 74HC/HCT40105

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
74HC(T)40105N	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC(T)40105D	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC(T)40105DB	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC(T)40105PW	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2	DIR	data-in ready output
3	SI	shift-in input (LOW-to-HIGH, edge-triggered)
4, 5, 6, 7	D <sub>0</sub> to D <sub>3</sub>	parallel data inputs
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
13, 12, 11, 10	Q <sub>0</sub> to Q <sub>3</sub>	3-state data outputs
14	DOR	data-out ready output
15	$\overline{SO}$	shift-out input (HIGH-to-LOW, edge-triggered)
16	V <sub>CC</sub>	positive supply voltage



## 4-bit x 16-word FIFO register

## 74HC/HCT40105

### INPUT AND OUTPUTS

#### Data inputs (D<sub>0</sub> to D<sub>3</sub>)

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 × 16 configuration, i.e. 3 × 16, down to 1 × 16, by tying unused data input pins to V<sub>CC</sub> or GND.

#### Data outputs (Q<sub>0</sub> to Q<sub>3</sub>)

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 × 16 configuration as described for data inputs. In a reduced format, the unused data outputs pins must be left open circuit.

#### Master-reset (MR)

When MR is HIGH, the control functions within the FIFO are cleared, and data content is declared invalid. The data-in ready (DIR) flag is set HIGH and the data-out-ready (DOR) flag is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

#### Status flag outputs (DIR, DOR)

Indication of the status of the FIFO is given by two status flags, data-in-ready (DIR) and data-out-ready (DOR):

DIR = HIGH indicates the input stage is empty and ready to accept valid data;

DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete (busy);

DOR = HIGH assures valid data is present at the outputs Q<sub>0</sub> to Q<sub>3</sub> (does not indicate that new data is awaiting transfer into the output stage);

DOR = LOW indicates the output stage is busy or there is no valid data.

#### Shift-in control (SI)

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. It also triggers an automatic data transfer process (ripple through). If SI is held HIGH during reset, data will be loaded at the falling edge of the MR signal.

#### Shift-out control ( $\overline{SO}$ )

A HIGH-to-LOW transition of  $\overline{SO}$  causes the DOR flags to go LOW. A HIGH-to-LOW transition of  $\overline{SO}$  causes upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

#### Output enable ( $\overline{OE}$ )

The outputs Q<sub>0</sub> to Q<sub>3</sub> are enabled when  $\overline{OE}$  = LOW. When  $\overline{OE}$  = HIGH the outputs are in the high impedance OFF-state.

### FUNCTIONAL DESCRIPTION

#### Data input

Following power-up, the master-reset (MR) input is pulsed HIGH to clear the FIFO memory (see Fig.8). The data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D<sub>0</sub> to D<sub>3</sub> can be shifted-in using the SI control input. With SI = HIGH, data is shifted into the input stage and a busy indication is given by DIR going LOW.

The data remains at the first location in the FIFO until DIR is set to HIGH and data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full (see Fig.6). The SI use must be made

LOW in order to complete the shift-in process.

With the FIFO full, SI can be held HIGH until a shift-out ( $\overline{SO}$ ) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in. This remains at the first FIFO location until SI goes LOW (see Fig.7).

#### Data transfer

After data has been transferred from the input stage of the FIFO following SI = LOW, data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as data moves through the device.

#### Data output

The data-out-ready flag (DOR = HIGH) indicates that there is valid data at the output (Q<sub>0</sub> to Q<sub>3</sub>). The initial master-reset at power-on (MR = HIGH) sets DOR to LOW (see Fig.8). After MR = LOW, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH.

As the DOR flag goes HIGH, data can be shifted-out using the  $\overline{SO}$  = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When  $\overline{SO}$  is made LOW, data moves through the FIFO to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted-out leaving the FIFO empty the DOR flag remains LOW (see Fig.9). With the FIFO empty, the last word that was shifted-out is latched at the output Q<sub>0</sub> to Q<sub>3</sub>.

With the FIFO empty, the  $\overline{SO}$  input can be held HIGH until the SI control input is used. Following an SI pulse,

---

## 4-bit x 16-word FIFO register

## 74HC/HCT40105

---

data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and a shift-out of data occurring. The  $\overline{SO}$  control must be made LOW before additional data can be shifted-out (see Fig.10).

### High-speed burst mode

If it is assumed that the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the shift-in/shift-out rates are determined by the status flags. However, without the status flags a high-speed burst mode can be implemented. In this mode, the burst-in/ burst-out rates are determined by the pulse widths of the shift-in/shift-out inputs and burst rates of 35 MHz can be obtained. Shift

pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed (see Figs 11 and 12).

### Expanded format

With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Fig.17). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flag outputs. If during application, the following occurs:

- SI is held HIGH when the FIFO is empty, some additional logic is required to produce a composite DIR pulse (see Figs 7 and 18).

Due to the part-to-part spread of the ripple through time, the SI signals of FIFO<sub>A</sub> and FIFO<sub>B</sub> will not always coincide and the AND-gate will not produce a composite flag signal. The solution is given in Fig.18.

The "40105" is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs. The intercommunication speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 32-words × 4-bits (see Fig.19).

4-bit x 16-word FIFO register

74HC/HCT40105

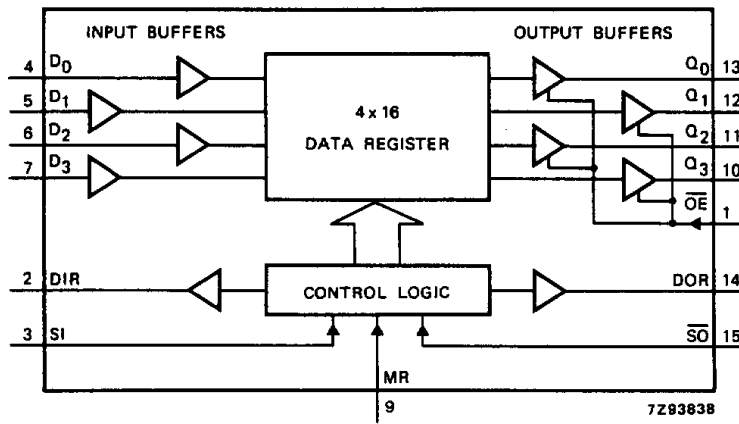
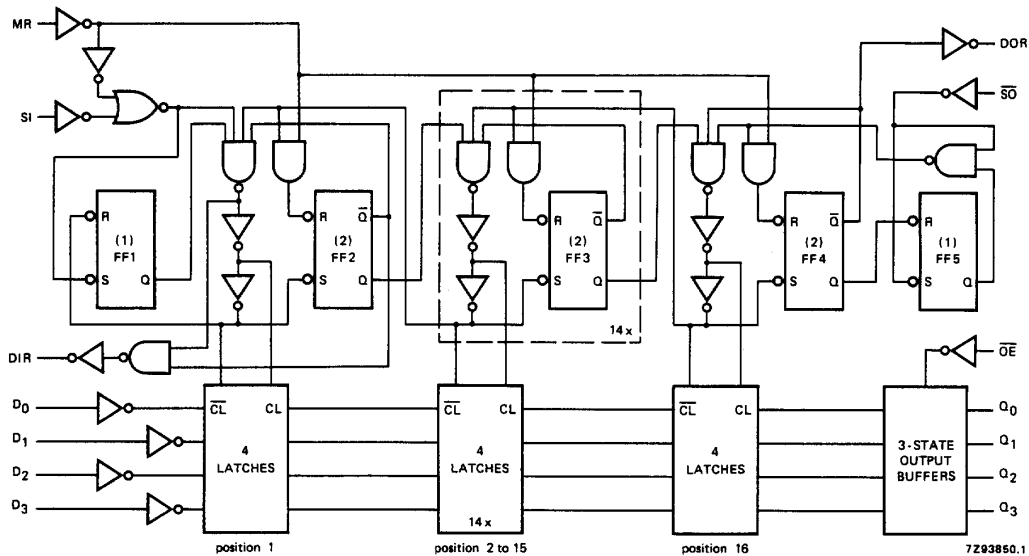


Fig.4 Functional diagram.



(see control flip-flops)

- (1) LOW on  $\bar{S}$  input of FF1, and FF5 will set Q output to HIGH independent of state on  $\bar{R}$  input.
- (2) LOW on  $\bar{R}$  input of FF2, FF3 and FF4 will set Q output to LOW independent of state on  $\bar{S}$  input.

Fig.5 Logic diagram.

## 4-bit x 16-word FIFO register

## 74HC/HCT40105

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay MR to DIR, DOR		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.8	
t <sub>PHL</sub>	propagation delay SI to DIR		52 19 15	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.6	
t <sub>PHL</sub>	propagation delay S <sub>O</sub> to DOR		55 20 16	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.9	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>O</sub> to Q <sub>n</sub>		116 42 34	400 80 68		500 100 85		600 120 102	ns	2.0 4.5 6.0	Fig.14	
t <sub>PLH</sub>	propagation delay/ ripple through delay SI to DOR		564 205 165	2000 400 340		2500 500 425		3000 600 510	ns	2.0 4.5 6.0	Fig.10	
t <sub>PLH</sub>	propagation delay/ bubble-up delay S <sub>O</sub> to DIR		701 255 204	2500 500 425		3125 625 532		3750 750 638	ns	2.0 4.5 6.0	Fig.7	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time O <sub>E</sub> to Q <sub>n</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.16	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time O <sub>E</sub> to Q <sub>n</sub>		41 15 12	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.16	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.14	
t <sub>w</sub>	SI pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6	

4-bit x 16-word FIFO register

74HC/HCT40105

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>w</sub>	$\overline{SO}$ pulse width HIGH or LOW	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig.9
t <sub>w</sub>	DIR pulse width HIGH	12 6 5	58 21 17	180 36 31	10 5 4	225 45 38	10 5 4	270 54 46	ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	DOR pulse width LOW	12 6 5	55 20 16	170 34 29	10 5 4	215 43 37	10 5 4	255 51 43	ns	2.0 4.5 6.0	Fig.9
t <sub>w</sub>	MR pulse width HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>rem</sub>	removal time MR to SI	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.15
t <sub>su</sub>	set-up time D <sub>n</sub> to SI	-5 -5 -5	-39 -14 -11		-5 -5 -5		-5 -5 -5		ns	2.0 4.5 6.0	Fig.13
t <sub>h</sub>	hold time D <sub>n</sub> to SI	125 25 21	44 16 13		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig.13
f <sub>max</sub>	maximum pulse frequency SI, $\overline{SO}$ using flags or burst mode	3.6 18 21	10 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Fig.6, 9, 11 and 12
f <sub>max</sub>	maximum pulse frequency SI, $\overline{SO}$ cascaded	3.6 18 21	10 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 6 and 9



## 4-bit x 16-word FIFO register

## 74HC/HCT40105

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	0.75
SI	0.40
D <sub>n</sub>	0.30
MR	1.50
$\overline{SO}$	0.40

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>f</sub> = t<sub>r</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay MR to DIR, DOR		18	35		44		53	ns	4.5	Fig.8	
t <sub>PHL</sub>	propagation delay SI to DIR		21	42		53		63	ns	4.5	Fig.6	
t <sub>PHL</sub>	propagation delay $\overline{SO}$ to DOR		20	42		53		63	ns	4.5	Fig.9	
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay $\overline{SO}$ to Q <sub>n</sub>		40	80		100		120	ns	4.5	Fig.14	
t <sub>PLH</sub>	propagation delay/ ripple through delay SI to DOR		188	400		500		600	ns	4.5	Fig.10	
t <sub>PLH</sub>	propagation delay/ bubble-up delay $\overline{SO}$ to DIR		244	500		625		750	ns	4.5	Fig.7	
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Q <sub>n</sub>		18	35		44		53	ns	4.5	Fig.16	
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Q <sub>n</sub>		15	30		38		45	ns	4.5	Fig.16	
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.14	

## 4-bit x 16-word FIFO register

## 74HC/HCT40105

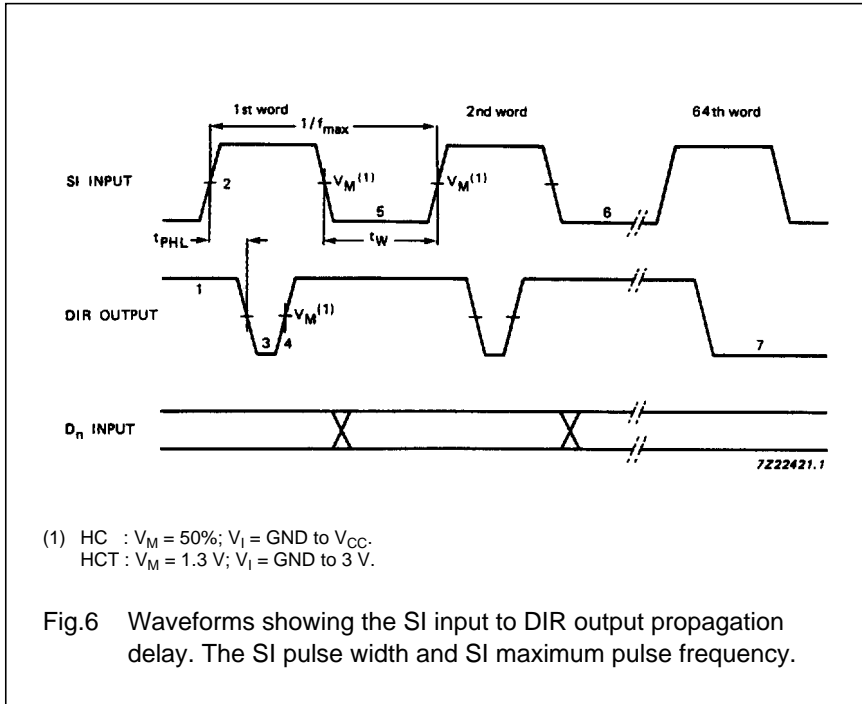
SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>W</sub>	SI pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig.6
t <sub>W</sub>	$\overline{\text{SO}}$ pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.9
t <sub>W</sub>	DIR pulse width HIGH or LOW	6	20	34	5	43	5	51	ns	4.5	Fig.7
t <sub>W</sub>	DOR pulse width HIGH or LOW	6	19	34	5	43	5	51	ns	4.5	Fig.9
t <sub>W</sub>	MR pulse width HIGH	16	7		20		24		ns	4.5	Fig.8
t <sub>rem</sub>	removal time MR to SI	15	7		19		22		ns	4.5	Fig.15
t <sub>su</sub>	set-up time D <sub>n</sub> to SI	-5	-14		-4		-4		ns	4.5	Fig.13
t <sub>h</sub>	hold time D <sub>n</sub> to SI	27	16		34		41		ns	4.5	Fig.13
f <sub>max</sub>	maximum pulse frequency SI, $\overline{\text{SO}}$ using flags or burst mode		28		12		10		MHz	4.5	Fig.6, 9, 11 and 12
f <sub>max</sub>	maximum pulse frequency SI, $\overline{\text{SO}}$ cascaded		28		12		10		MHz	4.5	Figs 6 and 9

4-bit x 16-word FIFO register

74HC/HCT40105

AC WAVEFORMS

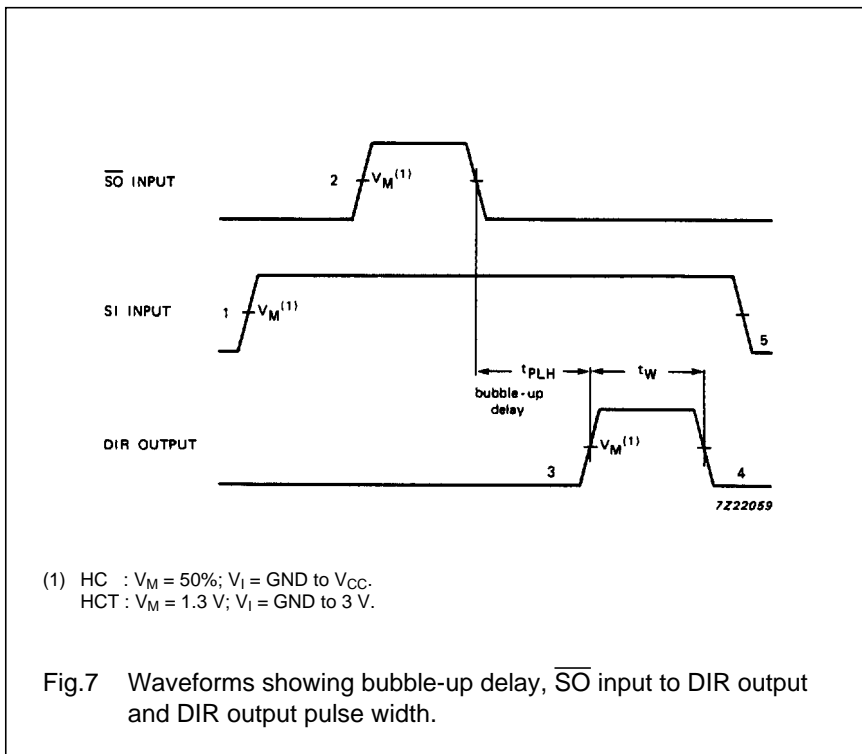
Shifting in sequence FIFO empty to FIFO full



Notes to Fig.6

1. DIR initially HIGH; FIFO is prepared for valid data.
2. SI set HIGH; data loaded into input stage.
3. DIR drops LOW, input stage "busy".
4. DIR goes HIGH, status flag indicates FIFO prepared for additional data; data from first location "ripple through".
5. SI set LOW; necessary to complete shift-in process.
6. Repeat process to load 2nd word through to 16th word into FIFO.
7. DIR remains LOW: with attempt to shift into full FIFO, no data transfer occurs.

With FIFO full; SI held HIGH in anticipation of empty location



Notes to Fig.7

1. FIFO is initially, shift-in is held HIGH.
2.  $\overline{SO}$  pulse; data in the output stage is unloaded, "bubble-up process of empty locations begins".
3. DIR HIGH; when empty location reached input stage, flag indicates FIFO is prepared for data input.
4. DIR returns to LOW; FIFO is full again.
5. SI brought LOW; necessary to complete whidt-in process, DIR remains LOW, because FIFO is full.

4-bit x 16-word FIFO register

74HC/HCT40105

Master reset applied with FIFO full

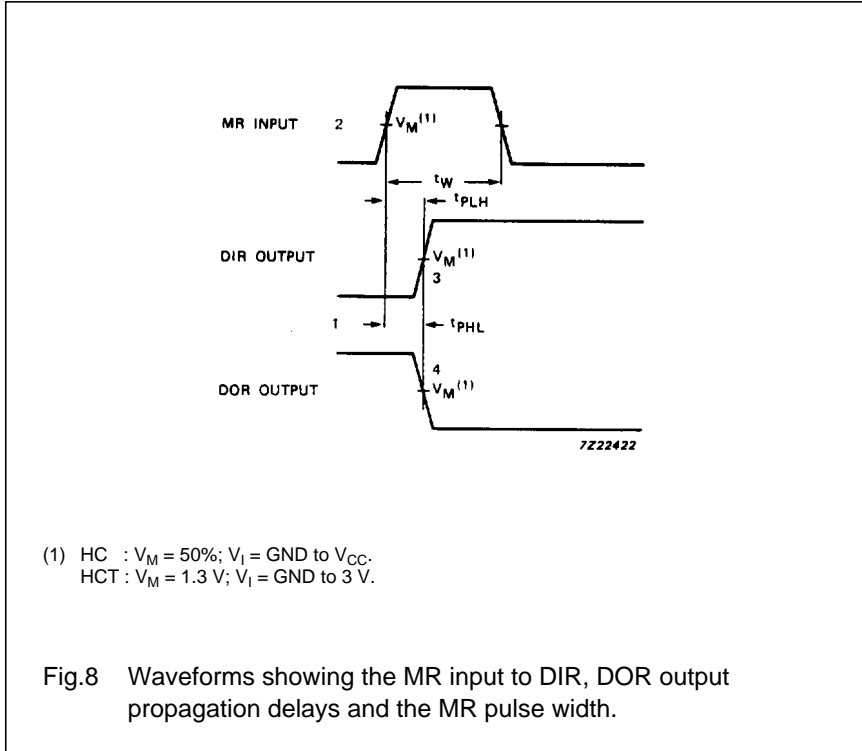


Fig.8 Waveforms showing the MR input to DIR, DOR output propagation delays and the MR pulse width.

Notes to Fig.8

1. DIR LOW, output ready HIGH; assume FIFO is full.
2. MR pulse HIGH; clears FIFO.
3. DIR goes HIGH; flag indicates input prepared for valid data.
4. DOR drops LOW; flag indicates FIFO empty.

Shifting out sequence; FIFO full to FIFO empty

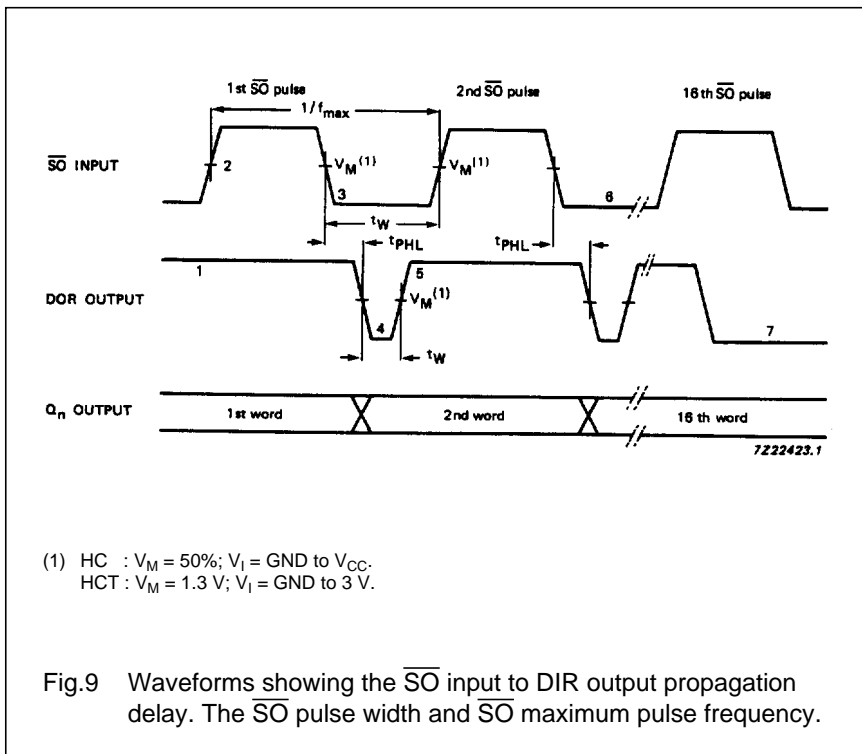


Fig.9 Waveforms showing the  $\overline{SO}$  input to DIR output propagation delay. The  $\overline{SO}$  pulse width and  $\overline{SO}$  maximum pulse frequency.

Notes to Fig.9

1. DOR HIGH; no data transfer in progress, valid data is present at output stage.
2.  $\overline{SO}$  set HIGH.
3.  $\overline{SO}$  is set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage.
4. DOR drops LOW; output stage "busy".
5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay.
6. Repeat process to unloaded the 3rd through to the 16th word from FIFO.
7. DOR remains LOW; FIFO is empty.

4-bit x 16-word FIFO register

74HC/HCT40105

With FIFO empty;  $\overline{SO}$  is held HIGH in anticipation

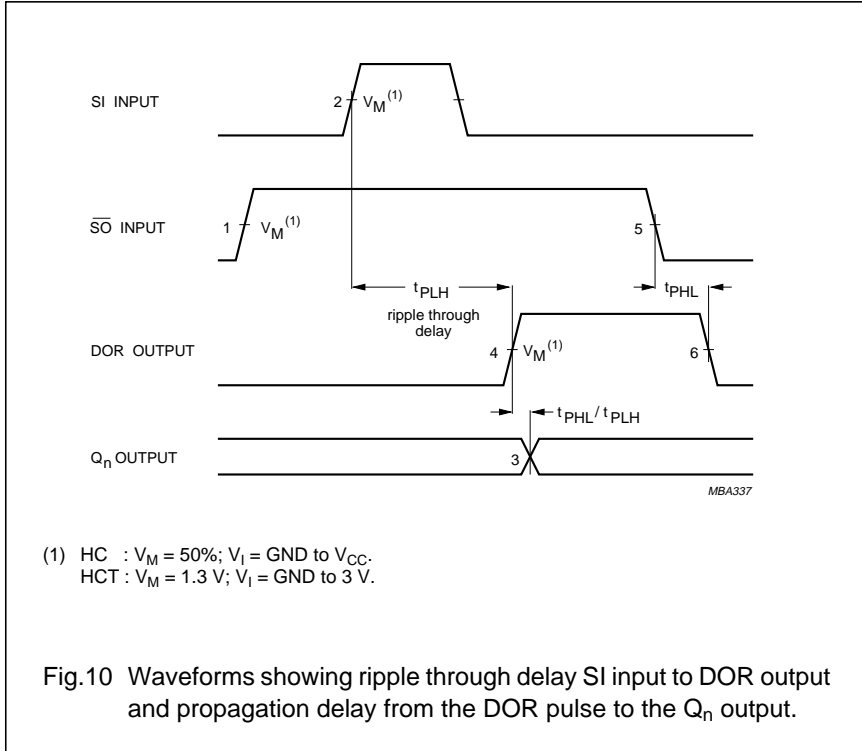


Fig.10 Waveforms showing ripple through delay SI input to DOR output and propagation delay from the DOR pulse to the  $Q_n$  output.

Notes to Fig.10

1. FIFO is initially empty,  $\overline{SO}$  is held HIGH.
2. SI pulse; loads data into FIFO and initiates ripple through process.
3. DOR flag signals the arrival of valid data at the output stage.
4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the  $Q_n$  output.
5.  $\overline{SO}$  set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.
6. DOR goes LOW; FIFO is empty again.

Shift-in operation; high-speed burst mode

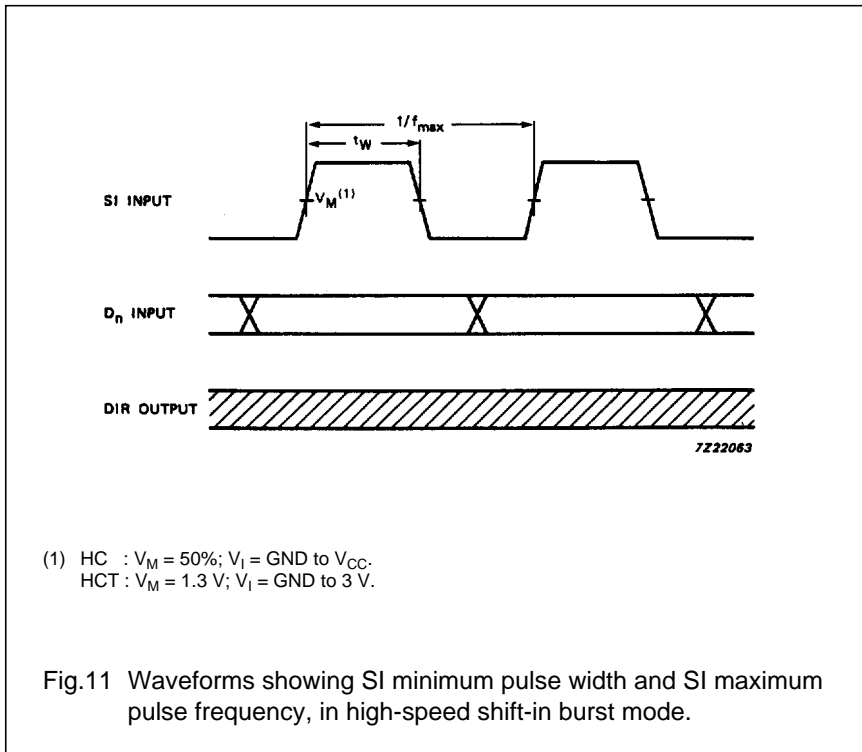


Fig.11 Waveforms showing SI minimum pulse width and SI maximum pulse frequency, in high-speed shift-in burst mode.

Note to Fig.11

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

4-bit x 16-word FIFO register

74HC/HCT40105

Shift-out operation; high-speed burst mode

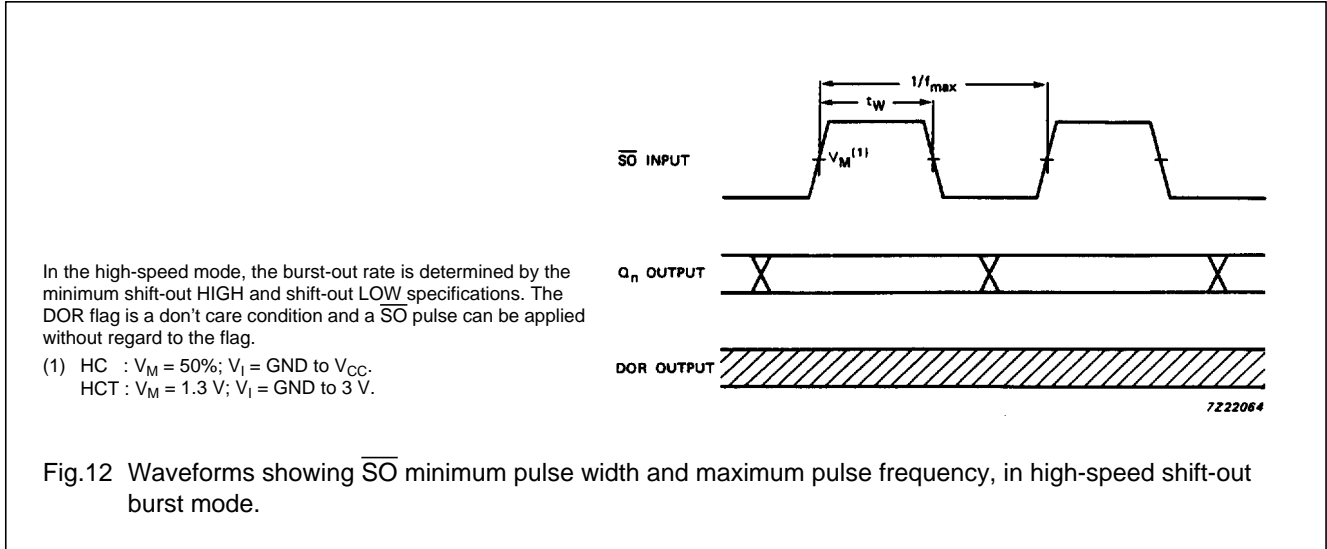


Fig.12 Waveforms showing  $\overline{SO}$  minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.

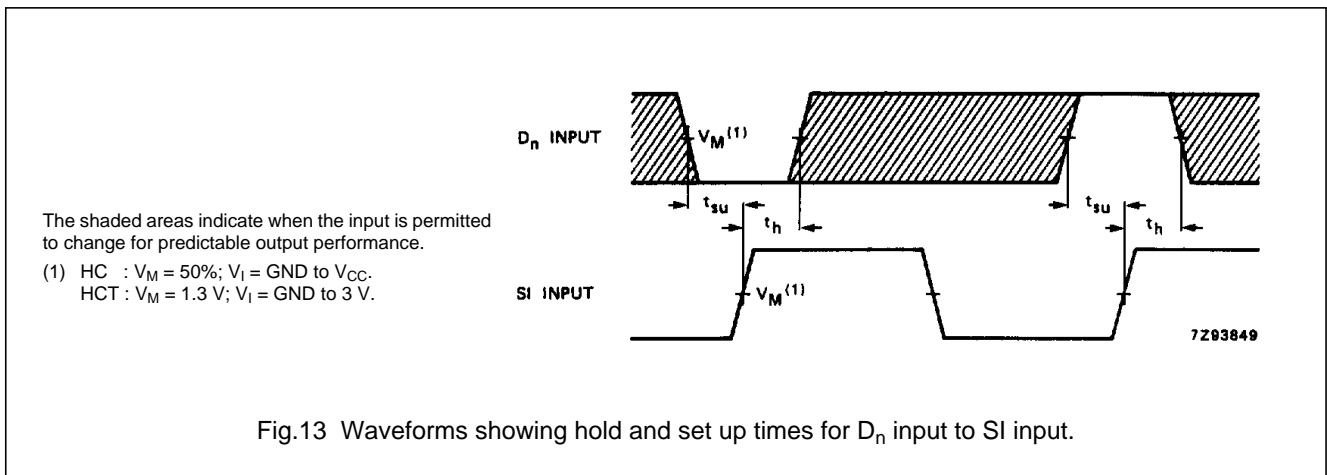


Fig.13 Waveforms showing hold and set up times for  $D_n$  input to  $SI$  input.

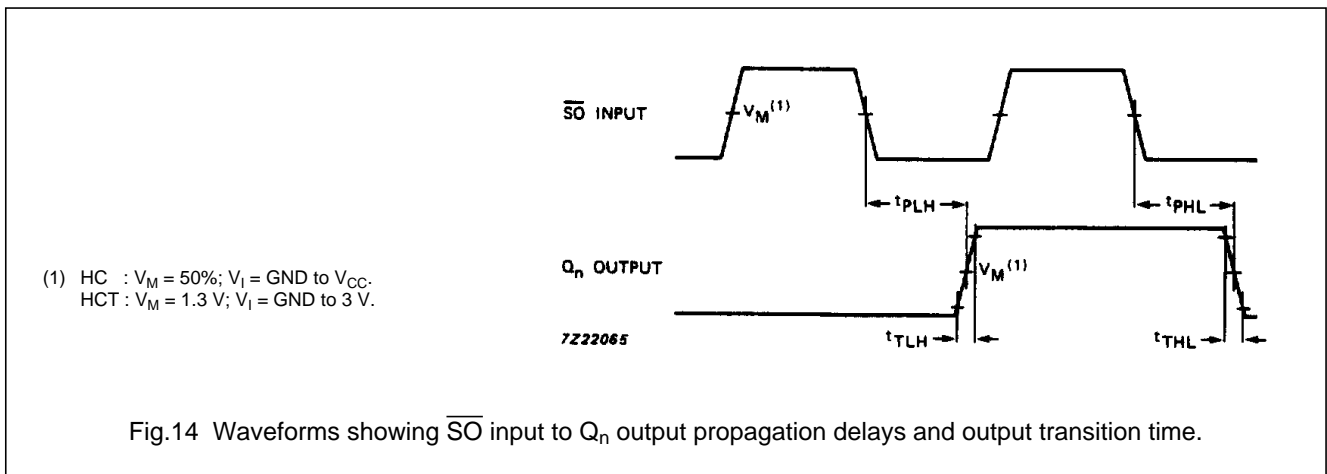
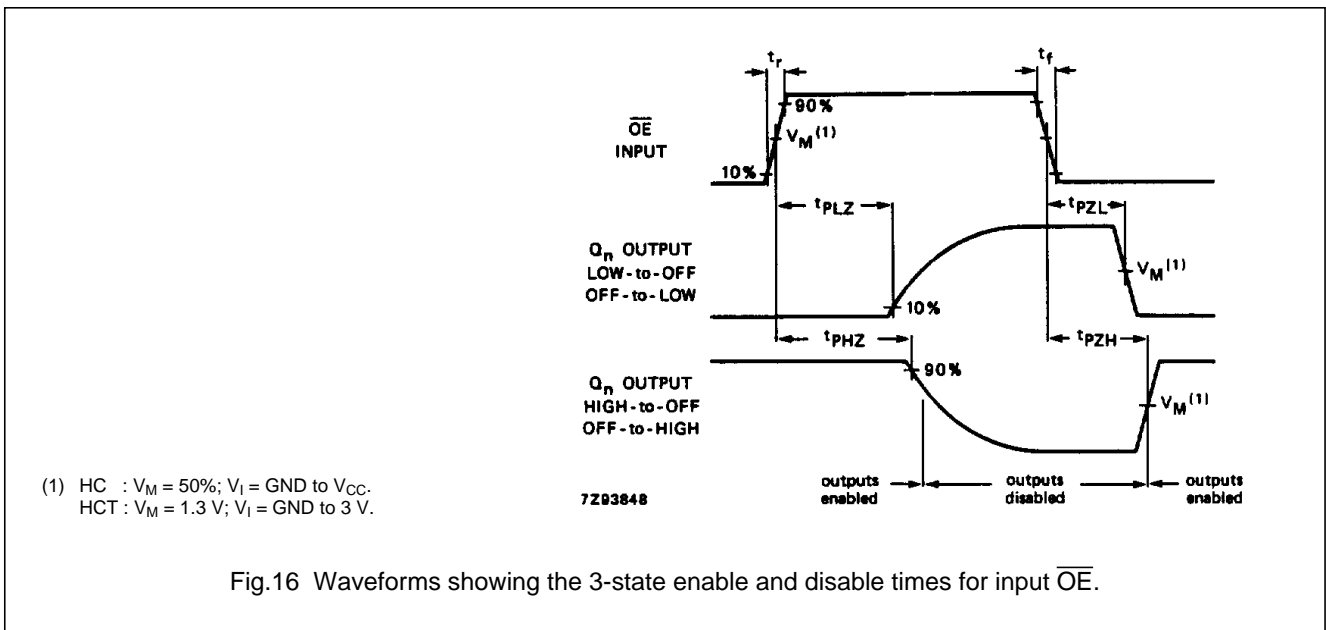
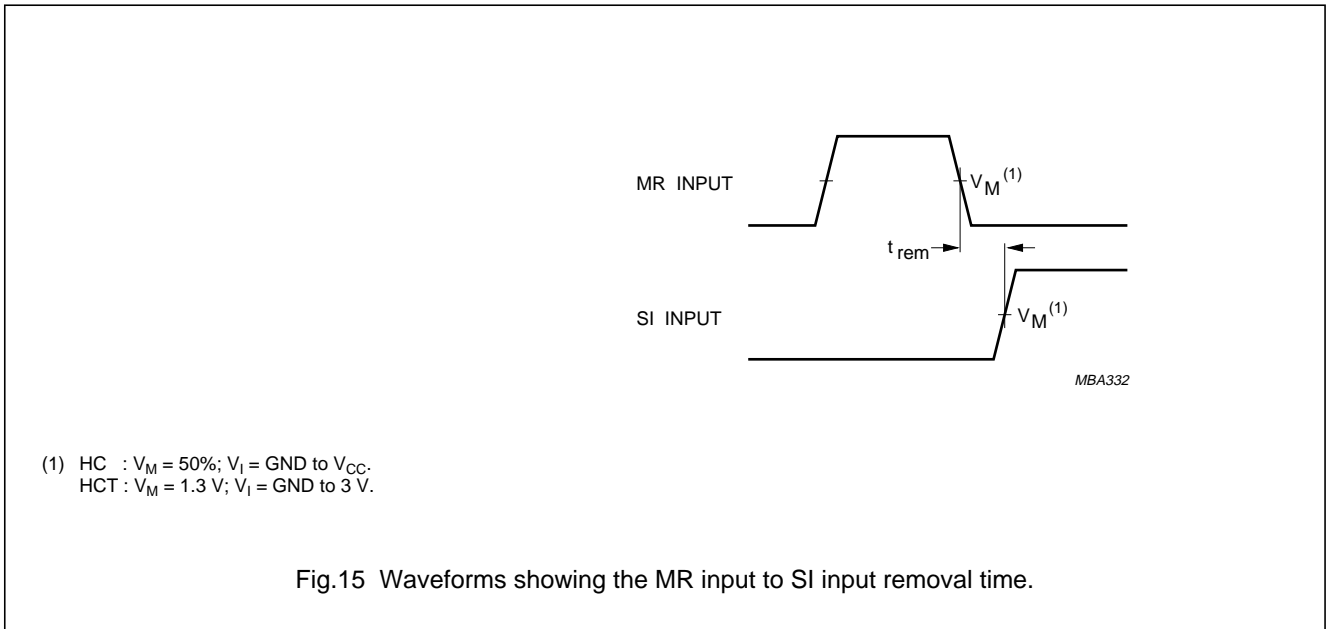


Fig.14 Waveforms showing  $\overline{SO}$  input to  $Q_n$  output propagation delays and output transition time.

4-bit x 16-word FIFO register

74HC/HCT40105



4-bit x 16-word FIFO register

74HC/HCT40105

APPLICATION INFORMATION

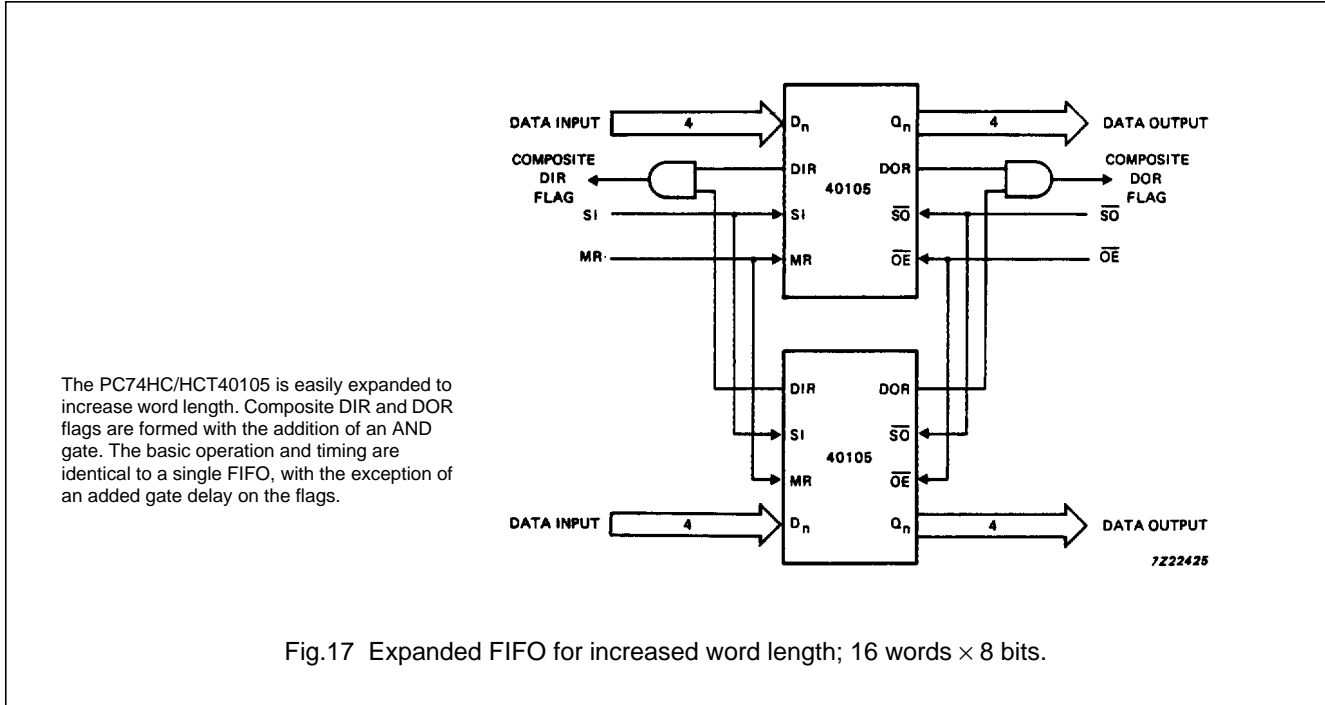


Fig.17 Expanded FIFO for increased word length; 16 words x 8 bits.

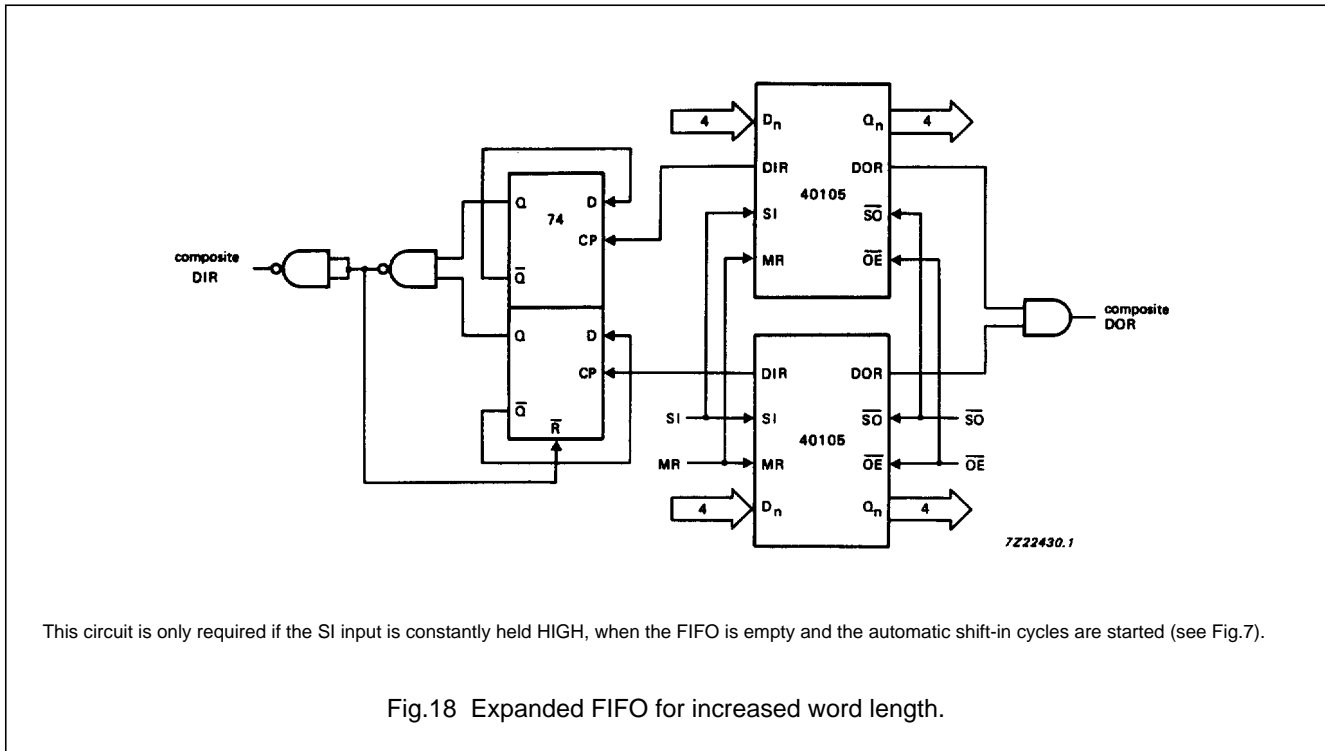


Fig.18 Expanded FIFO for increased word length.



# 4-bit x 16-word FIFO register

# 74HC/HCT40105

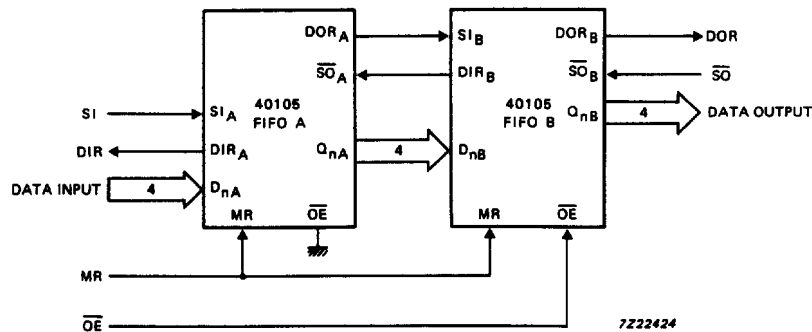
### Expanded format

Fig.19 shows two cascaded FIFOs providing a capacity of 32 words x 4 bits

Fig.20 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a rippled through delay, data arrives at the output of FIFO<sub>A</sub>. Due to  $\overline{SO}_A$  being HIGH, a DOR pulse is generated. The requirements of SI<sub>B</sub> and D<sub>nB</sub> are satisfied by the DOR<sub>A</sub> pulse width and the timing between the rising edge of DOR<sub>A</sub> and Q<sub>nA</sub>. After a second ripple through delay, data arrives at the output of FIFO<sub>B</sub>.

Fig.21 shows the signals on the nodes of both FIFOs after the application of a  $\overline{SO}_R$  pulse, when both FIFOs are initially full. After a bubble-up delay a DIR<sub>R</sub> pulse is generated, which acts as a  $\overline{SO}_A$  pulse for FIFO<sub>A</sub>. One word is transferred from the output of FIFO<sub>A</sub> to the input of FIFO<sub>B</sub>. The requirements of the  $\overline{SO}_A$  pulse for FIFO<sub>A</sub> is satisfied by the pulse width of DOR<sub>B</sub>. After a second bubble-up delay an empty space arrives at D<sub>nA</sub>, at which time DIR<sub>A</sub> goes HIGH.

Fig.22 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

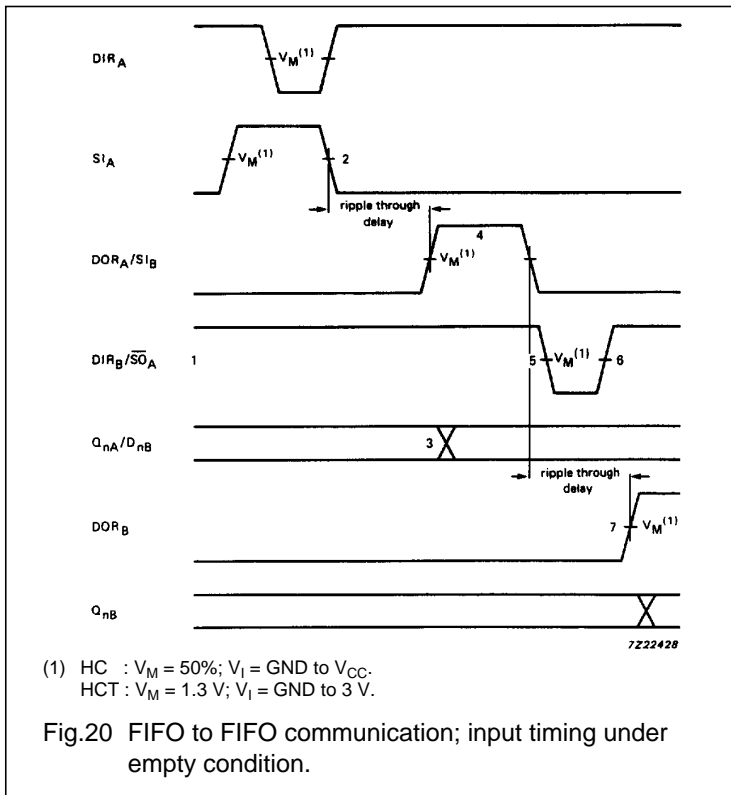


The PC7HC/HCT40105 is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figs 17 and 19 demonstrate the intercommunication timing between FIFO<sub>A</sub> and FIFO<sub>B</sub>. Fig.22 gives an overview of pulse and timing of two cascaded FIFOs, when shifted full and shifted empty again.

Fig.19 Cascading for increased word capacity; 32 words x 4 bits.

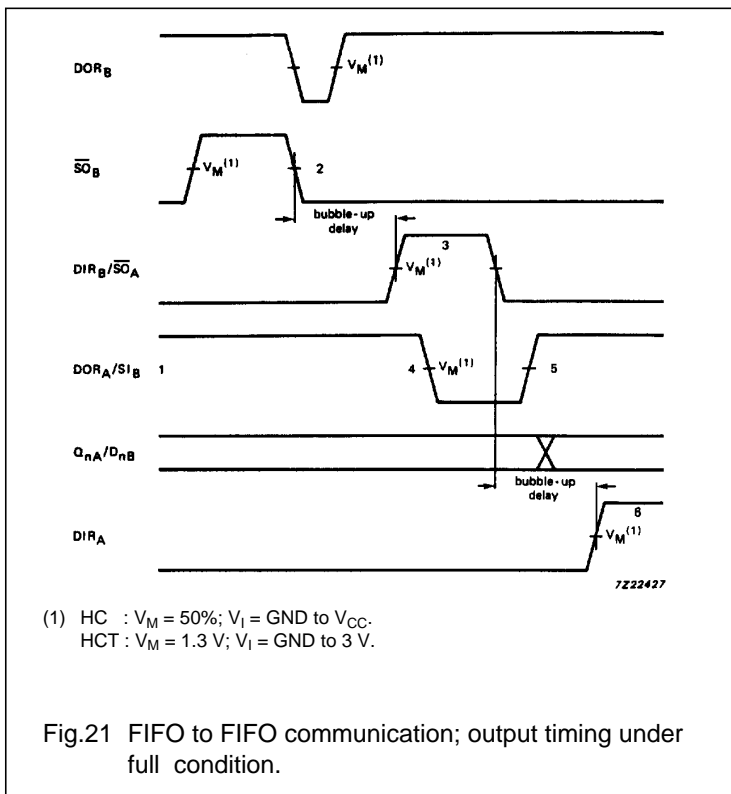
4-bit x 16-word FIFO register

74HC/HCT40105



Notes to Fig.20

1. FIFO<sub>A</sub> and FIFO<sub>B</sub> initially empty,  $\overline{SO}_A$  held HIGH in anticipation of data.
2. Load one word into FIFO<sub>A</sub>; SI pulse applied, results in DIR pulse.
3. Data out<sub>A</sub>/data in<sub>B</sub> transition; valid data arrives at FIFO<sub>A</sub> output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFO<sub>B</sub>.
4. DOR<sub>A</sub> and SI<sub>B</sub> pulse HIGH; (ripple through delay after SI<sub>A</sub> LOW) data is unloaded from FIFO<sub>A</sub> as a result of the data output ready pulse, data is shifted into FIFO<sub>B</sub>.
5. DIR<sub>B</sub> and  $\overline{SO}_A$  go LOW; flag indicates input stage of FIFO<sub>B</sub> is busy, shift-out of FIFO<sub>A</sub> is complete.
6. DIR<sub>B</sub> and  $\overline{SO}_A$  go HIGH automatically; the input stage of FIFO<sub>B</sub> is again able to receive data, SO is held HIGH in anticipation of additional data.
7. DOR<sub>B</sub> goes HIGH; (ripple through delay after SI<sub>B</sub> LOW) valid data is present one propagation delay later at the FIFO<sub>B</sub> output stage.



Notes to Fig.21

1. FIFO<sub>A</sub> and FIFO<sub>B</sub> initially empty, SI<sub>B</sub> held HIGH in anticipation of shifting in new data as empty location bubbles-up.
2. Unload one word into FIFO<sub>B</sub>;  $\overline{SO}$  pulse applied, results in DOR pulse.
3. DIR<sub>B</sub> and  $\overline{SO}_A$  pulse HIGH; (bubble-up delay after  $\overline{SO}_B$  LOW) data is loaded into FIFO<sub>B</sub> as a result of the DIR pulse, data is shifted out of FIFO<sub>A</sub>.
4. DOR<sub>A</sub> and SI<sub>B</sub> go LOW; flag indicates the output stage of FIFO<sub>A</sub> is busy, shift-in to FIFO<sub>B</sub> is complete.
5. DOR<sub>A</sub> and SI<sub>B</sub> go HIGH; flag indicates valid data is again available at FIFO<sub>A</sub> output stage, SI<sub>B</sub> is held HIGH, awaiting bubble-up of empty location.
6. DIR<sub>A</sub> goes HIGH; (bubble-up delay after  $\overline{SO}_A$  LOW) an empty location is present at input stage of FIFO<sub>A</sub>.

4-bit x 16-word FIFO register

74HC/HCT40105

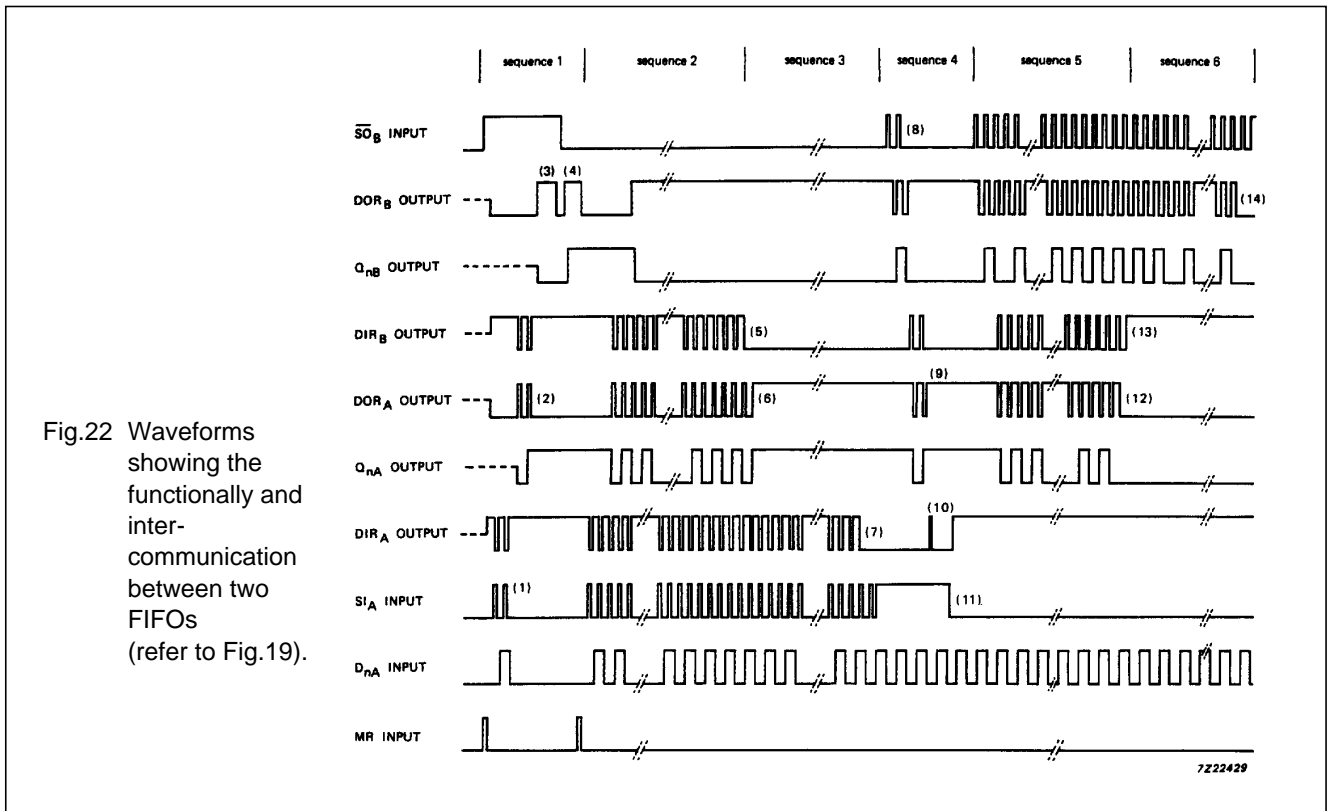


Fig.22 Waveforms showing the functionally and inter-communication between two FIFOs (refer to Fig.19).

**Note to Fig.22**

Sequence 1 (Both FIFOs empty, starting shift-in process): After a MR pulse has been applied FIFO<sub>A</sub> and FIFO<sub>B</sub> are empty. The DOR flags of FIFO<sub>A</sub> and FIFO<sub>B</sub> go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data.  $\overline{SO}_B$  is held HIGH and two SIA pulses are applied (1). These pulses allow two data words to ripple through to the output stage of FIFO<sub>A</sub> and to the input stage of FIFO<sub>B</sub> (2). When data arrives at the output of FIFO<sub>B</sub>, a DOR<sub>B</sub> pulse is generated (3). When  $\overline{SO}_B$  goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR<sub>B</sub> goes HIGH (4).

Sequence 2 (FIFO<sub>B</sub> runs full): After the MR pulse, a series of 16 SIA pulses are applied. When 16 words are shifted in, DIR<sub>B</sub> remains LOW due to FIFO<sub>B</sub> being full (5). DOR<sub>A</sub> goes LOW due to FIFO<sub>A</sub> being empty.

Sequence 3 (FIFO<sub>A</sub> runs full): When 17 words are shifted in, DOR<sub>A</sub> remains HIGH due to valid data remaining at the output of FIFO<sub>A</sub>. Q<sub>nA</sub> remains HIGH, being the polarity of the 17th data word (6). After the 32th SIA pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Sequence 4 (Both FIFOs full, starting shift-out process): SIA is held HIGH and two  $\overline{SO}_B$  pulses are applied (8). These pulses shift out two words and thus allow empty locations to bubble-up to the input stage of FIFO<sub>B</sub>, and proceed to FIFO<sub>A</sub> (9). When the first empty location arrives at the input of FIFO<sub>A</sub>, a DIR<sub>A</sub> pulse is generated (10) and a new word is shifted into FIFO<sub>A</sub>. SIA is made LOW and now the second empty location reaches the input stage of FIFO<sub>A</sub>, after which DIR<sub>A</sub> remains HIGH (11).

Sequence 5 (FIFO<sub>A</sub> runs empty): At the start of sequence 5 FIFO<sub>A</sub> contains 15 valid words due to two words being shifted out and one word being shifted in sequence 4. An additional series of  $\overline{SO}_B$  pulses are applied. After 15  $\overline{SO}_B$  pulses, all words from FIFO<sub>A</sub> are shifted into FIFO<sub>B</sub>. DOR<sub>A</sub> remains LOW (12).

Sequence 6 (FIFO<sub>B</sub> runs empty): After the next  $\overline{SO}_B$  pulse, DIR<sub>B</sub> remains HIGH due to the input stage of FIFO<sub>B</sub> being empty (13). After another 15  $\overline{SO}_B$  pulses, DOR<sub>B</sub> remains LOW due to both FIFOs being empty (14). Additional  $\overline{SO}_B$  pulses have no effect. The last word remains available at the output Q<sub>n</sub>.

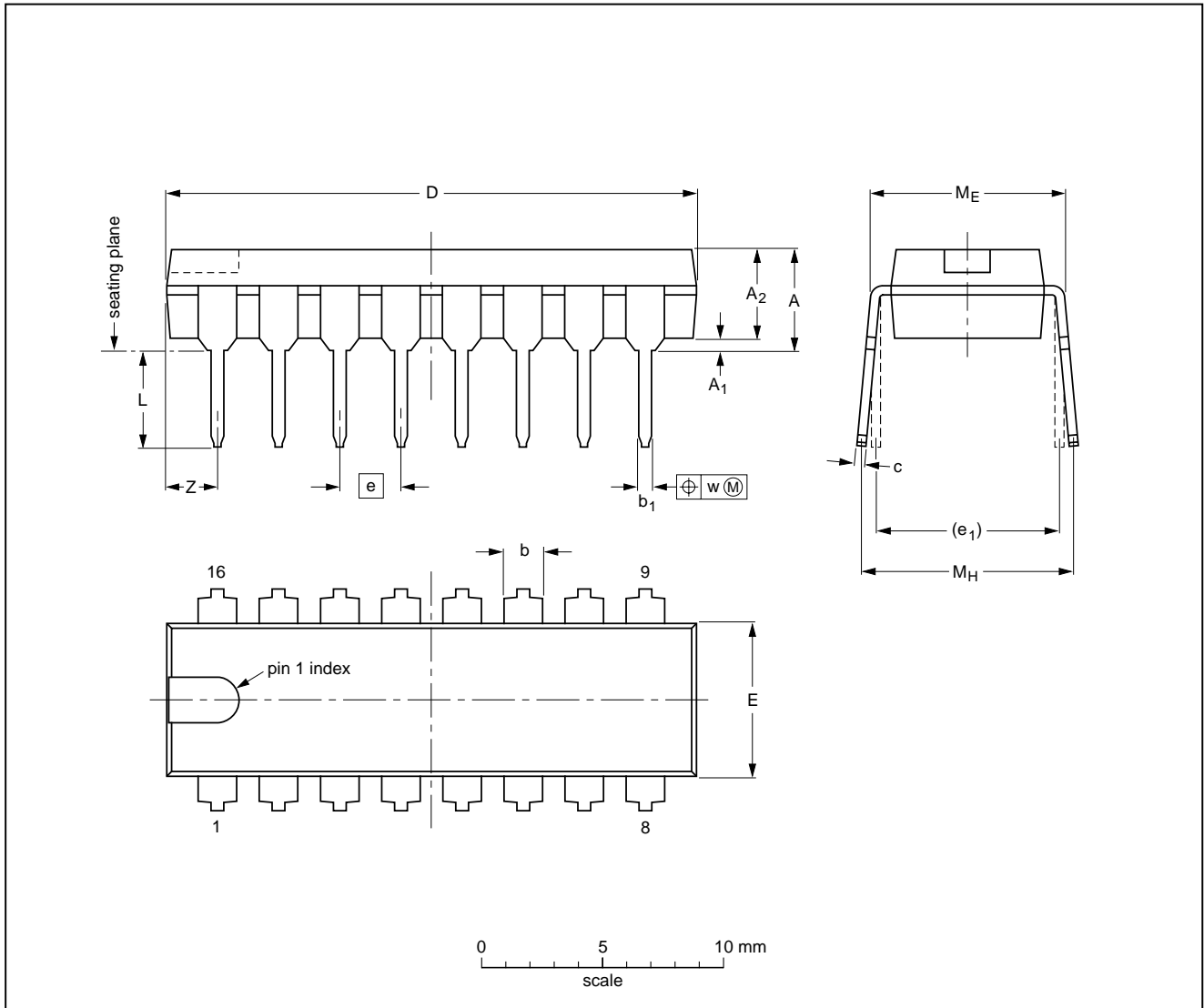
4-bit x 16-word FIFO register

74HC/HCT40105

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

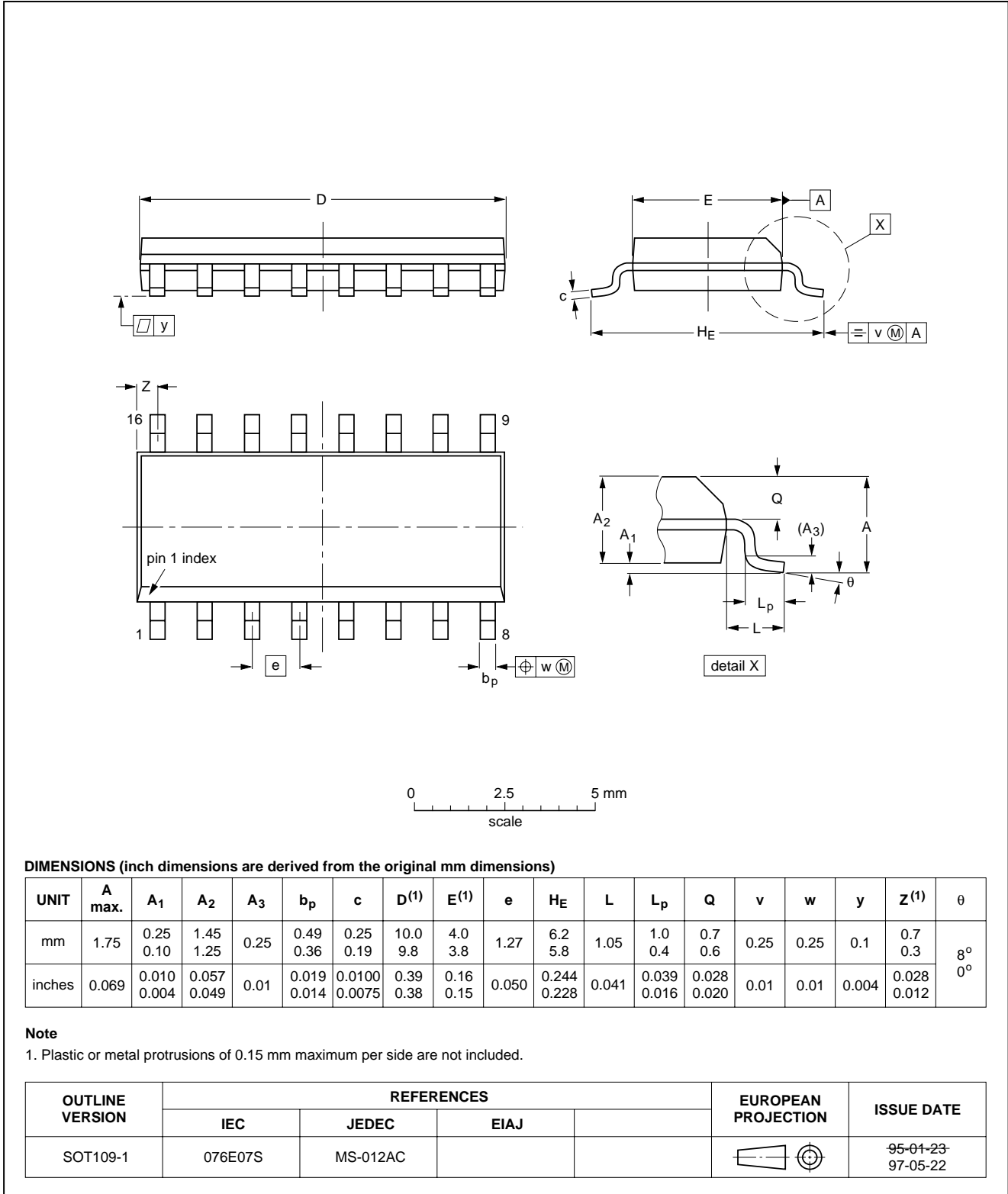
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				92-10-02 95-01-19

4-bit x 16-word FIFO register

74HC/HCT40105

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

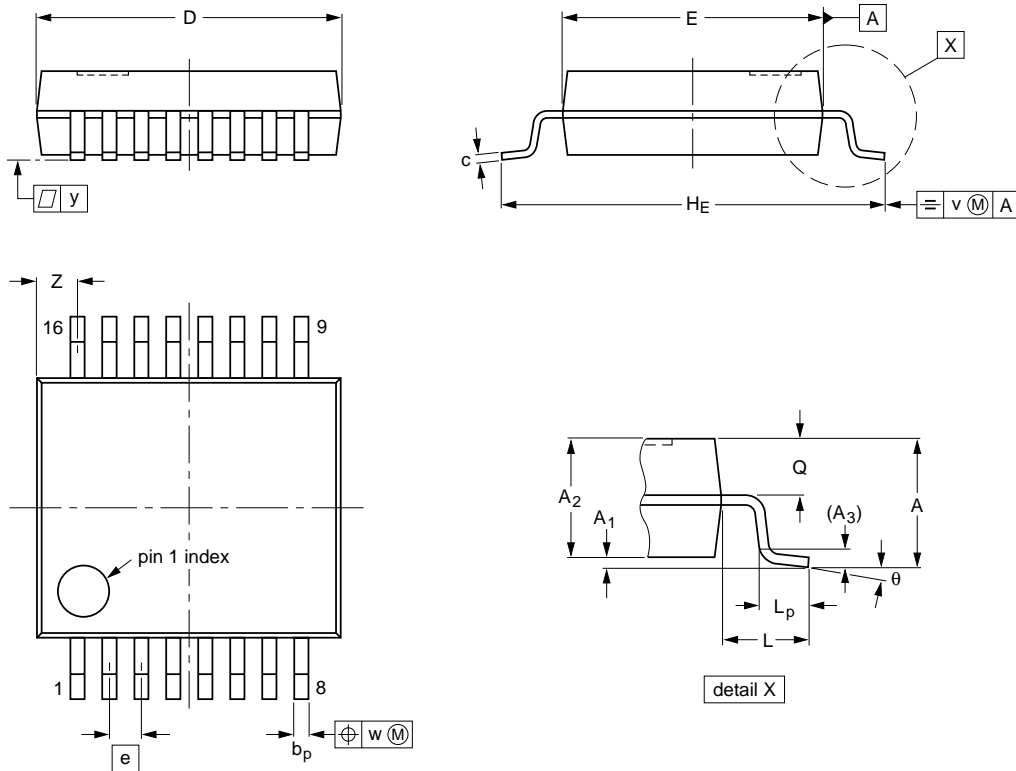


4-bit x 16-word FIFO register

74HC/HCT40105

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

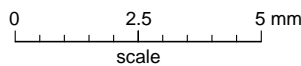
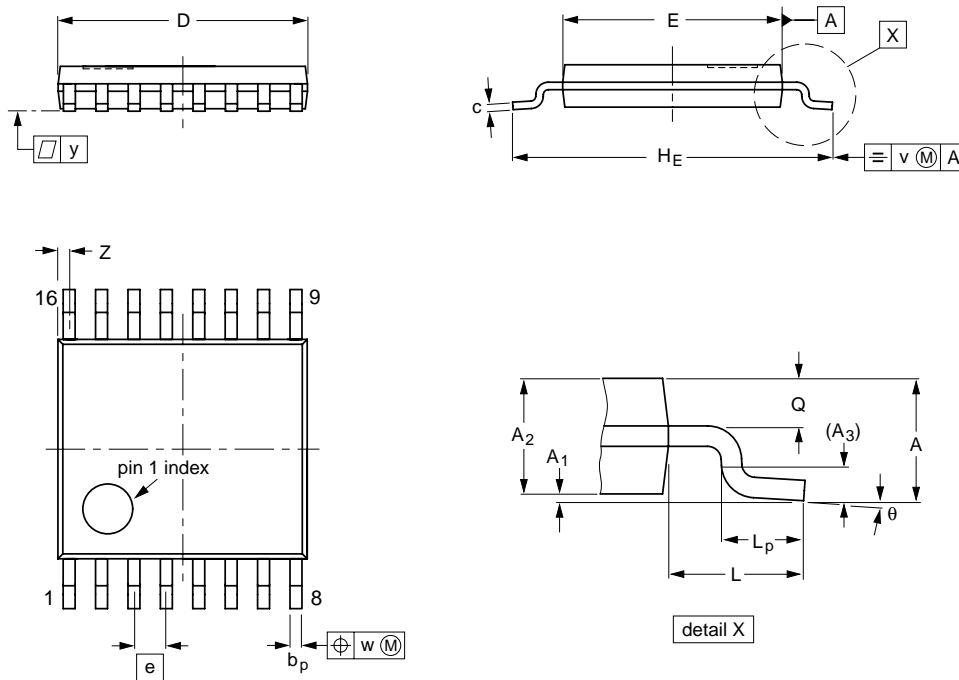
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT338-1		MO-150AC			94-01-14 95-02-04

4-bit x 16-word FIFO register

74HC/HCT40105

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

## 4-bit x 16-word FIFO register

## 74HC/HCT40105

**SOLDERING****Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

**DIP****SOLDERING BY DIPPING OR BY WAVE**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**REPAIRING SOLDERED JOINTS**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**SO, SSOP and TSSOP****REFLOW SOLDERING**

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

**WAVE SOLDERING**

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

**Even with these conditions:**

- **Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**
- **Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**REPAIRING SOLDERED JOINTS**

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



## 4-bit x 16-word FIFO register

74HC/HCT40105

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.



## Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

### Наши контакты:

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331