OPA857 Ultralow-Noise, Wideband, Selectable-Feedback Resistance Transimpedance Amplifier

1 Features

- Internal Midreference Voltage
- Pseudo-Differential Output
- Wide Dynamic Range
- Bandwidth:
  - 115 MHz (4.5-kΩ Transimpedance, 1.5-pF External Parasitic Capacitance)
  - 130 MHz (18.2-kΩ Transimpedance, 1.5-pF External Parasitic Capacitance)
- Ultralow Voltage Noise Density: 14.7 nA_{RMS} (NPBW = 85.7 MHz)
- Very Fast Overload Recovery Time: < 15 ns
- Internal Input Protection Diode
- Power Supply:
  - Voltage: +2.6 V to +3.6 V
  - Current: 23.4 mA
- Extended Temperature Range: –40°C to +85°C

2 Applications

- Photodiode Monitoring
- Precision I/V Conversion
- Optical Amplifiers
- CAT-Scanner Front-Ends

3 Description

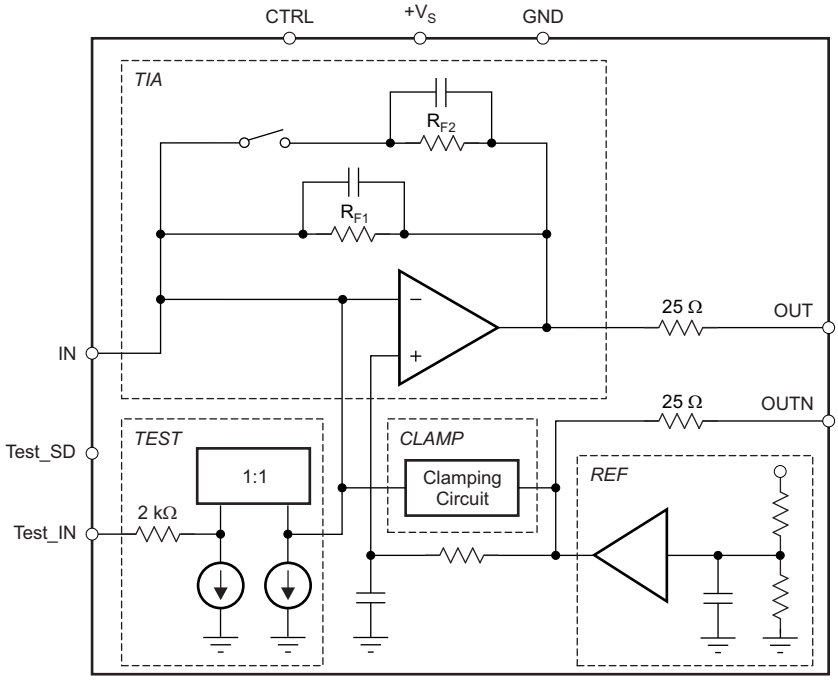
The OPA857 is a wideband, fast overdrive recovery, fast-settling, ultralow-noise transimpedance amplifier targeted at photodiode monitoring applications. With selectable feedback resistance, the OPA857 simplifies the design of high-performance optical systems. Very fast overload recovery time and internal input protection provide the best combination to protect the remainder of the signal chain from overdrive while minimizing recovery time. The two selectable transimpedance gain configurations allow high dynamic range and flexibility required in modern transimpedance amplifier applications. The OPA857 is available in a 3-mm × 3-mm VQFN package.

The device is characterized for operation over the full industrial temperature range from –40°C to +85°C.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
OPA857	VQFN (16)	3 mm × 3 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

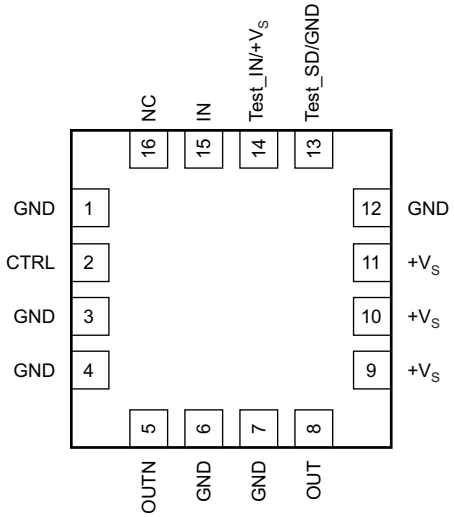
Changes from Revision B (January 2014) to Revision C	Page
• Changed document format to meet new data sheet standards; added *Handling Ratings* and *Device and Documentation Support* sections, and moved existing sections	1
• Changed OUTN to OUT in *Output Voltage Swing* parameter test conditions	5
• Changed Functional Block Diagram	13

Changes from Revision A (December 2013) to Revision B	Page
• Changed document status to Production Data	1
• Changed transimpedance value in both sub-bullets of *Bandwidth* Features bullet	1
• Changed *Extended Temperature Range* Features bullet to a range of –40°C to +85°C	1
• Changed first sentence of *Description* section: added "targeted at photodiode monitoring applications"	1
• Changed temperature range to –40°C to +85°C in last sentence of *Description* section	1
• Changed front-page graphic	1
• Added pages 2 through end of document	3

Changes from Original (December 2013) to Revision A	Page
• Changed document status to Product Preview	1
• Deleted all pages past page 1	1
• Deleted fourth Applications bullet	1
• Changed first sentence of *Description* section	1

5 Pin Configuration and Functions

RGT Package
VQFN-16
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CTRL	2	I	Control pin for transimpedance gain 0 = 5-kΩ internal resistance, 1 = 20-kΩ internal resistance
GND	1, 3, 4, 6, 7, 12	I	Ground
IN	15	I	Input
NC	16	—	Not connected
OUT	8	O	Signal output
OUTN	5	O	Common-mode voltage output reference
Test_IN/+V_S	14	I	Must be left floating or connected to +V_S for normal operation
Test_SD/GND	13	I	Must be left floating or connected to GND for normal operation
+V_S	9-11	I	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	Supply voltage, $V_{S–}$ to V_{S+}		3.8	V
	Input and output voltage, V_{IN}, V_{OUT} pins	$(V_{S–})$ – 0.7	(V_{S+}) + 0.7	V
	Differential input voltage		1	V
Current	Output current		50	mA
	Input current, V_{IN} pin		10	mA
Continuous power dissipation		See Thermal Information table		
Temperature	Maximum junction temperature, T_J		+150	°C
	Maximum junction temperature, T_J (continuous operation, long-term reliability)		+140	°C
	Operating free-air, T_A	–40	+85	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SS}	Supply input voltage	3.0	3.3	3.6	V
T_J	Operating junction temperature	-40		+85	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		OPA857 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	91.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	41.6	
ψ_{JT}	Junction-to-top characterization parameter	7.1	
ψ_{JB}	Junction-to-board characterization parameter	41.7	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	23.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = +25°C[1], V_S = +3.3 V, $V_{S+} – V_{S–}$ = +3.3 V, C_{Source} = 1.5 pF, V_{OUT} = 0.5 V_P (differential), R_L = 500 Ω differential, single-ended input, pseudo-differential output, and input and output referenced to midsupply (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL[2]
AC PERFORMANCE							
	Small-signal bandwidth	CTRL = 1, T_A = –40°C to +85°C		130		MHz	C
		CTRL = 0, T_A = –40°C to +85°C		115		MHz	C
SR	Slew rate (differential)	V_{OUT} = 1-V step		220		V/µs	C
t_S	Settling time to 1%	V_{OUT} = 0.5-V step, CTRL = 0, T_A = +25°C		7.2	8.1	ns	B
		V_{OUT} = 0.5-V step, CTRL = 0, T_A = –40°C to +85°C			8.2	ns	B
		V_{OUT} = 0.5-V step, CTRL = 1, T_A = +25°C		7.7	8.8	ns	B
		V_{OUT} = 0.5-V step, CTRL = 1, T_A = –40°C to +85°C			9.1	ns	B
	Settling time to 0.001%	V_{OUT} = 0.5-V step, CTRL = 0		152		ns	C
		V_{OUT} = 0.5-V step, CTRL = 1		165		ns	C
HD2	Second-harmonic distortion	V_{OUT} = 0.5 V_{PP}, f = 10 MHz, R_F = 5 kΩ, T_A = +25°C		–94		dBc	C
		V_{OUT} = 0.5 V_{PP}, f = 10 MHz, R_F = 20 kΩ, T_A = +25°C		–81		dBc	C
HD3	Third-harmonic distortion	V_{OUT} = 0.5 V_{PP}, f = 10 MHz, R_F = 5 kΩ, T_A = +25°C		–97		dBc	C
		V_{OUT} = 0.5 V_{PP}, f = 10 MHz, R_F = 20 kΩ, T_A = +25°C		–101		dBc	C
	Equivalent input-referred current noise	CTRL = 0, NPBW = 85.7 MHz, with 120-MHz, first-order, antialias filter		24.9		nA_{RMS}	C
		CTRL = 1, NPBW = 85.7 MHz, with 120-MHz, first-order, antialias filter		14.7		nA_{RMS}	C
	Overdrive recovery time	I_{IN} = 100 µA, CTRL = 1, settling to 1% of final value with 120-MHz, first-order, antialias filter			15	ns	B
	Closed-loop output impedance	f = 1 MHz (differential)		50		Ω	C
DC PERFORMANCE							
	Transimpedance gain	CTRL = 1 into 500 Ω[3][4]		18.2		kΩ	C
		CTRL = 0 into 500 Ω[3][4]		4.5		kΩ	C
	Transimpedance gain error	T_A = +25°C, R_F = 20 kΩ and R_F = 5 kΩ		±1%	±15%		A
V_{OO}	Output offset voltage	T_A = +25°C		±1	±5	mV	A
		T_A = –40°C to +85°C[5]			±6	mV	B
	Output offset voltage drift	T_A = –40°C to +85°C[5]			±15	µV/°C	C
V_{ICR}	Common-mode voltage range	T_A = +25°C, OUTN	1.78	1.83	1.88	V	A
INPUT							
	Input pin capacitance			2		pF	C
OUTPUT							
	Output voltage swing	OUT, T_A = +25°C	0.6		1.9	V	A
		T_A = –40°C to +85°C[5]			1.9	V	B
	Output current drive (for linear operation)	OUT, differential 50-Ω between OUT and OUTN		+5		mA	C
				–20		mA	C

(1) Junction temperature = ambient for +70°C specifications.
(2) Test levels: **(A)** 100% tested at +25°C. Overtemperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(3) See the *Application and Implementation* section for details on loading and effective transimpedance gain.
(4) Note that the effective transimpedance gain is reduced to 18.2 kΩ and 4.5 kΩ, respectively, with a 500-Ω load resulting from the internal series resistance on OUT and OUTN.
(5) Junction temperature = ambient at low temperature; junction temperature = ambient +3.5°C for overtemperature specifications.

Electrical Characteristics (continued)

At T_A = +25°C[1], V_S = +3.3 V, V_{S+} – $V_{S–}$ = +3.3 V, C_{Source} = 1.5 pF, V_{OUT} = 0.5 V_P (differential), R_L = 500 Ω differential, single-ended input, pseudo-differential output, and input and output referenced to midsupply (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL[2]
POWER SUPPLY							
	Specified operating voltage		2.6	3.3	3.6	V	B
	Quiescent operating current	CTRL = 0, T_A = +25°C	20.5	23.4	26.3	mA	A
		CTRL = 0, T_A = –40°C to +85°C[6]	20.0		26.8	mA	B
		CTRL = 1, T_A = +25°C	20.5	23.4	26.3	mA	A
		CTRL = 1, T_A = –40°C to +85°C[6]	20.0		26.8	mA	B
PSRR	Power-supply rejection ratio	At dc, T_A = +25°C	70	80		dB	A
		f = 10 MHz, T_A = –40°C to +85°C[6]	15	18		dB	B
LOGIC LEVEL (CTRL)							
V_{IH}	High-level input voltage		2			V	A
V_{IL}	Low-level input voltage				0.8	V	A
	High-level control pin input bias current				1	µA	A
	Low-level control pin input bias current				1	µA	A
TEMPERATURE							
	Specified operating range		–40		+85	°C	C

(6) Junction temperature = ambient at low temperature; junction temperature = ambient +3.5°C for overtemperature specifications.

6.6 Typical Characteristics

At T_A = +25°C, C_S = 1.5 pF, and R_L = 500 Ω differential between OUT and OUTN (unless otherwise noted).

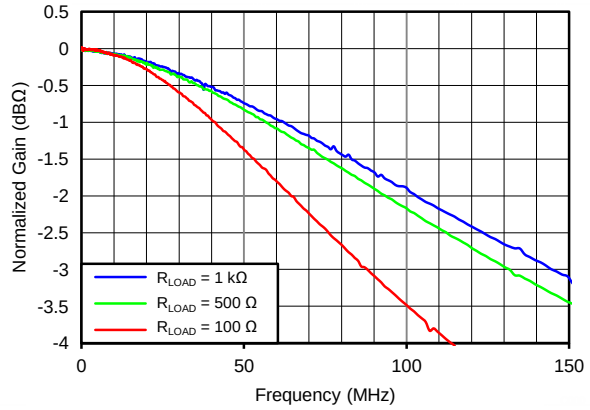


Figure 1. 18.2-kΩ Gain Frequency response

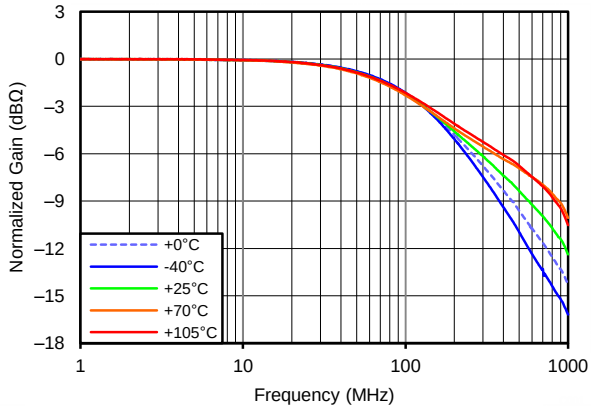


Figure 2. 18.2-kΩ Gain Frequency response vs Temperature

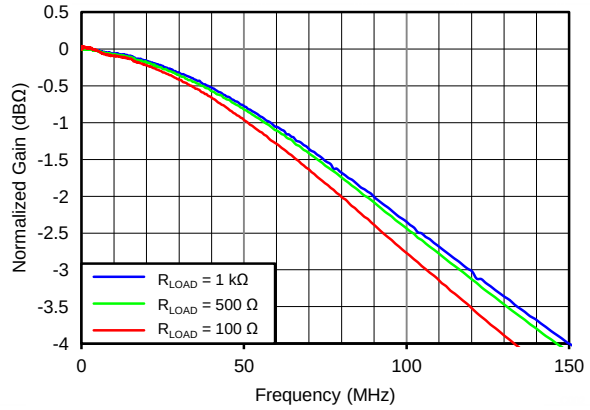


Figure 3. 4.5-kΩ Gain Frequency response

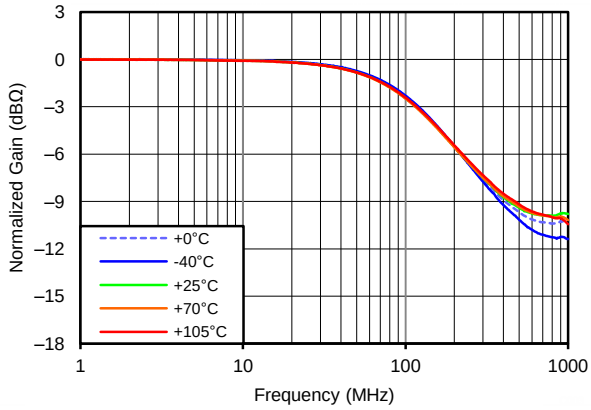


Figure 4. 4.5-kΩ Gain Frequency response vs Temperature

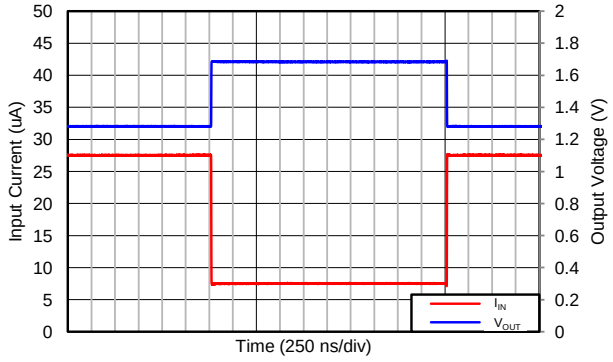


Figure 5. 18.2-kΩ Gain Pulse response

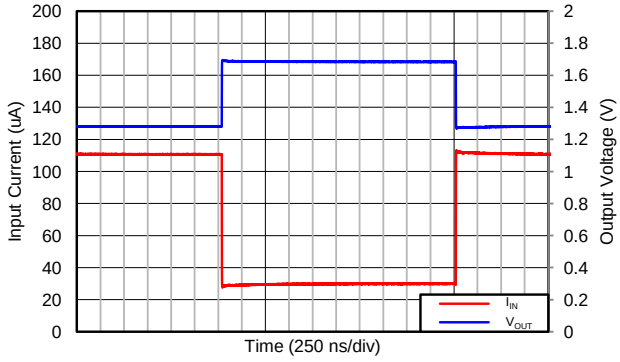


Figure 6. 4.5-kΩ Gain Pulse Response

Typical Characteristics (continued)

At T_A = +25°C, C_S = 1.5 pF, and R_L = 500 Ω differential between OUT and OUTN (unless otherwise noted).

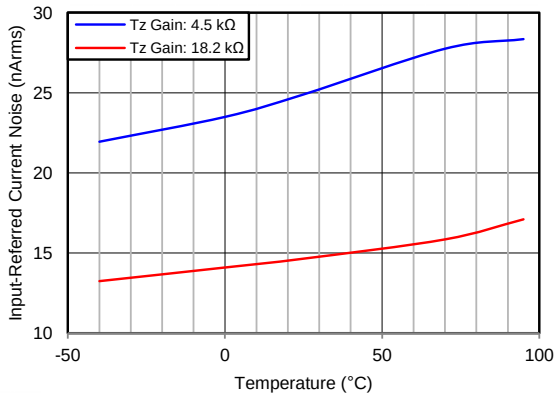


Figure 7. RMS Input-Referred Current Noise vs Temperature

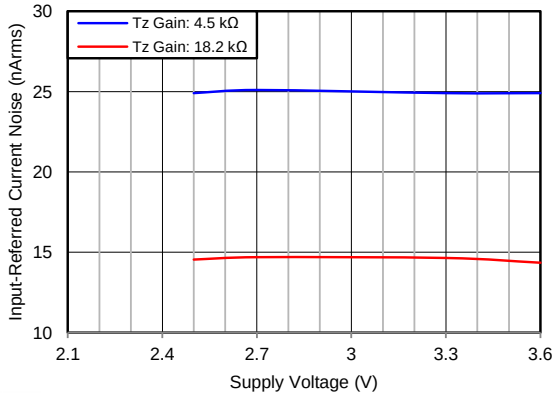


Figure 8. RMS Input-Referred Current Noise vs Supply Voltage

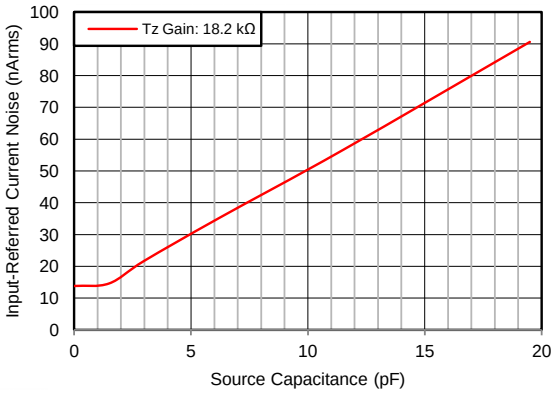


Figure 9. 18.2-kΩ Gain RMS Input-Referred Current Noise vs Capacitance

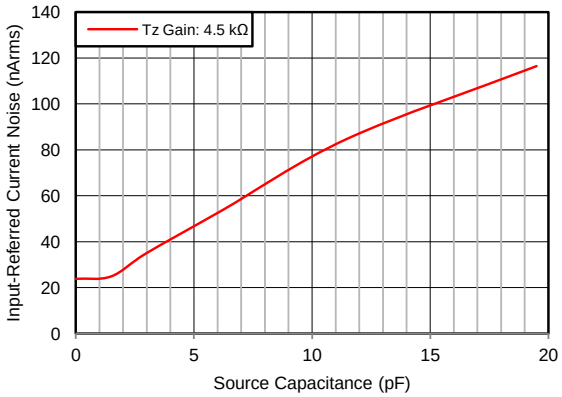


Figure 10. 4.5-kΩ Gain RMS Input-Referred Current Noise vs Input Capacitance

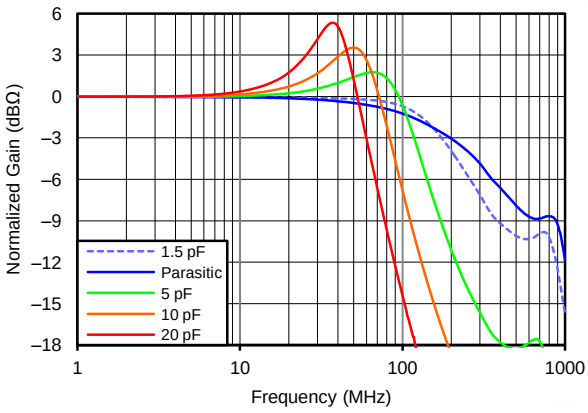


Figure 11. 18.2-kΩ Gain Frequency Response vs Input Capacitance

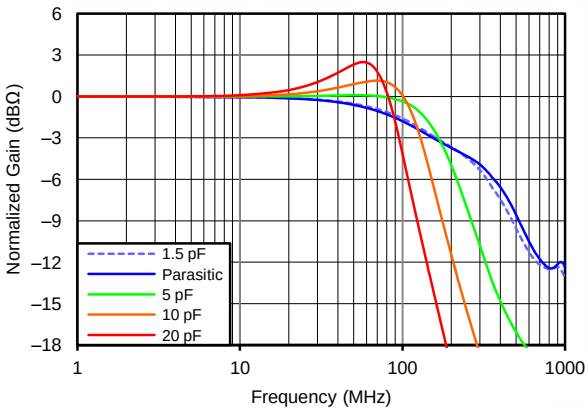


Figure 12. 4.5-kΩ Gain Frequency Response vs Input Capacitance

Typical Characteristics (continued)

At T_A = +25°C, C_S = 1.5 pF, and R_L = 500 Ω differential between OUT and OUTN (unless otherwise noted).

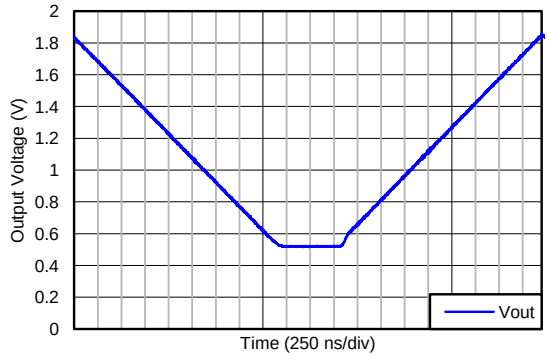


Figure 13. 18.2-kΩ Gain Overdrive Recovery

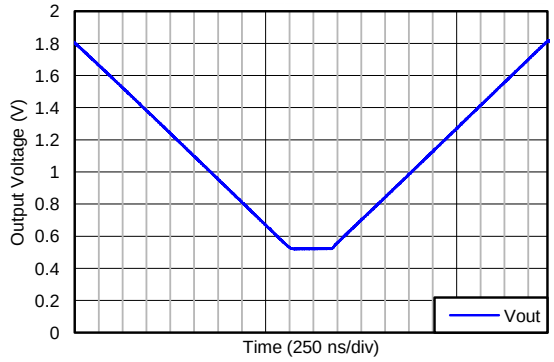


Figure 14. 4.5-kΩ Gain Overdrive Recovery

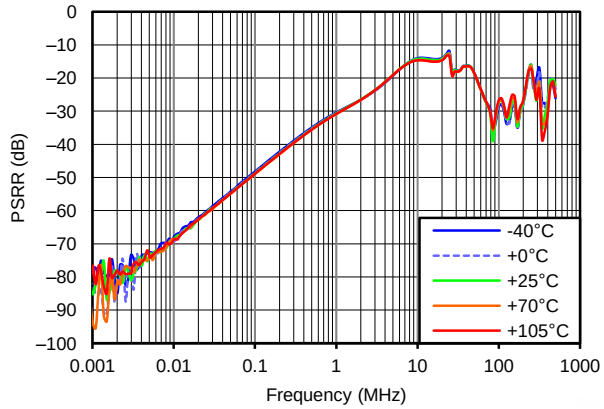


Figure 15. 18.2-kΩ Gain Power-Supply Rejection Ratio vs Frequency

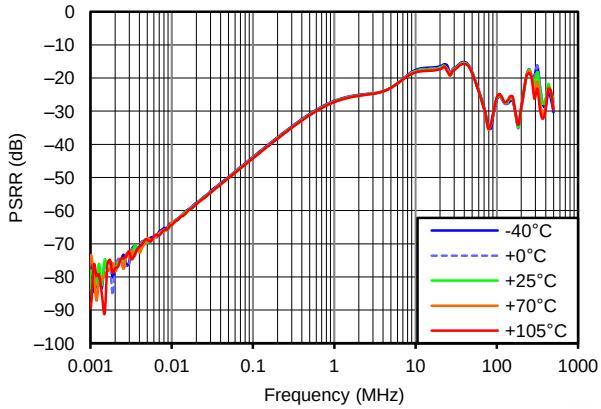


Figure 16. 4.5-kΩ Gain Power-Supply Rejection Ratio vs Frequency

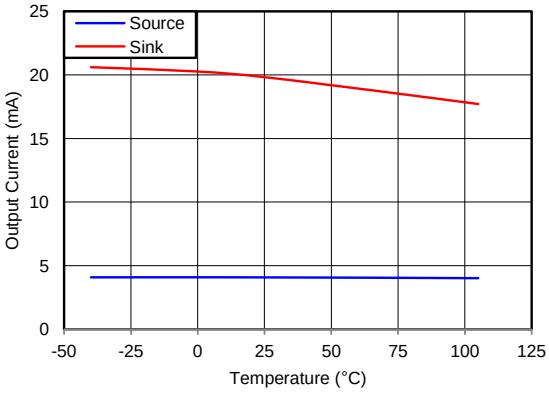
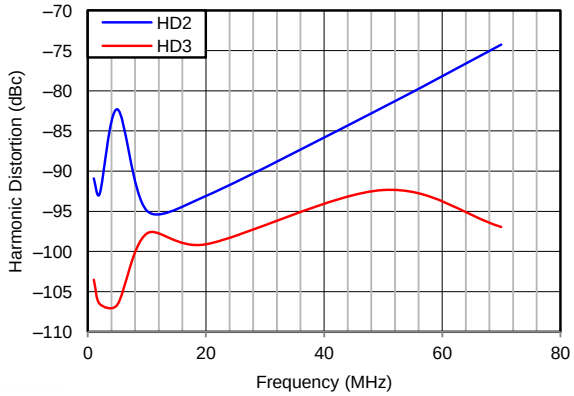


Figure 17. Output Current vs Temperature

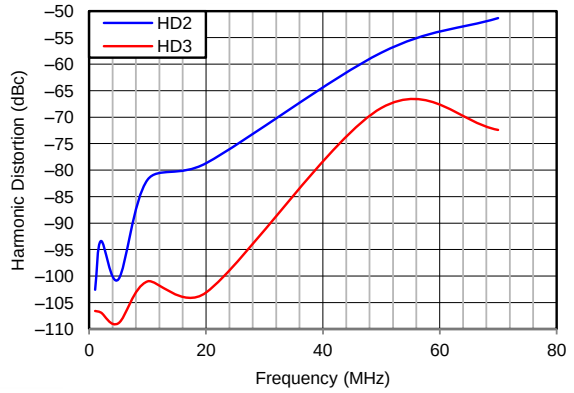


T_Z Gain: 4.5 kΩ
R_{LOAD} = 5 kΩ

Figure 18. Harmonic Distortion vs Frequency

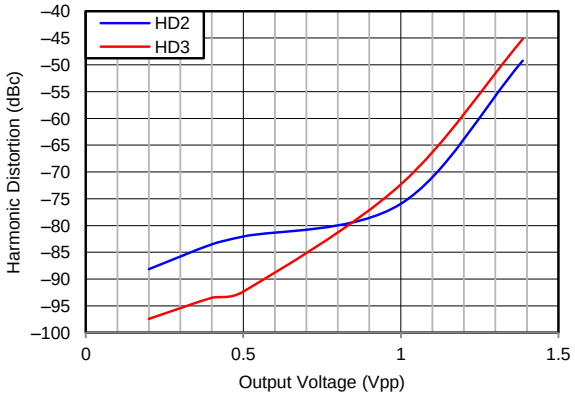
Typical Characteristics (continued)

At T_A = +25°C, C_S = 1.5 pF, and R_L = 500 Ω differential between OUT and OUTN (unless otherwise noted).



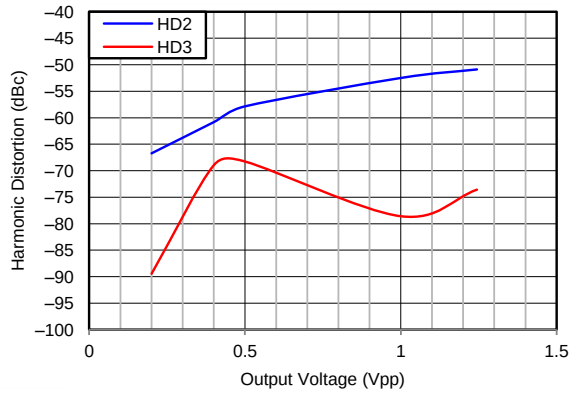
T_Z Gain: 18.2 kΩ
R_{LOAD} = 5 kΩ

Figure 19. Harmonic Distortion vs Frequency



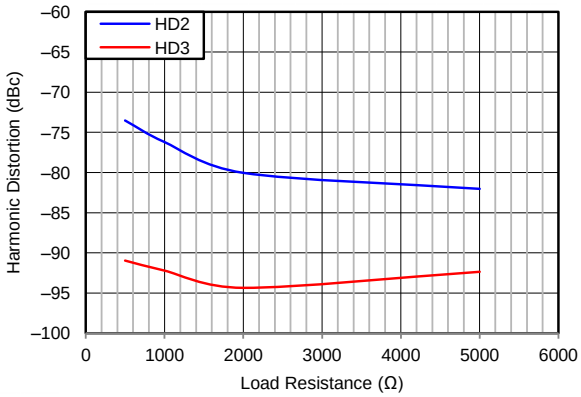
T_Z Gain: 4.5 kΩ
R_{LOAD} = 5 kΩ
f = 50 MHz

Figure 20. Harmonic Distortion vs Output Voltage



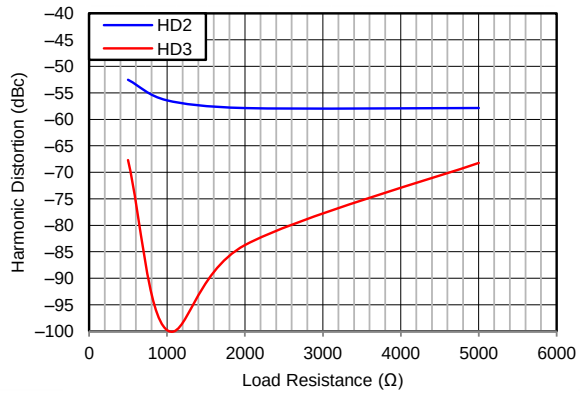
T_Z Gain: 18.2 kΩ
R_{LOAD} = 5 kΩ
f = 50 MHz

Figure 21. Harmonic Distortion vs Output Voltage



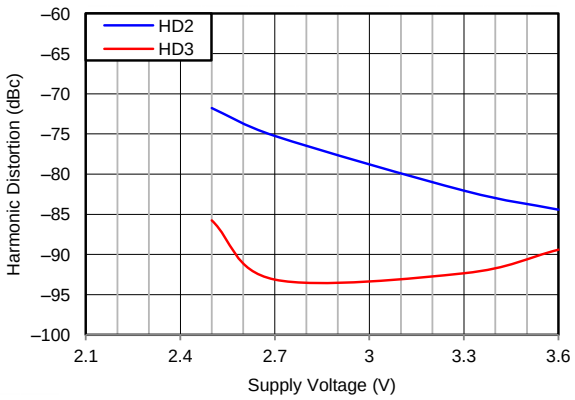
T_Z Gain: 4.5 kΩ
f = 50 MHz

Figure 22. Harmonic Distortion vs R_{LOAD}



T_Z Gain: 18.2 kΩ
f = 50 MHz

Figure 23. Harmonic Distortion vs R_{LOAD}

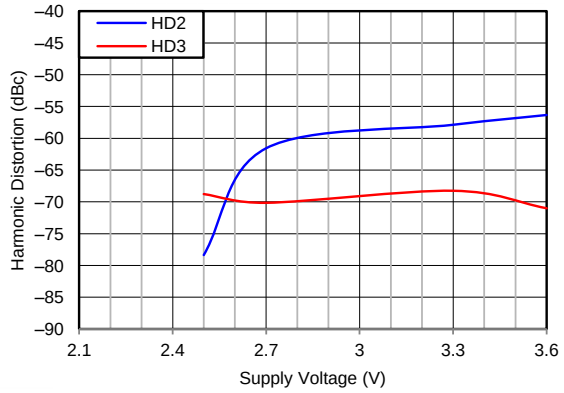


T_Z Gain: 4.5 kΩ
R_{LOAD} = 5 kΩ
T_A = +25 °C
f = 50 MHz

Figure 24. Harmonic Distortion vs Supply Voltage

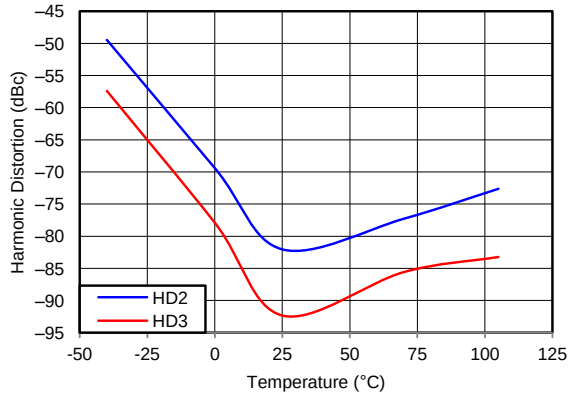
Typical Characteristics (continued)

At T_A = +25°C, C_S = 1.5 pF, and R_L = 500 Ω differential between OUT and OUTN (unless otherwise noted).



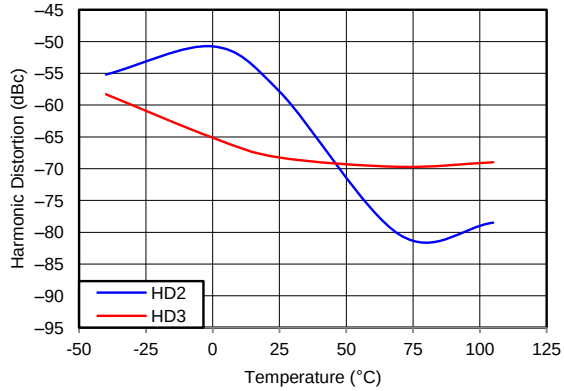
T_Z Gain: 18.2 kΩ T_A = +25 °C
R_{LOAD} = 5 kΩ f = 50 MHz

Figure 25. Harmonic Distortion vs Supply Voltage



T_Z Gain: 4.5 kΩ R_{LOAD} = 5 kΩ f = 50 MHz

Figure 26. Harmonic Distortion vs Temperature



T_Z Gain: 18.2 kΩ R_{LOAD} = 5 kΩ f = 50 MHz

Figure 27. Harmonic Distortion vs Temperature

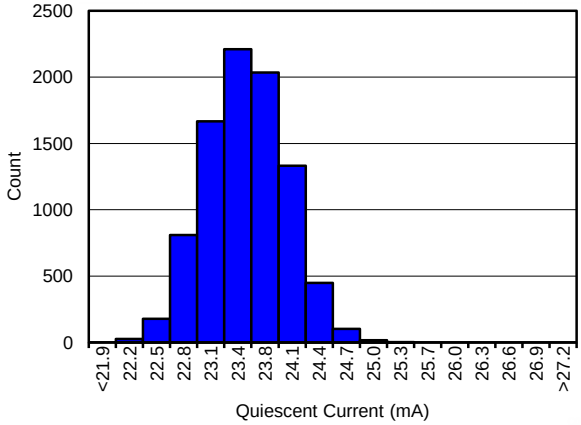


Figure 28. 18.2-kΩ I_Q Histogram

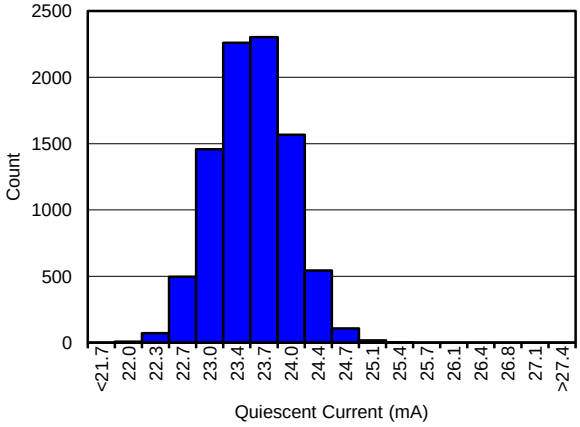


Figure 29. 4.5-kΩ I_Q Histogram

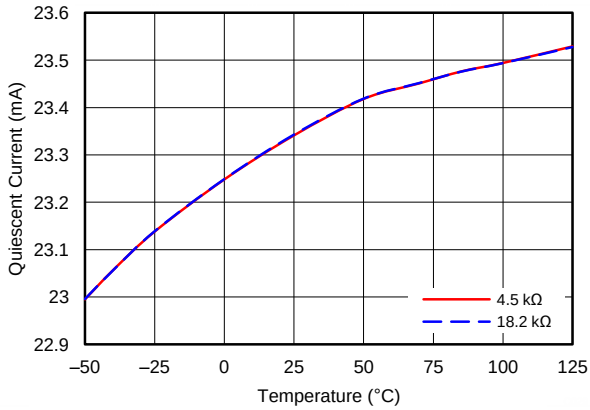


Figure 30. Quiescent Current vs Temperature

Typical Characteristics (continued)

At T_A = +25°C, C_S = 1.5 pF, and R_L = 500 Ω differential between OUT and OUTN (unless otherwise noted).

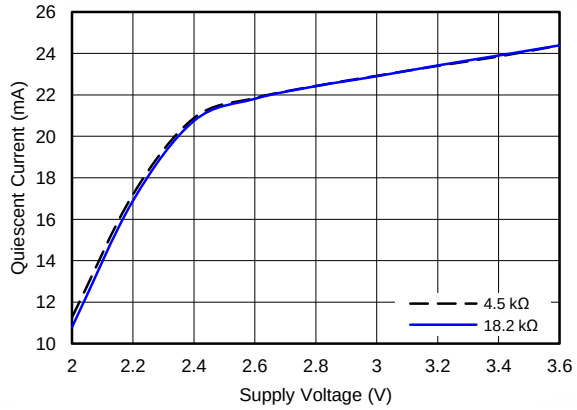
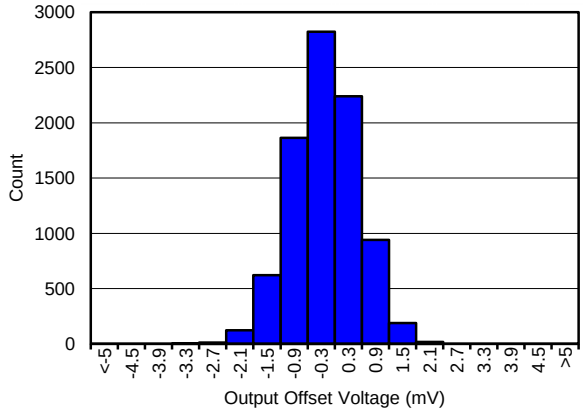
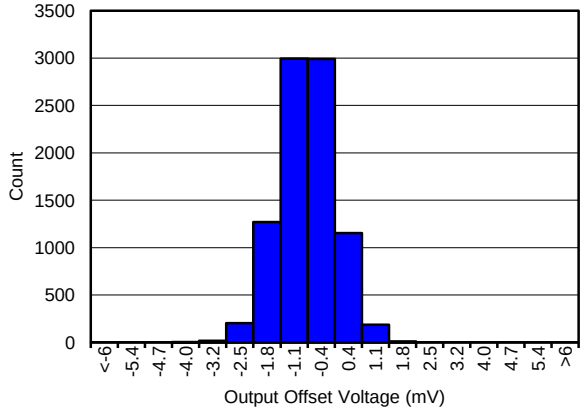


Figure 31. Quiescent Current vs Supply Voltage



T_Z Gain: 4.5 kΩ

Figure 32. 4.5-kΩ Differential V_{OSO}



T_Z Gain: 18.2 kΩ

Figure 33. 18.2-kΩ Differential V_{OSO}

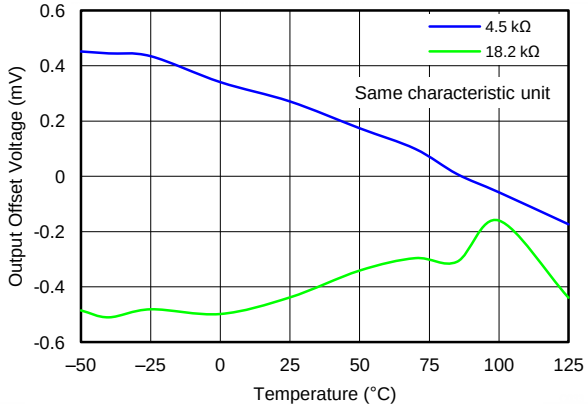


Figure 34. Output Voltage vs Temperature

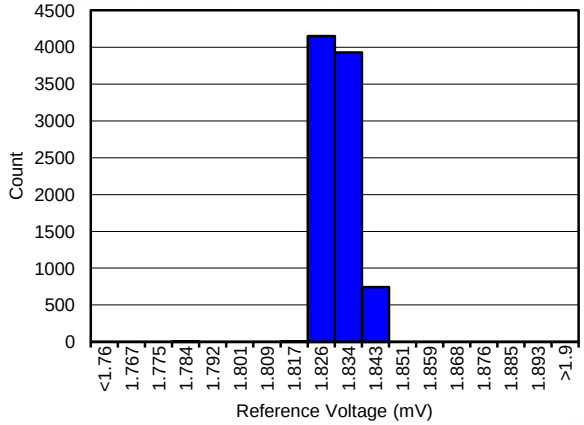


Figure 35. Reference Voltage (V_{OUTN}) Distribution

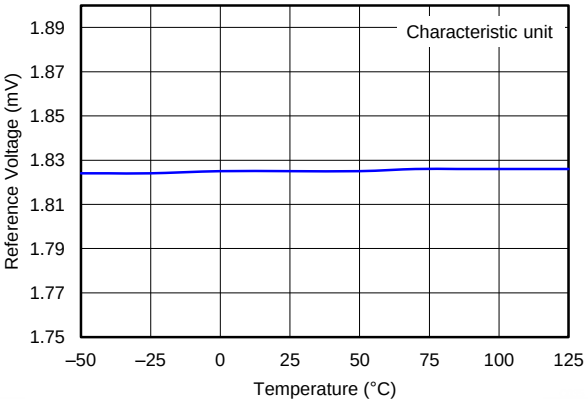


Figure 36. Reference Voltage (V_{OUTN}) vs Temperature

7 Detailed Description

7.1 Overview

The OPA857 provides a unique combination of low-noise, high-bandwidth, and high-transimpedance gain. The amplifier is optimized to achieve greater than 100-MHz bandwidth on either the 4.5-kΩ or 18.2-kΩ transimpedance gain for the lowest possible RMS noise on the output for a targeted low input capacitance of 1.5 pF. Note that this 1.5-pF capacitance includes the board parasitic; thus, great attention must be placed on minimizing stray capacitance in the layout. This value is selected because the device is expected to be driven by a photodiode with biasing high enough to include the photodiode capacitance contribution between approximately 0.5 pF and 0.7 pF, leaving between 0.8 pF to 1 pF for the external parasitic.

The OPA857 is a dedicated transimpedance amplifier with a pseudo-differential output. A block diagram is provided in the Functional Block Diagram section.

There are four distinct blocks in this diagram: a transimpedance amplifier (TIA), a reference voltage (REF), a test structure (TEST), and an internal clamping circuit (CLAMP).

The TIA block of the Functional Block Diagram includes two selectable gain configurations: R_{F1} and R_{F2}. For a 500-Ω load, including the GND alternatives resulting from the internal 25-Ω series resistor on each output, the resulting gain is 4.5 kΩ or 18.2 kΩ. The TIA block is designed to provide excellent bandwidth (> 100 MHz) in both gain configurations with the lowest possible RMS noise over the entire bandwidth. This level of performance is achieved by minimizing the noise gain peaking at higher frequencies. The noise gain peaking resulting from feedback and source capacitance is the main noise contributor in high-speed transimpedance amplifiers.

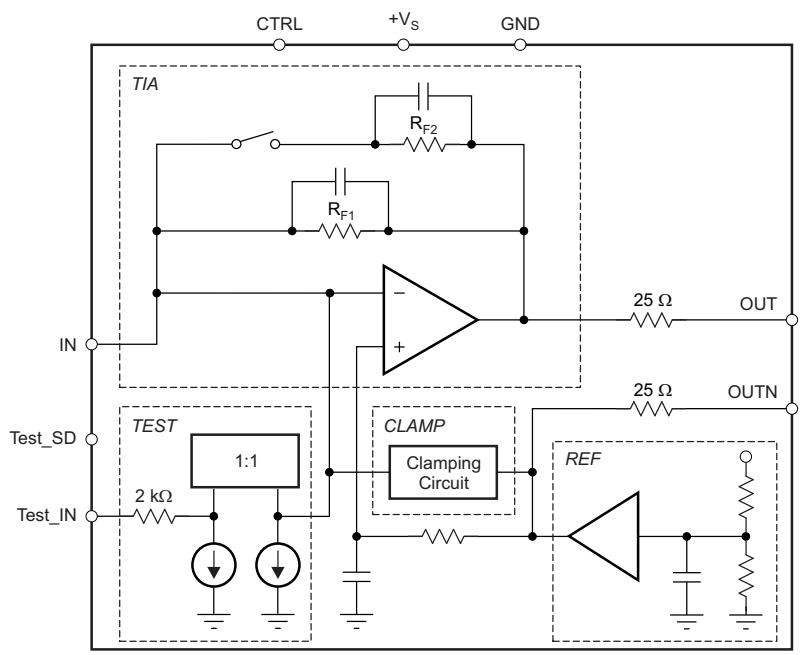
The reference voltage block of the Functional Block Diagram has several purposes: this block provides an adequate dc reference voltage to the input, and provides a dc reference at the output (thus allowing the dc-coupled solution to interface to a fully-differential signal chain). The CMRR provided by the fully-differential signal chain reduces any feedthrough from the OPA857 power supply, thereby increasing the PSRR of the amplifier.

The test structure block is available on the pinout, but the main purpose of this structure is to allow the device characterization to proceed as smoothly as possible.

The internal clamping circuit block and ESD diodes on the IN pin are used for internal protection and to make sure that the amplifier can recover quickly after saturation.

These blocks are each described in further detail in the *Feature Description* section.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Transimpedance Amplifier (TIA) Block

The amplifier of the TIA block has a class-A output stage, which limits its usable swing from the common-mode voltage of 1.83 V to the negative rail. Because the internal protection allows excellent overdrive recovery, the negative swing cannot go closer than 0.6 V to the rail. The resulting output dynamic range of the OPA857 on a +3.3-V supply is 1.2 V. This 1.2-V swing corresponds to a maximum input current of 60 µA in the high-gain configuration, and 240 µA in the low-gain configuration. A 25-Ω series resistance can also be found on OUT, which limits the loading the amplifier experiences providing protection against short-circuit conditions. These internal resistances on the output also reduce the overall gain. With a 500-Ω differential load, the attenuation resulting from the load is 0.83 dB, which affects the overall transimpedance gain. Because of the load attenuation, the 20-kΩ transimpedance gain is reduced to an effective 18.2 kΩ, while the 5-kΩ internal resistor gain is reduced to an effective 4.5-kΩ internal resistor.

7.3.2 Reference Voltage (REF) Block

The reference output voltage is set to be 5/9th of the power supply. Thus, for a single +3.3-V supply, the reference voltage is 1.83 V. The amplifier in the reference section is high bandwidth while maintaining low output impedance to high frequencies. After the amplifier, the reference voltage is provided to two paths: one path leads to the output (OUTN) through a 25-Ω series resistor; the other path goes to the noninverting input of the TIA block through an RC filter to minimize noise.

7.3.3 Integrated Test Structure (TEST) Block

In order to evaluate the low input capacitance condition on the input of the OPA857, simply evaluate the OPA857 performance without the photodiode. An integrated voltage-to-current conversion is implemented and can be accessed with the use of pins 13 and 14. This V-to-I converter structure is represented in Figure 37. If required, a capacitor can be added on the IN pin to match the desired operating conditions. This simple structure allows the emulation of a low-capacitance photodiode with minimum test equipment.

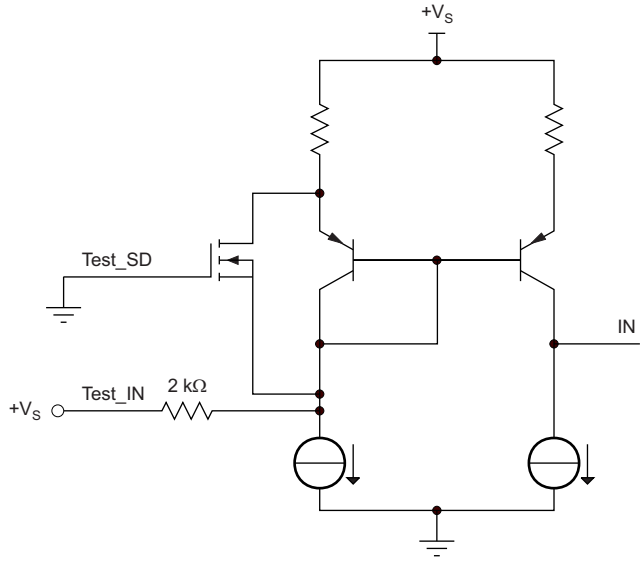


Figure 37. Internal V-to-I Converter

When using a photodiode, make sure that this source is turned off completely. This test structure is not intended to be used as a output dc-control voltage.

To eliminate any possible interaction between the internal current source and the photodiode, connect the Test_IN and Test_SD pins as described in Equation 1. To eliminate the current source from the schematic, Test_SD and Test_IN must be set as shown in Equation 1:

$$\text{Test\_SD} = \text{GND or floating, and Test\_IN} = \text{floating or } +V_S \quad (1)$$

Feature Description (continued)

When the internal V-to-I converter must be operated, set Test_SD to logic 1, turn on the internal current source, and set a voltage on Test_IN.

Set an adequate dc voltage at the input to make sure that the output is operating within normal operation. At minimum, the output of the TIA block must be set to 5/9th of the supply voltage in preparation for a pulse configuration. For sine-wave operation, as required when measuring a frequency response, set the dc voltage on the OUT pin to allow the full sine-wave amplitude and avoid clipping. In such a case, the OUT pin voltage is set lower than 5/9th of the supply voltage.

Note that the 2-kΩ internal resistance used for the V-to-I conversion is not trimmed and can vary ±15% with process. Therefore, the source must be capable of sourcing both dc and ac voltages to make sure that the output voltage swing is compliant with the class-A output stage of the TIA block. Any change in the test circuit configuration (such as gain change) requires a new calibration of the internal V-to-I converter.

Again if a photodiode is used, the internal V-to-I converter must be shut off completely. Failure to do so results in degraded performance and higher than normal quiescent current.

7.3.4 Internal Clamping Circuit (CLAMP) Block

The OPA857 is built using a very high-speed, complementary, BICMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 38.

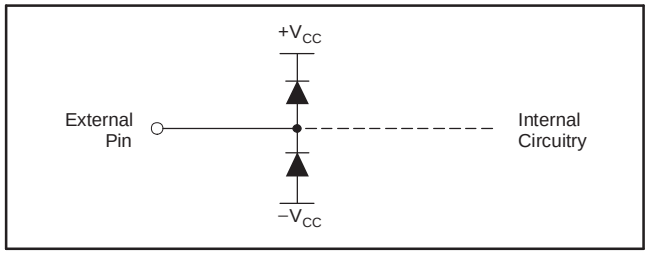


Figure 38. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Use additional external low-capacitance protection where higher currents are possible.

7.4 Device Functional Modes

7.4.1 Gain Control

The device transimpedance gain is controlled with the CTRL pin. Setting the CTRL pin high results in selecting the high-gain configuration. Setting the CTRL pin low results in selecting the low-gain configuration, as described in Table 1.

Table 1. Gain Control Logic Table

GAIN	CTRL (Pin 2)
4.5 kΩ	0
18.2 kΩ	1

8 Application and Implementation

8.1 Application Information

The OPA857 is a transimpedance amplifier offering two selectable gains. This device is used in conjunction with a photodiode at its input. The output is pseudo differential and may or may not require the use of a fully differential amplifier, depending on the analog-to-digital converter (ADC) used for implementation. The Detailed Design Procedures section describes the implementation.

8.2 Typical Application

The OPA857 requires a photodiode to be connected to the positive bias voltage because the output voltage can only swing down from the reference voltage (+1.85 V for a +3.3-V supply) to ground. Figure 39 presents the signal chain before and after the OPA857.

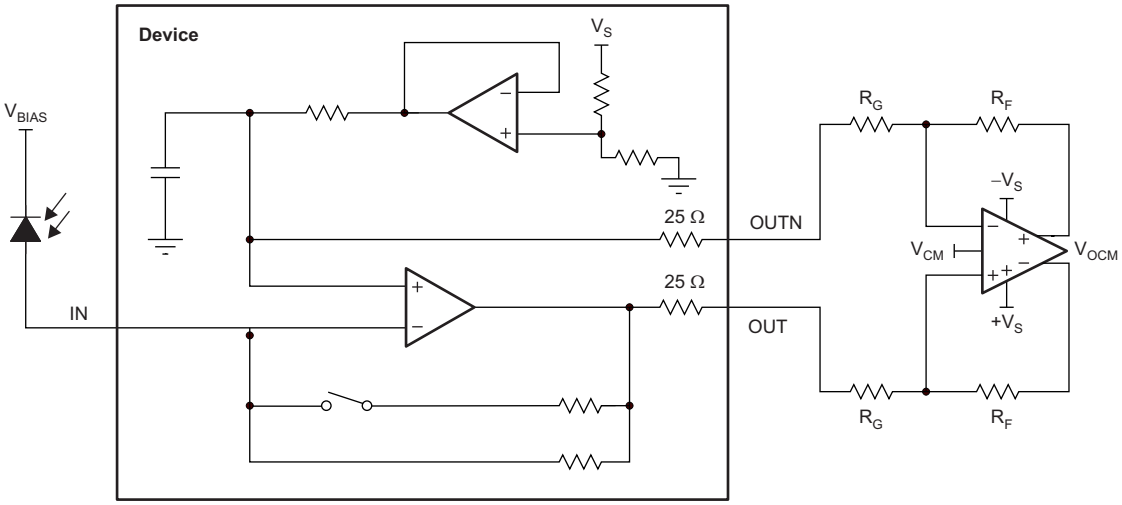


Figure 39. TIA with Associated Signal Chain

8.2.1 Design Requirements

For this example, use the values listed in Table 2 for the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage	3.3 V
Photodiode and loayout parasitic equivalent input capacitance	1.5 pF
Post-TIA gain resistors (2 × R_G)	500 Ω

8.2.2 Detailed Design Procedures

Maintain a 200-Ω differential minimum load to make sure that the device bandwidth is not reduced because the open-loop gain of the OPA857 varies with loading; refer to Figure 1 and Figure 3 in the Typical Characteristics section. At a 100-Ω differential load, the OPA857 has an 87-MHz bandwidth instead of 130 MHz. In the high-gain configuration, heavier loading also has higher attenuation that further reduces the amplifier gain for a 500-Ω load resistance. Suitable fully-differential amplifiers for the signal chain have a sufficient 0.1-dB to 100-MHz bandwidth to make sure that the overall system performance is not reduced. Figure 39 shows a diagram of an associated signal chain.

8.2.2.1 Signal Chain

For a system composed of two first-order elements with a –3-dB bandwidth of f_0 and f_1, the resulting bandwidth is set by Equation 2 and Equation 3:

$$f_{resulting} = \sqrt{f_0 \times f_1} \tag{2}$$

$$Q = \sqrt{\frac{f_0 \times f_1}{f_0 + f_1}} \tag{3}$$

The equivalent -3dB bandwidth for the system is then $f_{equivalent} = f_{resulting} \times Q$. The resulting noise power bandwidth (NPBW) is given by Equation 4:

$$NPBW = \sqrt{\frac{\pi}{2 \times Q \times f_{resulting}}} \tag{4}$$

A short list of suitable fully-differential amplifiers is provided in Table 3.

Table 3. Fully-Differential Amplifier Selection

AMPLIFIER	QUIESCENT CURRENT	-3-dB BANDWIDTH	FEEDBACK RESISTOR	DESCRIPTION
THS4520	13 mA	600 MHz	499 Ω	Rail-to-rail output
THS4521	1 mA	135 MHz	1000 Ω	Rail-to-rail output, low I_Q, limited bandwidth

The fully-differential amplifiers listed in Table 3 offer a good compromise between the OPA857 loading, while maintaining good gain and bandwidth. Note that the noise of the second stage in a high-speed transimpedance amplifier signal chain is not critical because the noise is dominated by the input stage. Also note that the THS4521 is selected for its low quiescent current and may not prove sufficient for higher bandwidth systems.

A summary of the recommended OPA857 implementation followed by a fully-differential amplifier is:

- Keep the trace length between the OPA857 and the fully-differential amplifier low to minimize reflection.
- For optimum bandwidth, keep the differential load detected by the OPA857 above 500 Ω.
- Ideally, select a fully-differential amplifier with 0.1-dB flatness in excess of 100 MHz to make sure that the overall frequency response is not affected.
- Gain can be added after the device without affecting SNR because the noise is dominated by the device stage.
- The common-mode output voltage of 5/9th × V_S of the OPA857 must be within the acceptable CMIR of the selected fully-differential amplifier.
- Although single-ended to differential conversions for connecting the device to the fully-differential amplifier is acceptable, best noise performance is achieved with the fully-differential connection described in Figure 39.
- The fully-differential connection has the advantage of reducing any common-mode signal. This reduction includes device power-supply variation, thus enhancing the PSRR capability of the circuit.

8.2.2.2 Noise, Bandwidth, and Input Capacitance Considerations

In a dedicated device such as a fixed gain transimpedance amplifier, where the input capacitance and load are carefully weighted and traded upon one another, understanding how the input capacitance specification, bandwidth, and the resulting noise behave is important.

As stated previously, the source input capacitance must stay low because of the fixed transimpedance configuration and associated internal compensation. The nominal design target is 1.5 pF, which includes board parasitic. For maximum flatness, do not exceed a total input capacitance of 5 pF in the low-gain configuration. At a 5-pF input capacitance, the OPA857 in the high-gain configuration peaks at 1.5 dB, as shown in Figure 40 and Figure 41. This frequency peaking is expressed as overshoot in the time domain.

The internal compensation also affects the open-loop gain of the amplifier and is normally designed for one value, with an allowable range of operation. This loop-gain variation with the load resistance results in bandwidth variation with load resistance. This effect is normally small for a heavy-duty line driver, but may be more visible for receiver amplifiers such as the OPA857. The heavier the load, the lower the bandwidth is going to be, as shown in Figure 42 through Figure 45. Note that the high-gain configuration is more sensitive than the low-gain configuration for heavier loads. Unless high-impedance buffers are used (one for each output immediately after the OPA857), the load is normally the gain resistor of a fully-differential amplifier. A programmable gain amplifier can also be used here, but because these amplifiers are generally intended for wireless infrastructure applications, the differential input impedance of the PGA is typically 150 Ω.

8.2.2.3 Thermal Analysis

Maximum-desired junction temperature sets the maximum allowed internal power dissipation, as described in this section. Do not exceed the absolute maximum rating.

Operating junction temperature (T_J) is given by Equation 5:

$$T_A + P_D \times \theta_{JA} \tag{5}$$

The total internal power dissipation (P_D) is the sum of the quiescent power (P_{DQ}) and any additional power dissipated in the output stage (P_{DL}) to deliver the output current. In the case of the OPA857, because the device has a low drive capability, consider the output-current induced P_{DL} to be negligible compared to the quiescent-power induced P_{DQ}.

As a worst-case example, compute the maximum T_J using an OPA857 in the circuit of Figure 39 operating at the maximum specified ambient temperature of +95°C. Equation 6 and Equation 7 calculate P_D and maximum T_J, respectively.

$$P_D = 3.3\ \text{V} \times 26.8\ \text{mA} = 88.5\ \text{mW} \tag{6}$$

$$\text{Maximum } T_J = +95°\text{C} + (0.09\ \text{W} \times 39.5°\text{C/W}) = 98.5°\text{C} \tag{7}$$

Although this result is still well below the specified maximum junction temperature, system reliability considerations may require lower tested junction temperatures.

8.2.3 Application Curves

Figure 40 through Figure 45 show frequency response and input referred noise for both gain configuration for several source input capacitance.

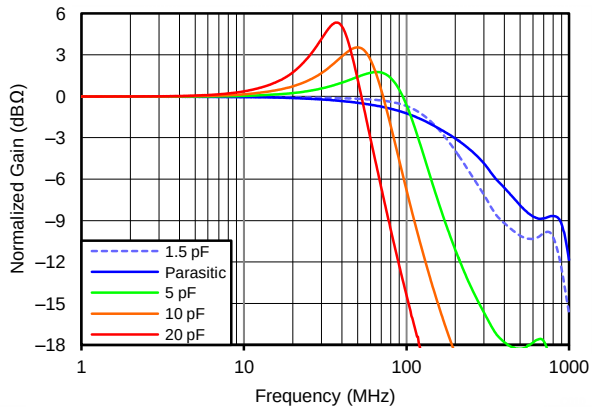


Figure 40. 18.2-kΩ Gain Frequency Response vs Input Capacitance

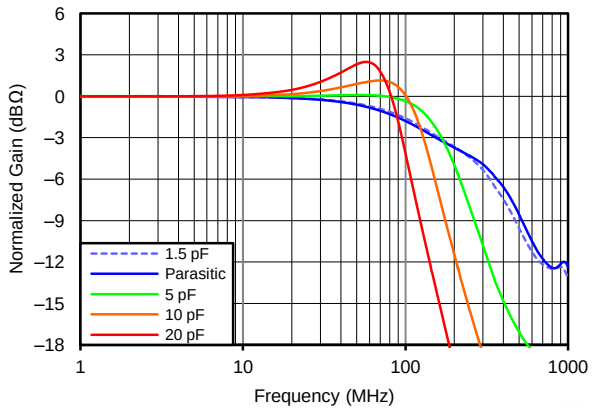


Figure 41. 4.5-kΩ Gain Frequency Response vs Input Capacitance

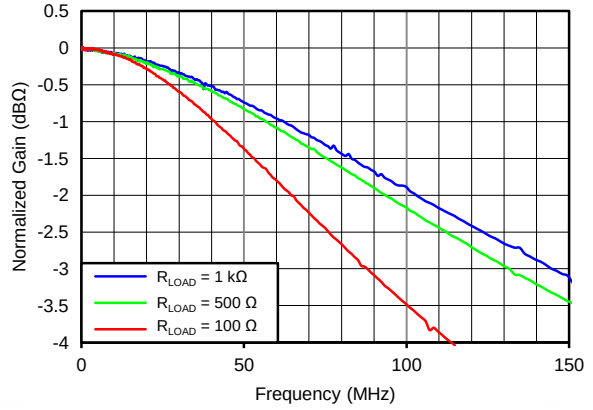


Figure 42. 18.2-kΩ Gain Frequency Response

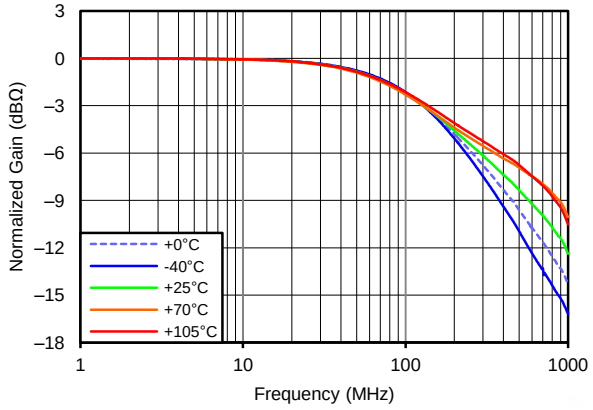


Figure 43. 18.2-kΩ Gain Frequency Response vs Temperature

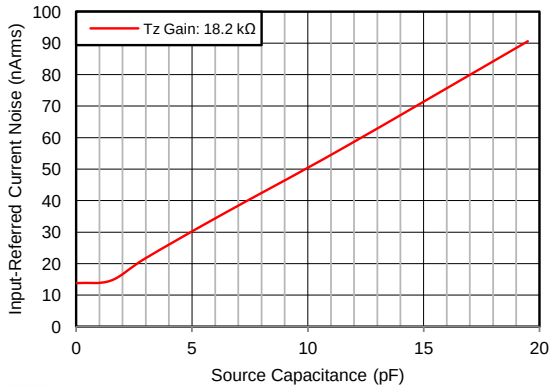


Figure 44. 18.2-kΩ Gain RMS Input-Referred Current Noise vs Capacitance

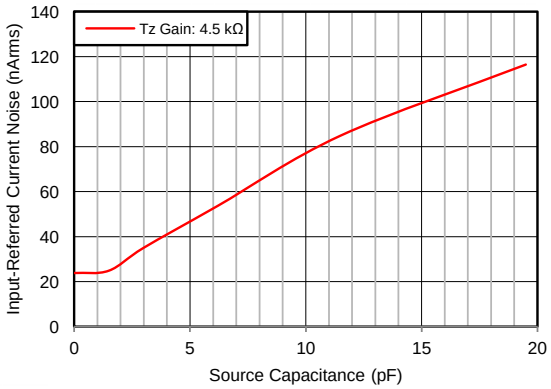


Figure 45. 4.5-kΩ Gain RMS Input-Referred Current Noise vs Capacitance

9 Power-Supply Recommendations

Use a linear power supply with good PSRR. For a good, high-frequency, power-supply bypass, use a ceramic capacitor connected as close as possible to the $+V_S$ pin.

10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the OPA857 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

a. **Minimize parasitic capacitance** to any ac ground for all signal I/O pins. Parasitic capacitance on the inverting input pin can cause instability. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.

b. **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1-µF decoupling capacitors, as shown in Figure 46. At the device pins, make sure that the ground and power-plane layout are not in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and decoupling capacitors. Always decouple the power-supply connections with these capacitors. An optional supply decoupling capacitor (0.1 µF) across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Use larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at lower frequencies, on the main supply pins. These capacitors can be placed somewhat farther from the device and can be shared among several devices in the same area of the PC board.

c. **Careful selection and placement of external components preserves the high-frequency performance of the OPA857.** Use very low reactance type resistors. Surface-mount resistors function best and allow a tighter overall layout. Metal-film or carbon composition, axially-leaded resistors also provide good high-frequency performance. Again, keep the leads and PC board traces as short as possible. Never use wirewound type resistors in a high-frequency application.

d. **Connections to other wideband devices** on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them.

e. **Do not socket a high-speed part such as the OPA857.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the OPA857 onto the board.

10.2 Layout Example

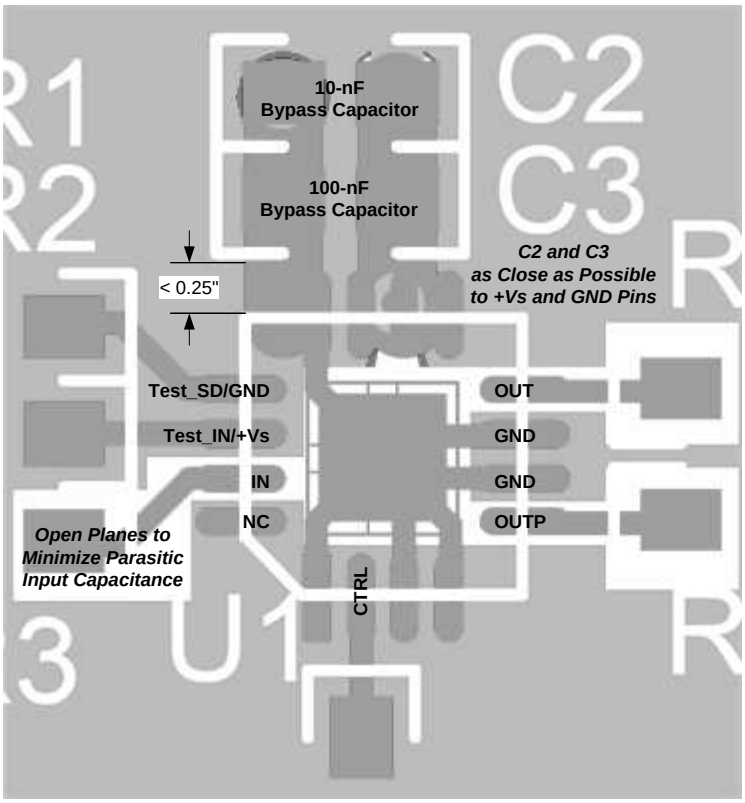


Figure 46. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the OPA857. The summary information for this fixture is shown in Table 4.

Table 4. EVM Ordering Information

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA857IRGT	RGT	OPA857EVM	SBOU138

The EVM can be requested at the Texas Instruments web site (www.ti.com) through the OPA857 product folder.

11.1.1.2 Spice Model

Computer simulation of circuit performance using spice is often useful when analyzing the performance of analog circuits and systems. The previous statement is particularly true for transimpedance applications where parasitic capacitance and inductance can have a major effect on circuit performance. A spice model for the OPA857 is available through the OPA857 product folder under simulation models. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. These models, however, do not do as well in predicting harmonic distortion.

11.2 Documentation Support

11.2.1 Related Documentation

SBOU138 — *OPA857EVM user's guide*.

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA857IRGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 95	OPA857	Samples
OPA857IRGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 95	OPA857	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

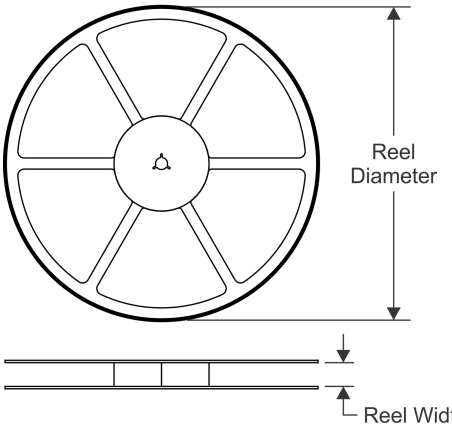
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

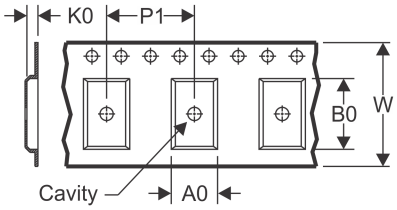
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

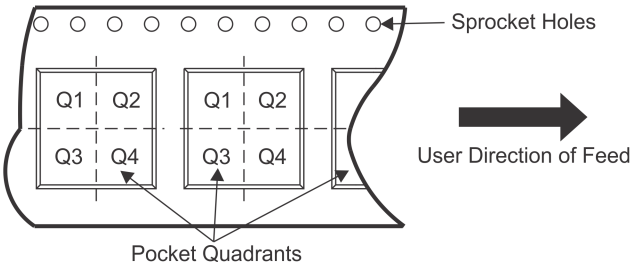


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

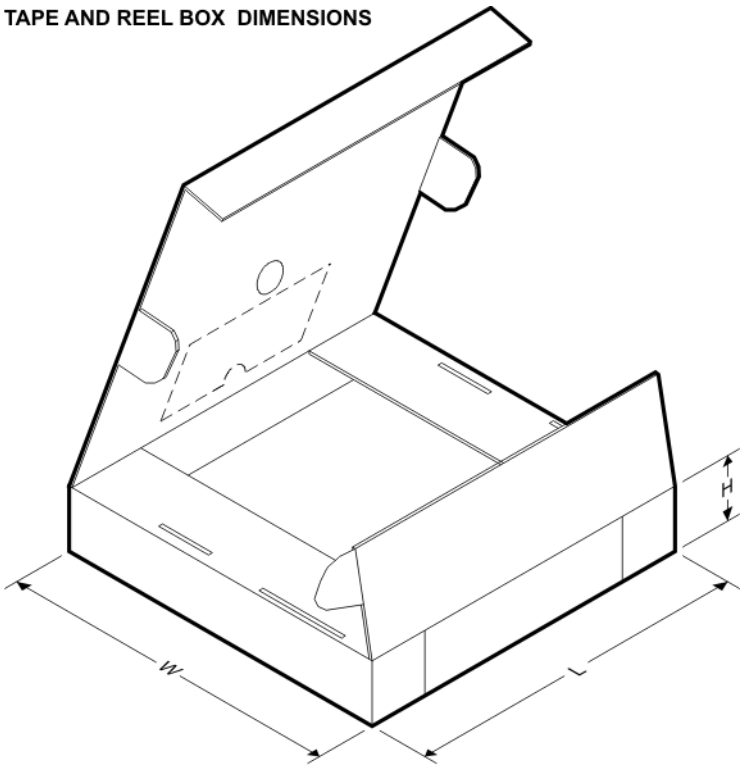
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA857IRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA857IRGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

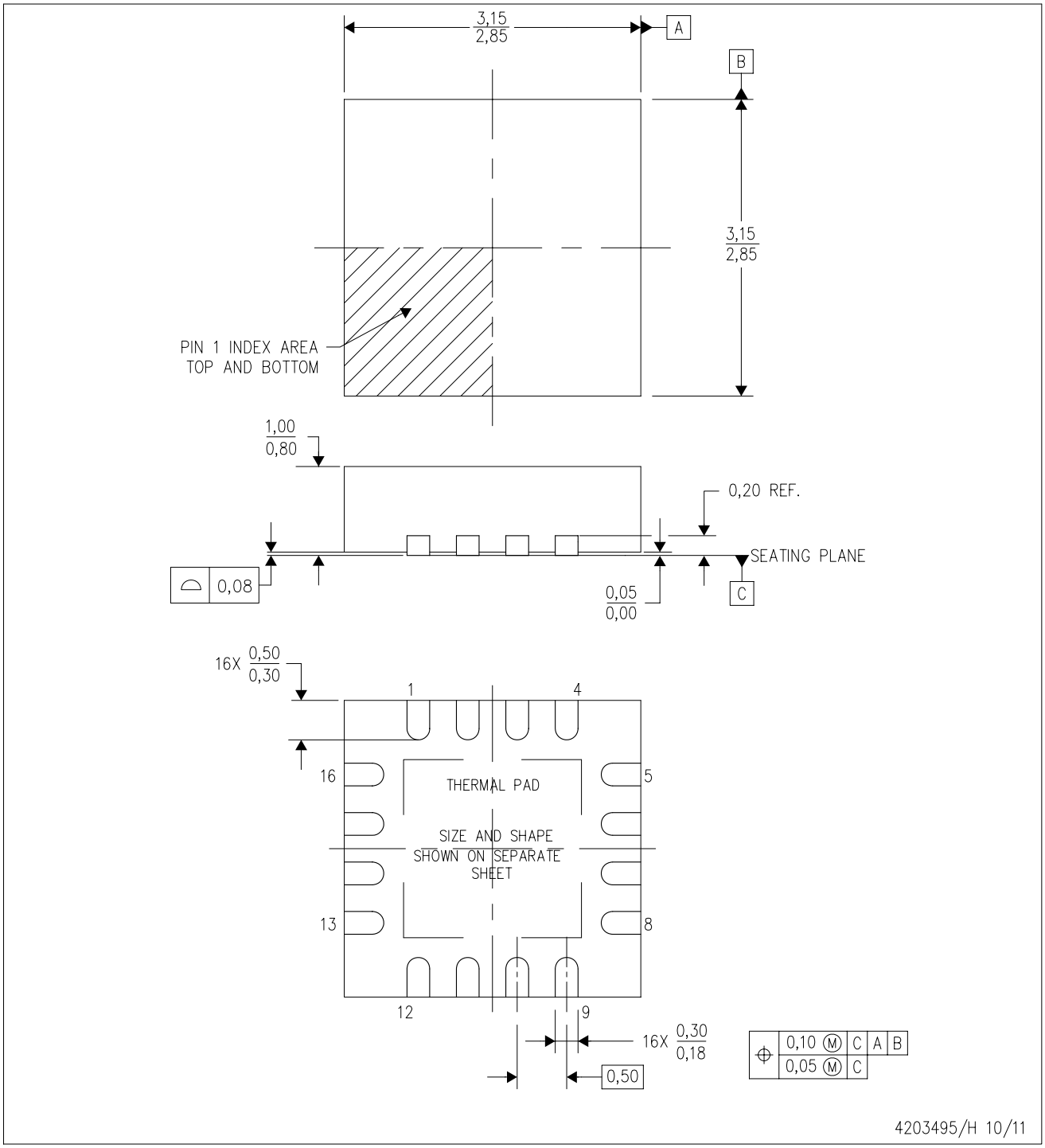
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA857IRGTR	QFN	RGT	16	3000	367.0	367.0	35.0
OPA857IRGTT	QFN	RGT	16	250	210.0	185.0	35.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

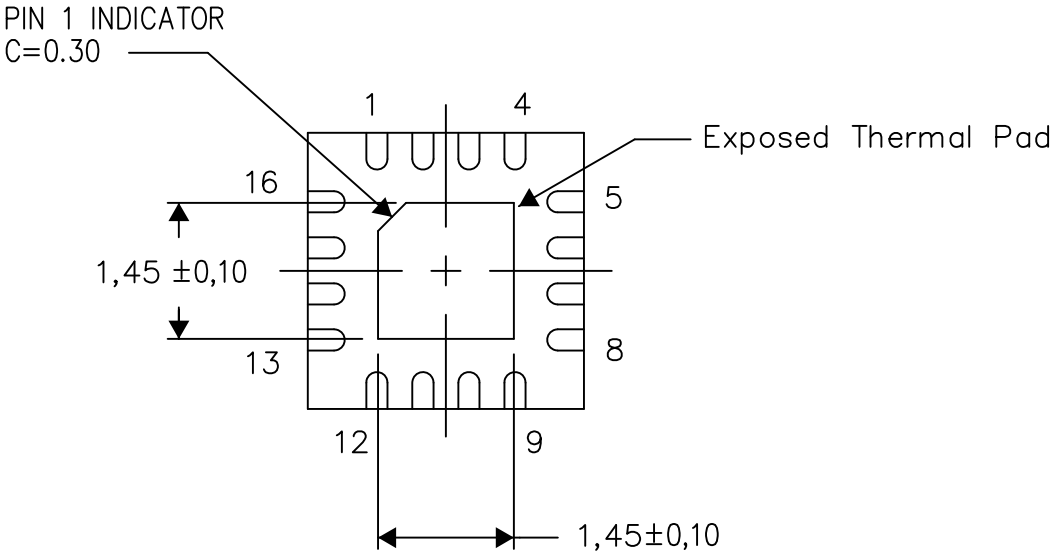
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



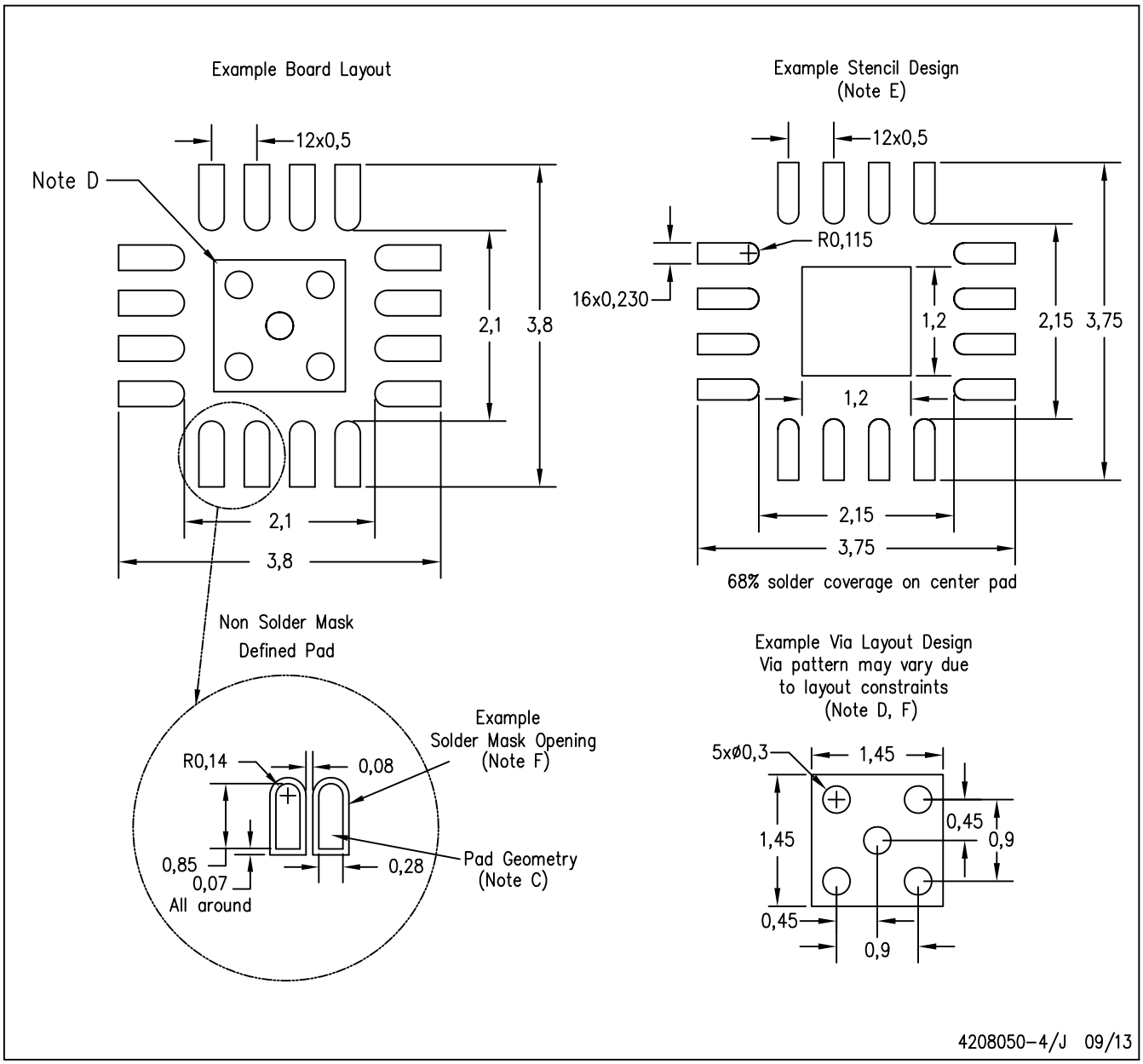
Bottom View

Exposed Thermal Pad Dimensions

4206349–2/U 09/13

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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