

# 74HC273; 74HCT273

Octal D-type flip-flop with reset; positive-edge trigger

Rev. 03 — 24 January 2006

Product data sheet

## 1. General description

The 74HC273; 74HCT273 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC273; 74HCT273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (pin CP) and master reset (pin  $\overline{\text{MR}}$ ) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the  $\overline{\text{MR}}$  input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

## 2. Features

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-C exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Quick reference data

**Table 1: Quick reference data**  
 $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74HC273</b>						
$t_{\text{PHL}}$ , $t_{\text{PLH}}$	propagation delay CP to Qn	$V_{\text{CC}} = 5\text{ V}$ ; $C_L = 15\text{ pF}$	-	15	-	ns
$t_{\text{PHL}}$	HIGH-to-LOW propagation delay $\overline{\text{MR}}$ to Qn	$V_{\text{CC}} = 5\text{ V}$ ; $C_L = 15\text{ pF}$	-	15	-	ns
$f_{\text{max}}$	maximum input clock frequency	$V_{\text{CC}} = 5\text{ V}$ ; $C_L = 15\text{ pF}$	-	66	-	MHz

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**Table 1: Quick reference data ...continued** $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f = 6\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_i$	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance	per flip-flop; $V_i = GND$ to $V_{CC}$	[1]	20	-	pF
<b>74HCT273</b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to Qn	$V_{CC} = 5\text{ V}$ ; $C_L = 15\text{ pF}$	-	15	-	ns
$t_{PHL}$	HIGH-to-LOW propagation delay MR to Qn	$V_{CC} = 5\text{ V}$ ; $C_L = 15\text{ pF}$	-	20	-	ns
$f_{max}$	maximum input clock frequency	$V_{CC} = 5\text{ V}$ ; $C_L = 15\text{ pF}$	-	36	-	MHz
$C_i$	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance	per flip-flop; $V_i = GND$ to $(V_{CC} - 1.5\text{ V})$	[1]	23	-	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where: $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = output load capacitance in pF; $V_{CC}$  = supply voltage in V; $N$  = number of inputs switching; $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 4. Ordering information

**Table 2: Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
<b>74HC273</b>				
74HC273N	-40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HC273D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC273DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HC273PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HC273BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
<b>74HCT273</b>				
74HCT273N	-40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT273D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

Table 2: Ordering information ...continued

Type number	Package			Version
	Temperature range	Name	Description	
74HCT273DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT273PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT273BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

## 5. Functional diagram

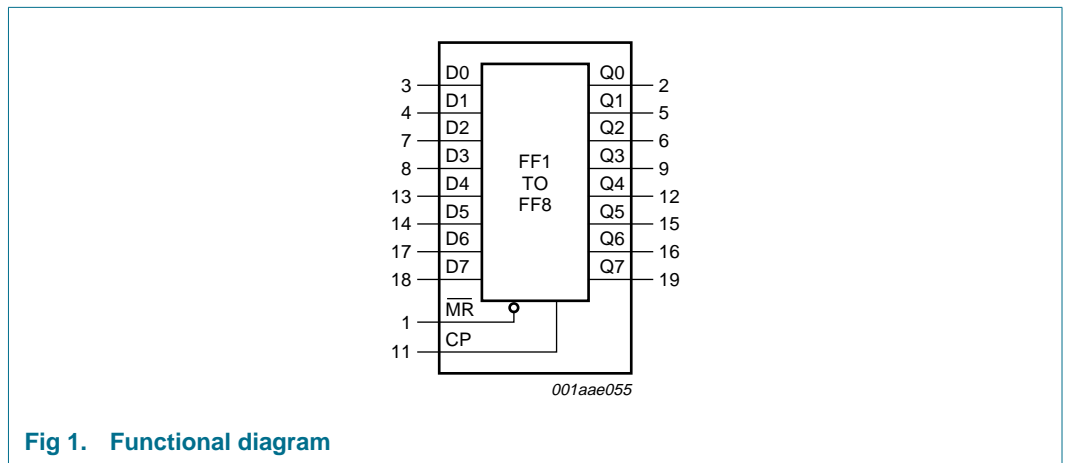


Fig 1. Functional diagram

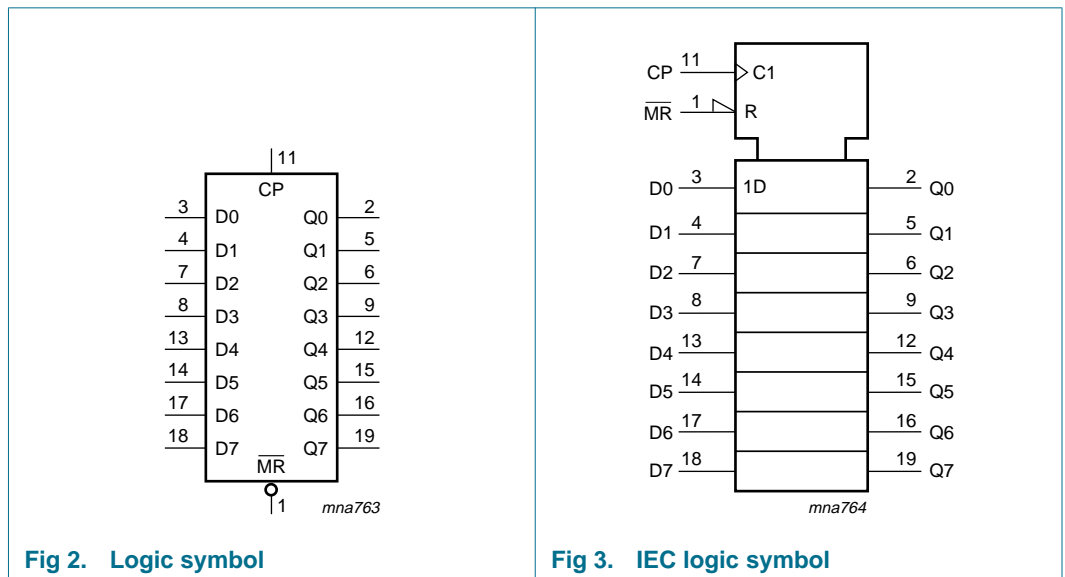


Fig 2. Logic symbol

Fig 3. IEC logic symbol

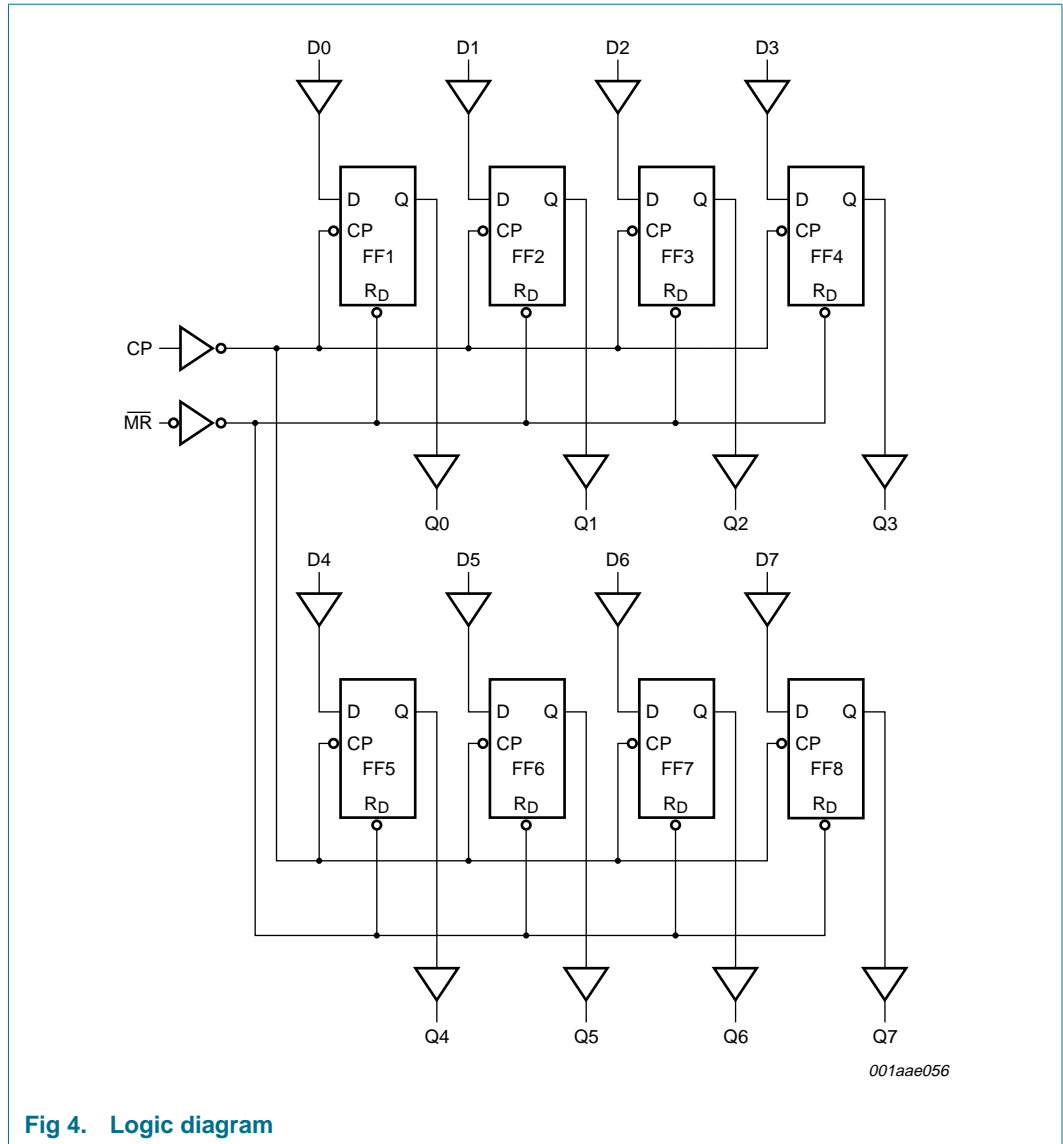
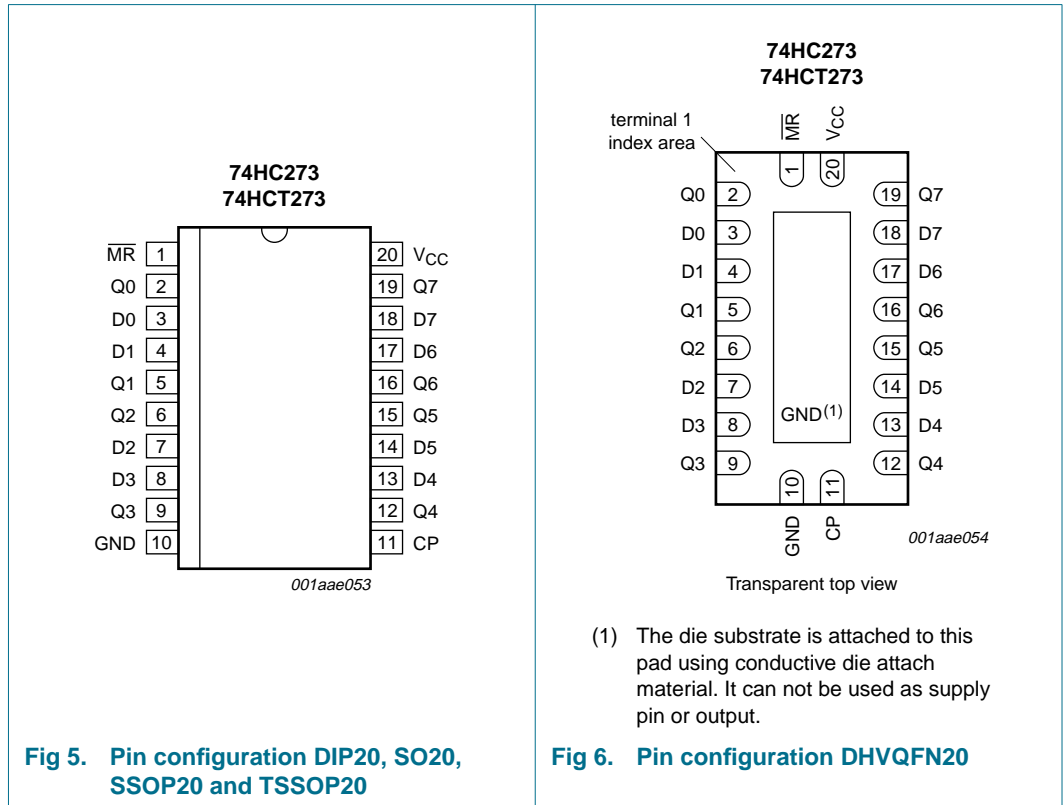


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
MR	1	master reset input (active LOW)
Q0	2	flip-flop output 0
D0	3	data input 0
D1	4	data input 1
Q1	5	flip-flop output 1
Q2	6	flip-flop output 2
D2	7	data input 2
D3	8	data input 3
Q3	9	flip-flop output 3
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge-triggered)
Q4	12	flip-flop output 4
D4	13	data input 4
D5	14	data input 5

Table 3: Pin description ...continued

Symbol	Pin	Description
Q5	15	flip-flop output 5
Q6	16	flip-flop output 6
D6	17	data input 6
D7	18	data input 7
Q7	19	flip-flop output 7
V <sub>CC</sub>	20	supply voltage

## 7. Functional description

### 7.1 Function table

Table 4: Function table [1]

Operating modes	Control		Input	Output
	$\overline{\text{MR}}$	CP	Dn	Qn
Reset (clear)	L	X	X	L
Load 1	H	↑	h	H
Load 0	H	↑	l	L

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 ↑ = LOW-to-HIGH transition;  
 X = don't care.

## 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>O</sub>	output current	V <sub>O</sub> = -0.5 V to (V <sub>CC</sub> + 0.5 V)	-	±25	mA
I <sub>CC</sub>	quiescent supply current		-	50	mA
I <sub>GND</sub>	ground current		-	-50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C

**Table 5: Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation				
	DIP20 package		[1] -	750	mW
	SO20 package		[2] -	500	mW
	SSOP20 package		[3] -	500	mW
	TSSOP20 package		[3] -	500	mW
	DHVQFN20 package		[4] -	500	mW

[1] For DIP20 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

[2] For SO20 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

[3] For SSOP20 and TSSOP20 packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN20 packages: P<sub>tot</sub> derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74HC273</b>						
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall time	V <sub>CC</sub> = 2.0 V	-	-	1000	ns
		V <sub>CC</sub> = 4.5 V	-	6.0	500	ns
		V <sub>CC</sub> = 6.0 V	-	-	400	ns
<b>74HCT273</b>						
V <sub>CC</sub>	supply voltage		4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall time	V <sub>CC</sub> = 4.5 V	-	6.0	500	ns

## 10. Static characteristics

**Table 7: Static characteristics 74HC273**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	V

**Table 7: Static characteristics 74HC273 ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	V
V <sub>OH</sub>	HIGH-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	V
V <sub>OL</sub>	LOW-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.5	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	μA
C <sub>i</sub>	input capacitance		-	3.5	-	pF
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	-	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.84	-	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.34	-	-	V
V <sub>OL</sub>	LOW-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.33	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	-	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±1.0	μA



**Table 7: Static characteristics 74HC273 ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±5.0	µA
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	80	µA
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>						
$V_{IH}$	HIGH-state input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 4.5$ V	3.15	-	-	V
		$V_{CC} = 6.0$ V	4.2	-	-	V
$V_{IL}$	LOW-state input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 4.5$ V	-	-	1.35	V
		$V_{CC} = 6.0$ V	-	-	1.8	V
$V_{OH}$	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$	-	-	-	
		$I_O = -20$ µA; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -20$ µA; $V_{CC} = 6.0$ V	5.9	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.7	-	-	V
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$	-	-	-	
		$I_O = 20$ µA; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 6.0$ V	-	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	-	0.4	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±1.0	µA
		$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±10.0	µA
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±10.0	µA
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	160	µA

**Table 8: Static characteristics 74HCT273**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25</math> °C</b>						
$V_{IH}$	HIGH-state input voltage	$V_{CC} = 4.5$ V to $5.5$ V	2.0	1.6	-	V
$V_{IL}$	LOW-state input voltage	$V_{CC} = 4.5$ V to $5.5$ V	-	1.2	0.8	V
$V_{OH}$	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V	-	-	-	
		$I_O = -20$ µA	4.4	4.5	-	V
		$I_O = -4.0$ mA	3.98	4.32	-	V
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V	-	-	-	
		$I_O = 20$ µA	-	0	0.1	V
		$I_O = 4.0$ mA	-	0.15	0.26	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	µA

**Table 8: Static characteristics 74HCT273 ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O = 0$ A	-	-	$\pm 0.5$	$\mu$ A
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	$\mu$ A
$\Delta I_{CC}$	additional quiescent supply current	$V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
	pin $\overline{MR}$		-	100	360	$\mu$ A
	pin CP		-	175	630	$\mu$ A
	pin Dn		-	15	54	$\mu$ A
$C_i$	input capacitance		-	3.5	-	pF
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>						
$V_{IH}$	HIGH-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
$V_{IL}$	LOW-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
$V_{OH}$	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V				
		$I_O = -20$ $\mu$ A	4.4	-	-	V
		$I_O = -4.0$ mA	3.84	-	-	V
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V				
		$I_O = 20$ $\mu$ A	-	-	0.1	V
		$I_O = 4.0$ mA	-	-	0.33	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	$\pm 1.0$	$\mu$ A
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O = 0$ A	-	-	$\pm 5.0$	$\mu$ A
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	$\mu$ A
$\Delta I_{CC}$	additional quiescent supply current	$V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
	pin $\overline{MR}$		-	-	450	$\mu$ A
	pin CP		-	-	787.5	$\mu$ A
	pin Dn		-	-	67.5	$\mu$ A
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>						
$V_{IH}$	HIGH-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
$V_{IL}$	LOW-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
$V_{OH}$	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V				
		$I_O = -20$ $\mu$ A	4.4	-	-	V
		$I_O = -4.0$ mA	3.7	-	-	V
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V				
		$I_O = 20$ $\mu$ A	-	-	0.1	V
		$I_O = 4.0$ mA	-	-	0.4	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	$\pm 1.0$	$\mu$ A

**Table 8:** Static characteristics 74HCT273 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O = 0$ A	-	-	±10	µA
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160	µA
$\Delta I_{CC}$	additional quiescent supply current	$V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
	pin $\overline{MR}$		-	-	490	µA
	pin CP		-	-	857.5	µA
	pin Dn		-	-	73.5	µA

## 11. Dynamic characteristics

**Table 9:** Dynamic characteristics 74HC273

Voltages are referenced to GND (ground = 0 V);  $t_r = t_f = 6$  ns;  $C_L = 50$  pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25</math> °C</b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to Qn	see <a href="#">Figure 7</a>				
		$V_{CC} = 2.0$ V	-	41	150	ns
		$V_{CC} = 4.5$ V	-	15	30	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	ns
		$V_{CC} = 6.0$ V	-	13	26	ns
$t_{PHL}$	HIGH-to-LOW propagation delay MR to Qn	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0$ V	-	44	150	ns
		$V_{CC} = 4.5$ V	-	16	30	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	ns
		$V_{CC} = 6.0$ V	-	14	26	ns
$t_{THL}$ , $t_{TLH}$	output transition time	see <a href="#">Figure 7</a>				
		$V_{CC} = 2.0$ V	-	19	75	ns
		$V_{CC} = 4.5$ V	-	7	15	ns
		$V_{CC} = 6.0$ V	-	6	13	ns
$t_w$	pulse width					
	clock HIGH or LOW	see <a href="#">Figure 7</a>				
		$V_{CC} = 2.0$ V	80	14	-	ns
		$V_{CC} = 4.5$ V	16	5	-	ns
		$V_{CC} = 6.0$ V	14	4	-	ns
	master reset LOW	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0$ V	60	17	-	ns
		$V_{CC} = 4.5$ V	12	6	-	ns
		$V_{CC} = 6.0$ V	10	5	-	ns

**Table 9: Dynamic characteristics 74HC273 ...continued**

Voltages are referenced to GND (ground = 0 V);  $t_r = t_f = 6$  ns;  $C_L = 50$  pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{rec}$	recovery time $\overline{MR}$ to CP	see <a href="#">Figure 8</a>					
		$V_{CC} = 2.0$ V	+50	-6	-	ns	
		$V_{CC} = 4.5$ V	+10	-2	-	ns	
		$V_{CC} = 6.0$ V	+9	-2	-	ns	
$t_{su}$	set-up time Dn to CP	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0$ V	60	11	-	ns	
		$V_{CC} = 4.5$ V	12	4	-	ns	
		$V_{CC} = 6.0$ V	10	3	-	ns	
$t_h$	hold time Dn to CP	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0$ V	+3	-6	-	ns	
		$V_{CC} = 4.5$ V	+3	-2	-	ns	
		$V_{CC} = 6.0$ V	+3	-2	-	ns	
$f_{max}$	maximum input clock frequency	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0$ V	6.0	20.6	-	MHz	
		$V_{CC} = 4.5$ V	30	103	-	MHz	
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	66	-	MHz	
		$V_{CC} = 6.0$ V	35	122	-	MHz	
$C_{PD}$	power dissipation capacitance	per flip-flop; $V_I = GND$ to $V_{CC}$	<a href="#">(1)</a> -	20	-	pF	
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>							
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to Qn	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0$ V	-	-	185	ns	
		$V_{CC} = 4.5$ V	-	-	37	ns	
		$V_{CC} = 6.0$ V	-	-	31	ns	
$t_{PHL}$	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	see <a href="#">Figure 8</a>					
		$V_{CC} = 2.0$ V	-	-	185	ns	
		$V_{CC} = 4.5$ V	-	-	37	ns	
		$V_{CC} = 6.0$ V	-	-	31	ns	
$t_{THL}$ , $t_{TLH}$	output transition time	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0$ V	-	-	95	ns	
		$V_{CC} = 4.5$ V	-	-	19	ns	
		$V_{CC} = 6.0$ V	-	-	15	ns	
$t_w$	pulse width	clock HIGH or LOW	see <a href="#">Figure 7</a>				
			$V_{CC} = 2.0$ V	100	-	-	ns
			$V_{CC} = 4.5$ V	20	-	-	ns
			$V_{CC} = 6.0$ V	17	-	-	ns
	master reset LOW	see <a href="#">Figure 8</a>					
		$V_{CC} = 2.0$ V	75	-	-	ns	
		$V_{CC} = 4.5$ V	15	-	-	ns	
		$V_{CC} = 6.0$ V	13	-	-	ns	

**Table 9: Dynamic characteristics 74HC273 ...continued**

Voltages are referenced to GND (ground = 0 V);  $t_r = t_f = 6$  ns;  $C_L = 50$  pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{rec}$	recovery time $\overline{MR}$ to CP	see <a href="#">Figure 8</a>					
		$V_{CC} = 2.0$ V	65	-	-	ns	
		$V_{CC} = 4.5$ V	13	-	-	ns	
		$V_{CC} = 6.0$ V	11	-	-	ns	
$t_{su}$	set-up time Dn to CP	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0$ V	75	-	-	ns	
		$V_{CC} = 4.5$ V	15	-	-	ns	
		$V_{CC} = 6.0$ V	13	-	-	ns	
$t_h$	hold time Dn to CP	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0$ V	3	-	-	ns	
		$V_{CC} = 4.5$ V	3	-	-	ns	
		$V_{CC} = 6.0$ V	3	-	-	ns	
$f_{max}$	maximum input clock frequency	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0$ V	4.8	-	-	MHz	
		$V_{CC} = 4.5$ V	24	-	-	MHz	
		$V_{CC} = 6.0$ V	28	-	-	MHz	
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>							
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to Qn	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0$ V	-	-	225	ns	
		$V_{CC} = 4.5$ V	-	-	45	ns	
		$V_{CC} = 6.0$ V	-	-	38	ns	
$t_{PHL}$	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	see <a href="#">Figure 8</a>					
		$V_{CC} = 2.0$ V	-	-	225	ns	
		$V_{CC} = 4.5$ V	-	-	45	ns	
		$V_{CC} = 6.0$ V	-	-	38	ns	
$t_{THL}$ , $t_{TLH}$	output transition time	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0$ V	-	-	110	ns	
		$V_{CC} = 4.5$ V	-	-	22	ns	
		$V_{CC} = 6.0$ V	-	-	19	ns	
$t_w$	pulse width clock HIGH or LOW	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0$ V	120	-	-	ns	
		$V_{CC} = 4.5$ V	24	-	-	ns	
		$V_{CC} = 6.0$ V	20	-	-	ns	
	master reset LOW	see <a href="#">Figure 8</a>					
		$V_{CC} = 2.0$ V	90	-	-	ns	
$V_{CC} = 4.5$ V		18	-	-	ns		
		$V_{CC} = 6.0$ V	15	-	-	ns	

**Table 9: Dynamic characteristics 74HC273 ...continued**

*Voltages are referenced to GND (ground = 0 V);  $t_r = t_f = 6$  ns;  $C_L = 50$  pF unless otherwise specified; for test circuit see Figure 10.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rec}$	recovery time $\overline{MR}$ to CP	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0$ V	75	-	-	ns
		$V_{CC} = 4.5$ V	15	-	-	ns
		$V_{CC} = 6.0$ V	13	-	-	ns
$t_{su}$	set-up time Dn to CP	see <a href="#">Figure 9</a>				
		$V_{CC} = 2.0$ V	90	-	-	ns
		$V_{CC} = 4.5$ V	18	-	-	ns
		$V_{CC} = 6.0$ V	15	-	-	ns
$t_h$	hold time Dn to CP	see <a href="#">Figure 9</a>				
		$V_{CC} = 2.0$ V	3	-	-	ns
		$V_{CC} = 4.5$ V	3	-	-	ns
		$V_{CC} = 6.0$ V	3	-	-	ns
$f_{max}$	maximum input clock frequency	see <a href="#">Figure 7</a>				
		$V_{CC} = 2.0$ V	4.0	-	-	MHz
		$V_{CC} = 4.5$ V	20	-	-	MHz
		$V_{CC} = 6.0$ V	24	-	-	MHz

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

**Table 10: Dynamic characteristics 74HCT273**

*Voltages are referenced to GND (ground = 0 V);  $t_r = t_f = 6$  ns;  $C_L = 50$  pF unless otherwise specified; for test circuit see Figure 10.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b><math>T_{amb} = 25</math> °C</b>							
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to Qn	see <a href="#">Figure 7</a>					
		$V_{CC} = 4.5$ V	-	16	30	ns	
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	ns	
$t_{PHL}$	HIGH-to-LOW propagation delay MR to Qn	see <a href="#">Figure 8</a>					
		$V_{CC} = 4.5$ V	-	23	34	ns	
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	20	-	ns	
$t_{THL}$ , $t_{TLH}$	output transition time	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	-	7	15	ns	
$t_W$	pulse width						
		clock HIGH or LOW	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	16	9	-	ns
		master reset LOW	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	16	8	-	ns

**Table 10: Dynamic characteristics 74HCT273 ...continued**

Voltages are referenced to GND (ground = 0 V);  $t_r = t_f = 6$  ns;  $C_L = 50$  pF unless otherwise specified; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{rec}$	recovery time $\overline{MR}$ to CP	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	+10	-2	-	ns	
$t_{su}$	set-up time Dn to CP	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	12	5	-	ns	
$t_h$	hold time Dn to CP	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	+3	-4	-	ns	
$f_{max}$	maximum input clock frequency	see <a href="#">Figure 7</a>					
		$V_{CC} = 4.5$ V	30	56	-	MHz	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	36	-	MHz	
$C_{PD}$	power dissipation capacitance	per flip-flop; $V_I = GND$ to $(V_{CC} - 1.5$ V) <a href="#">[1]</a>	-	23	-	pF	
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>							
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	-	-	38	ns	
$t_{PHL}$	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	-	-	43	ns	
$t_{THL}$ , $t_{TLH}$	output transition time	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	-	-	19	ns	
$t_W$	pulse width						
		clock HIGH or LOW	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	20	-	-	ns
		master reset LOW	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	20	-	-	ns
$t_{rec}$	recovery time $\overline{MR}$ to CP	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	13	-	-	ns	
$t_{su}$	set-up time Dn to CP	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	15	-	-	ns	
$t_h$	hold time Dn to CP	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	3	-	-	ns	
$f_{max}$	maximum input clock frequency	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	24	-	-	MHz	
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>							
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	-	-	45	ns	
$t_{PHL}$	HIGH-to-LOW propagation delay $\overline{MR}$ to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	-	-	51	ns	
$t_{THL}$ , $t_{TLH}$	output transition time	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	-	-	22	ns	
$t_W$	pulse width						
		clock HIGH or LOW	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	24	-	-	ns
		master reset LOW	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	24	-	-	ns
$t_{rec}$	recovery time $\overline{MR}$ to CP	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	15	-	-	ns	
$t_{su}$	set-up time Dn to CP	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	18	-	-	ns	
$t_h$	hold time Dn to CP	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	3	-	-	ns	
$f_{max}$	maximum input clock frequency	$V_{CC} = 4.5$ V; see <a href="#">Figure 7</a>	20	-	-	MHz	

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

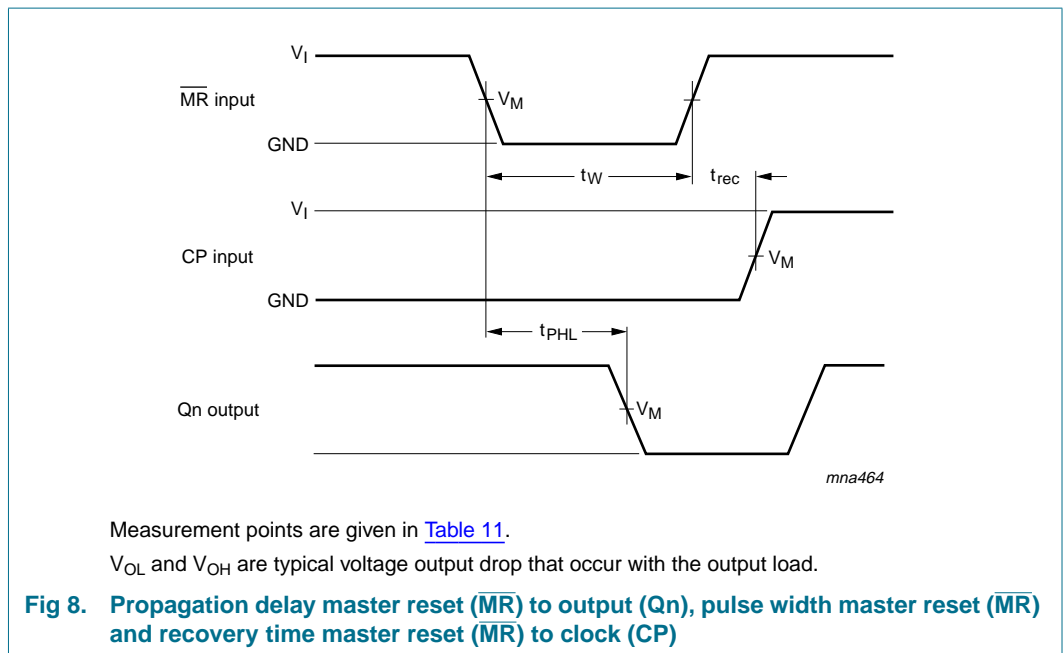
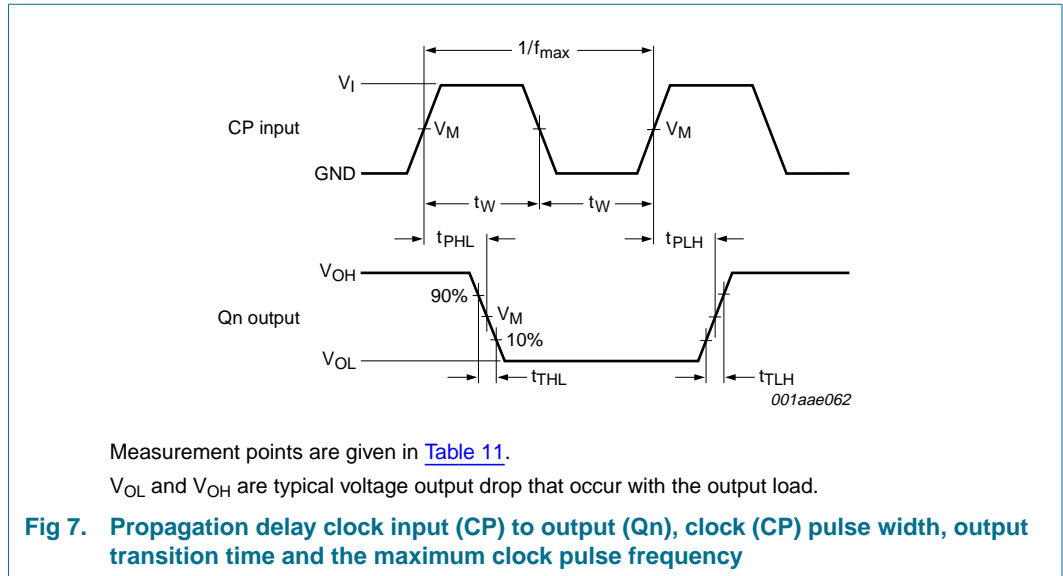
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

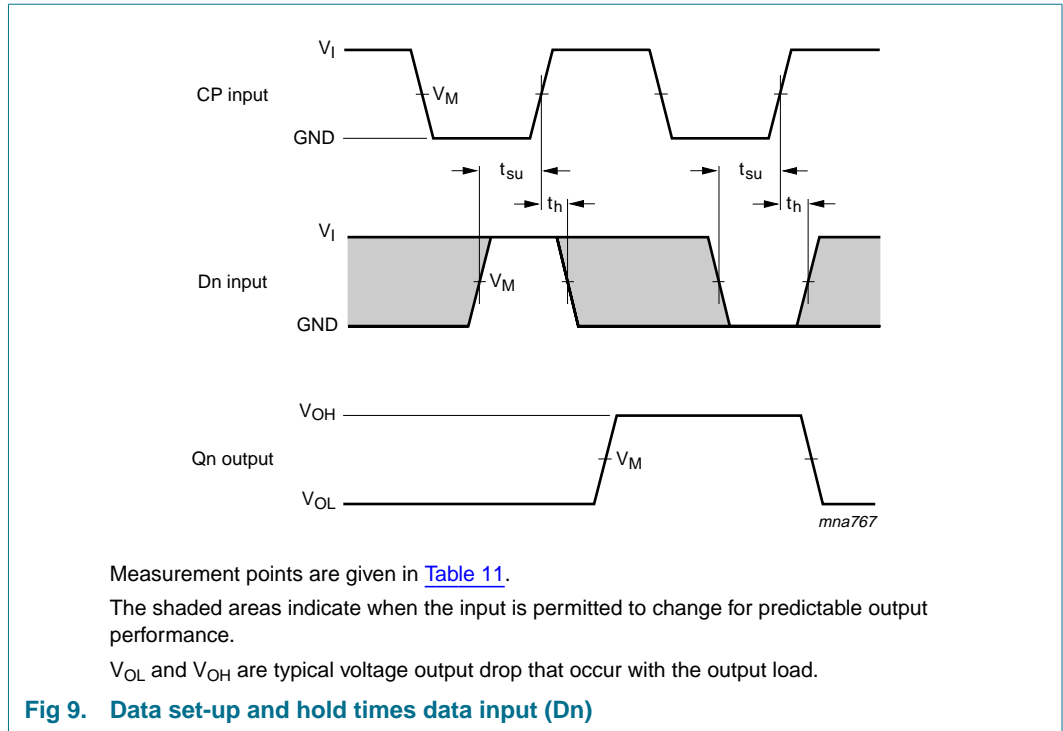
$N$  = number of inputs switching;

$$\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$$

## 12. Waveforms

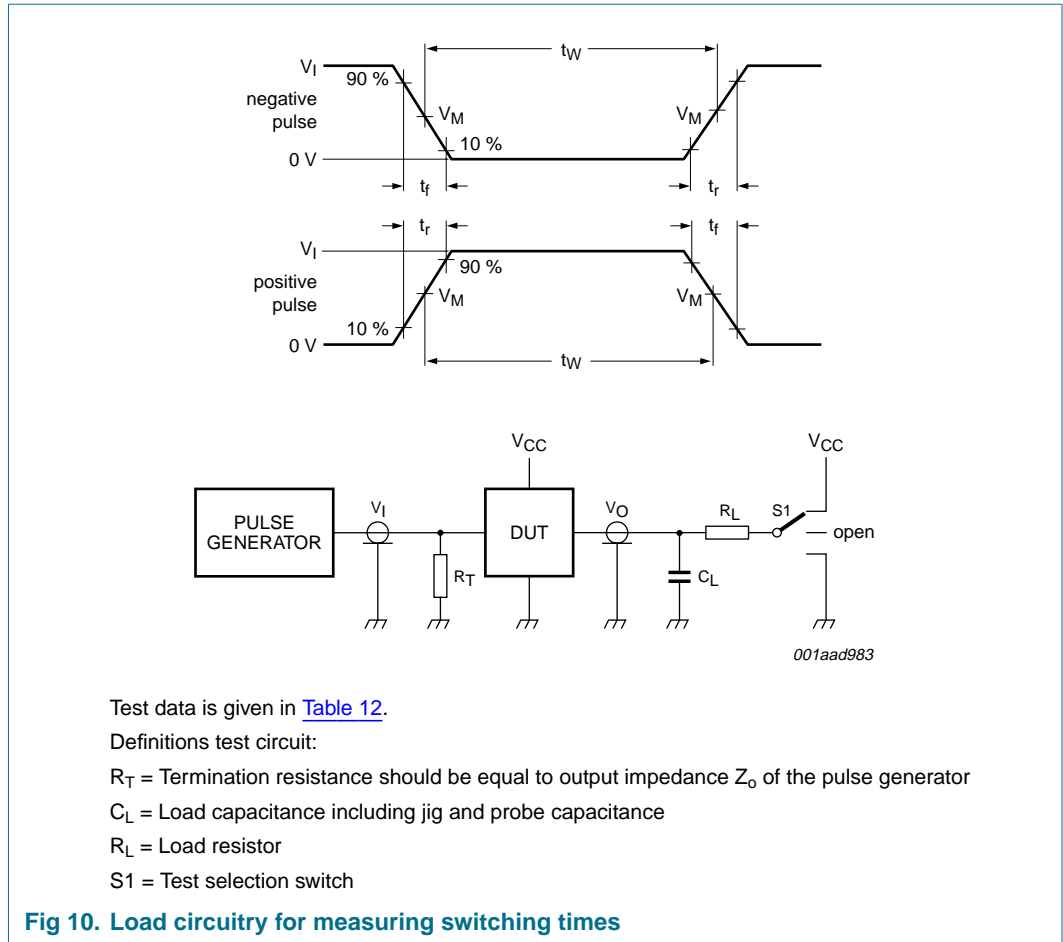






**Table 11: Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74HC273	$0.5V_{CC}$	$0.5V_{CC}$
74HCT273	1.3 V	1.3 V



**Table 12: Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC273	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT273	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

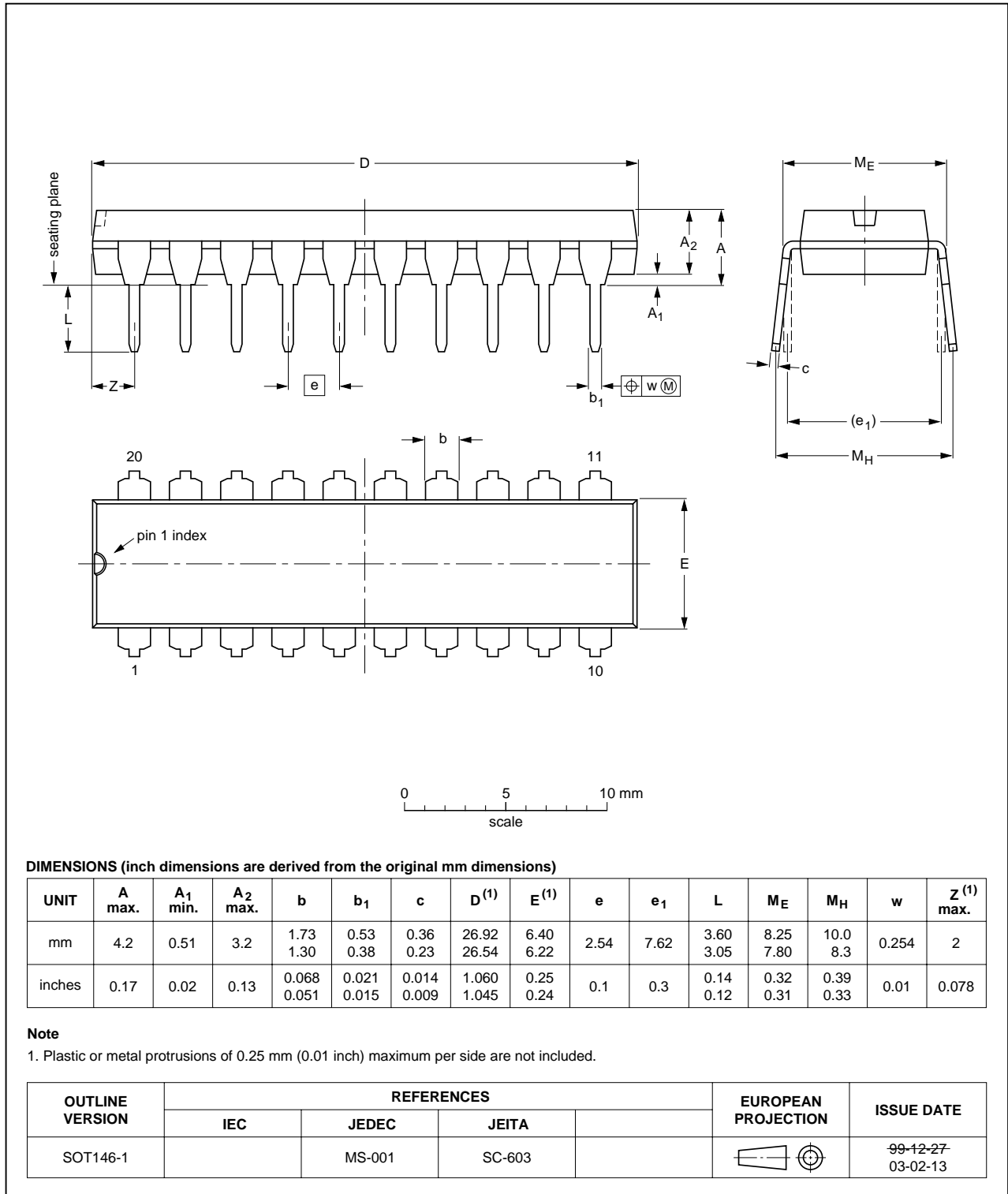


Fig 11. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

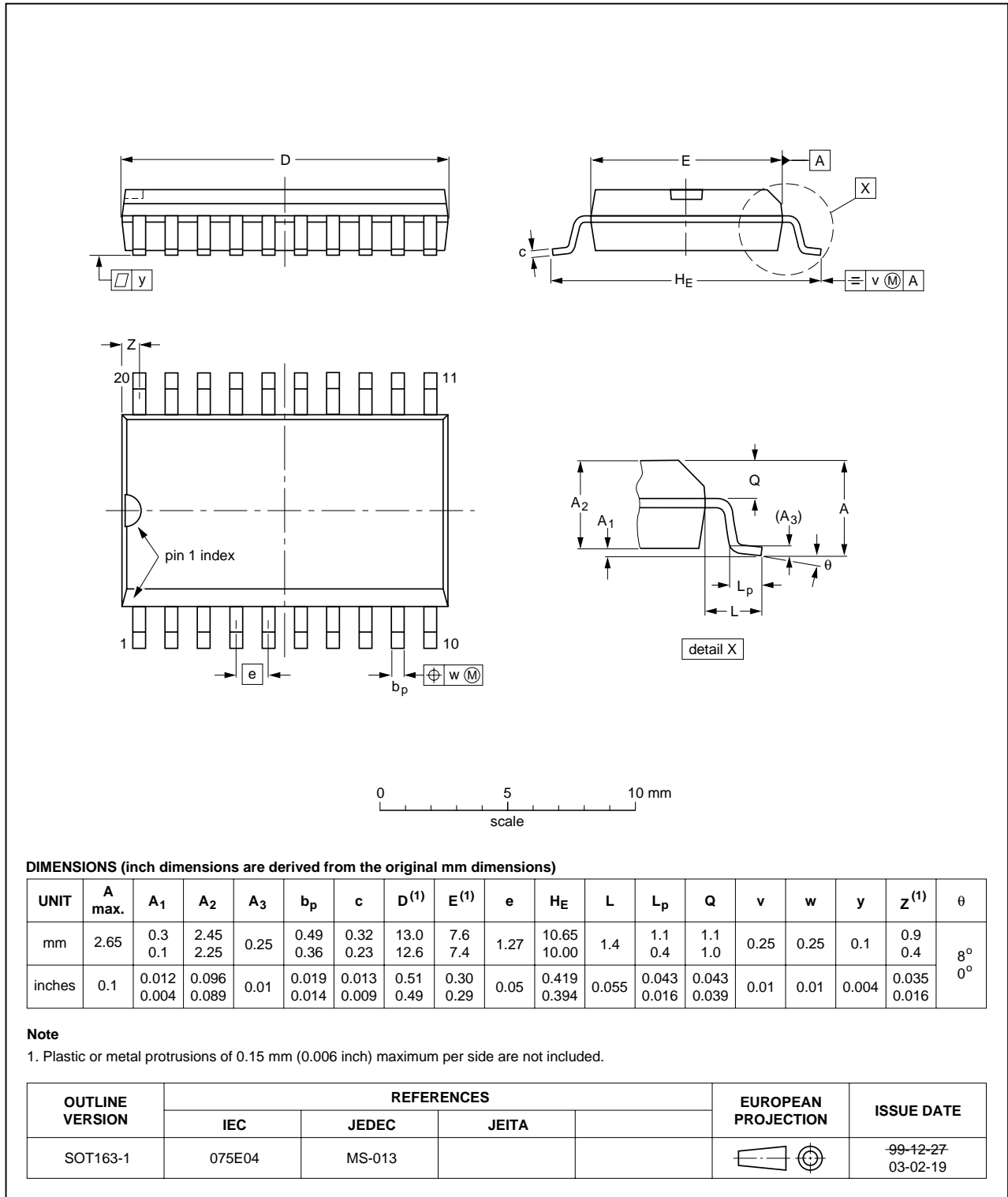


Fig 12. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



Fig 13. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 14. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig 15. Package outline SOT764-1 (DHVQFN20)

## 14. Abbreviations

Table 13: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
MOS	Metal Oxide Semiconductor

## 15. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC_HCT273_3	20060124	Product data sheet	-	-	74HC_HCT273_CNV_2
Modifications:					<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Section 4 "Ordering information"</a>, <a href="#">Section 6 "Pinning information"</a> and <a href="#">Section 13 "Package outline"</a>: Added DHVQFN package information</li> <li><a href="#">Section 10 "Static characteristics"</a>: Added from the family specification</li> </ul>
74HC_HCT273_CNV_2	19970827	Product specification	-	-	-



## 16. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 21. Contents

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