

## Quad PIN-Electronics Drivers / Comparators / Analog Switches

### ■ GENERAL DESCRIPTION

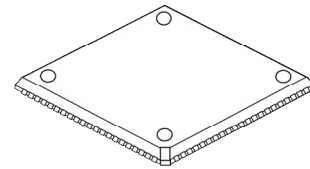
NJU6496 includes four-channel PIN Driver, Comparator, and Analog Switch for kelvin connection. It is designed specifically for Test During Burn-In (TDBI) applications where cost, functional density, and power are all at a premium. Driver is able to set up threshold voltage, and control high level and low level output voltage, and high impedance independently. Comparator is able to control threshold voltage independently at each channel, and set up high level and low level output voltage. Analog Switch that includes two switches for a SENSE and FORCE in each channel is a switch for making Kelvin connection for current detection.

This device has a 15V driver output range and comparator input range. NJU6496 is suitable for an interface to circuits, such as TTL, ECL, CMOS (3V, 5V and 7V), and LVCMOS, not only various tests of a Flash Devices.

### ■ FEATURES

- 15V Input and Output Voltage Range
- Low Consumption Current
- Low Output Leakage Current :  $I_{leak} < 2nA$
- 45 MHz Operation
- Driver DC Output Current :  $I_o = 125mA$
- Package : QFN84-D4 (10.2mm x 10.2mm , t=0.2mm)
- CMOS Structure

### ■ PACKAGE OUTLINE

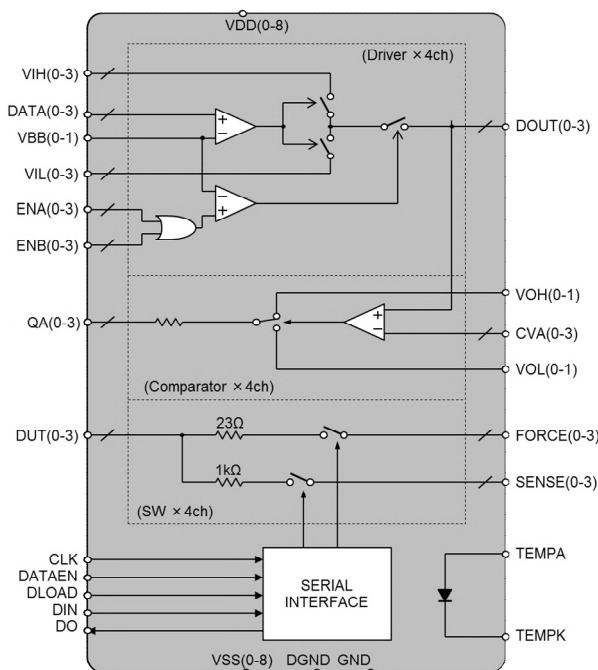


NJU6496KD4

### ■ APPLICATION

- Burn-In Testers
- ATE
- Measuring Instrument

### ■ BLOCK DIAGRAM



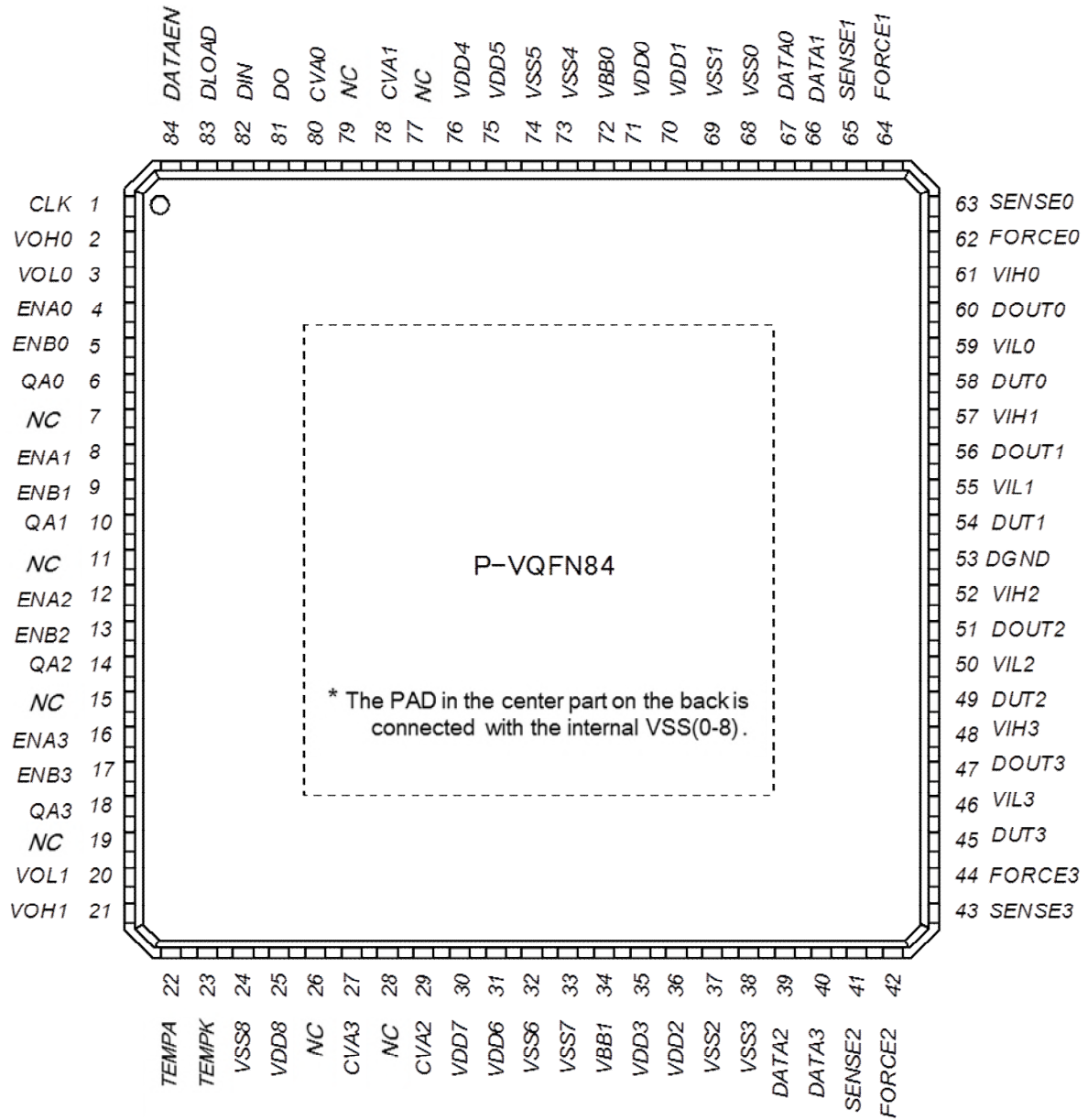
\*1) Driver, Comparator and SW shows per 1 channel.

\*2) (0-3) is applied to one of a figure 0 to 3, and it shows each channel.

\*3) (0-1) and (0-8) is applied to one of a 0 to 1 or 0 to 8, and it is shortened within the IC.

# NJU6496

## ■ PIN INFORMATION



No	Symbol	Function
39,40,66,67	DATA(0-3)	Driver Mode Input (0-3ch)
4,8,12,16 5,9,13,17	ENA(0-3) ENB(0-3)	Driver Output Enable / Hi-Z Setting Input(0-3ch)
47,51,56,60	DOUT(0-3)	Driver Output, Comparator Input(0-3ch)
48,52,57,61	VIH(0-3)	Driver Output High Level Voltage Input (0-3ch)
46,50,55,59	VIL(0-3)	Driver Output Low Level Voltage Input (0-3ch)
34,72	VBB(0-1)	Driver Input (DATA,EN) Threshold Voltage Input
27,29,78,80	CVA(0-3)	Comparator Threshold Voltage Input (0-3ch)
2,21	VOH(0-1)	Comparator Output High Level Voltage Input
3,20	VOL(0-1)	Comparator Output Low Level Voltage Input
6,10,14,18	QA(0-3)	Comparator Output (0-3ch)
45,49,54,58	DUT(0-3)	DUT Connecting (0-3ch)
41,43,63,65	SENSE(0-3)	PMU Sense Connecting (0-3ch)
42,44,62,64	FORCE(0-3)	PMU Force Connecting (0-3ch)
81	DO	Serial Data Output
82	DIN	Serial Data Input
83	DLOAD	Serial Data Load
84	DATAEN	Serial Data Input Enable
1	CLK	Serial Data Input Clock
25,30,31,35,36,70,71,75,76	VDD(0-8)	Positive Power Supply
24,32,33,37,38,68,69,73,74	VSS(0-8)	Negative Power Supply
22	TEMPA	Thermal Diode (Anode)
23	TEMPK	Thermal Diode (Cathode)
53	DGND	Digital GND
7,11,15,19,26,28,77,79	NC	not connected to internal circuits

# NJU6496

## ■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	CONDITION	RATINGS	UNIT
Supply Voltage	V <sub>DD</sub> - V <sub>SS</sub>	V <sub>DD</sub> , V <sub>SS</sub> total Voltage	17.0	V
Input Voltage	V <sub>IN</sub>	Each Input Terminal	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> (Note1)	V
Power Dissipation	P <sub>D</sub>	(Note2)	4400	mW
Output Current	I <sub>OUT</sub>		130	mA
Operating Temperature Range	T <sub>opr</sub>		-20 to +85	
Storage Temperature Range	T <sub>stg</sub>		-40 to +150	°C

(Note 1 ) For supply voltage less than 17V, the maximum input voltage is equal to the supply voltage.

(Note 2 ) Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers) Back side center PAD mounting

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

## ■ RECOMMENDED OPERATION CONDITIONS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply	V <sub>DD</sub> - V <sub>SS</sub>	10.0 to 15.0 (total)	V

## ■ ELECTRICAL CHARACTERISTICS

V<sub>DD</sub>=10V, V<sub>SS</sub>=-3V, V<sub>B</sub>=1.5V, DATA=1.5±1.5V, V<sub>IH</sub>=5V, V<sub>IL</sub>=0V, ENA=ENB=0V, CL=33pF, R<sub>L</sub>=1kΩ, Ta=25°C unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>Driver DC Characteristics</b>						
High Level Output Voltage	D <sub>OUTH</sub>	DATA=5.0V	4.75	-	-	V
Low Level Output Voltage	D <sub>OUTL</sub>	DATA=0V	-	-	0.25	V
Output Leak Current (HiZ)	I <sub>leak</sub>	ENA=3V, DUT=9.5V or -3V	-2	-	2	nA
Output Resistance	R <sub>out</sub>		19.8	22.8	25.8	Ω
DC Output Current (source)	I <sub>source DC</sub>		125	-	-	mA
DC Output Current (sink)	I <sub>sink DC</sub>		125	-	-	mA
High Level Input Voltage	V <sub>IH</sub>		2.0	-	-	V
Low Level Input Voltage	V <sub>IL</sub>		-	-	1.0	V
Input Bias Current	I <sub>in</sub>		-100	-	100	nA
<b>Driver AC Characteristics</b> (f=10MHz)						
<b>Propagation Delay</b>						
DATA to DUT Fig.1	T <sub>pdr</sub> , T <sub>pdf</sub>	V <sub>IH</sub> =3V, V <sub>IL</sub> =0V	15.4	16.9	18.4	ns
EN to DUT (Active to HiZ) Fig.2	T <sub>az</sub>	V <sub>IH</sub> =3V, V <sub>IL</sub> =0V, DATA=3.0V, ENA=0V to 3.0V, f=500kHz	18	19.5	21	ns
EN to DUT (HiZ to Active) Fig.2	T <sub>za</sub>	V <sub>IH</sub> =3V, V <sub>IL</sub> =0V, DATA=3.0V, ENA=3.0V to 0V, f=500kHz	15.5	17.0	18.5	ns
Propagation Delay Mismatch Fig.1	T <sub>pdr</sub> - T <sub>pdf</sub>	V <sub>H</sub> =3V, V <sub>L</sub> =0V	-	-	1	ns

VDD=10V, VSS= -3V, VBB=1.5V, DATA=1.5±1.5V 10MHz, VIH=3V,VIL= 0V, ENA=ENB=0V, CL=33pF, RL=1kΩ, Ta=25°C, unless otherwise noted

PARAMETER		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>Driver AC Characteristics</b> (f=10MHz)							
<b>Rise / Fall Time</b>							
1V Swing	Fig.3	Tr 1/ Tf1	VIH=1V, VIL=0V, 20% to 80%	-	4.8	11.0	ns
3V Swing	Fig.3	Tr 3/ Tf3	VIH=3V, VIL=0V, 10% to 90%	-	6.7	15.5	ns
5V Swing	Fig.3	Tr 5/ Tf5	VIH=5V, VIL=0V, 10% to 90%	-	6.8	15.5	ns
10V Swing	Fig.3	Tr 10/ Tf10	VIH=10V, VIL=0V, 10% to 90%	-	7.2	-	ns
15V Swing	Fig.3	Tr15 / Tf15	VDD=12V ,VIH=12V VIL= - 3V, 10% to 90%	-	7.4	-	ns
Rise / Fall Time Mismatch	Fig.3	Tr - Tf		-	-	2	ns
Overshoot, Undershoot, Preshoot		Vshoot	VIH=3V, VIL=0V,CL=33pF	-	150	-	mV
Max. Operating Frequency	Fig.4	Fmax	VIH=5V, VIL=0V	45	-	-	MHz
Min. Pulse Width	Fig.4	Tpw	VIH=5V, VIL=0V	-	-	11	ns

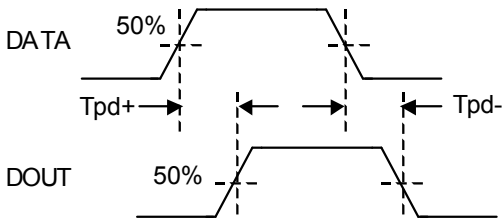


Fig.1

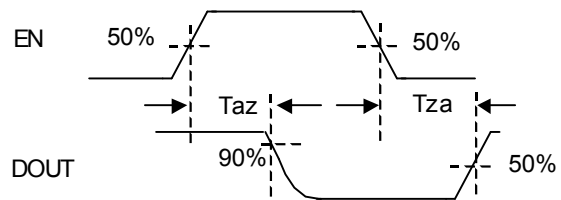


Fig.2

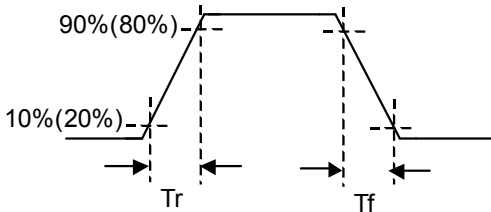


Fig.3

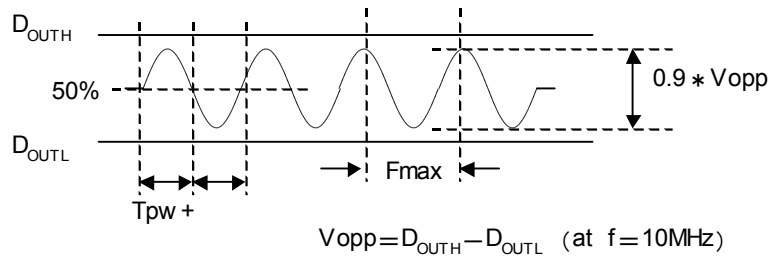


Fig.4

# NJU6496

VDD=10V, VSS= -3V, ENA=ENB=3V, CVA=1.5V, DOUT=1.5±1.5V 10MHz, VOH=3V, VOL= 0V, CL=33pF, RL=1kΩ, Ta=25° C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT		
<b>Comparator DC Characteristics</b>								
High Level Output Voltage	Vch		2.75	3.0		V		
Low Level Output Voltage	Vcl			0	0.25	V		
Input Offset Voltage	Voff		-50	0	50	mV		
Output Resistance	Rcout		25	35	45	Ω		
<b>Comparator AC Characteristics</b>								
<b>Propagation Delay</b>								
DUT to QA,QB	Tcpdr, Tcpdf		9	12	15	ns		
Overdrive Voltage Variation	$\frac{\Delta Tpd}{\Delta DUTamp1}$	DOUT=1.5V±[100mV~1V]	-	8	10	ns/V		
		DOUT=1.5V±[1V~2.5V]	-	0.8	1.5	ns/V		
Common Voltage Variation	$\Delta Tpdcm$	CVA=0V~3.0V, DOUT=CVA±1.5V	-	-	2	ns		
Propagation Delay Mismatch	Tcpdr-Tcpdf		-	-	2	ns		
<b>Others</b>								
Rise / Fall Time	Fig.3	Tcr / Tcf		10% to 90%	-	3.0	ns	
Max. Operating Frequency	Fig.4	Fmax		VOH=3V, VOL=0V	60	-	MHz	
Min. Pulse Width	Fig.4	Tpw		VOH=3V, VOL=0V	-	-	8	ns

VDD=10V, VSS= -3V, Ta=25° C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>Analog Switch Characteristics</b>						
FORCE Switch Resistance	Rf	V <sub>FORCE</sub> =0V, I <sub>DUT</sub> =10mA	18	23	28	Ω
SENSE Switch Resistance	Rs	V <sub>SENSE</sub> =0V, I <sub>DUT</sub> =1mA	0.7	1	1.3	kΩ
FORCE Capacitance	Cf	SW open		9		pF
SENSE Capacitance	Cs	SW open		8		pF
DUT Capacitance	Cd	SW open		10		pF
Switch Current Leakage	Iswleak	V <sub>DUT</sub> =0V, V <sub>SENSE</sub> =-3 or 9.5V, V <sub>FORCE</sub> =-3 or 9.5V	-2	-	2	nA

VDD=10V, VSS= -3V, VBB=1.5V, DATA=0V, VIH=3V, VIL=0V, ENA=ENB=0V, RL=1kΩ, CL=33pF, CVA=1.5V, VOH=3V, VOL=0V, Ta=25°C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>Power Supplies</b>						
Positive Power Supply DC Current	I <sub>DD</sub>	No Signal	-	45	65	mA
Negative Power Supply DC Current	I <sub>SS</sub>	No Signal	-65	-45	-	mA

VDD=10V, VSS= -3V, Ta=25°C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>Data Interface</b>						
Setup Time	T <sub>st</sub>		-	200	-	ns
High Level Data Pulse Width Fig.5	T <sub>pwh</sub>		-	33	-	ns
Low Level Data Pulse Width Fig.5	T <sub>pwl</sub>		-	33	-	ns
DATAEN Low Hold Timing Fig.5	T <sub>cel</sub>		5	-	20	ns
DATAEN High Hold Timing Fig.5	T <sub>ceh</sub>		5	-	20	ns
CLK Max. Input Frequency	F <sub>clk</sub>		15	-	-	MHz
DO Output Propagation Delay Fig.5	T <sub>co</sub>		-	-	30	ns
Max. Logic Setting Time Fig.5	T <sub>el</sub>		-	20	-	ns
DLOAD Data Pulse Width Fig.5	T <sub>lw</sub>		30	-	-	ns
High Level Input Voltage	V <sub>dh</sub>		2.4	-	10	V
Low Level Input Voltage	V <sub>dl</sub>		-3	-	0.6	V
DO Rise / Fall Time	T <sub>rdo</sub> , T <sub>fdo</sub>	CL=10pF	-	6	-	ns

## TRUTH TABLES

Driver

DATA, ENA, ENB	Status
$\geq V_{BB}+0.5V$	H
$\leq V_{BB}-0.5V$	L

ENA	ENB	DATA	DOUT
H	X	X	HiZ(OPEN)
X	H	X	HiZ(OPEN)
L	L	H	VIH
L	L	L	VIL

Comparator

DOUT	Status
$\geq CVA+0.1$	H
$\leq CVA-0.1$	L

DOUT	QA
H	VOH
L	VOL

## SWITCH CONTROL

Timing Table

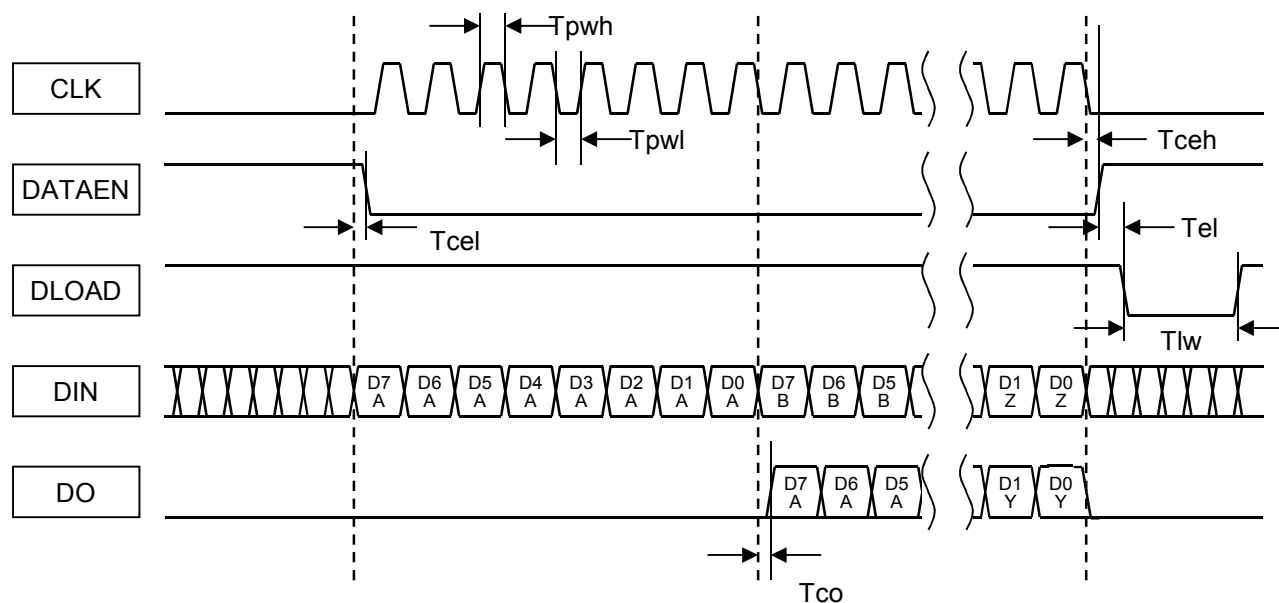


Fig.5 Data Input Timing Table



Input Data Table

DATA	FUNCTION	BIT STATE		DEFAULT
		0	1	
D0	CH3 FORCE SW	OPEN	CLOSE	0
D1	CH3 SENSE SW	OPEN	CLOSE	0
D2	CH2 FORCE SW	OPEN	CLOSE	0
D3	CH2 SENSE SW	OPEN	CLOSE	0
D4	CH1 FORCE SW	OPEN	CLOSE	0
D5	CH1 SENSE SW	OPEN	CLOSE	0
D6	CH0 FORCE SW	OPEN	CLOSE	0
D7	CH0 SENSE SW	OPEN	CLOSE	0

## Data Interface

NJU6496 includes the serial interface for analog switch control. This serial interface consists of an 8-bit shift register and a switch control register. Data input is CLK, DATAEN, DLAOD, and DIN, and a data output is DO.

### - Data input

While DATAEN is set as LOW, data input and an output will be in an active state. DIN is loaded to a shift register by the rising edge of CLK.

### - Data output

The data of a shift register is outputted through DO. DO is a buffer output of the last bit of a shift register, and is outputted with the voltage level of VDD and VSS. It is possible to carry out daisy chain connection of multiple devices using DO.

### - Loading of switch (or Switch Loading)

The load timing of an analog switch is controlled by DLOAD. The data of a shift register is loaded to a switch control register with the falling edge of DLOAD, and the state of an analog switch is changed. The data loaded to the switch control register holds data, as long as there is no rewriting of data.

### - OFF state

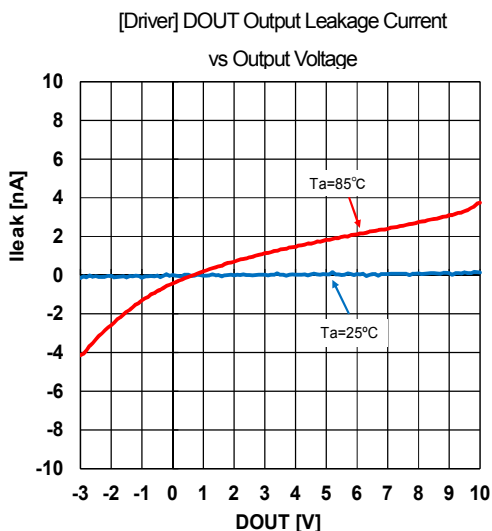
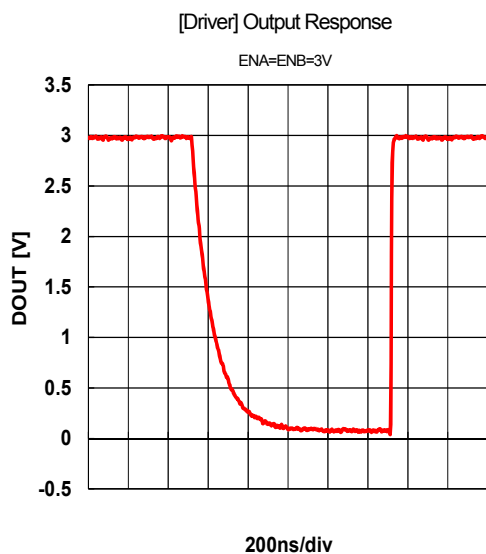
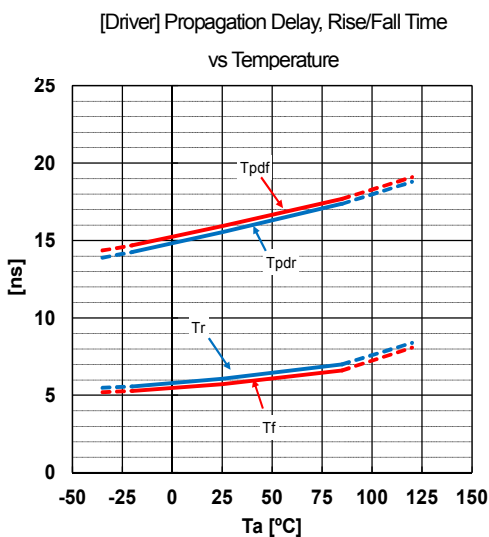
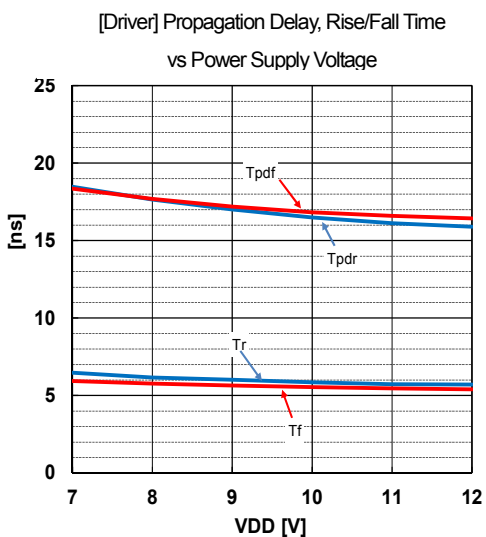
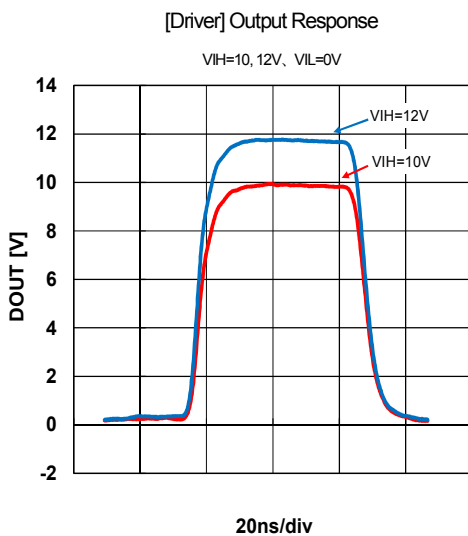
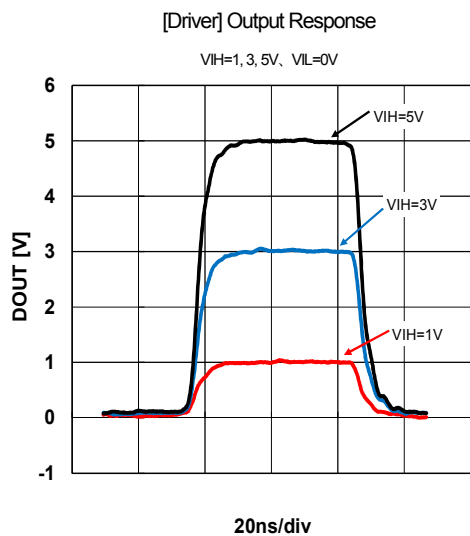
While DATAEN is set as HIGH, data is not loaded but DO is simultaneously fixed to LOW. Moreover, it is not necessary to input CLK.

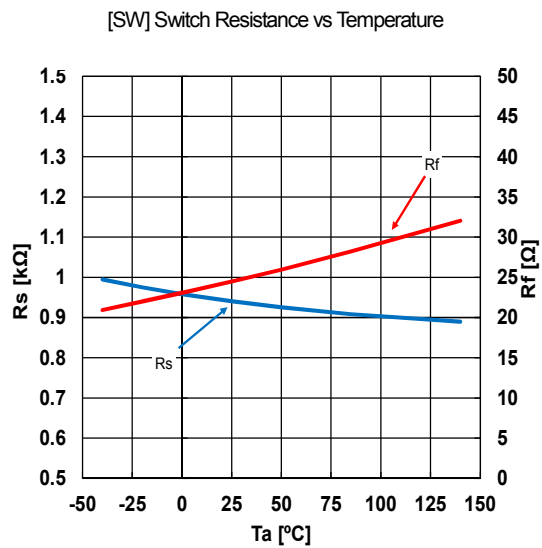
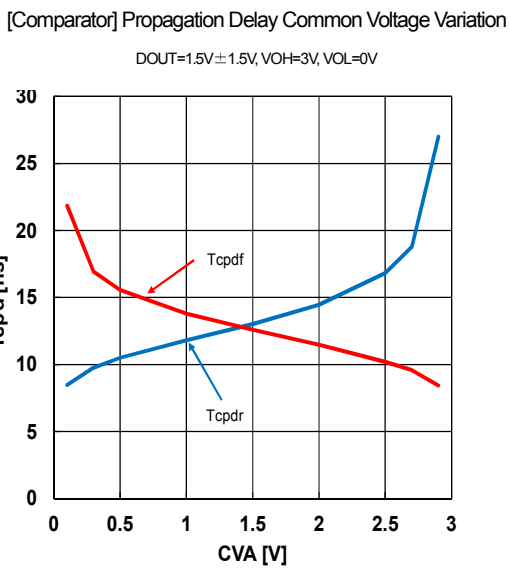
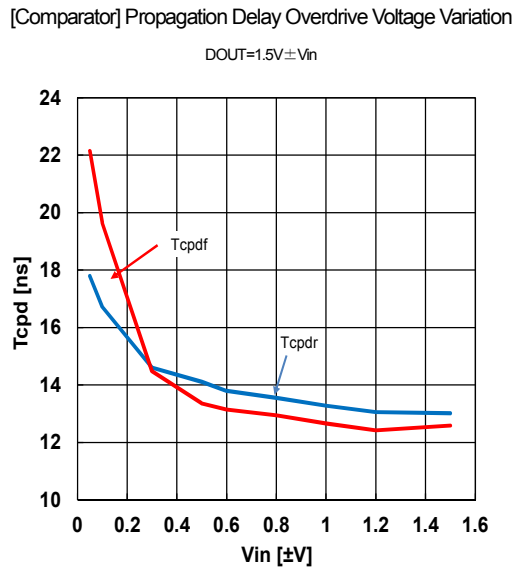
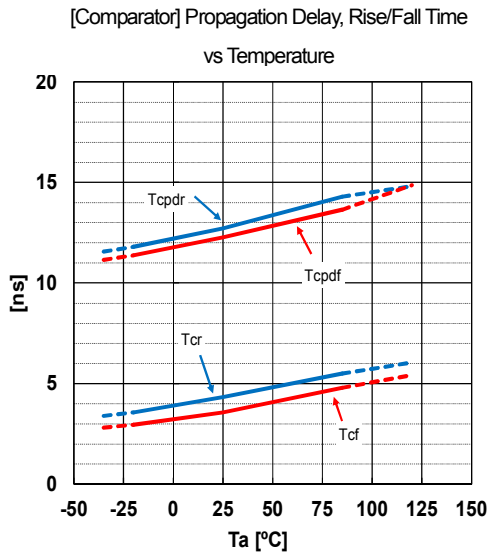
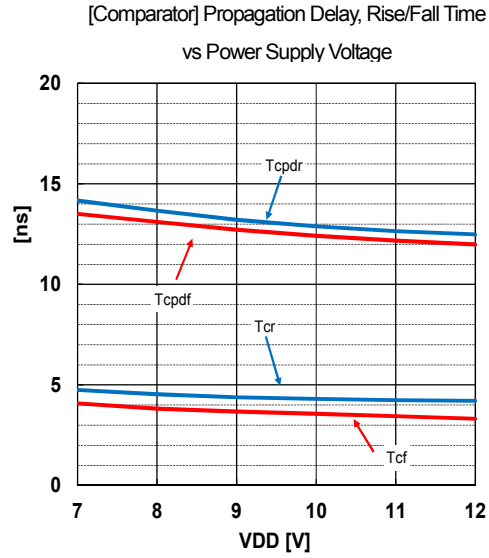
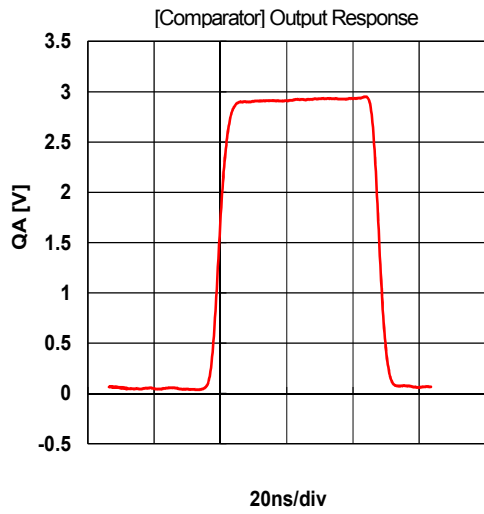
### - Power-on state

The switch control register immediately after power activation is set as LOW, and an analog switch will be in a CLOSE (OFF) state.

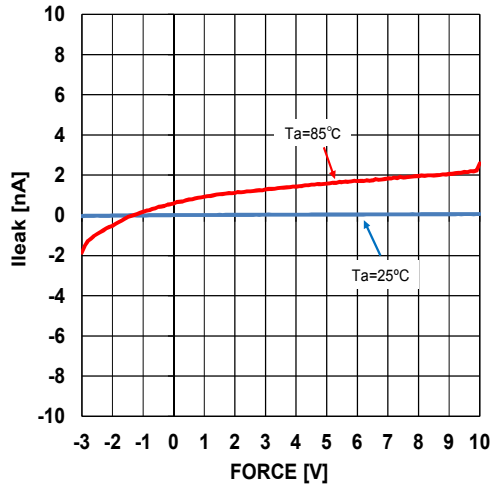
## TYPICAL CHARACTERISTICS

VDD=10V, VSS=-3V, VBB=1.5V, ENAx=ENBx=0V, VIHx=3V, VILx=0V, CVAx=1.5V, VOH=3V, VOL=0V, RL=1kΩ, CL=33pF, Ta=25°C unless otherwise specified.

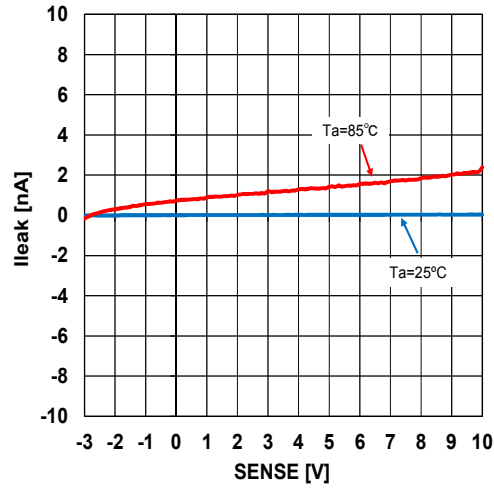




[SW] FORCE Leakage Current

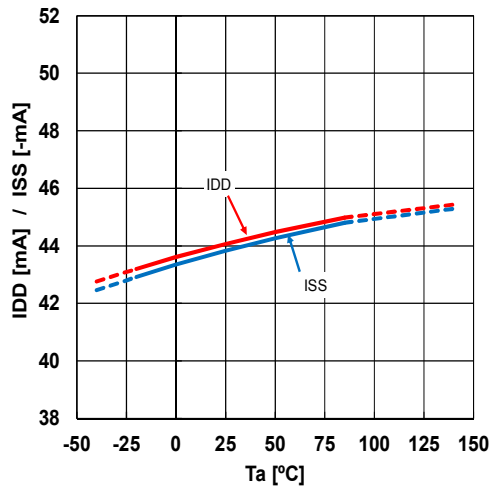


[SW] SENSE Leakage Current



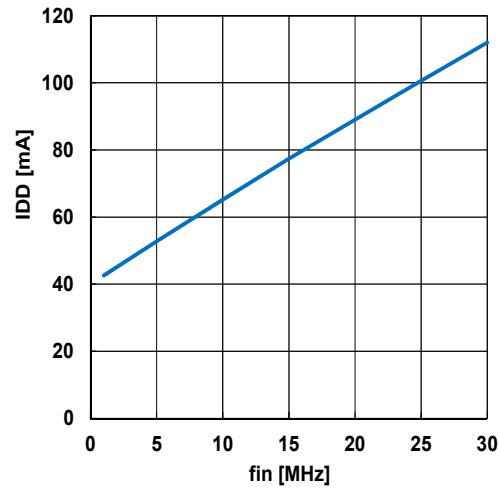
Supply Current vs Temperature

No Signal



Supply Current vs Operating Frequency

4ch Operation



## ■ NOTICE, CAUTIONS

1) Short pins in IC and connection to them on the board  
VSS(0-8),VDD(0-8),VBB(0-1) and VOH(0-1),VOL(0-1) are shorted in the IC, respectively. But you should connect all of the pins to decrease the impedance of power supplies.

2) Power-on Sequence

You should power on with the following sequence: first VSS(0-8), second VDD(0-8), third VBB(0-1) and CVA(0-3), then power on the other inputs.

Otherwise sequence may cause a permanent damage to the IC.

3) Leak Current in HiZ Mode

The leak current might exceed 2nA in case of the following:

1. When DOUT(0-3) or VIH(0-3) or VIL(0-3) voltage set near VDD voltage
2. When the junction temperature is high.

[CAUTION]

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