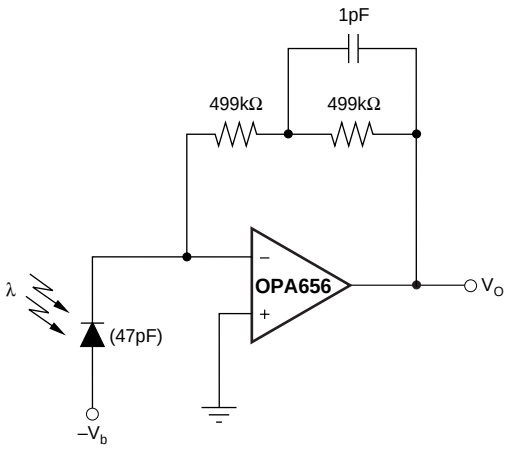
Wideband, Unity-Gain Stable, FET-Input OPERATIONAL AMPLIFIER

FEATURES

- 500MHz UNITY-GAIN BANDWIDTH
- LOW INPUT BIAS CURRENT: 2pA
- LOW OFFSET AND DRIFT: ±0.25mV, ±2μV/°C
- LOW DISTORTION: 74dB SFDR at 5MHz
- HIGH OUTPUT CURRENT: 70mA
- LOW INPUT VOLTAGE NOISE: 7nV/√Hz

APPLICATIONS

- WIDEBAND PHOTODIODE AMPLIFIERS
- SAMPLE-AND-HOLD BUFFERS
- CCD OUTPUT BUFFERS
- ADC INPUT BUFFERS
- WIDEBAND PRECISION AMPLIFIERS
- TEST AND MEASUREMENT FRONT ENDS



Wideband Photodiode Transimpedance Amplifier

DESCRIPTION

The OPA656 combines a very wideband, unity-gain stable, voltage-feedback op amp with a FET-input stage to offer an ultra high dynamic-range amplifier for ADC (Analog-to-Digital Converter) buffering and transimpedance applications. Extremely low DC errors give good precision in optical applications.

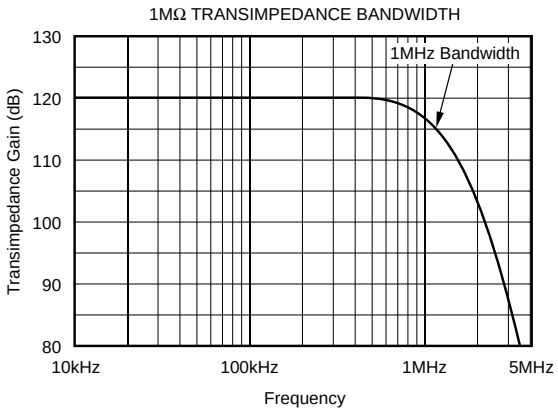
The high unity-gain stable bandwidth and JFET input allows exceptional performance in high-speed, low-noise integrators.

The high input impedance and low bias current provided by the FET input is supported by the ultra-low 7nV/√Hz input voltage noise to achieve a very low integrated noise in wideband photodiode transimpedance applications.

Broad transimpedance bandwidths are achievable given the OPA656's high 230MHz gain bandwidth product. As shown below, a –3dB bandwidth of 1MHz is provided even for a high 1MΩ transimpedance gain from a 47pF source capacitance.

RELATED OPERATIONAL AMPLIFIER PRODUCTS

DEVICE	V_S (V)	BW (MHz)	SLEW RATE (V/μS)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA355	+5	200	300	5.8	Unity-Gain Stable CMOS
OPA655	±5	400	290	6	Unity-Gain Stable FET-Input
OPA657	±5	1600	700	4.8	Gain of +7 Stable FET-Input
OPA627	±15	16	55	4.5	Unity-Gain Stable FET-Input
THS4601	±15	180	100	5.4	Unity-Gain Stable FET-Input



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±6.5V
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	$\pm V_S$
Input Voltage Range	$\pm V_S$
Storage Temperature Range	–65°C to +125°C
Lead Temperature	+260°C
Junction Temperature (T_J)	+150°C
ESD Rating (Human Body Model)	2000V
(Machine Model)	200V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

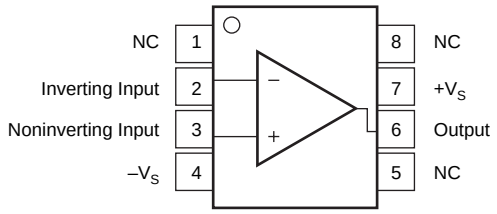
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[2]	TRANSPORT MEDIA, QUANTITY
OPA656U	SO-8 Surface Mount	D	–40°C to +85°C	OPA656U	OPA656U	Rails, 100
"	"	"	"	"	OPA656U/2K5	Tape and Reel, 2500
OPA656UB	SO-8 Surface Mount	D	–40°C to +85°C	OPA656UB	OPA656UB	Rails, 100
"	"	"	"	"	OPA656UB/2K5	Tape and Reel, 2500
OPA656N	SOT23-5	DBV	–40°C to +85°C	B56	OPA656N/250	Tape and Reel, 250
"	"	"	"	"	OPA656N/3K	Tape and Reel, 3000
OPA656NB	SOT23-5	DBV	–40°C to +85°C	B56	OPA656NB/250	Tape and Reel, 250
"	"	"	"	"	OPA656NB/3K	Tape and Reel, 3000

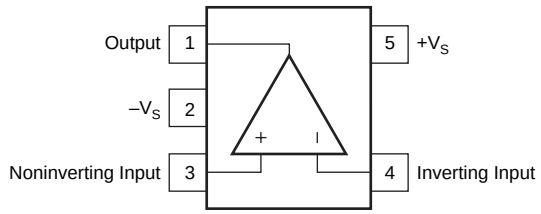
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com. (2) UB and NB are high grade, while U and N are standard grade.

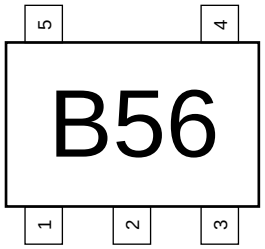
PIN CONFIGURATIONS

Top View **SO**



Top View **SOT23**





Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

$R_F = 250\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted. Figure 1 for AC performance.

PARAMETER	CONDITIONS	OPA656U, N (Standard-Grade)						TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	
AC PERFORMANCE (Figure 1)								
Small-Signal Bandwidth	G = +1, V_O = 200mV$_{PP}$, $R_F = 0\Omega$	500				MHz	Typ	C
	G = +2, V_O = 200mV$_{PP}$	200				MHz	Typ	C
	G = +5, V_O = 200mV$_{PP}$	59				MHz	Typ	C
	G = +10, V_O = 200mV$_{PP}$	23				MHz	Typ	C
Gain-Bandwidth Product	G > +10	230				MHz	Typ	C
Bandwidth for 0.1dB flatness	G = +2, V_O = 200mV$_{PP}$	30				MHz	Typ	C
Peaking at a Gain of +1	V_O < 200mV$_{PP}$, $R_F = 0\Omega$	1.5				dB	Typ	C
Large-Signal Bandwidth	G = +2, V_O = 2V$_{PP}$	75				MHz	Typ	C
Slew Rate	G = +2, 1V Step	290				V/µs	Typ	C
Rise-and-Fall Time	0.2V Step	1.5				ns	Typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	21				ns	Typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2V$_{PP}$							
2nd-Harmonic	$R_L = 200\Omega$	–71				dBc	Typ	C
	$R_L > 500\Omega$	–74				dBc	Typ	C
3rd-Harmonic	$R_L = 200\Omega$	–81				dBc	Typ	C
	$R_L > 500\Omega$	–100				dBc	Typ	C
Input Voltage Noise	f > 100kHz	7				nV/$\sqrt{Hz}$	Typ	C
Input Current Noise	f > 100kHz	1.3				fA/$\sqrt{Hz}$	Typ	C
Differential Gain	G = +2, PAL, $R_L = 150\Omega$	0.02				%	Typ	C
Differential Phase	G = +2, PAL, $R_L = 150\Omega$	0.05				°	Typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V, $R_L = 100\Omega$	65	**60**	59	58	dB	Min	A
Input Offset Voltage	V_{CM} = 0V	±0.25	**±1.8**	±2.2	±2.6	mV	Max	A
Average Offset Voltage Drift	V_{CM} = 0V	±2	**±12**	±12	±12	µV/°C	Max	A
Input Bias Current	V_{CM} = 0V	±2	**±20**	±1800	±5000	pA	Max	A
Input Offset Current	V_{CM} = 0V	±1	**±10**	±900	±2500	pA	Max	B
INPUT								
Most Positive Input Voltage(5)		+2.75	**+2.1**	+2.05	+2.0	V	Min	A
Most Negative Input Voltage(5)		–4.5	**–4.0**	–3.9	–3.8	V	Min	A
Most Positive Input Voltage(6)		+3.25	**+2.6**	+2.5	+2.4	V	Min	A
Most Negative Input Voltage(6)		–4.5	**–4.0**	–3.9	–3.8	V	Min	A
Common-Mode Rejection Ratio (CMRR)	$V_{CM} = \pm 0.5V$	86	**80**	78	76	dB	Min	A
Input Impedance								
Differential		10^{12} || 0.7				Ω || pF	Typ	C
Common-Mode		10^{12} || 2.8				Ω || pF	Typ	C
OUTPUT								
Voltage Output Swing	No Load	±3.9	**±3.7**			V	Typ	
	$R_L = 100\Omega$	±3.5	**±3.3**	±3.2	±3.1	V	Min	A
Current Output, Sourcing		+70	**50**	48	46	mA	Min	A
Current Output, Sinking		–70	**–50**	–48	–46	mA	Min	A
Closed-Loop Output Impedance	G = +1, f = 0.1MHz	0.01				Ω	Typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	Typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	Max	A
Maximum Quiescent Current		14	**16**	16.2	16.3	mA	Max	A
Minimum Quiescent Current		14	**11.7**	11.4	11.1	mA	Min	A
Power-Supply Rejection Ratio (+PSRR)	$+V_S$ = 4.50V to 5.50V	76	**72**	70	68	dB	Min	A
(–PSRR)	$–V_S$ = 4.50V to –5.50V	62	**56**	54	52	dB	Min	A
TEMPERATURE RANGE								
Specified Operating Range: U,N Package		–40 to 85				°C	Typ	
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
U: SO-8		125				°C/W	Typ	
N: SOT23-5		150				°C/W	Typ	

NOTES: (1) Junction temperature = ambient for 25°C min/max specifications.

(2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +20°C at high temperature limit for over temperature min/max specifications.

(3) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

(6) Input range to give > 53dB CMRR.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$: High Grade DC Specifications[1]

$R_F = 250\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted.

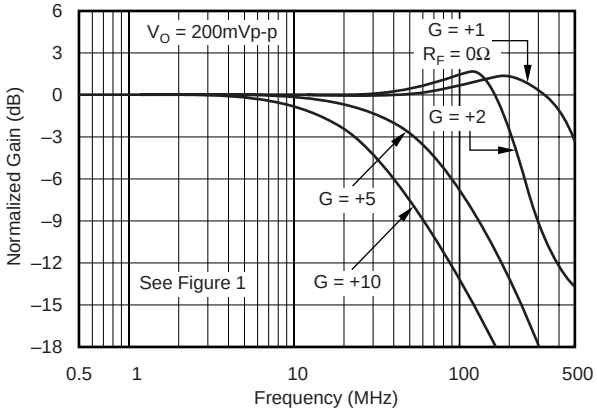
PARAMETER	CONDITIONS	OPA656UB, NB (High-Grade)						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[4]
Input Offset Voltage	V_{CM} = 0V	±0.1	**±0.6**	±0.85	±0.9	mV	Max	A
Input Offset Voltage Drift	V_{CM} = 0V	±2	**±6**	±6	±6	µV/°C	Max	A
Input Bias Current	V_{CM} = 0V	±1	**±5**	±450	±1250	pA	Max	A
Input Offset Current	V_{CM} = 0V	±0.5	**±5**	±450	±1250	pA	Max	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±0.5V	95	**88**	86	84	dB	Min	A
Power-Supply Rejection Ratio (+PSRR)	$+V_S$ = 4.5V to 5.5V	78	**74**	72	70	dB	Min	A
(–PSRR)	$–V_S$ = –4.5V to –5.5V	68	**62**	60	58	dB	Min	A

NOTES: (1) All other specifications are the same as the standard-grade.
(2) Junction temperature = ambient for 25°C min/max specifications.
(3) Junction temperature = ambient at low temperature limit: junction temperature = ambient +20°C at high temperature limit for over temperature min/max specifications.
(4) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation.

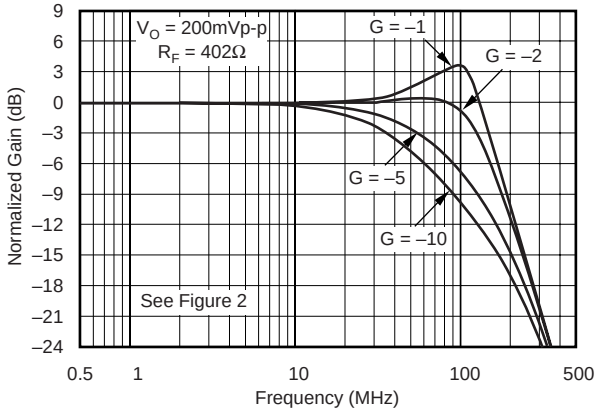
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

T_A = +25°C, G = +2, R_F = 250Ω, R_L = 100Ω, unless otherwise noted.

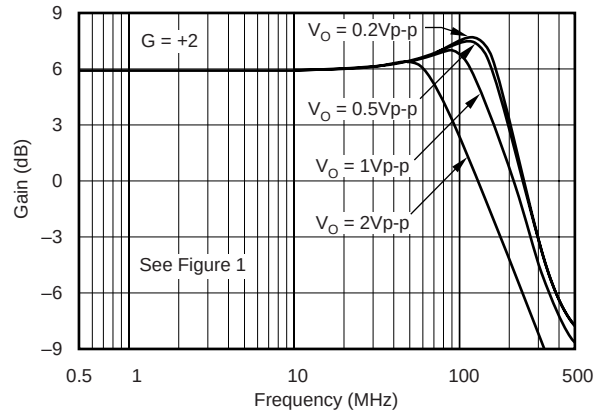
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



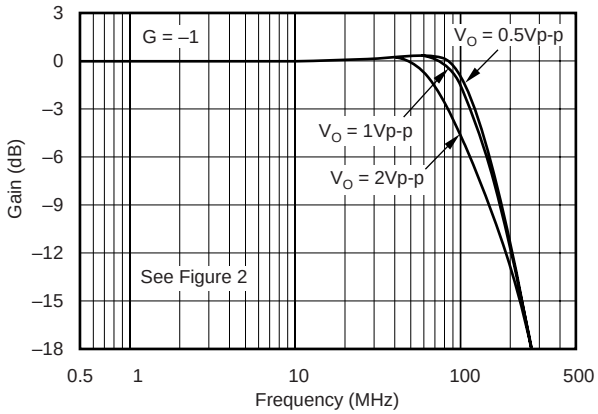
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



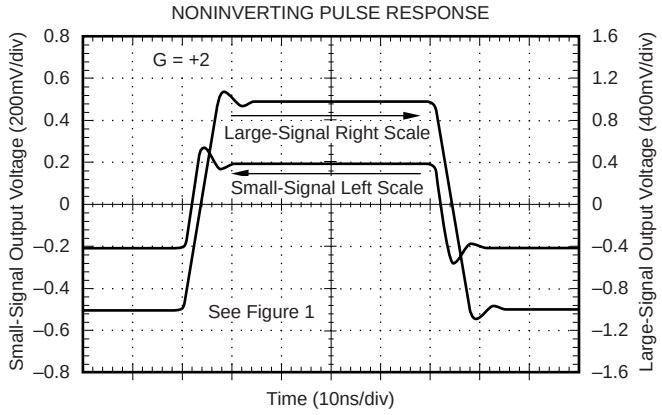
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



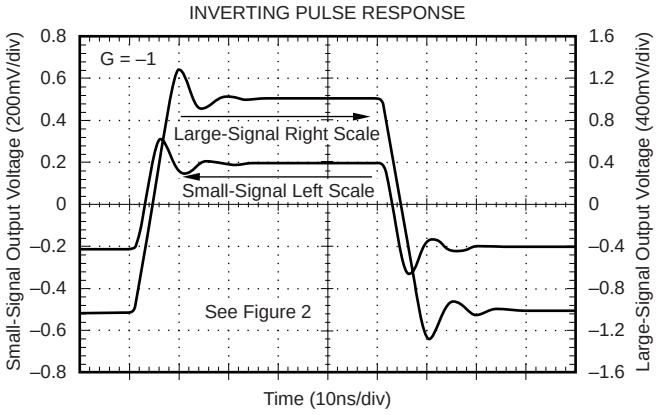
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



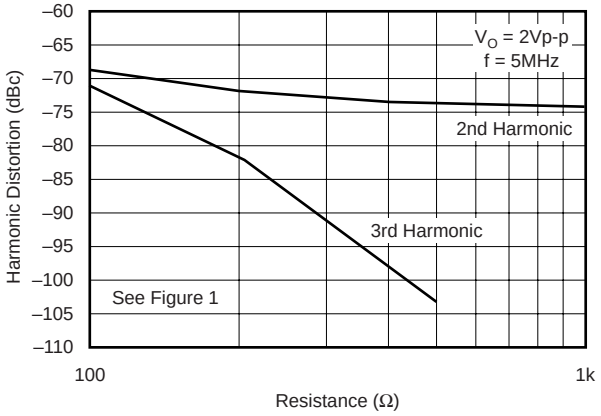
INVERTING PULSE RESPONSE



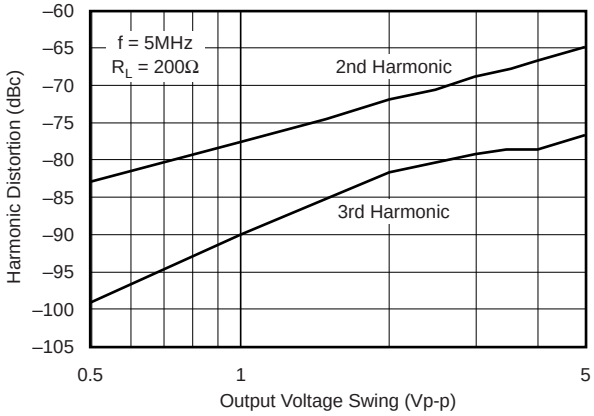
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, R_F = 250Ω, R_L = 100Ω, unless otherwise noted.

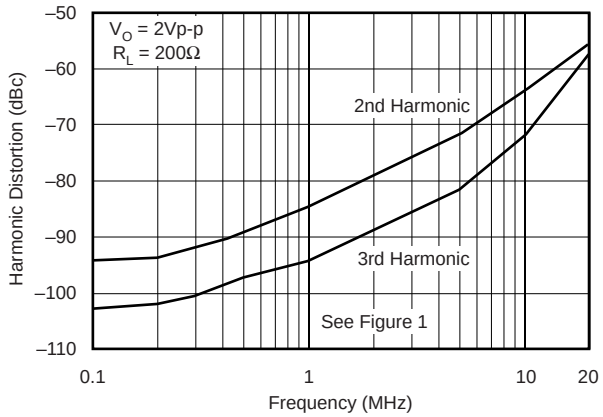
HARMONIC DISTORTION vs LOAD RESISTANCE



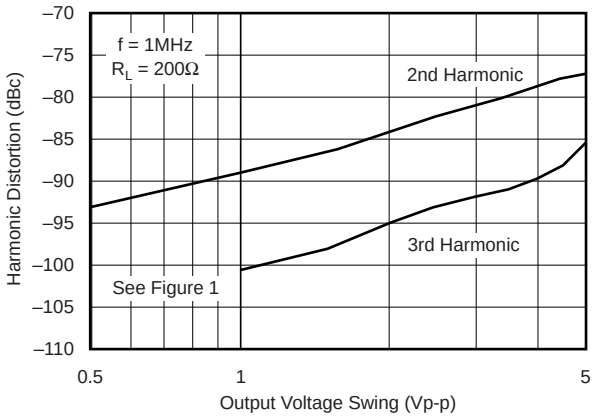
HARMONIC DISTORTION vs OUTPUT VOLTAGE (5MHz)



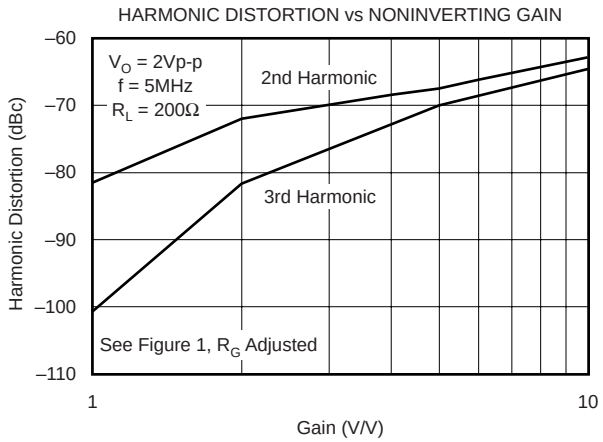
HARMONIC DISTORTION vs FREQUENCY



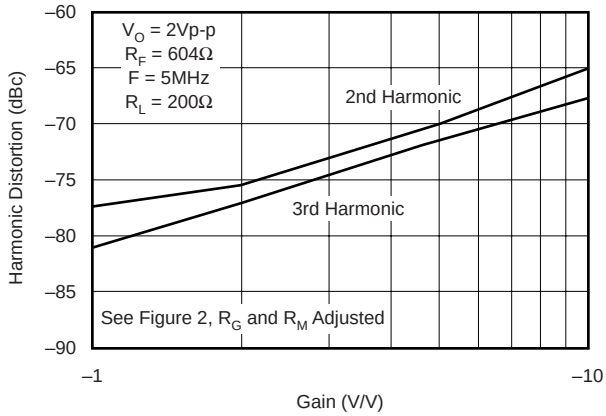
HARMONIC DISTORTION vs OUTPUT VOLTAGE (1MHz)



HARMONIC DISTORTION vs NONINVERTING GAIN



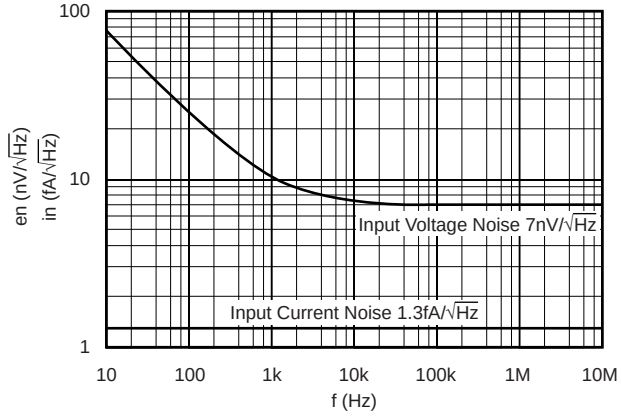
HARMONIC DISTORTION vs INVERTING GAIN



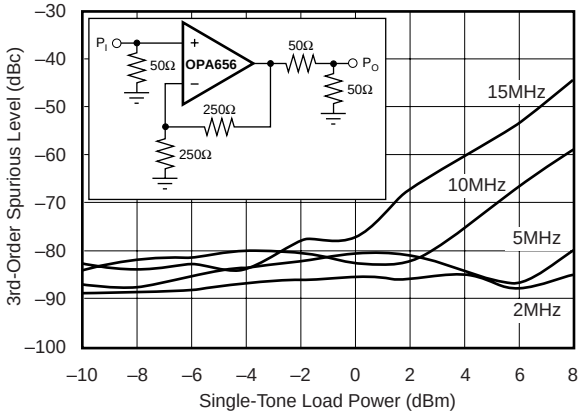
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, R_F = 250Ω, R_L = 100Ω, unless otherwise noted.

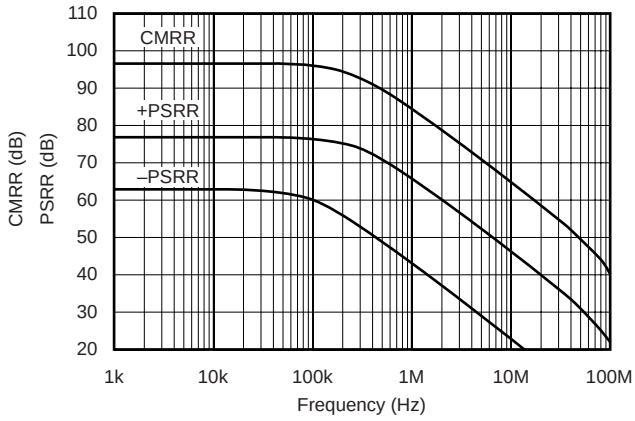
INPUT CURRENT AND VOLTAGE NOISE DENSITY



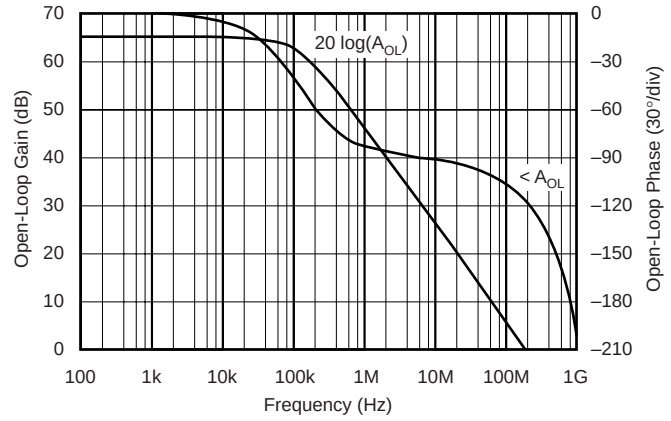
2-TONE, 3RD-ORDER
INTERMODULATION SPURIOUS



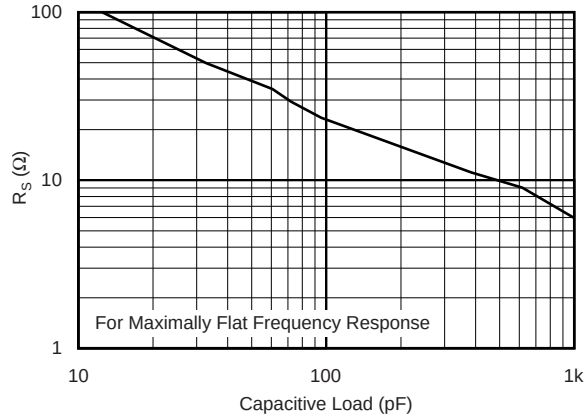
COMMON-MODE REJECTION RATIO AND
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



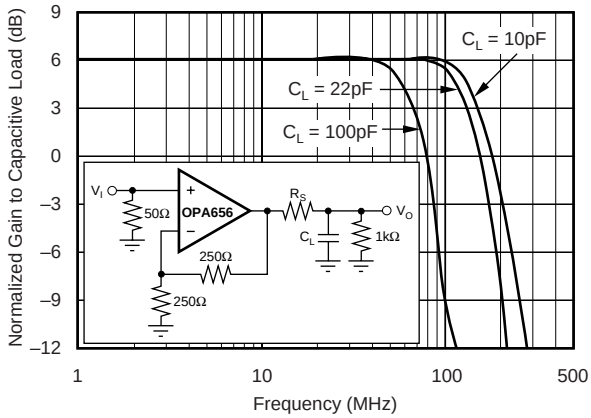
OPEN-LOOP GAIN AND PHASE



RECOMMENDED R_S vs CAPACITIVE LOAD



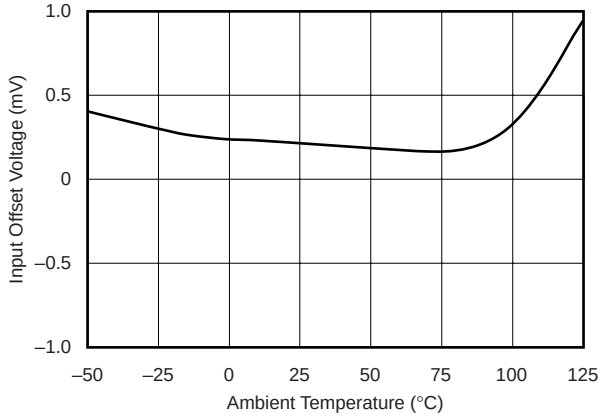
FREQUENCY RESPONSE vs CAPACITIVE LOAD



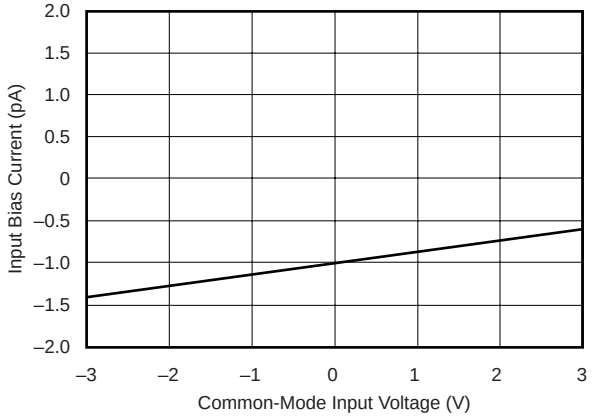
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, R_F = 250Ω, R_L = 100Ω, unless otherwise noted.

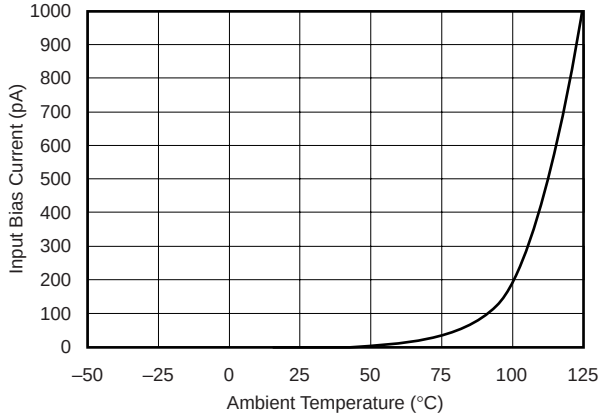
TYPICAL INPUT OFFSET VOLTAGE DRIFT OVER TEMPERATURE



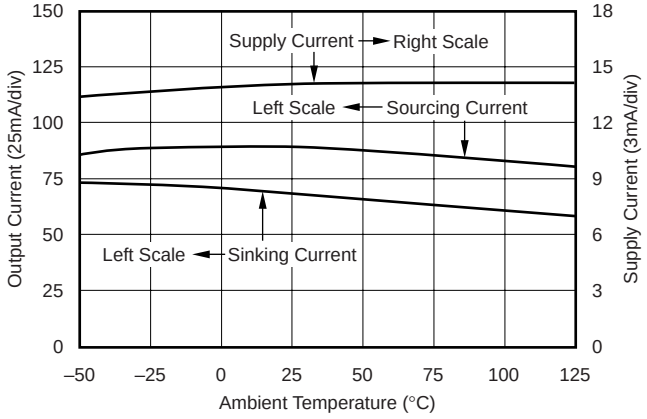
TYPICAL INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE



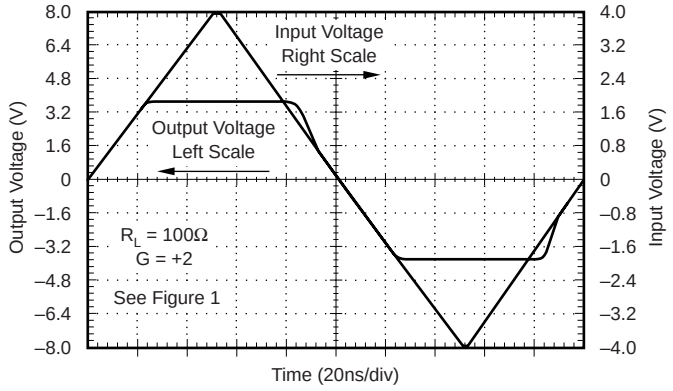
TYPICAL INPUT BIAS CURRENT DRIFT OVER TEMPERATURE



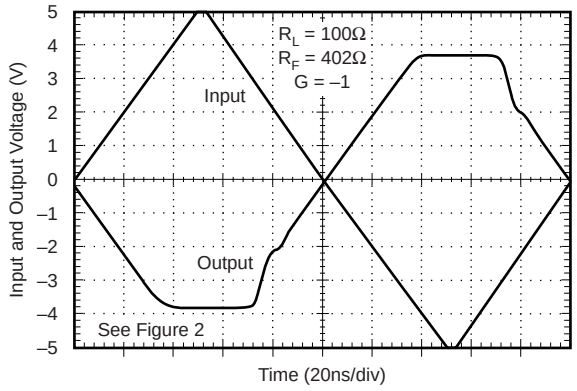
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



NONINVERTING INPUT OVERDRIVE RECOVERY



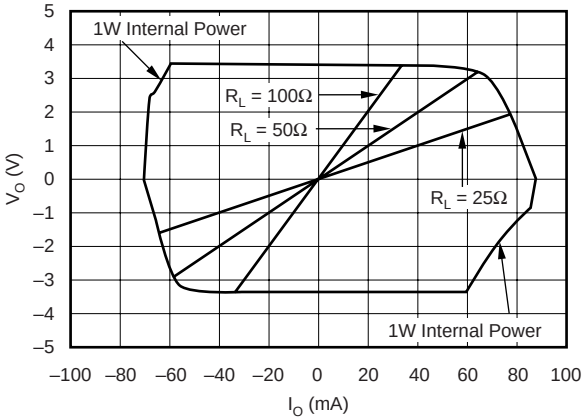
INVERTING OVERDRIVE RECOVERY



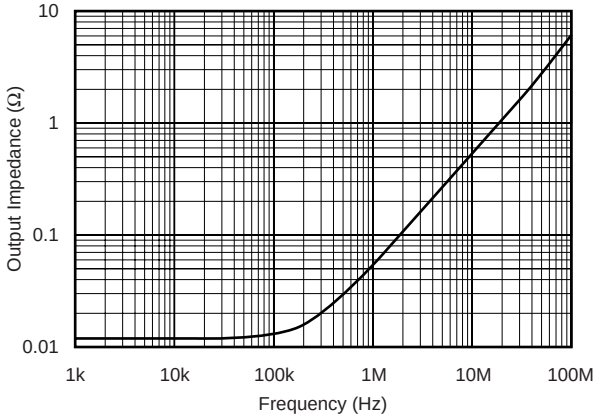
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, R_F = 250Ω, R_L = 100Ω, unless otherwise noted.

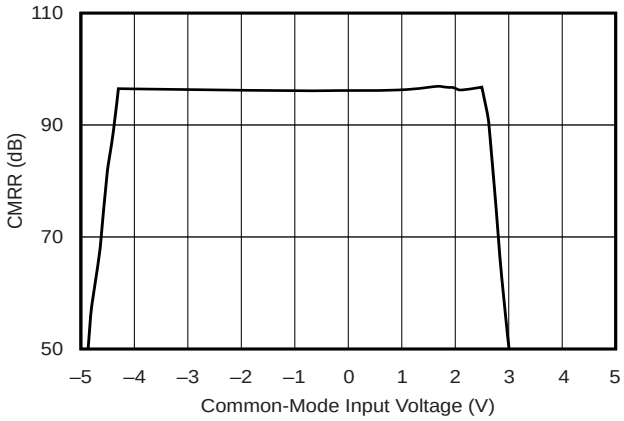
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND, NONINVERTING OPERATION

The OPA656 provides a unique combination of a broadband, unity gain stable, voltage-feedback amplifier with the DC precision of a trimmed JFET-input stage. Its very high Gain Bandwidth Product (GBP) of 230MHz can be used to either deliver high signal bandwidths for low-gain buffers, or to deliver broadband, low-noise transimpedance bandwidth to photodiode-detector applications. To achieve the full performance of the OPA656, careful attention to printed circuit board (PCB) layout and component selection is required as discussed in the remaining sections of this data sheet.

Figure 1 shows the noninverting gain of +2 circuit used as the basis for most of the Typical Characteristics. Most of the curves were characterized using signal sources with 50Ω driving impedance, and with measurement equipment presenting a 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in Figure 1) while output power specifications are at the matched 50Ω load. The total 100Ω load at the output combined with the 500Ω total feedback network load, presents the OPA656 with an effective output load of 83Ω for the circuit of Figure 1.

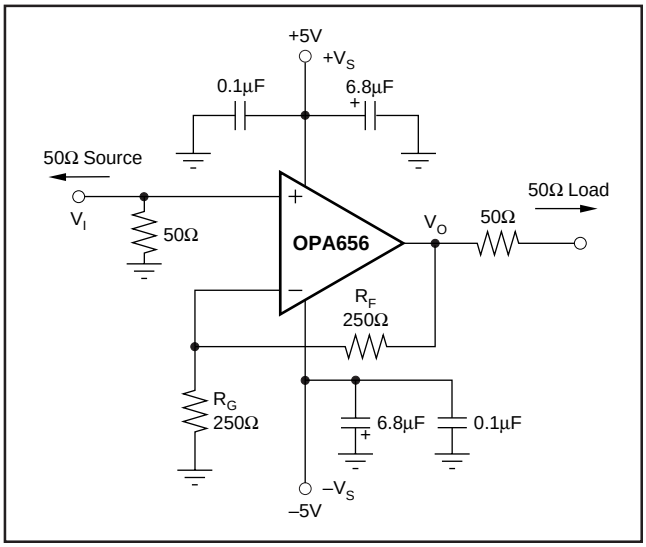


FIGURE 1. Noninverting G = +2 Specifications and Test Circuit.

Voltage-feedback op amps, unlike current feedback products, can use a wide range of resistor values to set their gain. To retain a controlled frequency response for the noninverting voltage amplifier of Figure 1, the parallel combination of R_F || R_G should always < 200Ω. In the noninverting configuration, the parallel combination of R_F || R_G will form a pole with the parasitic input capacitance at the inverting node of the OPA656 (including layout parasitics). For best performance, this pole should be at a frequency greater than the closed loop bandwidth for the OPA656. For this reason, a direct short from output to inverting input is recommended for the unity gain follower application.

WIDEBAND, INVERTING GAIN OPERATION

The circuit of Figure 2 shows the inverting gain of –1 test circuit used for most of the inverting Typical Characteristics. In this case, an additional resistor R_M is used to achieve the 50Ω input impedance required by the test equipment using in characterization. This input impedance matching is optional in a circuit board environment where the OPA656 is used as an inverting amplifier at the output of a prior stage.

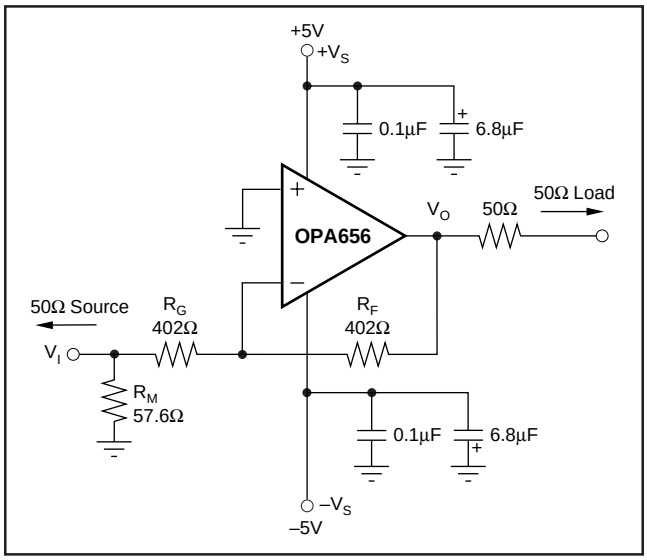


FIGURE 2. Inverting G = –1 Specifications and Test Circuit.

In this configuration, the output sees the feedback resistor as an additional load in parallel with the 100Ω load used for test. It is often useful to increase the R_F value to decrease the loading on the output (improving harmonic distortion) with the constraint that the parallel combination of R_F || R_G < 200Ω. For higher inverting gains with the DC precision provided by the FET input OPA656, consider the higher gain bandwidth product OPA657.

Figure 2 also shows the noninverting input tied directly to ground. Often, a bias current canceling resistor to ground is included here to null out the DC errors caused by input bias current effects. This is only useful when the input bias currents are matched. For a JFET part like the OPA656, the input bias currents do not match but are so low to begin with (< 5pA) that DC errors due to input bias currents are negligible. Hence, no resistor is recommended at the noninverting inputs for the inverting signal path condition.

WIDEBAND, HIGH SENSITIVITY, TRANSIMPEDANCE DESIGN

The high GBP and low input voltage and current noise for the OPA656 make it an ideal wideband transimpedance amplifier for low to moderate transimpedance gains. Higher transimpedance gains (> 100kΩ) will benefit from the low input noise current of a FET input op amp such as the OPA656. One transimpedance design example is shown on the front page of the data sheet. Designs that require high bandwidth from a large area detector will benefit from the low input voltage noise for the OPA656. This input voltage noise

is peaked up over frequency by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage ($-V_B$) applied, the desired transimpedance gain, R_F, and the GBP for the OPA656 (230MHz). Figure 3 shows a design from a 25pF source capacitance diode through a 50kΩ transimpedance gain. With these 3 variables set (including the parasitic input capacitance for the OPA656 added to C_D), the feedback capacitor value (C_F) may be set to control the frequency response.

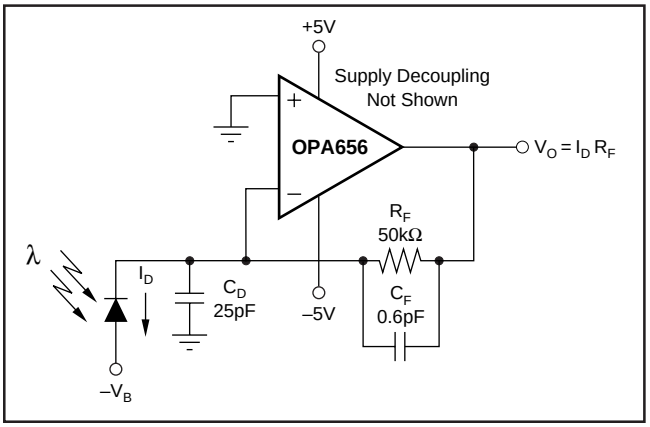


FIGURE 3. Wideband, Low-Noise, Transimpedance Amplifier.

To achieve a maximally flat 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$1/(2\pi R_F C_F) = \sqrt{(GBP/(4\pi R_F C_D))}$$

Adding the common mode and differential mode input capacitance (0.7 + 2.8)pF to the 25pF diode source capacitance of Figure 3, and targeting a 50kΩ transimpedance gain using the 230MHz GBP for the OPA656 will require a feedback pole set to 3.8MHz. This will require a total feedback capacitance of 0.8pF. Typical surface-mount resistors have a parasitic capacitance of 0.2pF leaving the required 0.6pF value shown in Figure 3 to get the required feedback pole.

This will give an approximate –3dB bandwidth set by:

$$f_{-3dB} = \sqrt{GBP/2\pi R_F C_D)}\ Hz$$

The example of Figure 3 will give approximately 5.7MHz flat bandwidth using the 0.6pF feedback compensation.

If the total output noise is bandlimited to a frequency less than the feedback pole frequency ($1/R_F C_F$), a very simple expression for the equivalent input noise current can be derived as:

$$I_{EQ} = \sqrt{I_N^2 + \frac{4kT}{R_F} + \left(\frac{E_N}{R_F}\right)^2 + \frac{(E_N 2\pi C_D F)^2}{3}}$$

Where:

i_{EQ} = Equivalent input noise current if the output noise is bandlimited to $F < 1/(2\pi R_F C_D)$.

i_N = Input current noise for the op amp inverting input.

e_N = Input voltage noise for the op amp.

C_D = Diode capacitance.

F = Bandlimiting frequency in Hz (usually a postfilter prior to further signal processing).

4kT = 1.6E – 20J at 290°K.

Evaluating this expression up to the feedback pole frequency at 3.8MHz for the circuit of Figure 3, gives an equivalent input noise current of 2.7pA/$\sqrt{Hz}$. This is much higher than the 1.3fA/$\sqrt{Hz}$ for just the op amp itself. This result is being dominated by the last term in the equivalent input noise current expression. It is essential in this case to use a low voltage noise op amp.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA656 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA656U	SO-8	DEM-OPA-SO-1A	SBOU009
OPA656N	SOT23-5	DEM-OPA-SOT-1A	SBOU010

TABLE I. Demonstration Fixtures by Package.

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA656 product folder.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO MINIMIZE NOISE

The OPA656 provides a very low input noise voltage while requiring a low 14mA quiescent supply current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. Figure 4 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

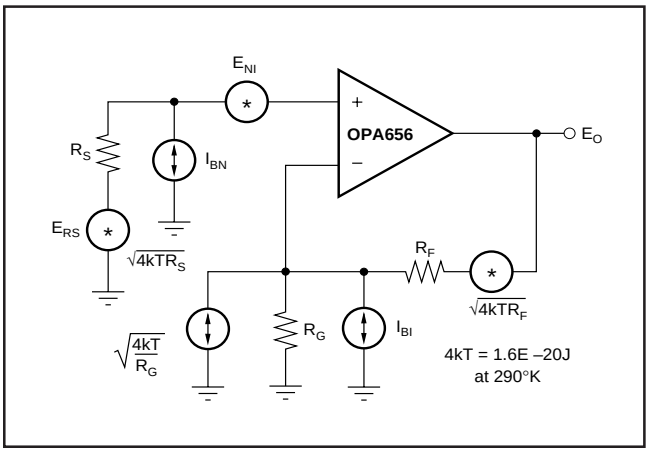


FIGURE 4. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 1 shows the general form for this output noise voltage using the terms shown in Figure 4.

(1)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain ($G_N = 1+R_F/R_G$) will give the equivalent input referred spot noise voltage at the noninverting input as shown in Equation 2.

(2)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Putting high resistor values into Equation 2 can quickly dominate the total equivalent input referred noise. A source impedance on the noninverting input of 3kΩ will add a Johnson voltage noise term equal to just that for the amplifier itself (7nV/$\sqrt{Hz}$). While the JFET input of the OPA656 is ideal for high source impedance applications, both the overall bandwidth and noise will be limited by higher source impedances in the noninverting configuration of Figure 1.

FREQUENCY RESPONSE CONTROL

Voltage-feedback op amps like the OPA656 exhibit decreasing signal bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the Electrical Characteristics. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factors), most high-speed amplifiers will exhibit a more complex response with lower phase margin. The OPA656 is compensated to give a maximally flat 2nd-order Butterworth closed loop response at a noninverting gain of +2 (Figure 1). This results in a typical gain of +2 bandwidth of 200MHz, far exceeding that predicted by dividing the 230MHz GBP by 2. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10 the OPA656 will show the 23MHz bandwidth predicted using the simple formula and the typical GBP of 230MHz.

Unity-gain stable op amps like the OPA656 can also be bandlimited using a capacitor across the feedback resistor. For the noninverting configuration of Figure 1, a capacitor across the feedback resistor will decrease the gain with frequency down to a gain of +1. For instance, to bandlimit the gain of +2 design to 20MHz, a 32pF capacitor can be placed in parallel with the 250Ω feedback resistor. This will, however, only decrease the gain from 2 to 1. Using a feedback capacitor to limit the signal bandwidth is more effective in the inverting configuration of Figure 2. Adding that same capacitor to the feedback of Figure 2 will set a pole in the signal frequency response at 20MHz, but in this case it will continue to attenuate the signal gain to below 1. However, the output noise contribution due the input voltage noise of the OPA656 will still only be reduced to a gain of 1 with the addition of the feedback capacitor.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA656 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between

the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus Capacitive Load and the resulting frequency response at the load. In this case, a design target of a maximally flat frequency response was used. Lower values of R_S may be used if some peaking can be tolerated. Also, operating at higher gains (than the +2 used in the Typical Characteristics) will require lower values of R_S for a minimally peaked frequency response. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA656. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA656 output pin (see Board Layout section).

DISTORTION PERFORMANCE

The OPA656 is capable of delivering a low distortion signal at high frequencies over a wide range of gains. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic will dominate the distortion with negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration this is sum of $R_F + R_G$, while in the inverting configuration this is just R_F (see Figure 1). Increasing output voltage swing increases harmonic distortion directly. A 6dB increase in output swing will generally increase the 2nd-harmonic 12dB and the 3rd-harmonic 18dB. Increasing the signal gain will also increase the 2nd-harmonic distortion. Again a 6dB increase in gain will increase the 2nd- and 3rd-harmonic by about 6dB even with a constant output power and frequency. And finally, the distortion increases as the fundamental frequency increases due to the rolloff in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open loop pole at approximately 100kHz. Starting from the –70dBc 2nd-harmonic for a 5MHz, $2V_{PP}$ fundamental into a 200Ω load at G = +2 (from the Typical Characteristics), the 2nd-harmonic distortion for frequencies lower than 100kHz will be < –105dBc.

The OPA656 has an extremely low 3rd-order harmonic distortion. This also shows up in the 2-tone 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low (< –80dBc) at low output power levels. The output stage continues to hold them low even as the fundamental power reaches higher levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For 2 tones centered at 10MHz, with 4dBm/tone into a matched 50Ω load (that is, $1V_{PP}$ for each tone at the load, which requires $4V_{PP}$ for the overall 2-tone envelope at the output pin), the Typical Characteristics show a 78dBc difference between the test tone and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies and/or higher load impedances.

DC ACCURACY AND OFFSET CONTROL

The OPA656 can provide excellent DC accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and its trimmed input offset voltage (and drift) along with the negligible errors introduced by the low input bias current. For the best DC precision, a high-grade version (OPA656UB or OPA656NB) screens the key DC parameters to an even tighter limits. Both standard- and high-grade versions take advantage of a new final test technique to 100% test input offset voltage drift over temperature. This discussion will use the high-grade typical and min/max electrical characteristics for illustration; however, an identical analysis applies to the standard-grade version.

The total output DC offset voltage in any configuration and temperature will be the combination of a number of possible error terms. In a JFET part like the OPA656, the input bias current terms are typically quite low but are unmatched. Using bias current cancellation techniques, more typical in bipolar input amplifiers, does not improve output DC offset errors. Errors due to the input bias current will only become dominant at elevated temperatures. The OPA656 shows the typical 2x increase in every 10°C common to JFET-input stage amplifiers. Using the 5pA maximum tested value at 25°C, and a 20°C internal self heating (see thermal analysis), the maximum input bias current at 85°C ambient will be $5pA \bullet 2^{(105 - 25)/10} = 1280pA$. For noninverting configurations, this term only begins to be a significant term versus the input offset voltage for source impedances > 750kΩ. This would also be the feedback-resistor value for transimpedance applications (see Figure 3) where the output DC error due to inverting input bias current is on the order of that contributed by the input offset voltage. In general, except for these extremely high impedance values, the output DC errors due to the input bias current may be neglected.

After the input offset voltage itself, the most significant term contributing to output offset voltage is the PSRR for the negative supply. This term is modeled as an input offset voltage shift due to changes in the negative power-supply voltage (and similarly for the +PSRR). The high-grade test limit for –PSRR is 62dB. This translates into 1.59mV/V input offset voltage shift = $10^{(-62/20)}$. In the worst case, a ±0.38V (±7.6%) shift in the negative supply voltage will produce a ±0.6mV apparent input offset voltage shift. Since this is comparable to the tested limit of ±0.6mV input offset voltage,

a careful control of the negative supply voltage is required. The +PSRR is tested to a minimum value of 74dB. This translates into $10^{(-74/20)}$ = 0.2mV/V sensitivity for the input offset voltage to positive power supply changes.

As an example, compute the worst-case output DC error for the transimpedance circuit of Figure 1 at 25°C and then the shift over the 0°C to 70°C range given the following assumptions.

Negative Power Supply

= –5V ±0.2V with a ±5mV/°C worst-case shift

Positive Power Supply

= +5V ±0.2V with a ±5mV/°C worst-case shift

Initial 25°C Output DC Error Band

= ±0.3mV (due to the –PSRR = 1.59mV/V • ±0.2V)

±0.04mV (due to the +PSRR = 0.2mV/V • ±0.2V)

±0.6mV Input Offset Voltage

Total = ±0.94mV

This would be the worst-case error band in volume production at 25°C acceptance testing given the conditions stated.

Over the temperature range of 0°C to 70°C, we can expect the following worst-case shifting from initial value. A 20°C internal junction self heating is assumed here.

±0.36mV (OPA656 high-grade input offset drift)

= ±6µV/°C • (70°C + 20°C – 25°C))

±0.23mV (–PSRR of 60dB with 5mV • (70°C – 25°C) supply shift)

±0.06mV (+PSRR of 72dB with 5mV • (70°C – 25°C) supply shift)

Total = ±0.65mV

This would be the worst-case shift from initial offset over a 0°C to 70°C ambient for the conditions stated. Typical initial output DC error bands and shifts over temperature will be much lower than these worst-case estimates.

In the transimpedance configuration, the CMRR errors can be neglected since the input common mode voltage is held at ground. For noninverting gain configurations (see Figure 1), the CMRR term will need to be considered but will typically be far lower than the input offset voltage term. With a tested minimum of 80dB (100µV/V), the added apparent DC error will be no more than ±0.2mV for a ±2V input swing to the circuit of Figure 1.

POWER-SUPPLY CONSIDERATIONS

The OPA656 is intended for operation on ±5V supplies. Single-supply operation is allowed with minimal change from the stated specifications and performance from a single supply of +8V to +12V maximum. The limit to lower supply voltage operation is the useable input voltage range for the JFET-input stage. Operating from a single supply of +12V can have numerous advantages. With the negative supply at ground, the DC errors due to the –PSRR term can be minimized. Typically, AC performance improves slightly at +12V operation with minimal increase in supply current.

THERMAL ANALYSIS

The OPA656 will not require heatsinking or airflow in most applications. Maximum allowed junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA656N (SOT23-5 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load.

$P_D = 10V \bullet 16.1mA + 5^2 /(4 \bullet (100\Omega \parallel 800\Omega)) = 231mW$

Maximum T_J = +85°C + (0.23W • 150°C/W) = 120°C.

All actual applications will be operating at lower internal power and junction temperature.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier like the OPA656 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1uF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) **Careful selection and placement of external components will preserve the high frequency performance of the OPA656**. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. It has been suggested here that a good starting point for design would be to keep $R_F \parallel R_G$ < 250Ω for voltage amplifier applications. Doing this will automatically keep the resistor noise terms low, and minimize the effect of their parasitic capacitance. Transimpedance applications (see Figure 3) can use whatever feedback resistor is required by the application as long as the feedback compensation capacitor is set considering all parasitic capacitance terms on the inverting node.

d) **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA656 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin) If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA656 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device—this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *Recommended R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) **Socketing a high speed part like the OPA656 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA656 onto the board.

INPUT AND ESD PROTECTION

The OPA656 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 5.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±12V supply parts driving into the OPA656), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

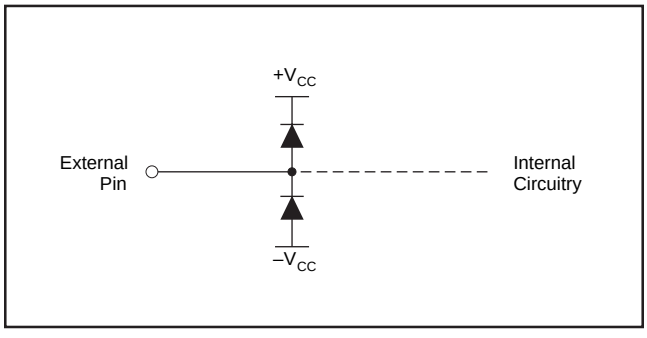


FIGURE 5. Internal ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
11/08	G	2	Abs Max Ratings	Changed Storage Temperature Range from –40°C to +125C to –65°C to +125C.
		3	Electrical Characteristics	DC Performance section; deleted *Drift* from Input Offset Current specifications.
3/06	F	11	Design-In Tools	Added Design-In Tools paragraph and table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA656N/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA656N/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA656NB/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA656NB/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
OPA656U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
OPA656U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
OPA656U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
OPA656UB	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
OPA656UB/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
OPA656UB/2K5G4	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	Samples Not Available
OPA656UBG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
OPA656UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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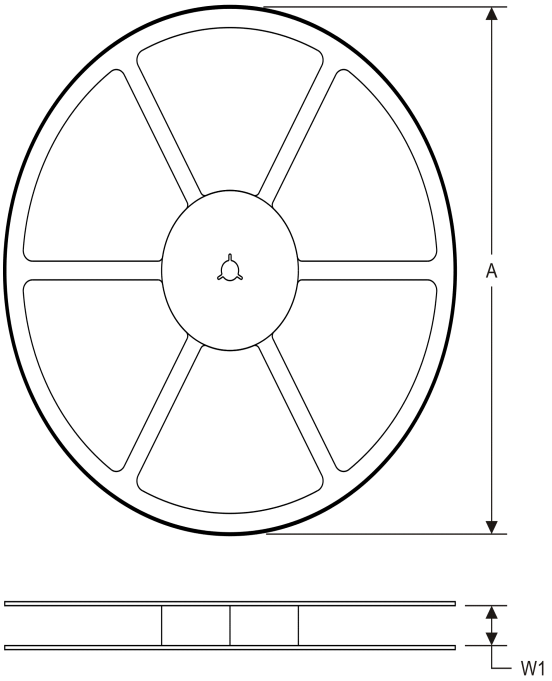
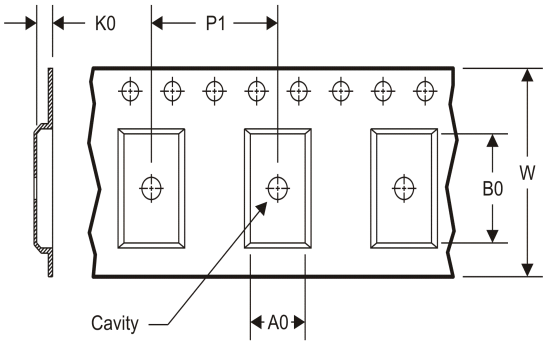
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



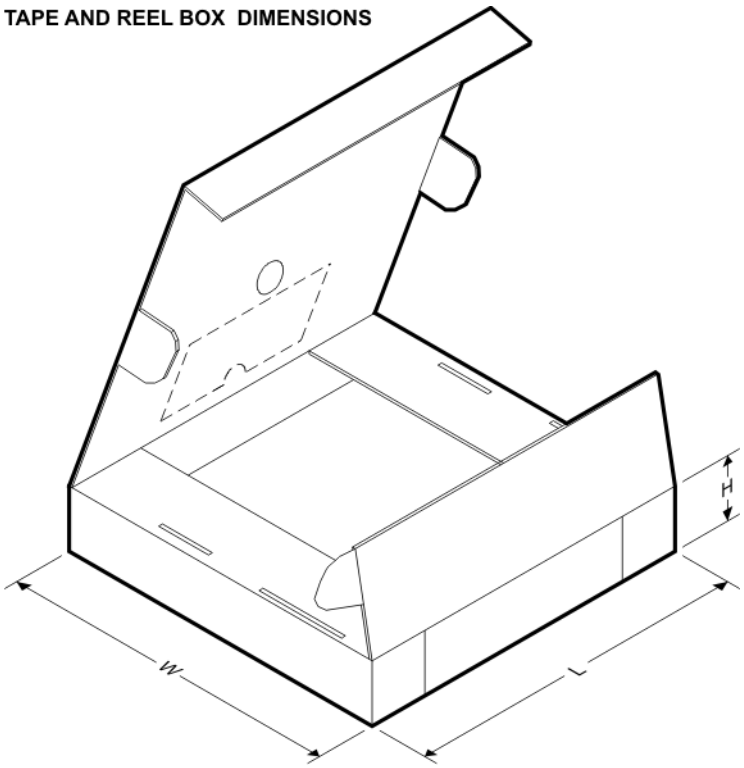
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA656N/250	SOT-23	DBV	5	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA656NB/250	SOT-23	DBV	5	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA656U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA656UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

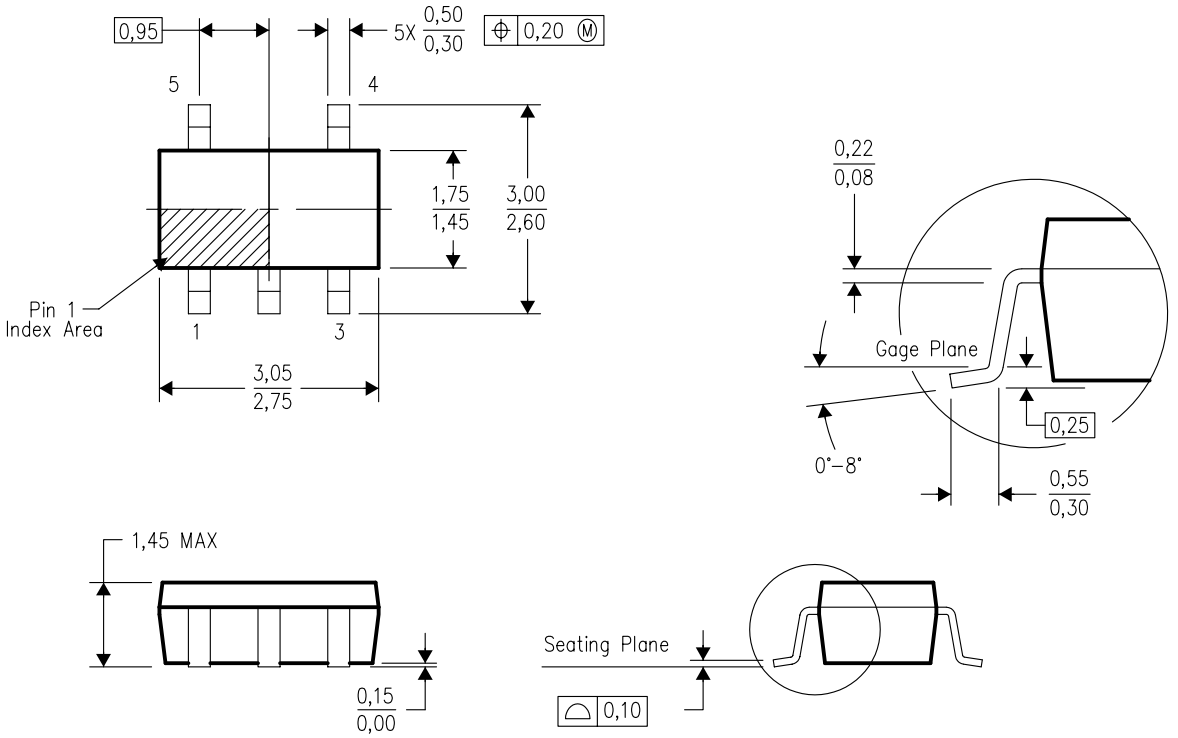
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA656N/250	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA656NB/250	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA656U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA656UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0

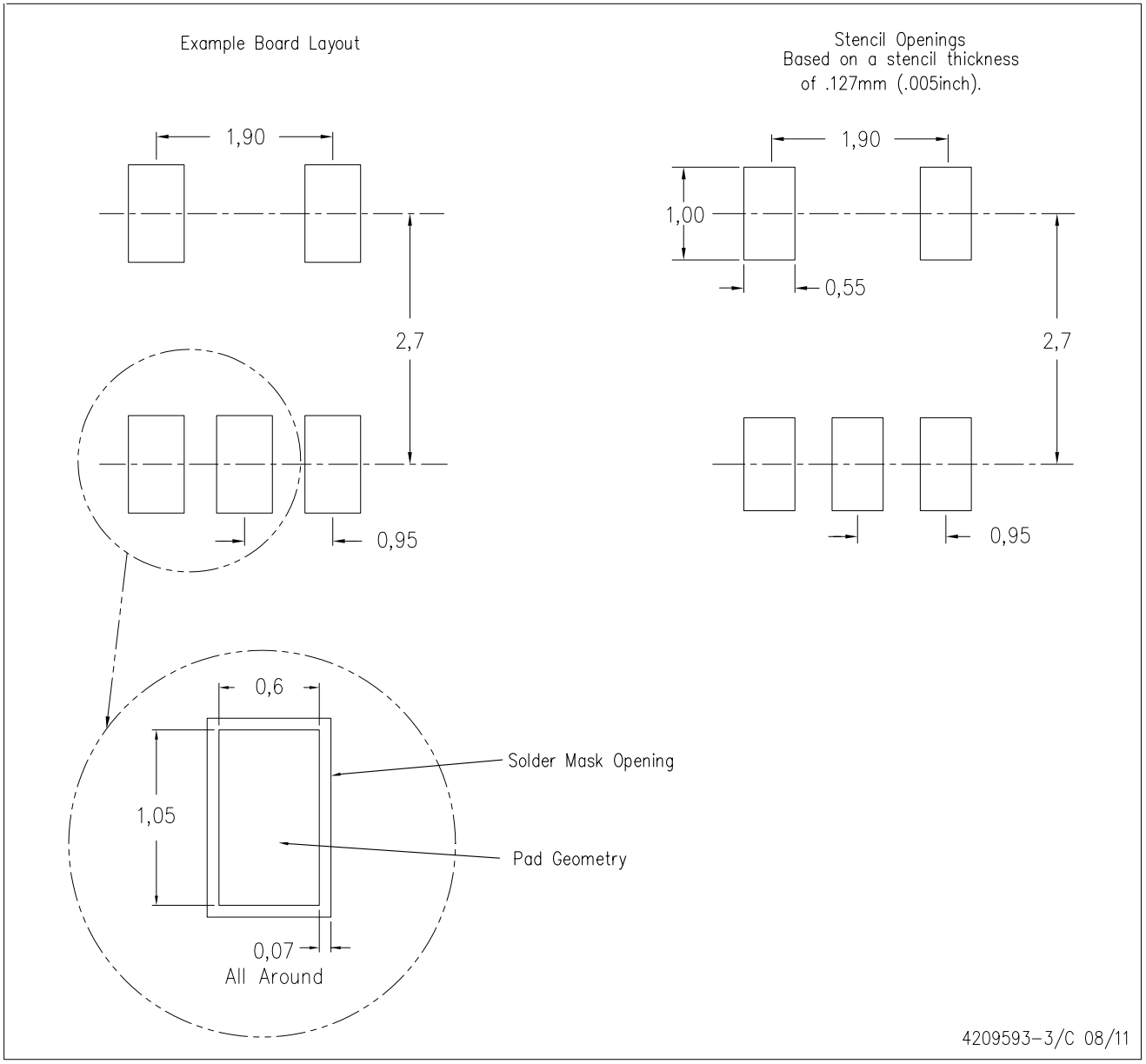
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

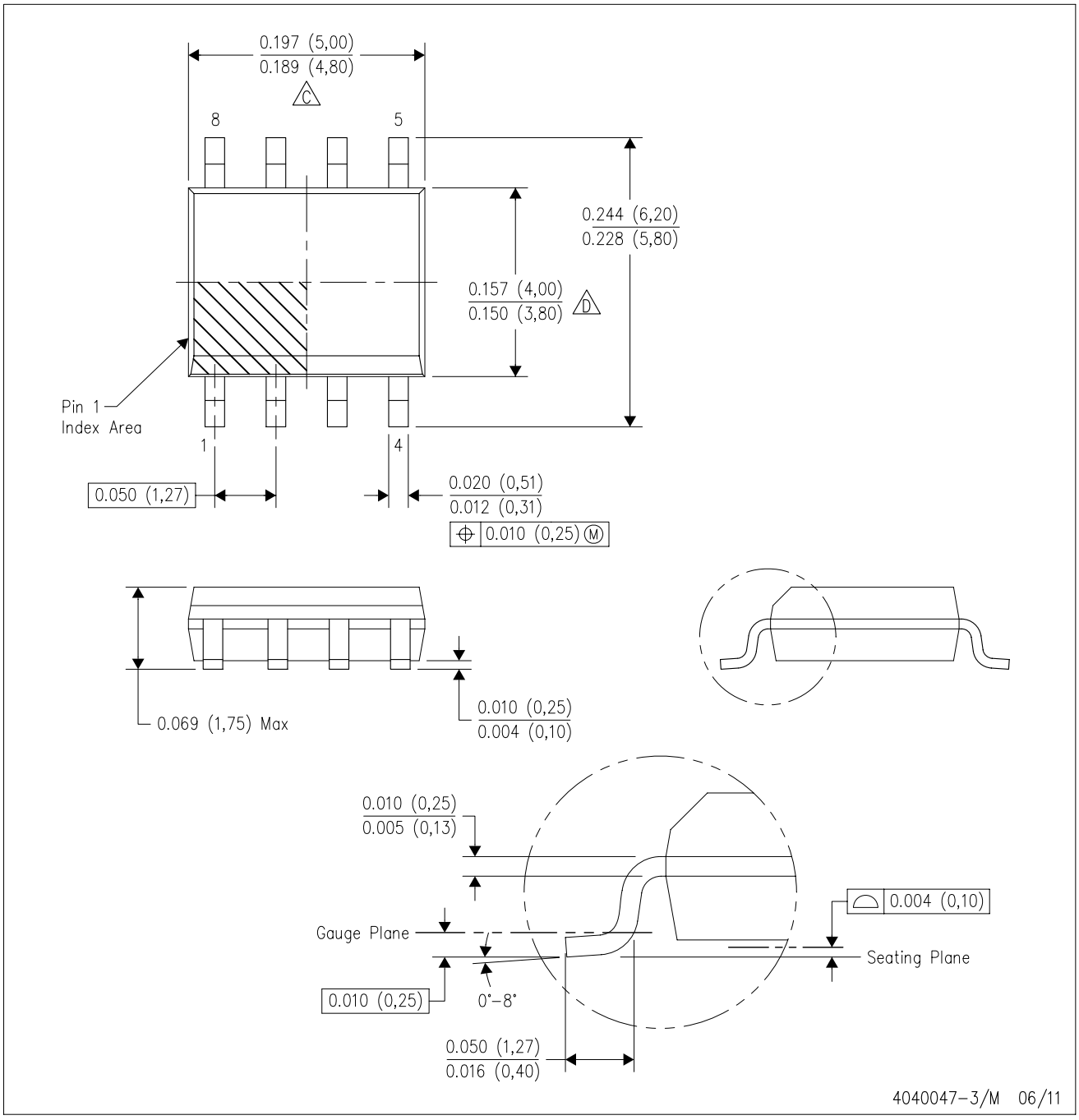
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



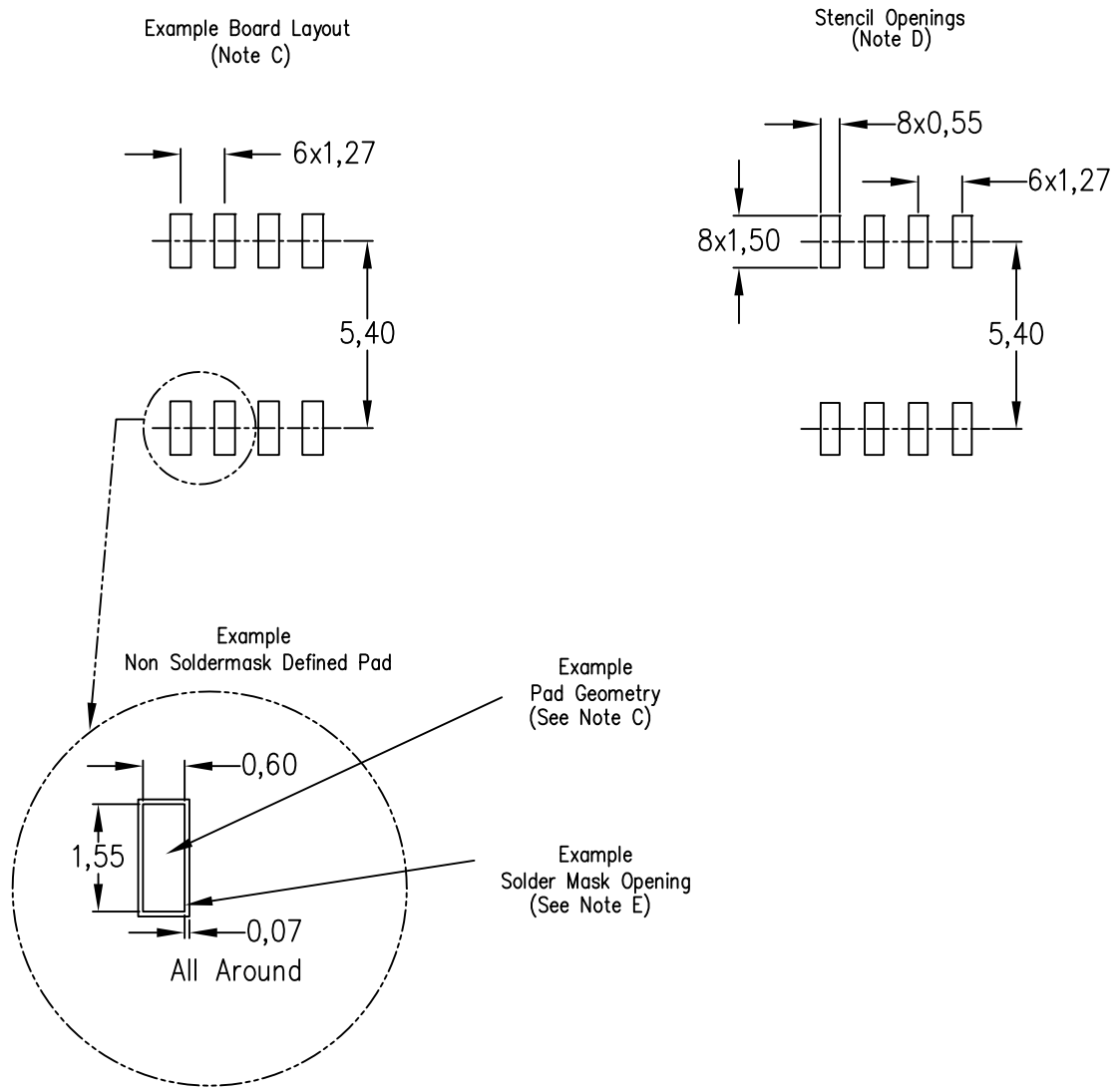
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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