400MHz Quadrature IF Demodulator with RSSI

FEATURES

- **Single 1.8V to 5.25V Supply**
- **IF Frequency Range: 70MHz to 400MHz**
- **84dB Limiting IF Gain**
- **90dB Linear RSSI Range**
- **7.7MHz Lowpass Output Filter**
- Baseband I/Q Amplitude Imbalance: <0.7dB
- 4dB Noise Figure
- Low Supply Current: 25mA
- Outputs Biased Up While in Standby
- Shutdown Current: 1µA
- 24-Lead Narrow SSOP Package

APPLICATIONS

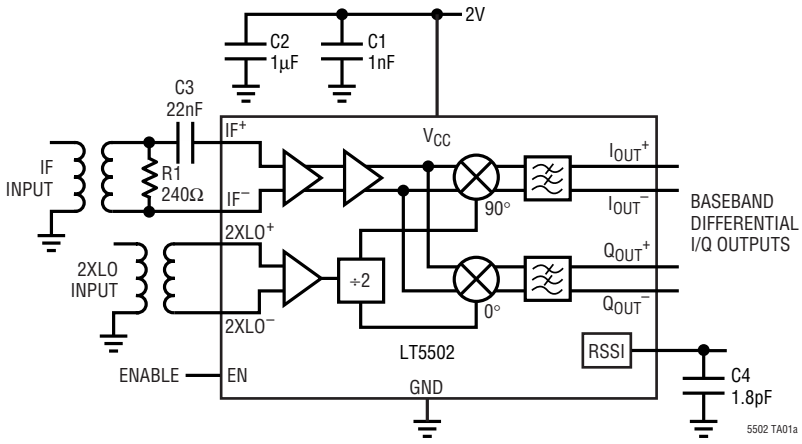
- IEEE802.11
- High Speed Wireless LAN
- Wireless Local Loop

DESCRIPTION

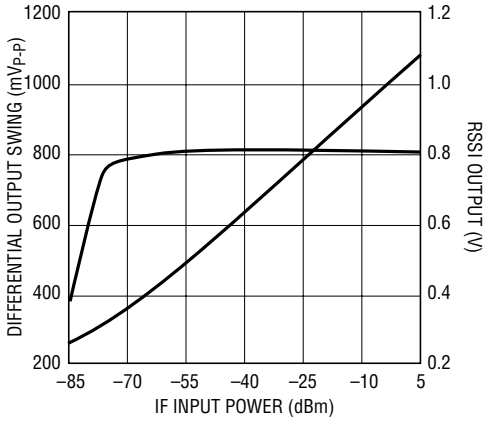
The LT®5502 is a 70MHz to 400MHz monolithic integrated quadrature IF demodulator. It consists of an IF limiter, quadrature down mixers, integrated lowpass filters, and divide-by-two LO buffers. The demodulator provides all building blocks for demodulation of I and Q baseband signals with a single supply voltage of 1.8V to 5.25V. The IF limiter has 84dB small-signal gain, and a built-in receive signal strength indicator (RSSI) with over 90dB linear range. The input referred noise-spectral-density is 1.45nV/√Hz, which is equivalent to a 4dB noise figure when the input is terminated with a 50Ω source. The integrated lowpass output filters act as antialiasing and pulse-shaping filters for demodulated I/Q-baseband signals. The 3dB cutoff frequency of the filters is about 7.7MHz. The VCO frequency is required to be twice the desired operating frequency to provide quadrature local oscillator (LO) signals to the mixers. The standby mode provides fast transient response to the receive mode with reduced supply current when the I/Q outputs are AC-coupled to a baseband chip.

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TYPICAL APPLICATION



I/Q Output Swing, RSSI Output vs IF Input Power



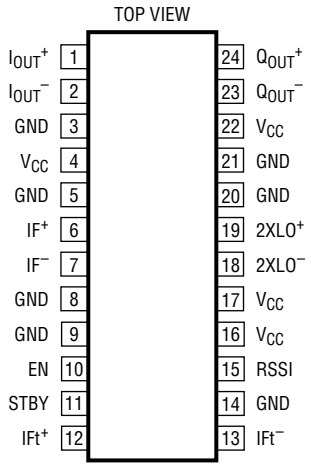
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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage 5.5V
LO Input Power 10dBm
IF Input Power 10dBm
Operating Ambient
Temperature (Note 2) .....–40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C
Voltage on any Pin not to Exceed ..... V_{CC}

PACKAGE/ORDER INFORMATION



GN PACKAGE
24-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LT5502EGN

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3V, f_{2XLO} = 570MHz, P_{2XLO} = –10dBm, f_{IF} = 280MHz, P_{IF} = –50dBm, T_A = 25°C, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IF Input						
f_{IF}	Frequency Range			70 to 400		MHz
	3dB Limiting Sensitivity			–79		dBm
	Noise Figure	Terminated 50Ω Source		4		dB
	DC Common Mode Voltage			2.6		V
Demodulator I/Q Output						
	I/Q Output Voltage Swing	Differential		850		mV_{P-P}
	I/Q Amplitude Mismatch			0.1	0.7	dB
	I/Q Phase Mismatch			0.6		DEG
	Output Driving Capability	Differential; C_{MAX} = 10pF	1.5			kΩ
	DC Common Mode Voltage			1.84		V
RSSI						
	Linear Dynamic Range (Note 4)	±3dB Linearity Error		90		dB
	Output Impedance			3.8		kΩ
	Output Voltage	Input = –70dBm	0.27	0.41	0.54	V
	Output Voltage	Input = 0dBm	0.8	1.01	1.2	V
	Output Voltage Slope	Input from –70dBm to 0dBm		8.7		mV/dB
	Linearity Error	Input from –70dBm to 0dBm		1		dB
Baseband Lowpass Filter						
	3dB Cutoff Frequency			7.7		MHz
	Group Delay Ripple			16.4		ns

ELECTRICAL CHARACTERISTICS

V_{CC} = 3V, f_{2XLO} = 570MHz, P_{2XLO} = –10dBm, f_{IF} = 280MHz, P_{IF} = –50dBm, T_A = 25°C, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2XLO						
f_{2XLO}	Frequency Range			140 to 800		MHz
P_{2XLO}	Input Power		–20		–5	dBm
	DC Common Mode Voltage			2.6		V
Power Supply						
V_{CC}	Supply Voltage		1.8		5.25	V
I_{CC}	Supply Current	EN = High		25	32	mA
I_{OFF}	Shutdown Current	EN = Low; Standby = Low		1	100	µA
	Standby Mode Current	EN = Low; Standby = High		2.6	3.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life a device may be impaired.

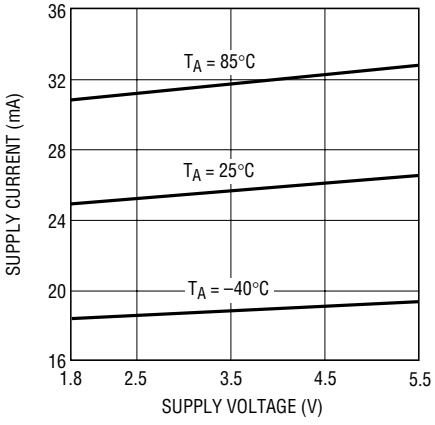
Note 2: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Tests are performed as shown in the configuration of Figure 3.

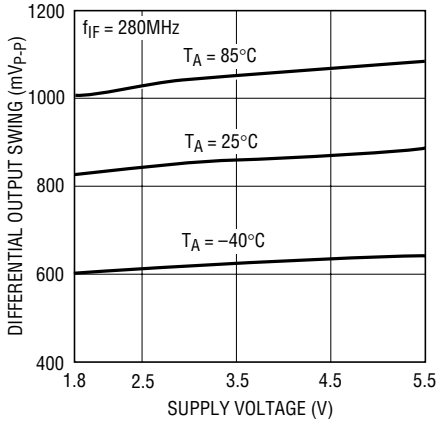
Note 4: Tests are performed as shown in the configuration of Figure 1 for IF input.

TYPICAL PERFORMANCE CHARACTERISTICS (Note 3)

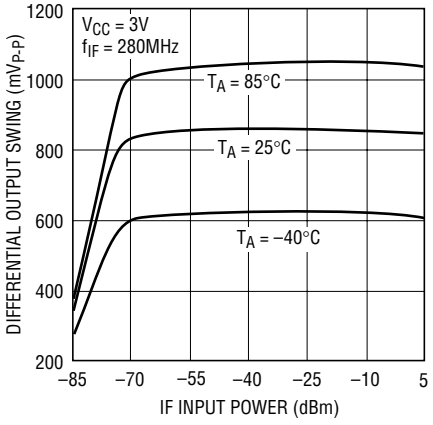
Power Supply Current vs Temperature



I/Q Output Swing vs Temperature

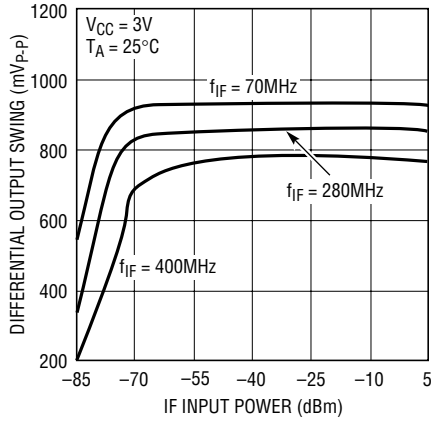


I/Q Output Swing vs IF Input Power



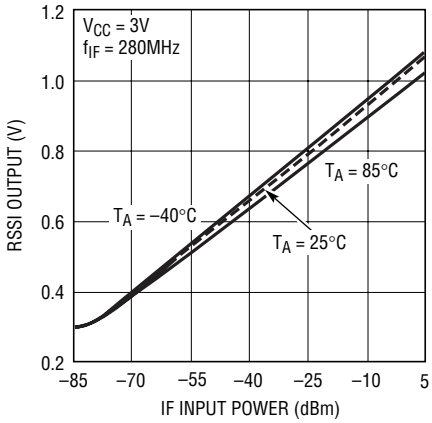
TYPICAL PERFORMANCE CHARACTERISTICS (Note 3)

I/Q Output Swing vs IF Input Power



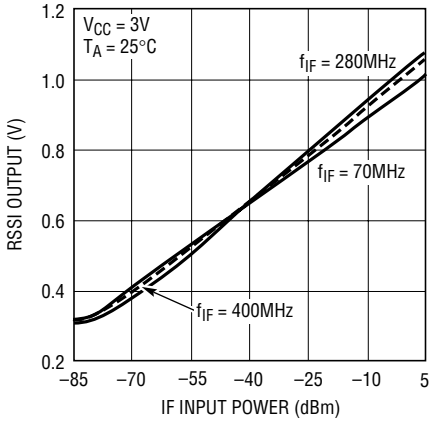
5502 G04

RSSI Output vs Temperature



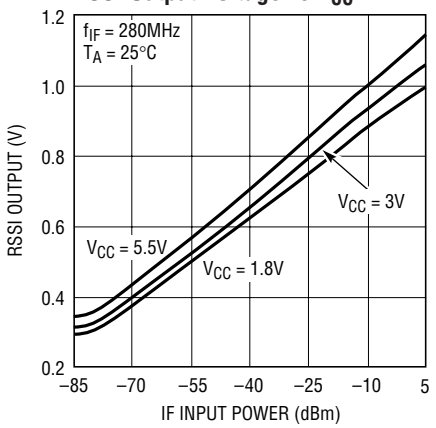
5502 G05

RSSI Output Voltage vs IF Frequency



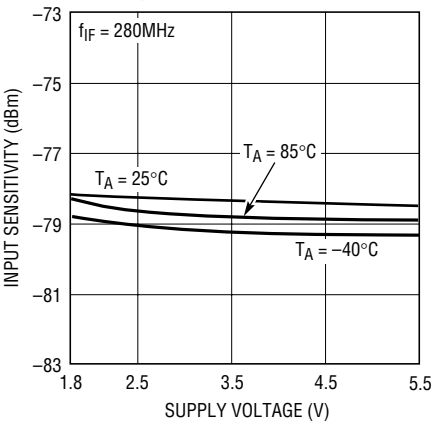
5502 G06

RSSI Output Voltage vs V_{CC}



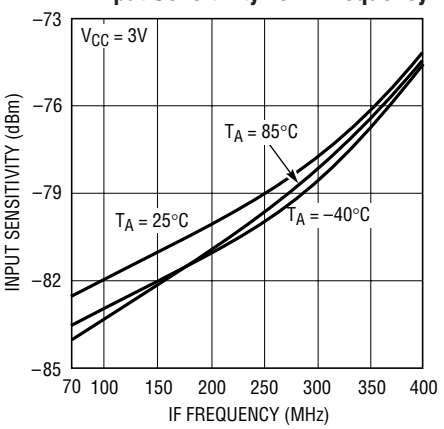
5502 G07

IF Input Sensitivity vs Temperature



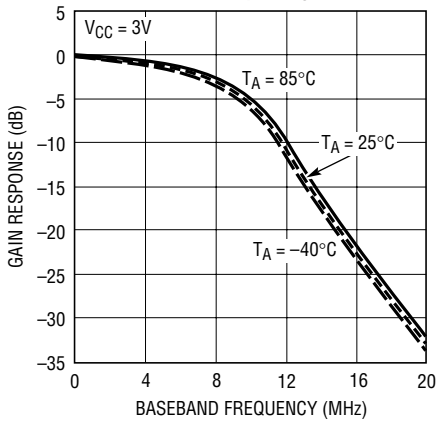
5502 G08

IF Input Sensitivity vs IF Frequency



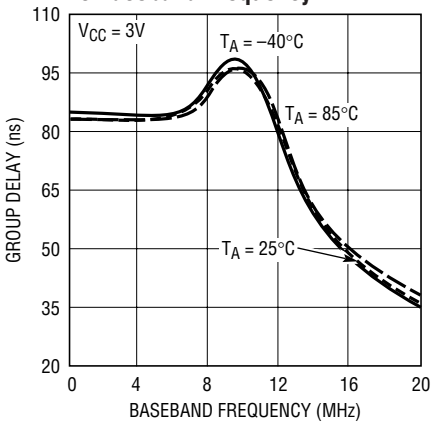
5502 G09

LPF Frequency Response vs Baseband Frequency



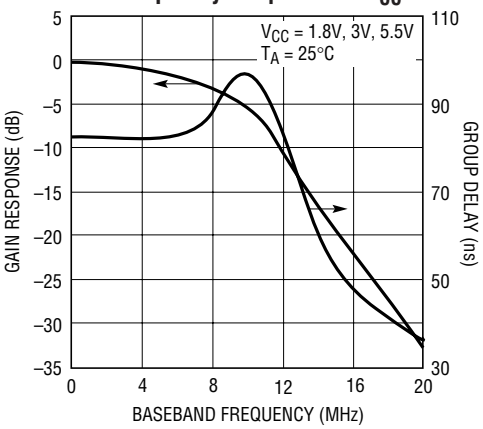
5502 G10

LPF Group Delay vs Baseband Frequency



5502 G11

LPF Frequency Response vs V_{CC}



5502 G12

PIN FUNCTIONS

I_{OUT}^+ (Pin 1): Positive Baseband Output Pin of I-Channel. The DC bias voltage is V_{CC} – 1.16V. This pin should not be shorted to ground.

I_{OUT}^- (Pin 2): Negative Baseband Input Pin of I-Channel. The DC bias voltage is V_{CC} – 1.16V. This pin should not be shorted to ground.

GND (Pins 3, 5, 8, 9, 14, 20, 21): Ground Pin.

V_{CC} (Pins 4, 16, 17, 22): Power Supply Pin. This pin should be decoupled using 1000pF and 0.1μF capacitors.

IF^+ (Pin 6): Positive IF Input Pin. The DC bias voltage is V_{CC} – 0.4V.

IF^- (Pin 7): Negative IF Input Pin. The DC bias voltage is V_{CC} – 0.4V.

EN (Pin 10): Enable Pin. When the input voltage is higher than 0.9V or up to V_{CC}, the circuit is completely turned on. When the input voltage is less than 0.7V or down to ground, the circuit is turned off except the part of the circuit associated with standby mode.

STBY (Pin 11): Standby Pin. When the input voltage is higher than 0.9V or up to V_{CC}, the circuit of standby mode is turned on to bias the I/Q buffers to desired quiescent voltage. When the input voltage is less than 0.7V or down to ground, it is turned off.

IFt^+ (Pin 12): Interstage IF Positive Pin. The DC bias voltage is V_{CC} – 0.25V.

IFt^- (Pin 13): Interstage IF Negative Pin. The DC bias voltage is V_{CC} – 0.25V.

RSSI (Pin 15): RSSI Output Pin.

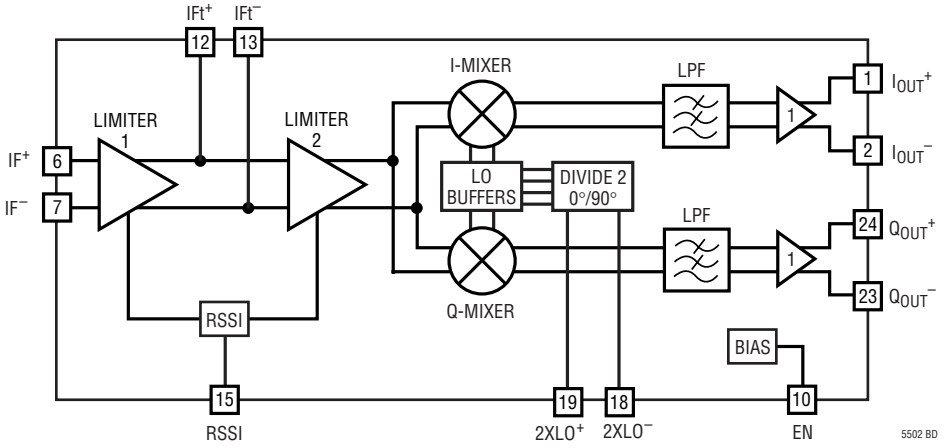
$2XLO^-$ (Pin 18): Negative Carrier Input Pin. The input-signal's frequency must be twice that of the desired demodulator LO frequency. The DC bias voltage is V_{CC} – 0.4V.

$2XLO^+$ (Pin 19): Positive Carrier Input Pin. The input-signal's frequency must be twice that of the desired demodulator LO frequency. The DC bias voltage is V_{CC} – 0.4V.

Q_{OUT}^- (Pin 23): Negative Baseband Output Pin of the Q-Channel. The DC bias voltage is V_{CC} – 1.16V. This pin should not be shorted to ground.

Q_{OUT}^+ (Pin 24): Positive Baseband Output Pin of the Q-Channel. The DC bias voltage is V_{CC} – 1.16V. This pin should not be shorted to ground.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT5502 consists of the following sections: IF limiter, I/Q demodulators, quadrature LO carrier generator, integrated lowpass filters (LPFs), and bias circuitry.

An IF signal is fed to the inputs of the IF limiter. The limited IF signal is then demodulated into I/Q baseband signals using the quadrature LO carriers that are generated from the divide-by-two circuit. The demodulated I/Q signals are passed through 5th order LPFs and buffered with an output driver.

IF Limiter

The IF limiter has 84dB small-signal gain with a frequency range of 70MHz to 400MHz. It consists of two cascaded stages of IF amplifiers/limiters. The differential outputs of the first stage are connected internally to the differential inputs of the second stage. An interstage filtering is possible in between (Pin 12 and Pin 13) with minimum off-chip components. It can be a simple parallel LC tank circuit L1 and C8 as shown in Figure 3. The 22nF blocking capacitor, C19, is used for the proper operation of the internal DC offset canceling circuit. To achieve the best receiver sensitivity, a differential configuration at the IF input is recommended due to its better immunity to 2XLO signal coupling to the IF limiter. Otherwise, the 2XLO interference, presented at the IF inputs, may saturate the IF limiter and reduce the gain of the wanted IF signal. The receiver's 3dB input-limiting sensitivity will be affected correspondingly. The interstage bandpass filter will minimize both 2XLO feedthrough and the receiver's noise bandwidth. Therefore, the receiver's input sensitivity can be improved. Without the interstage filter, the second stage will be limited by the broadband noise amplified by the first stage. The noise bandwidth in this case can be as high as 500MHz. The 3dB input limiting sensitivity is about –79dBm at an IF frequency of 280MHz when terminated with 200Ω at the input. The differential IF input impedance is 2.2kΩ. Therefore, a 240Ω resistor is used for R3 as shown in Figure 3. Using a bandpass filter with 50MHz bandwidth, the input sensitivity is improved to –86dBm.

The 1:4 IF input transformer can also be replaced with a narrow band single-to-differential conversion circuit using three discreet elements as shown in Figure 1. Their nominal values are listed in Table 1. Due to the parasitics of the PCB, their values need to be compensated. The receiver's input sensitivity in this case is improved to –85dBm even without interstage filtering. The matching circuit is essentially a second order bandpass filter. Therefore, the requirement for the front-end channel-select filter can be eased too.

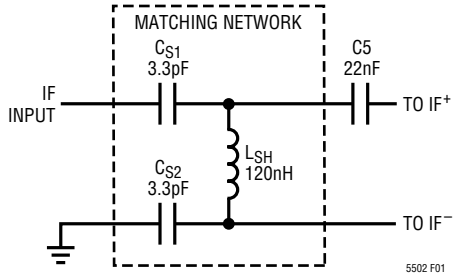


Figure 1. IF Input Matching Network at 280MHz

Table 1. The Component Values of Matching Network L_{SH}, C_{S1} and C_{S2}

f_{IF} (MHz)	L_{SH} (nH)	C_{S1}/C_{S2} (pF)
70	642	13.7
100	422	9.6
150	256	6.4
200	176	4.8
250	130	3.8
300	101	3.2
350	80.4	2.7
400	66.0	2.4

In an application where a lower input sensitivity is satisfactory, one of the IF inputs can be simply AC-terminated with a 50Ω resistor and the other AC-grounded. The input receiver's sensitivity is about – 76dBm at 280MHz in this case.

APPLICATIONS INFORMATION

The receive signal strength indicator (RSSI) is built into the IF limiter. The input IF signal is detected in a current output proportional to the IF input power. The current outputs from two cascaded stages of IF amplifiers/limiters are summed and converted into the RSSI voltage. The RSSI output has an excellent linear range of 90dB. The characteristic of RSSI output voltage versus input IF power is independent of temperature and process variation. The nominal output impedance is 3.8kΩ. An off-chip capacitor C7 is needed to reduce the RSSI voltage ripple. Its value can be determined using the following formula:

$$C7 \geq \frac{1}{760\pi \bullet f_{IF}} F$$

I/Q Demodulators

The quadrature demodulators are double balanced mixers, down converting the limited IF signals from the IF Limiter into I/Q baseband signals. The quadrature LO carriers are obtained from the internal quadrature LO carrier generator. The nominal output voltage of differential I/Q baseband signals is about 850mV$_{P-P}$. These magnitudes are well matched, and their phases are 90° apart.

Quadrature LO Carrier Generator

The quadrature LO carrier generator consists of a divide-by-two circuit and LO buffers. An input signal (2XLO) with twice the desired LO carrier frequency is used as the clock for the divide-by-two circuit, producing the quadrature LO carriers for the demodulators. The outputs are buffered and then drive the down converting mixers. With a full differential approach, the quadrature LO carriers are well matched.

Integrated Low Pass Filters

The 5th order integrated lowpass filters are used for filtering the down converted baseband outputs for both the I-channel and the Q-channel. They serve as anti-aliasing and pulse-shaping filters. The I/Q filters are well matched in gain response and group delay. The 3dB corner frequency is 7.7MHz and the group delay ripple is 16.4ns. The I/Q differential outputs have output driving capability of 1.5kΩ with maximum capacitive loading of 10pF. The outputs are internally biased at V_{CC} –1.16V. Figure 2 shows the simplified output circuit schematic of I-channel or Q-channnel.

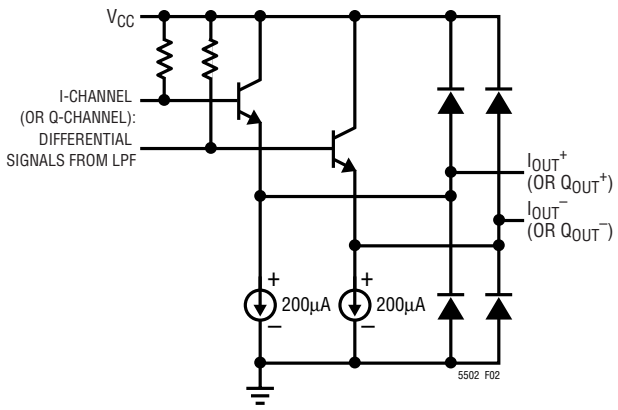


Figure 2. Simplified Circuit Schematic of I-Channel (or Q-Channel) Outputs

The I/Q baseband outputs can be directly DC-coupled to the inputs of a baseband chip. For AC-coupled applications with large coupling capacitors, the STBY pin can be used to prebias the outputs to the desired quiescent voltage at much reduced current. This mode only draws 2.6mA. When the EN pin is then turned on, the chip is quickly switched to normal operating mode without long time constants due to charging or discharging the large coupling capacitors. Table 2 shows the logic of the EN pin and STBY pin. In both normal operating mode and standby mode, the maximum discharging current is about 200µA, and the maximum charging current is more than 10mA.

Table 2. The logic of different operating modes

EN	STBY	Comments
Low	Low	Shutdown Mode
Low	High	Standby Mode
High	Low or High	Normal Operation Mode

TYPICAL APPLICATIONS

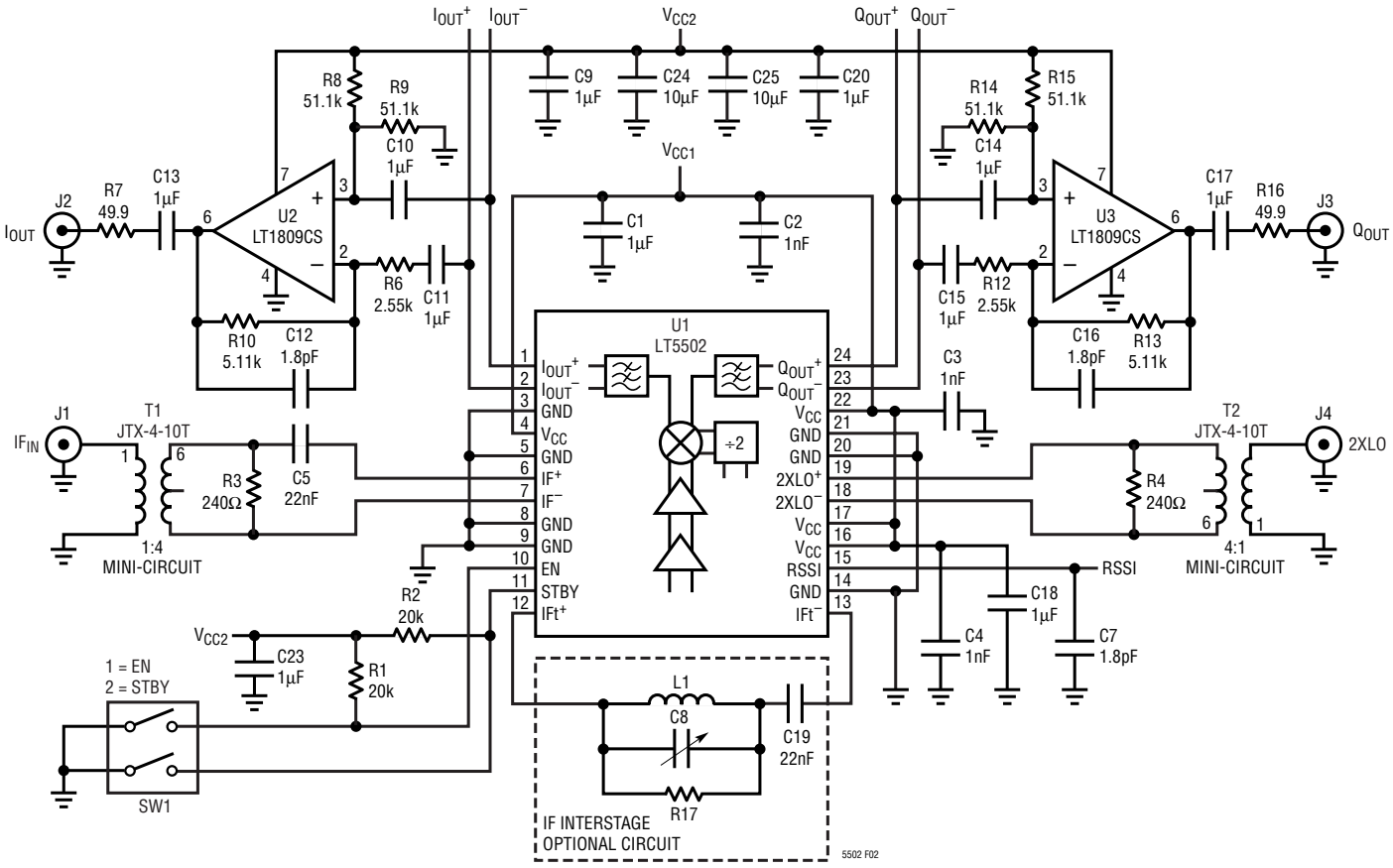


Figure 3. Evaluation Circuit Schematic With I/Q Output Buffers

TYPICAL APPLICATIONS

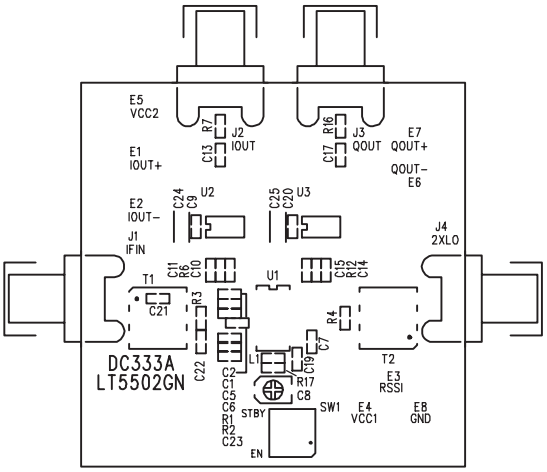


Figure 4.Component Side Silkscreen of Evaluation Board

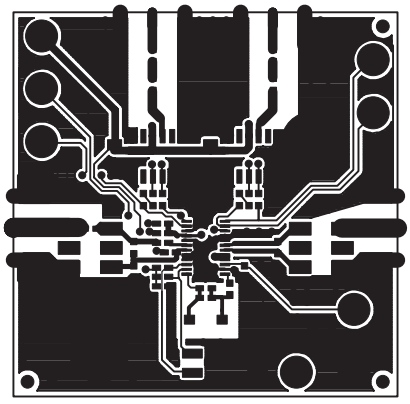


Figure 5. Component Side Layout of Evaluation Board

TYPICAL APPLICATIONS

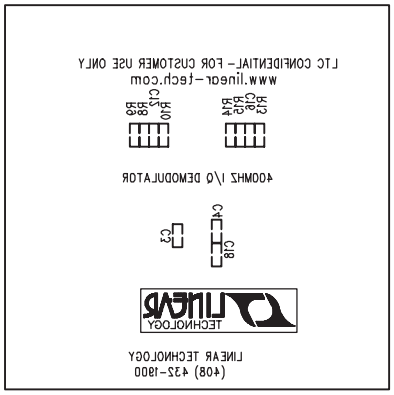


Figure 6.Bottom Side Silkscreen of Evaluation Board

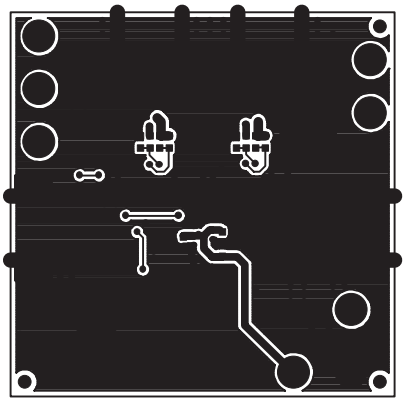
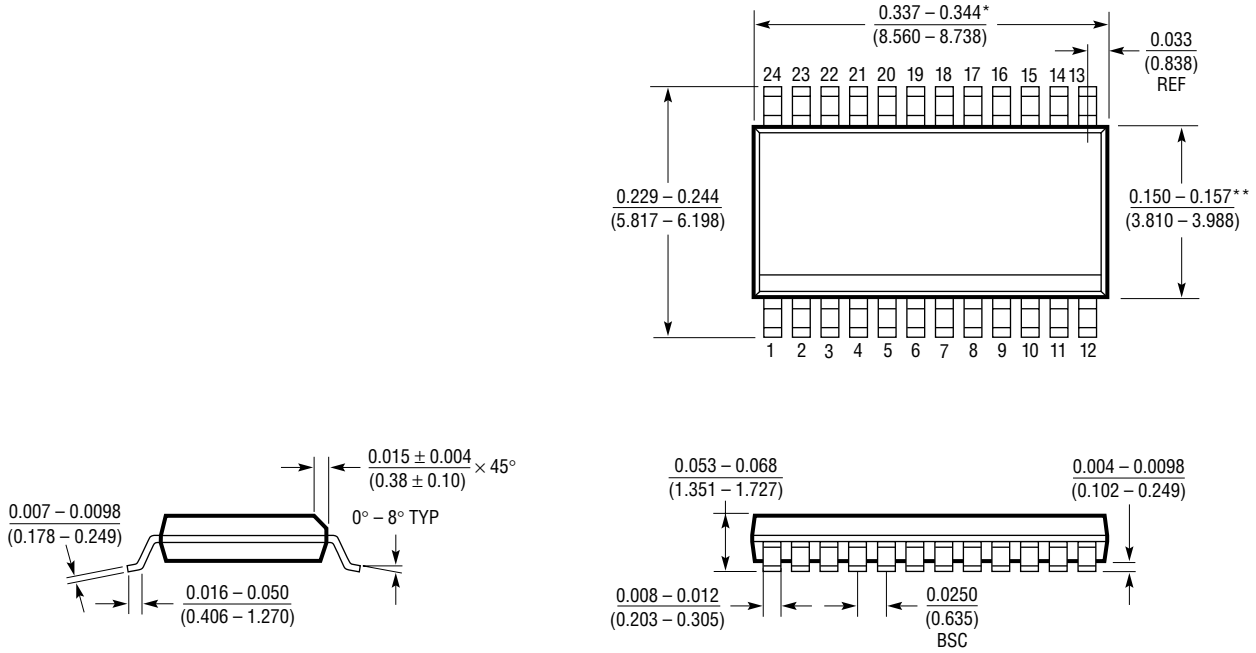


Figure 7. Bottom Side Layout of Evaluation Board

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
24-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



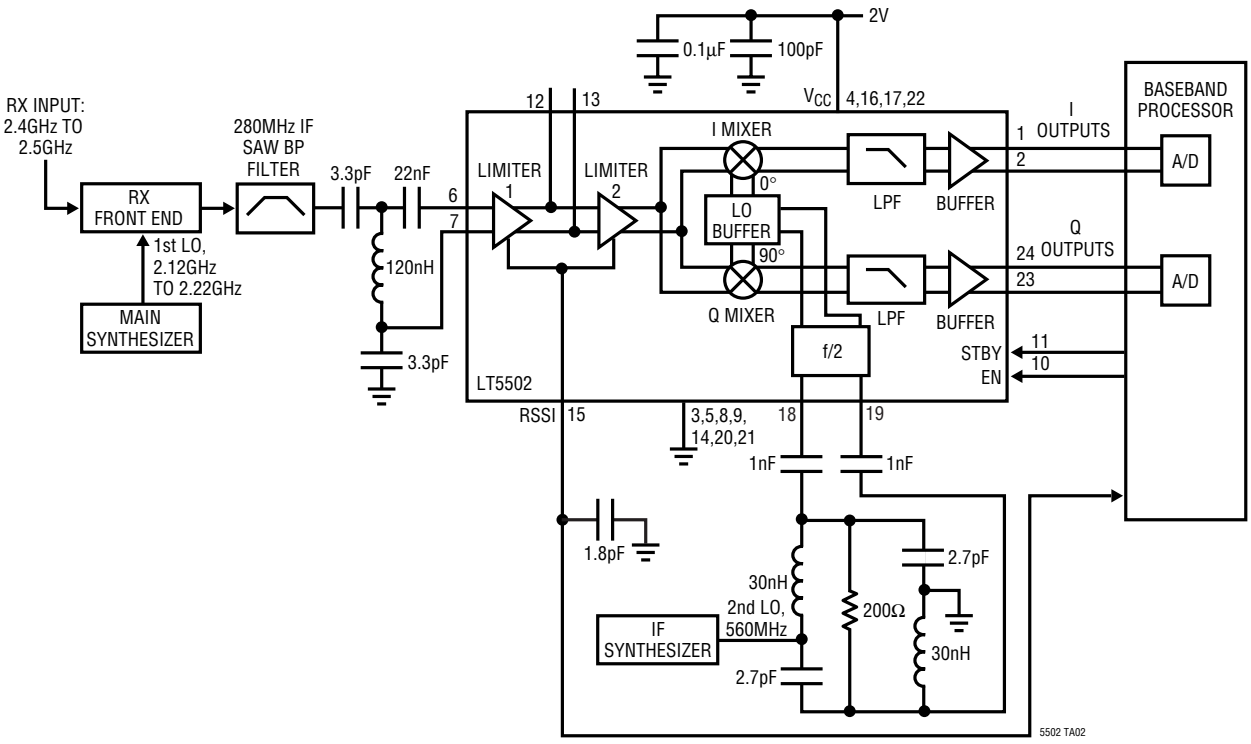
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN24 (SSOP) 1098

TYPICAL APPLICATION

Example: 2.4GHz to 2.5GHz Receiver Application (RX IF = 280MHz)



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