HEF4067B

16-channel analog multiplexer/demultiplexer

Rev. 6 — 16 November 2011 **Product data sheet**

1. General description

The HEF4067B is a 16-channel analog multiplexer/demultiplexer with four address inputs (A0 to A3), an active LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y0 to Y15) and a common input/output (Z). The device contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y15) and the other side connected to the common input/output (Z). With $\overline{E}$ LOW, one of the sixteen switches is selected (low-impedance ON-state) by A0 to A3. All unselected switches are in the high-impedance OFF-state. With $\overline{E}$ HIGH all switches are in the high-impedance OFF-state, independent of A0 to A3. The analog inputs/outputs (Y0 to Y15 and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 15 V.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4067BP	–40 °C to +85 °C	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
HEF4067BT	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

5. Functional diagram

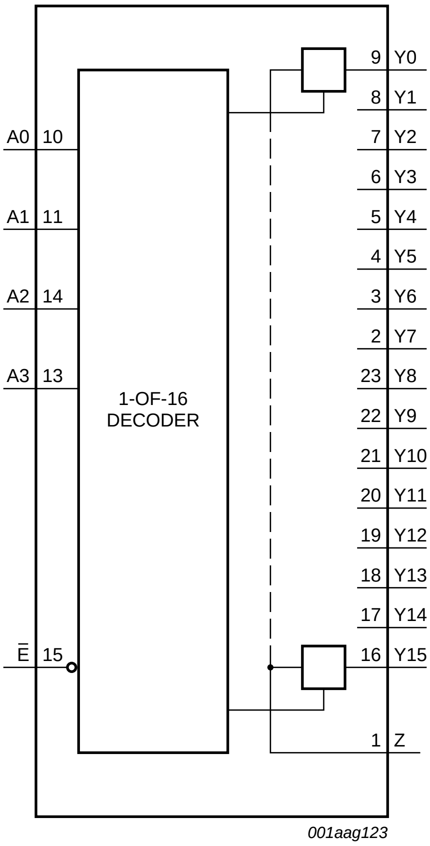


Fig 1. Functional diagram

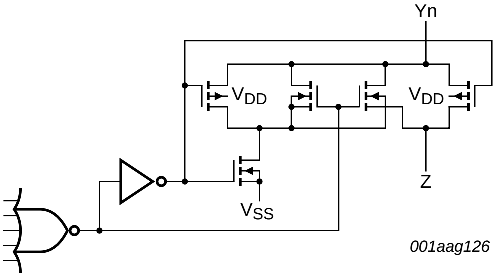


Fig 2. Schematic diagram (one switch)

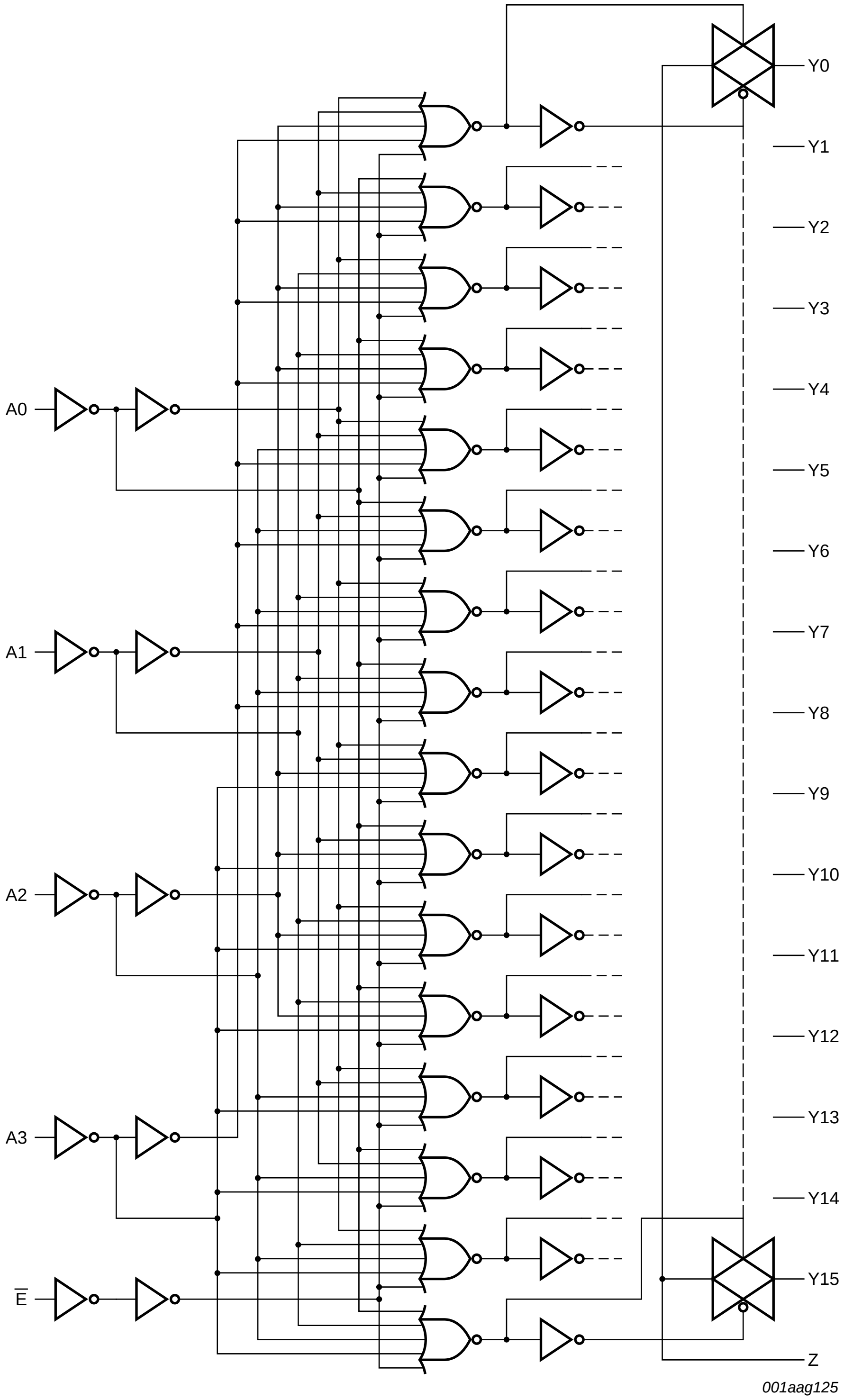


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

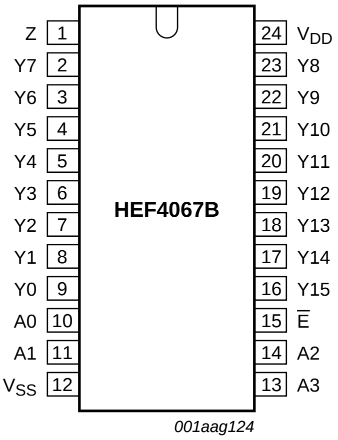


Fig 4. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Z	1	common input/output
Y0 to Y15	9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16	independent input/output
A0 to A3	10, 11, 14, 13	address input
V_{SS}	12	ground (0 V)
$\overline{E}$	15	enable input (active LOW)
V_{DD}	24	supply voltage

7. Functional description

Table 3. Function table[1]

Control	Address				Channel ON
$\overline{E}$	A3	A2	A1	A0	
L	L	L	L	L	Y0 = Z
L	L	L	L	H	Y1 = Z
L	L	L	H	L	Y2 = Z
L	L	L	H	H	Y3 = Z
L	L	H	L	L	Y4 = Z
L	L	H	L	H	Y5 = Z
L	L	H	H	L	Y6 = Z
L	L	H	H	H	Y7 = Z
L	H	L	L	L	Y8 = Z
L	H	L	L	H	Y9 = Z
L	H	L	H	L	Y10 = Z
L	H	L	H	H	Y11 = Z
L	H	H	L	L	Y12 = Z
L	H	H	L	H	Y13 = Z
L	H	H	H	L	Y14 = Z
L	H	H	H	H	Y15 = Z
H	X	X	X	X	none

[1] H = HIGH voltage level; L = LOW voltage level; X = don’t care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+18	V
I_{IK}	input clamping current	pins An and $\overline{E}$; $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	±10	mA
V_I	input voltage		–0.5	V_{DD} + 0.5	V
$I_{I/O}$	input/output current	[1]	-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+85	°C

Table 4. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
		DIP24	[2]	-	750	mW
		SO24	[3]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Yn, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS}.

[2] For DIP24 packages: above T_{amb} = 70 °C, P_{tot} derates linearly at 12 mW/K.

[3] For SO24 packages: above T_{amb} = 70 °C, P_{tot} derates linearly at 8 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IL}	LOW-level input voltage	$\lvert I_O \rvert$ < 1 μA								
		V_O = 0.5 V or 4.5 V	5 V	-	1	-	1	-	1	V
		V_O = 1.0 V or 9.0 V	10 V	-	2	-	2	-	2	V
		V_O = 1.5 V or 13.5 V	15 V	-	2.5	-	2.5	-	2.5	V
V_{IH}	HIGH-level input voltage	$\lvert I_O \rvert$ < 1 μA								
		V_O = 0.5 V or 4.5 V	5 V	4	-	4	-	4	-	V
		V_O = 1.0 V or 9.0 V	10 V	8	-	8	-	8	-	V
		V_O = 1.5 V or 13.5 V	15 V	12.5	-	12.5	-	12.5	-	V
I_I	input leakage current	V_I = 0 V or 15 V	15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{OZ}	OFF-state output current	output at V_{DD}	15 V	-	1.6	-	1.6	-	12.0	μA
		output at V_{SS}	15 V	-	–1.6	-	–1.6	-	–12.0	μA

Table 6. Static characteristics *…continued*

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
$I_{S(OFF)}$	OFF-state leakage current	Z port; all channels OFF; see Figure 5	15 V	-	-	-	1000	-	-	nA
		Yn port; per channel; see Figure 6	15 V	-	-	-	200	-	-	nA
I_{DD}	supply current	all valid input combinations; I_O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance	digital inputs	15 V	-	-	-	7.5	-	-	pF

10.1 Test circuits

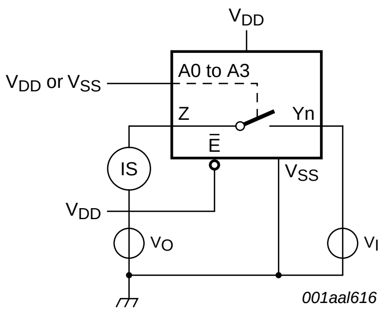


Fig 5. Test circuit for measuring OFF-state leakage current Z port

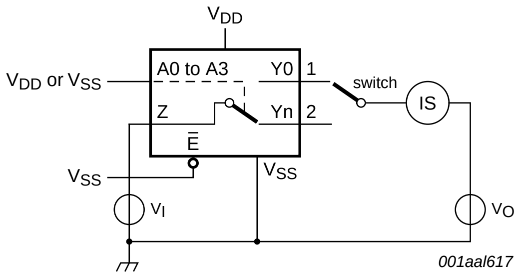


Fig 6. Test circuit for measuring OFF-state leakage current Yn port

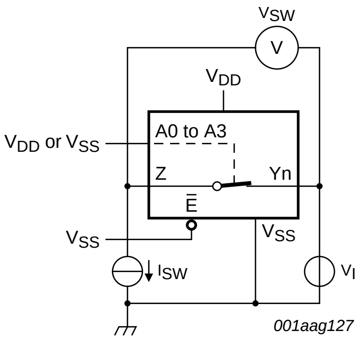
10.2 On resistance

Table 7. ON resistance

T_{amb} = 25 °C; I_{SW} = 200 µA; V_{SS} = 0 V.

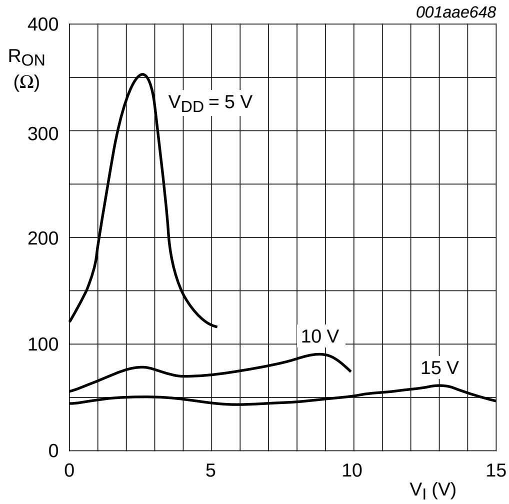
Symbol	Parameter	Conditions	V_{DD}	Typ	Max	Unit
$R_{ON(peak)}$	ON resistance (peak)	V_I = 0 V to V_{DD}; see Figure 7 and Figure 8	5 V	350	2500	Ω
			10 V	80	245	Ω
			15 V	60	175	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = 0 V; see Figure 7 and Figure 8	5 V	115	340	Ω
			10 V	50	160	Ω
			15 V	40	115	Ω
		V_I = V_{DD}; see Figure 7 and Figure 8	5 V	120	365	Ω
			10 V	65	200	Ω
			15 V	50	155	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = 0 V to V_{DD}; see Figure 7	5 V	25	-	Ω
			10 V	10	-	Ω
			15 V	5	-	Ω

10.2.1 On resistance waveform and test circuit



$R_{ON} = V_{SW} / I_{SW}$.

Fig 7. Test circuit for measuring R_{ON}



I_{is} = 200 µA; V_{SS} = 0 V.

Fig 8. Typical R_{ON} as a function of input voltage

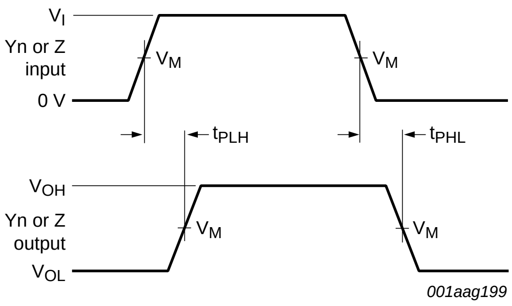
11. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = 25 °C; V_{SS} = 0 V; for test circuit see Figure 12.

Symbol	Parameter	Conditions	V_{DD}	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	Yn, Z to Z, Yn; see Figure 9	5 V	-	30	60	ns
			10 V	-	15	25	ns
			15 V	-	10	20	ns
		An to Yn, Z; see Figure 10	5 V	-	190	380	ns
			10 V	-	70	145	ns
			15 V	-	50	100	ns
t_{PLH}	LOW to HIGH propagation delay	Yn, Z to Z, Yn; see Figure 9	5 V	-	25	50	ns
			10 V	-	10	20	ns
			15 V	-	10	20	ns
		An to Yn, Z; see Figure 10	5 V	-	175	345	ns
			10 V	-	70	140	ns
			15 V	-	50	100	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{E}$ to Yn, Z; see Figure 11	5 V	-	195	385	ns
			10 V	-	140	280	ns
			15 V	-	130	260	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{E}$ to Yn, Z; see Figure 11	5 V	-	215	435	ns
			10 V	-	180	355	ns
			15 V	-	170	340	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{E}$ to Yn, Z; see Figure 11	5 V	-	155	315	ns
			10 V	-	70	135	ns
		$\overline{E}$ to Yn, Z; see Figure 11	15 V	-	50	100	ns
t_{PZL}	OFF-state to LOW propagation delay		5 V	-	170	340	ns
			10 V	-	70	140	ns
			15 V	-	50	100	ns

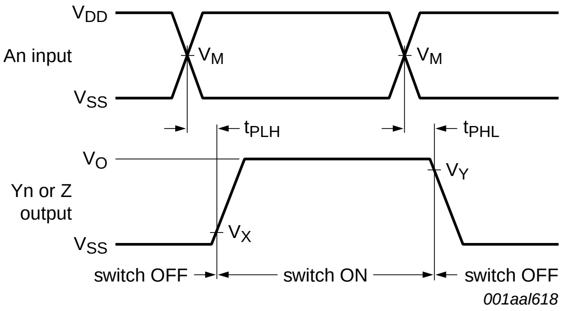
11.1 Waveforms and test circuit



Measurement points are given in Table 9.

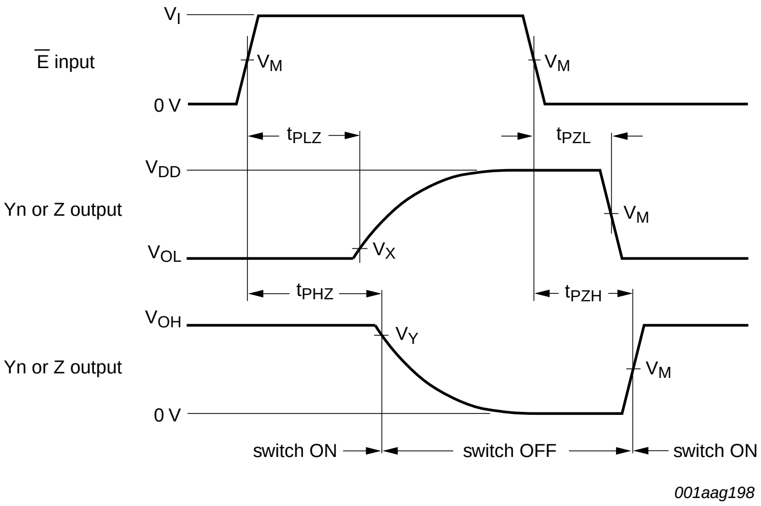
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Yn, Z to Z, Yn propagation delays



Measurement points are given in Table 9.

Fig 10. Sn to Yn, Z propagation delays



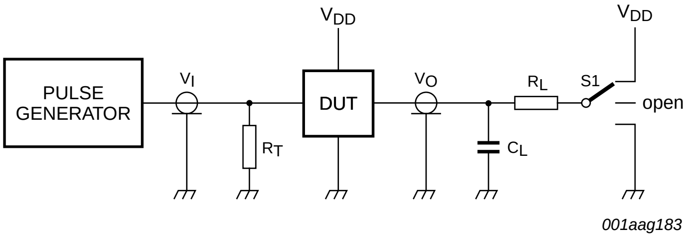
Measurement points are shown in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 11. Enable and disable times

Table 9. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_M	V_I	V_M	V_X	V_Y
5 V to 15 V	$0.5V_{DD}$	GND to V_{DD}	$0.5V_{DD}$	10%	90%



Test data is given in Table 10.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = load capacitance including jig and probe capacitance

R_L = load resistor

S1 = test selection switch

Fig 12. Test circuit for measuring switching times

Table 10. Test data

Input				Load		S1 position				
Yn, Z	**An and $\overline{E}$**	**t_r, t_f**	**V_M**	**C_L**	**R_L**	**t_{PHL}[1]**	**t_{PLH}**	**t_{PZH}, t_{PHZ}**	**t_{PZL}, t_{PLZ}**	**other**
V_{DD} or V_{SS}	V_{DD} or V_{SS}	≤ 20 ns	$0.5V_{DD}$	50 pF	10 kΩ	V_{DD} or V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}

[1] For Yn to Z or Z to Yn propagation delays use V_{SS}. For An or to Yn or Z propagation delays use V_{DD}.

11.2 Additional dynamic parameters

Table 11. Additional dynamic characteristics
V_{SS} = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	V_{DD}		Typ	Max	Unit
THD	total harmonic distortion	see Figure 13; R_L = 10 kΩ; C_L = 15 pF; channel ON; V_I = 0.5V_{DD} (p-p); f_i = 1 kHz	5 V	[1]	0.25	-	%
			10 V	[1]	0.04	-	%
			15 V	[1]	0.04	-	%
$f_{(-3dB)}$	−3 dB frequency response	see Figure 14; R_L = 1 kΩ; C_L = 5 pF; channel ON; V_I = 0.5V_{DD} (p-p)	5 V	[1]	13	-	MHz
			10 V	[1]	40	-	MHz
			15 V	[1]	70	-	MHz
α_{iso}	isolation (OFF-state)	see Figure 15; f_i = 1 MHz; R_L = 1 kΩ; C_L = 5 pF; channel OFF; V_I = 0.5V_{DD} (p-p)	10 V	[1]	−50	-	dB
V_{ct}	crosstalk voltage	digital inputs to switch; see Figure 16; R_L = 10 kΩ; C_L = 15 pF; $\overline{E}$ or An = V_{DD} (square-wave)	10 V		50	-	mV
Xtalk	crosstalk	between switches; see Figure 17; f_i = 1 MHz; R_L = 1 kΩ; V_I = 0.5V_{DD} (p-p)	10 V	[1]	−50	-	dB

[1] f_i is biased at 0.5 V_{DD}; V_I = 0.5V_{DD} (p-p).

Table 12. Dynamic power dissipation P_D
P_D can be calculated from the formulas shown; V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 1000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz;
		10 V	$P_D = 5500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz;
		15 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF;
				V_{DD} = supply voltage in V;
				$\Sigma(C_L \times f_o)$ = sum of the outputs.

11.2.1 Test circuits

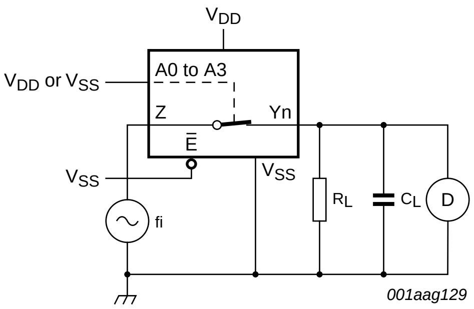


Fig 13. Test circuit for measuring total harmonic distortion

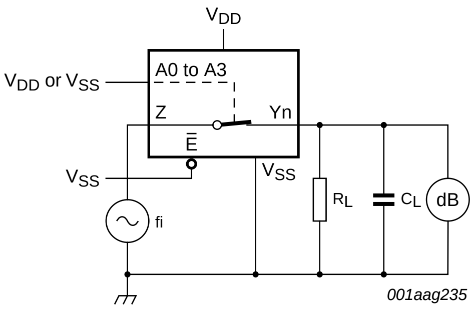


Fig 14. Test circuit for measuring frequency response

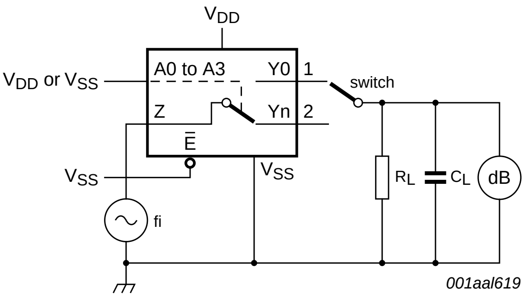
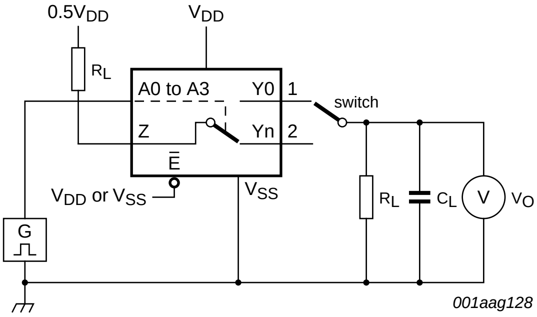
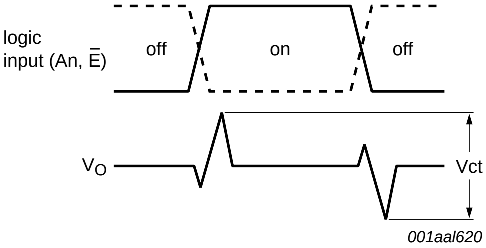


Fig 15. Test circuit for measuring isolation (OFF-state)

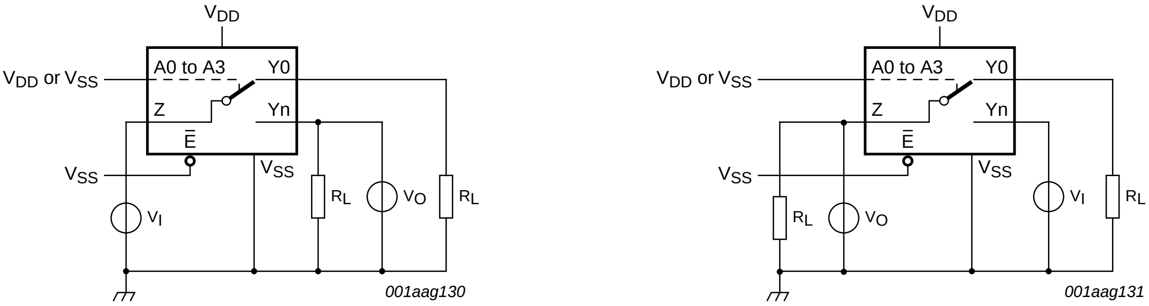


a. Test circuit



b. Input and output pulse definitions

Fig 16. Test circuit for measuring crosstalk voltage between digital inputs and switch



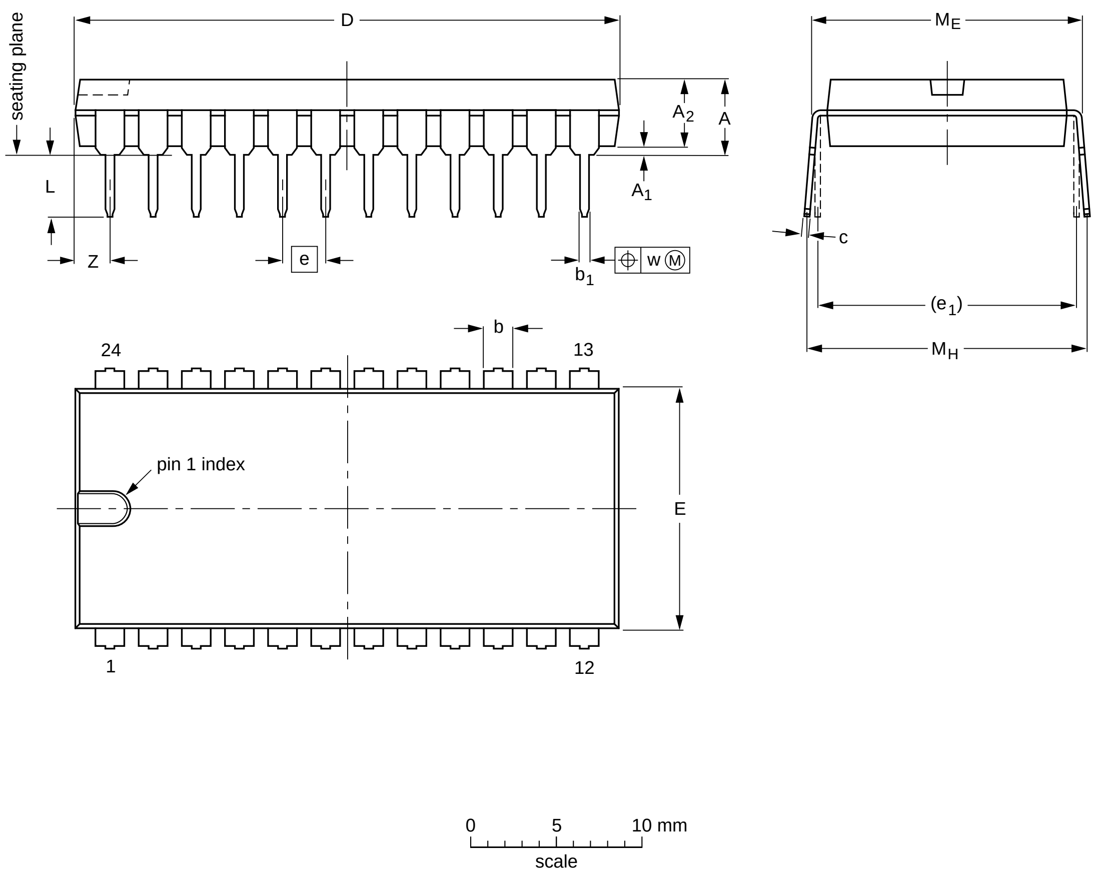
a. Switch closed condition

b. Switch open condition

Fig 17. Test circuit for measuring crosstalk between switches

12. Package outline

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.2	0.02	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

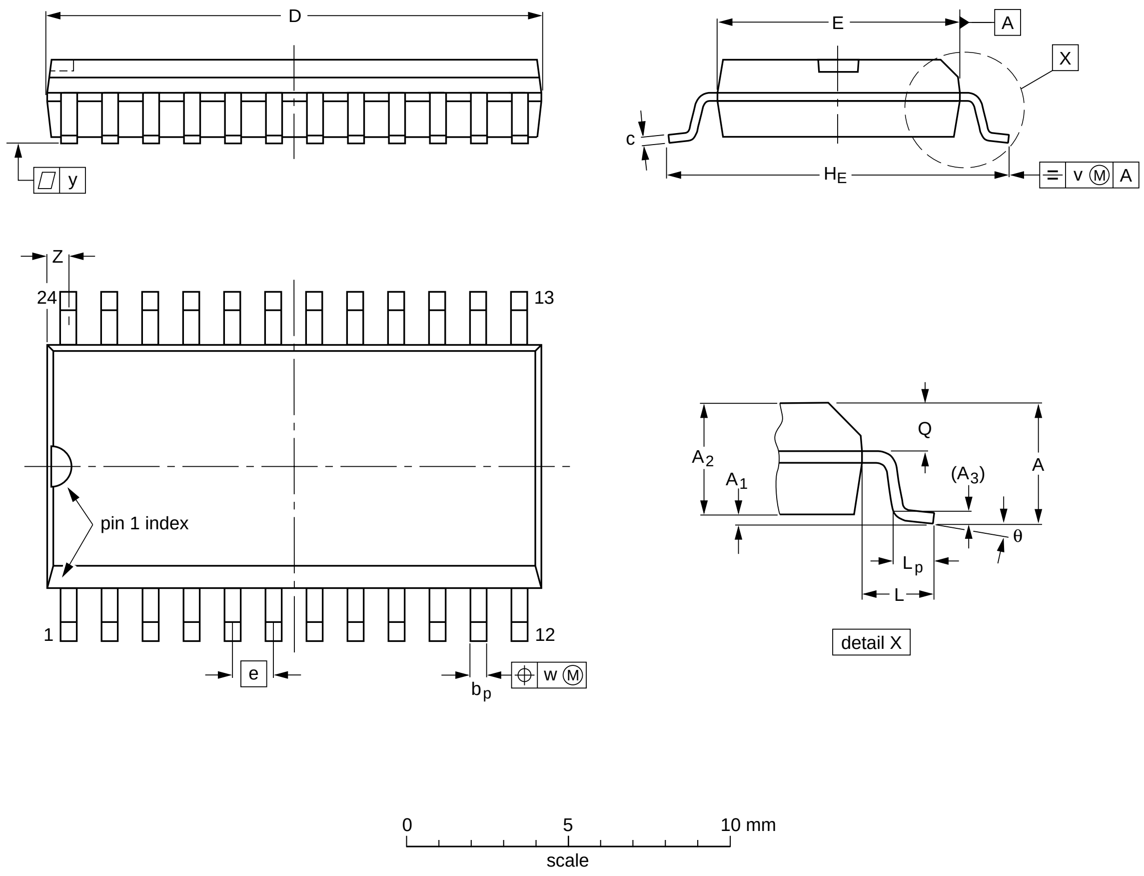
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT101-1	051G02	MO-015	SC-509-24			~~99-12-27~~ 03-02-13

Fig 18. Package outline SOT101-1 (DIP24)

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^{o} 0^{o}
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT137-1 (SO24)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
DUT	Device Under Test

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4067B v.6	20111116	Product data sheet	-	HEF4067B v.5
Modifications:	• Legal pages updated. • Changes in “General description”, “Features and benefits” and “Applications”.			
HEF4067B v.5	20100325	Product data sheet	-	HEF4067B v.4
HEF4067B v.4	20100308	Product data sheet	-	HEF4067B_CNV v.3
HEF4067B_CNV v.3	19950101	Product specification	-	HEF4067B_CNV v.2
HEF4067B_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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17. Contents

1 General description 1
2 Features and benefits 1
3 Applications 1
4 Ordering information 1
5 Functional diagram 2
6 Pinning information 4
6.1 Pinning 4
6.2 Pin description 4
7 Functional description 5
8 Limiting values 5
9 Recommended operating conditions 6
10 Static characteristics 6
10.1 Test circuits 7
10.2 On resistance 8
10.2.1 On resistance waveform and test circuit 8
11 Dynamic characteristics 9
11.1 Waveforms and test circuit 10
11.2 Additional dynamic parameters 12
11.2.1 Test circuits 12
12 Package outline 14
13 Abbreviations 16
14 Revision history 16
15 Legal information 17
15.1 Data sheet status 17
15.2 Definitions 17
15.3 Disclaimers 17
15.4 Trademarks 18
16 Contact information 18
17 Contents 19

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